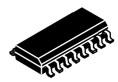
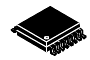



MULTIPOINT-LVDS QUAD DIFFERENTIAL LINE DRIVER

FEATURES

- **Differential Line Drivers for 30-Ω to 55-Ω Loads and Data Rates(1) Up to 200 Mbps, Clock Frequencies up to 100 MHz**
- **Supports Multipoint Bus Architectures**
- **Meets the Requirements of TIA/EIA-899**
- **Operates from a Single 3.3-V Supply**
- **Characterized for Operation from –40°C to 85°C**
- **16-Pin SOIC (JEDEC MS-012) and 16-Pin TSSOP (JEDEC MS-153) Packaging**

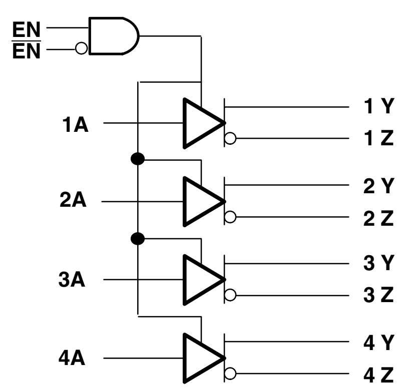
APPLICATIONS

- **AdvancedTCA™ (ATCA™) Clock Bus Driver**
- **Clock Distribution**
- **Backplane or Cabled Multipoint Data Transmission in Telecommunications, Automotive, Industrial, and Other Computer Systems**
- **Cellular Base Stations**
- **Central-Office and PBX Switching**
- **Bridges and Routers**
- **Low-Power High-Speed Short-Reach Alternative to TIA/EIA-485**

DESCRIPTION

The SN65MLVD047A is a quadruple line driver that complies with the TIA/EIA-899 standard, Electrical Characteristics of Multipoint-Low-Voltage Differential Signaling (M–LVDS). The output current of this M–LVDS device has been increased, in comparison to standard LVDS compliant devices, in order to support doubly terminated transmission lines and heavily loaded backplane bus applications. Backplane applications generally require impedance matching termination resistors at both ends of the bus. The effective impedance of a doubly terminated bus can be as low as 30 Ω due to the bus terminations, as well as the capacitive load of bus interface devices. SN65MLVD047A drivers allow for operation with loads as low as 30 Ω. The SN65MLVD047A devices allow for multiple drivers to be present on a single bus. SN65MLVD047A drivers are high impedance when disabled or unpowered. Driver edge rate control is incorporated to support operation. The M–LVDS standard allows up to 32 nodes (drivers and/or receivers) to be connected to the same media in a backplane when multiple bus stubs are expected from the main transmission line to interface devices. The SN65MLVD047A provides 9-kV ESD protection on all bus pins.

LOGIC DIAGRAM (POSITIVE LOGIC)



(1)The data rate of a line, is the number of voltage transitions that are made per second expressed in the units bps (bits per second).
AdvancedTCA and ATCA are trademarks of the PCI Industrial Computer Manufacturers Group.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE/CARRIER
SN65MLVD047AD	MLVD047A	16-Pin SOIC/Tube
SM65MLVD047ADR	MLVD047A	16-Pin SOIC/Tape and Reel
SN65MLVD047APW	BUL	16-Pin TSSOP/Tube
SM65MLVD047APWR	BUL	16-Pin TSSOP/Tape and Reel

NOTE: For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PACKAGE DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$[1]	$T_A = 85°C$ POWER RATING
D(16)	Low-K[2]	898 mW	7.81 mW/°C	429 mW
PW(16)	Low-K[2]	592 mW	5.15 mW/°C	283 mw
	High-K[3]	945 mW	8.22 mW/°C	452 mw

(1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.
(2) In accordance with the Low-K thermal metric difinitions of EIA/JESD51–3.
(3) In accordance with the High-K thermal metric difinitions of EIA/JESD51–7.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

			UNITS
Supply voltage range[2], V_{CC}			–0.5 V to 4 V
Input voltage range, V_I	A, EN, $\overline{EN}$		–0.5 V to 4 V
Output voltage range, V_O	Y, Z		–1.8 V to 4 V
Electrostatic discharge	Human Body Model[3]	Y and Z	±9 kV
		All pins	±4 kV
	Charged-Device Model[4]	All pins	±1500 V
	Machine Model[5]	All pins	200 V
Junction temperature, T_J			140°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to the circuit ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114–B.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101–A.
(5) Tested in accordance with JEDEC Standard 22, Test Method A115–A.

RECOMMENDED OPERATING CONDITIONS (see Figure 1)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	0		0.8	V
Voltage at any bus terminal (separate or common mode) V_Y or V_Z	–1.4		3.8	V
Differential load resistance, R_L	30		55	Ω
Signaling rate, $1/t_{UI}$			200	Mbps
Clock frequency, f			100	MHz
Junction temperature, T_J	–40		125	°C

THERMAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Junction-to-ambient thermal resistance, Θ_{JA}	Low-K board(1), no airflow	D		128		°C/W
	Low-K board(1), no airflow	PW		194.2		
	Low-K board(1), 150 LFM			146.8		
	Low-K board(1), 250 LFM			133.1		
	High-K board(2), no airflow			121.6		
Junction-to-board thermal resistance, Θ_{JB}	High-K board(2)	D		51.1		°C/W
		PW		85.3		
Junction-to-case thermal resistance, Θ_{JC}		D		45.4		°C/W
		PW		34.7		
Device power dissipation, P_D	EN = V_{CC}, $\overline{EN}$ = GND, R_L = 50 Ω, Input 100 MHz 50 % duty cycle square wave to all data inputs, T_A = 85°C				288.5	mW

(1) In accordance with the Low-K thermal metric difinitions of EIA/JESD51–3.
(2) In accordance with the High-K thermal metric difinitions of EIA/JESD51–7.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	Driver enabled	EN = V_{CC}, $\overline{EN}$ = GND, R_L = 50 Ω, All data inputs = V_{CC} or GND		59	70	mA
		Driver disabled	EN = GND, $\overline{EN}$ = V_{CC}, R_L = No load, All data inputs = V_{CC} or GND		2	4	

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN[(1)]	TYP[(2)]	MAX	UNIT
LVTTL (EN, $\overline{EN}$, 1A:4A)						
$\lvert I_{IH} \rvert$	High-level input current	V_{IH} = 2 V or V_{CC}	0		10	μA
$\lvert I_{IL} \rvert$	Low-level input current	V_{IL} = GND or 0.8 V	0		10	μA
C_i	Input capacitance	V_I = 0.4 sin(30E6πt) + 0.5 V[(3)]		5		pF
M–LVDS (1Y/1Z:4Y/4Z)						
$\lvert V_{YZ} \rvert$	Differential output voltage magnitude	See Figure 2	480		650	mV
$\Delta \lvert V_{YZ} \rvert$	Change in differential output voltage magnitude between logic states		–50		50	mV
$V_{OS(SS)}$	Steady-state common-mode output voltage	See Figure 3	0.8		1.2	V
$\Delta V_{OS(SS)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OS(PP)}$	Peak-to-peak common-mode output voltage				150	mV
$V_{Y(OC)}$	Maximum steady-state open-circuit output voltage	See Figure 7	0		2.4	V
$V_{Z(OC)}$	Maximum steady-state open-circuit output voltage		0		2.4	V
$V_{P(H)}$	Voltage overshoot, low-to-high level output	See Figure 5			1.2 V_{SS}	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output		–0.2 V_{SS}			V
$\lvert I_{OS} \rvert$	Differential short-circuit output current magnitude	See Figure 4			24	mA
I_{OZ}	High-impedance state output current	–1.4 V ≤ (V_Y or V_Z) ≤ 3.8 V, Other output = 1.2 V	–15		10	μA
$I_{O(OFF)}$	Power-off output current	–1.4 V ≤ (V_Y or V_Z) ≤ 3.8 V, Other output = 1.2 V, V_{CC} ≤ 1.5 V	–10		10	μA
C_Y or C_Z	Output capacitance	V_Y or V_Z = 0.4 sin(30E6πt) + 0.5 V, [(3)] Other outputs at 1.2 V, driver disabled		3		pF
C_{YZ}	Differential output capacitance	V_{YZ} = 0.4 sin(30E6πt) V, [(3)] Driver disabled			2.5	pF
$C_{Y/Z}$	Output capacitance balance, (C_Y/C_Z)		0.99		1.01	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) All typical values are at 25°C and with a 3.3-V supply voltage.
(3) HP4194A impedance analyzer (or equivalent)

SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{pLH}	Propagation delay time, low-to-high-level output	See Figure 5	1	1.5	2.4	ns
t_{pHL}	Propagation delay time, high-to-low-level output		1	1.5	2.4	ns
t_r	Differential output signal rise time		1		1.9	ns
t_f	Differential output signal fall time		1		1.9	ns
$t_{sk(o)}$	Output skew(2)				100	ps
$t_{sk(p)}$	Pulse skew ($\|t_{pHL} – t_{pLH}\|$)			22	100	ps
$t_{sk(pp)}$	Part-to-part skew(3)				600	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation)(4)	See Figure 8, All data inputs 100 MHz clock input		0.2	1	ps
$t_{jit(c–c)}$	Cycle-to-cycle jitter(4)	See Figure 8, All data inputs 100 MHz clock input		5	36	ps
$t_{jit(pp)}$	Peak-to-peak jitter(3)(5)	See Figure 8, All data inputs 200 Mbps 2^{15}–1 PRBS input		46	158	ps
t_{pZH}	Enable time, high-impedance-to-high-level output	See Figure 6			9	ns
t_{pZL}	Enable time, high-impedance-to-low-level output				9	ns
t_{pHZ}	Disable time, high-level-to-high-impedance output	See Figure 6			10	ns
t_{pLZ}	Disable time, low-level-to-high-impedance output				10	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.
(2) $t_{sk(o)}$, output skew is the magnitude of the time difference in propagation delay times between any specified terminals of a device.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(4) Stimulus jitter has been subtracted from the measurements.
(5) Peak-to-peak jitter includes jitter due to pulse skew ($t_{sk(p)}$).

PARAMETER MEASUREMENT INFORMATION

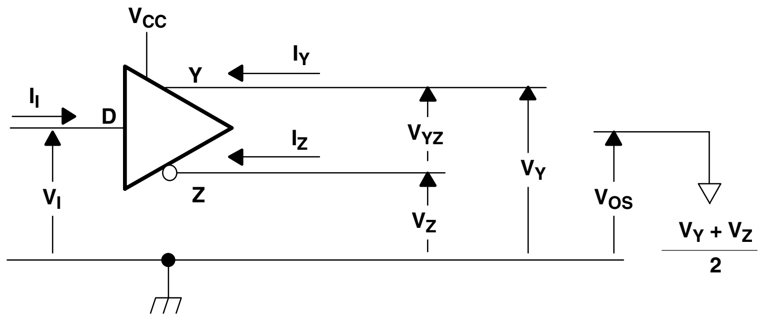
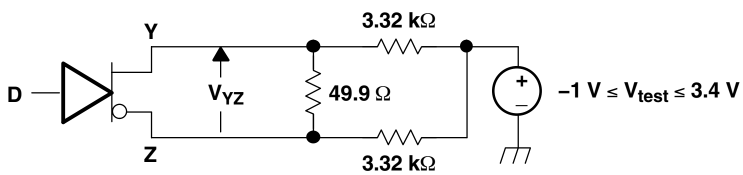
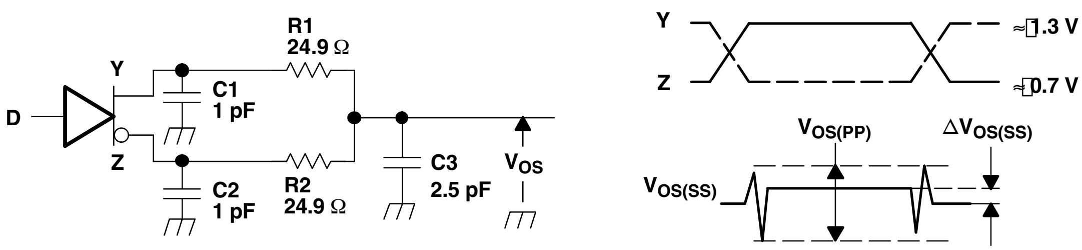


Figure 1. Driver Voltage and Current Definitions



NOTE: All resistors are 1% tolerance.

Figure 2. Differential Output Voltage Test Circuit



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse frequency = 500 kHz, duty cycle = 50 ± 5%.
B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.
C. R1 and R2 are metal film, surface mount, ±1%, and located within 2 cm of the D.U.T.
D. The measurement of $V_{OS(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 3. Test Circuit and Definitions for the Common-Mode Output Voltage

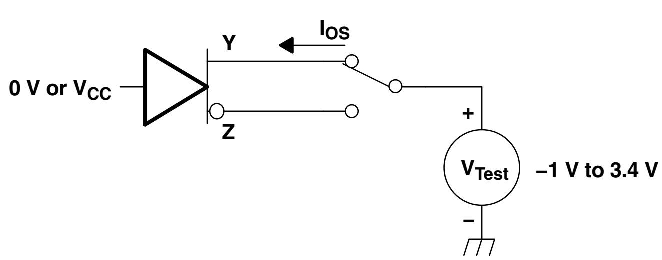
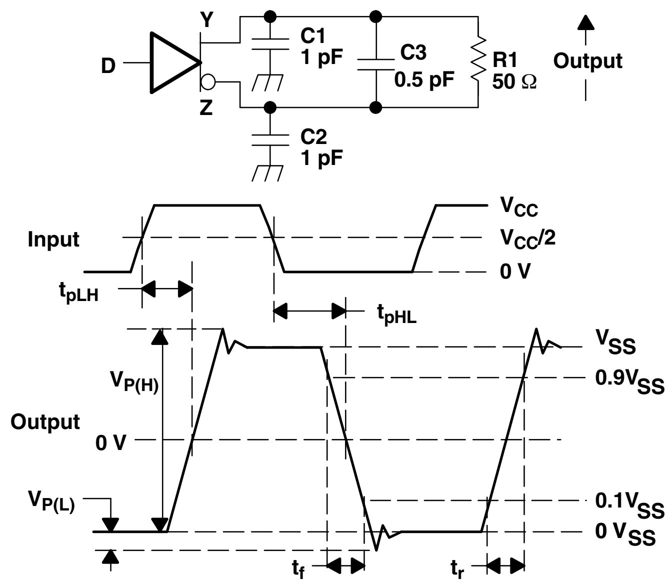


Figure 4. Short-Circuit Test Circuit



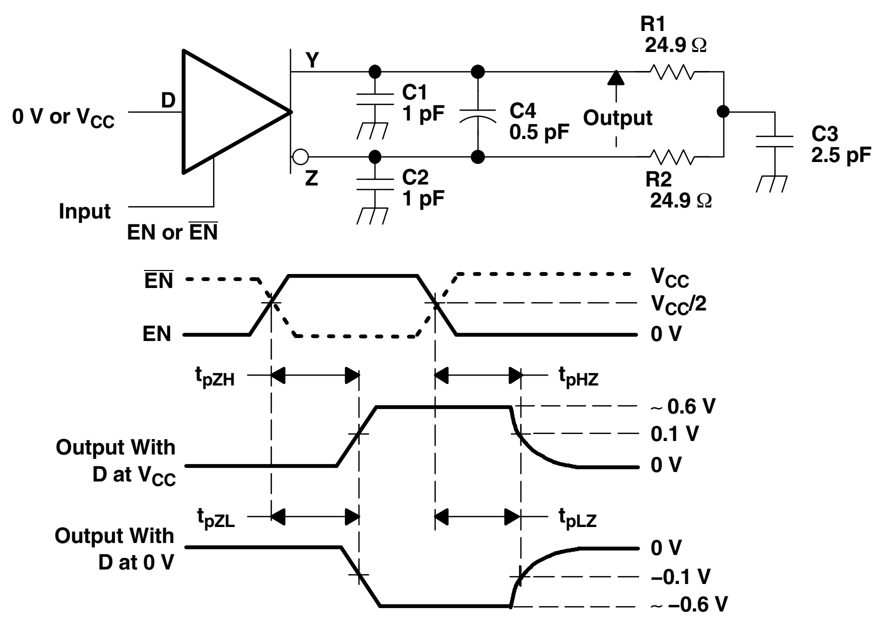
NOTES:A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, frequency = 500 kHz, duty cycle = 50 ±5%.

B. C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.

C. R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.

D. The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



NOTES:A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, frequency = 500 kHz, duty cycle = 50 ± 5%.

B. C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.

C. R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.

D. The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 6. Driver Enable and Disable Time Circuit and Definitions

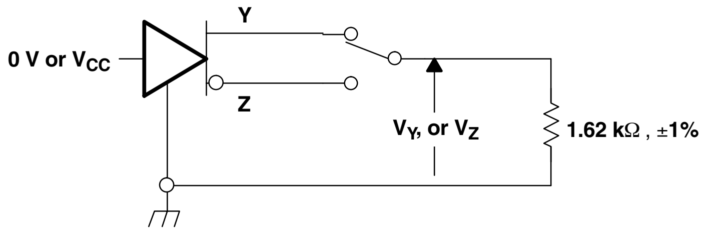
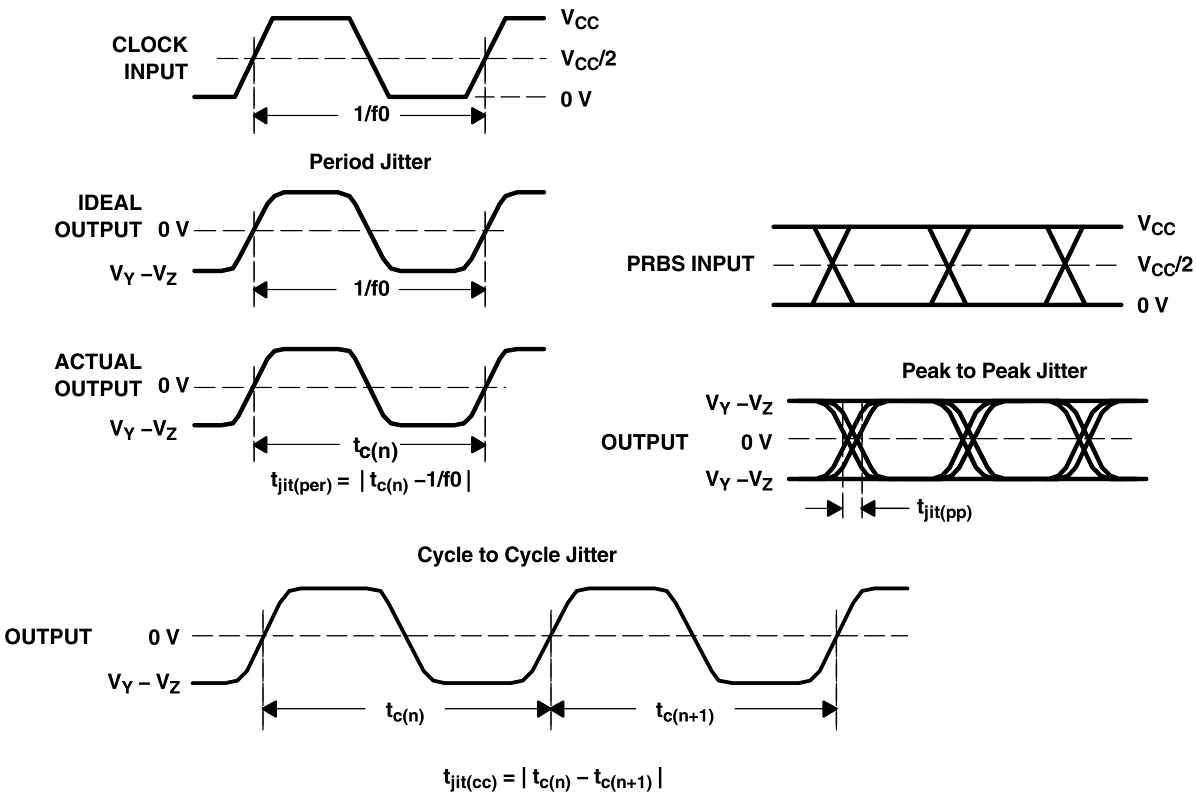


Figure 7. Driver Maximum Steady State Output Voltage



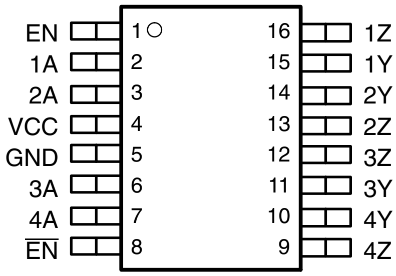
NOTES:
- A. All input pulses are supplied by an Agilent 8304A Stimulus System.
- B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
- C. Period jitter and cycle-to-cycle jitter are measured using a 100 MHz 50 ±1% duty cycle clock input.
- D. Peak-to-peak jitter is measured using a 200 Mbps 2^{15}–1 PRBS input.

Figure 8. Driver Jitter Measurement Waveforms

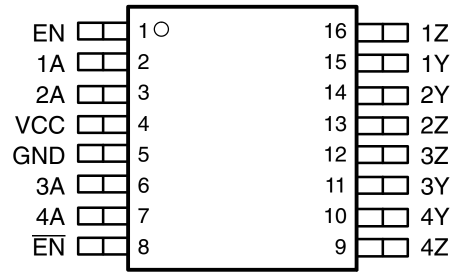
DEVICE INFORMATION

PIN ASSIGNMENTS

D PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



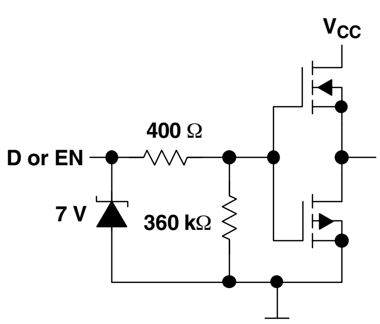
DEVICE FUNCTION TABLE

INPUTS			OUTPUTS	
D	EN	$\overline{EN}$	Y	Z
L	H	L	L	H
H	H	L	H	L
OPEN	H	L	L	H
X	L or OPEN	X	Z	Z
X	X	H or OPEN	Z	Z

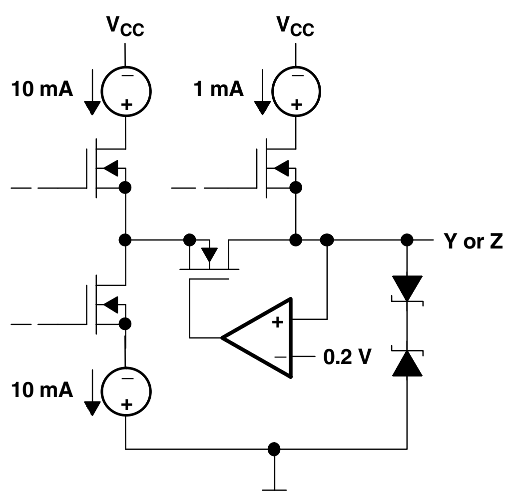
H = high level, L = low level, Z = high impedance, X = Don't care

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

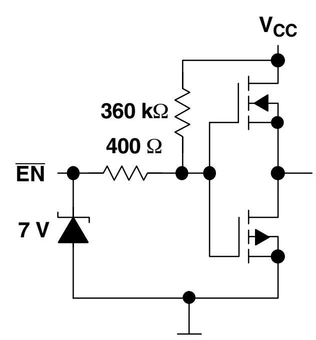
DRIVER INPUT AND ACTIVE–HIGH ENABLE



DRIVER OUTPUT



ACTIVE–LOW ENABLE



TYPICAL CHARACTERISTICS

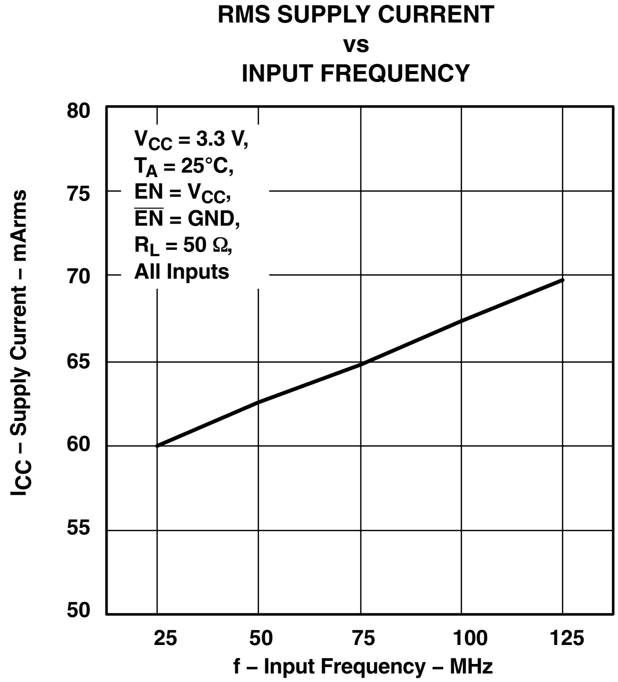


Figure 9

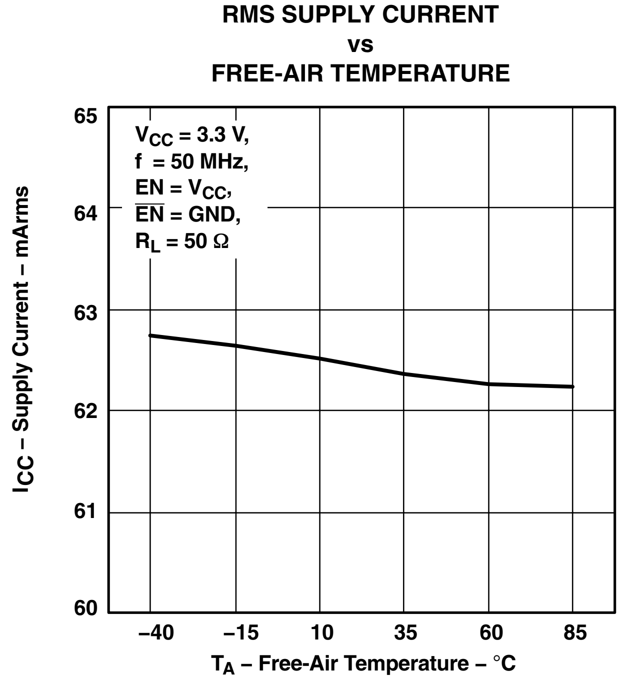


Figure 10

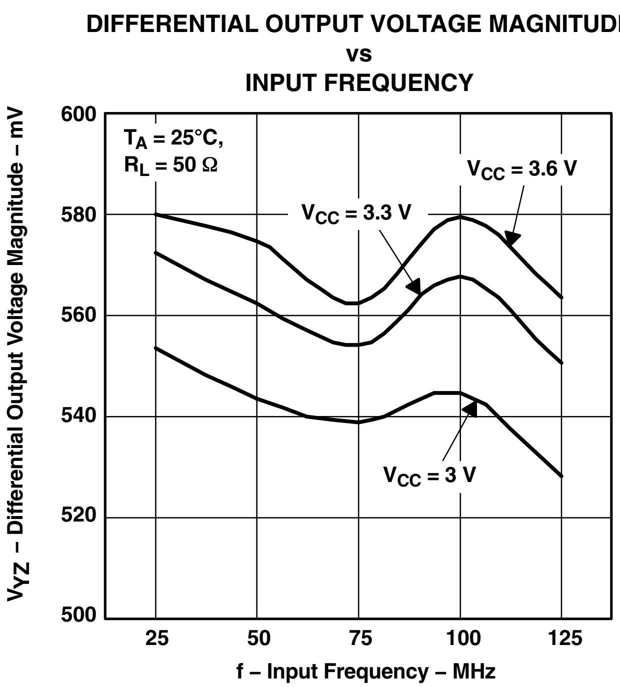


Figure 11

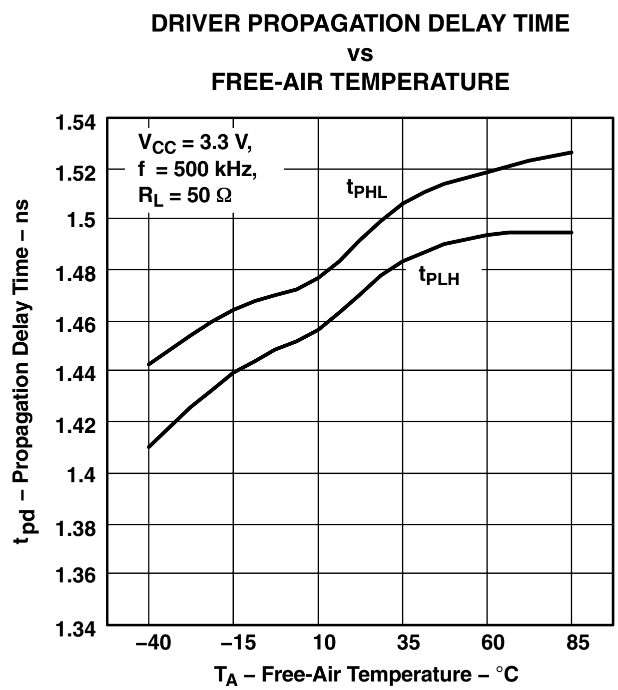


Figure 12

TYPICAL CHARACTERISTICS

DRIVER TRANSITION TIME
vs
FREE-AIR TEMPERATURE

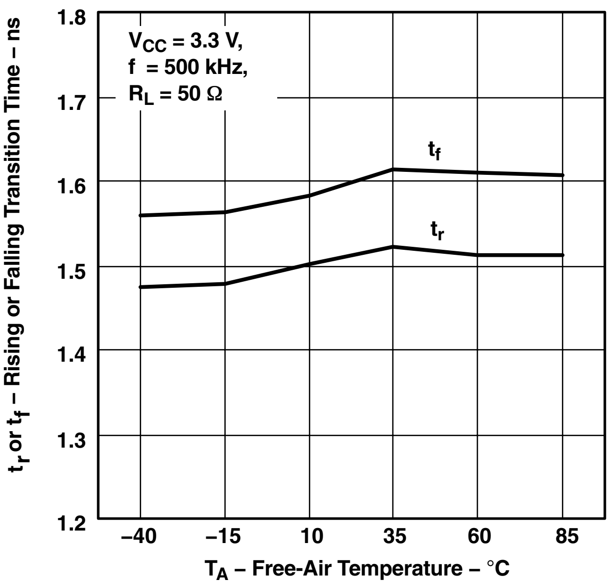


Figure 13

PEAK-TO-PEAK JITTER
vs
DATA RATE

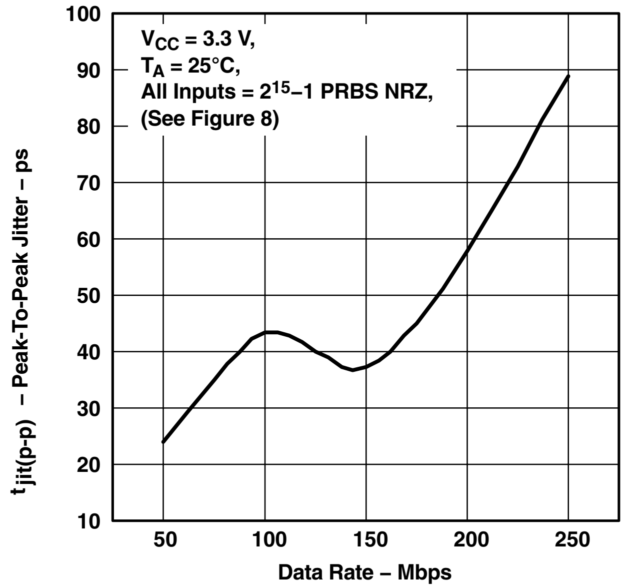


Figure 14

PERIOD JITTER
vs
CLOCK FREQUENCY

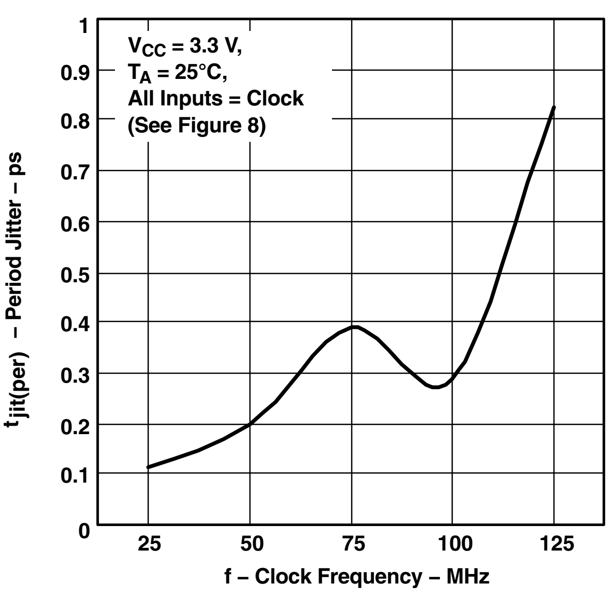


Figure 15

CYCLE-TO-CYCLE JITTER
vs
CLOCK FREQUENCY

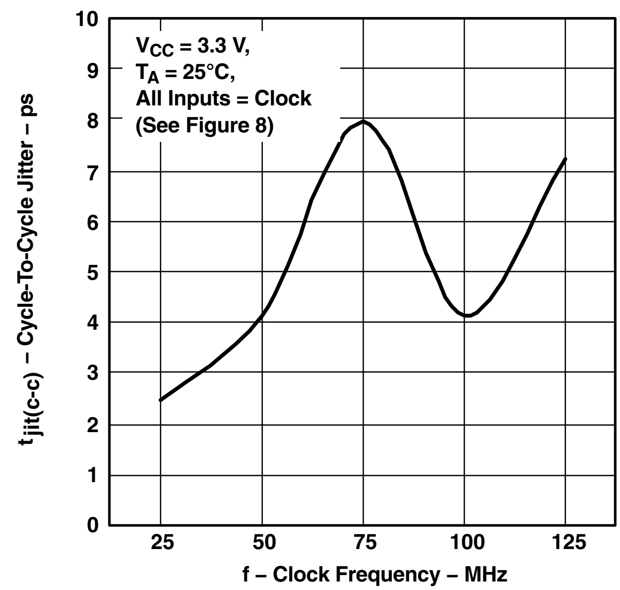


Figure 16

APPLICATION INFORMATION

SYNCHRONIZATION CLOCK IN ADVANCEDTCA

Advanced Telecommunications Computing Architecture, also known as AdvancedTCA, is an open architecture to meet the needs of the rapidly changing communications network infrastructure. M−LVDS bused clocking is recommended by the ATCA.

The ATCA specification includes requirements for three redundant clock signals. An 8-KHz and a 19.44-MHz clock signal, as well as an user-defined clock signal are included in the specification. The SN65MLVD047A quad driver supports distribution of these three ATCA clock signals, supporting operation beyond 100 MHz, which is the highest clock frequency included in the ATCA specification. A pair of SN65MLVD047A devices can be used to support the ATCA redundancy requirements.

MULTIPOINT CONFIGURATION

The SN65MLVD047A is designed to meet or exceed the requirement of the TIA/EIA−899 (M−LVDS) standard, which allows multipoint communication on a shared bus.

Multipoint is a bus configuration with multiple drivers and receivers present. An example is shown in Figure 17. The figure shows transceivers interfacing to the bus, but a combination of drivers, receivers, and transceivers is also possible. Termination resistors need to be placed on each end of the bus, with the termination resistor value matched to the loaded bus impedance.

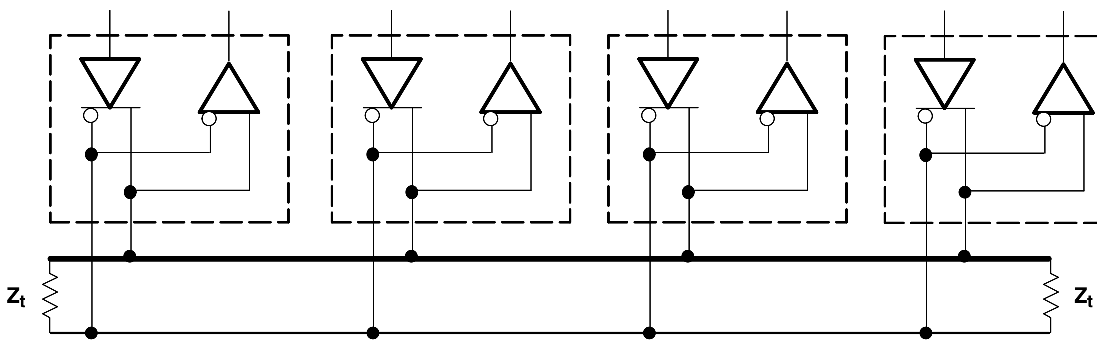


Figure 17. Multipoint Architecture

MULTIDROP CONFIGURATION

Multidrop configuration is similar to multipoint configuration, but only one driver is present on the bus. A multidrop system can be configured with the driver at one end of the bus, or in the middle of the bus. When a driver is located at one end, a single termination resistor is located at the far end, close to the last receiver on the bus. Alternatively, the driver can be located in the middle of the bus, to reduce the maximum flight time. With a centrally located driver, termination resistors are located at each end of the bus. In both cases the termination resistor value should be matched to the loaded bus impedance. Figure 18 shows examples of both cases.

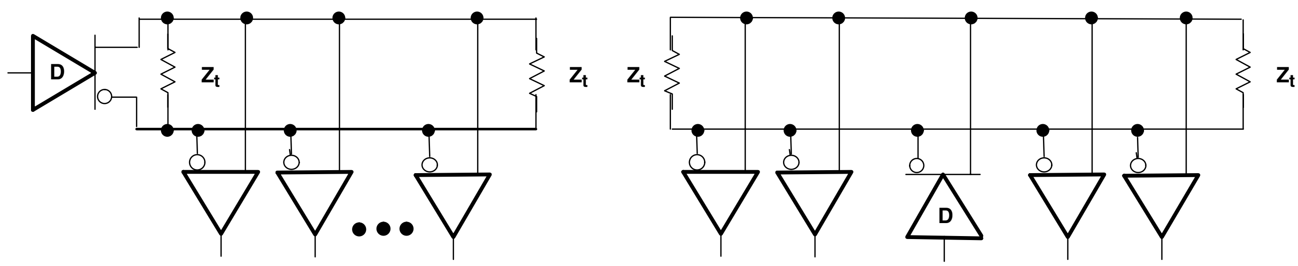


Figure 18. Multidrop Architectures With Different Driver Locations

UNUSED CHANNEL

A 360−kΩ pull−down resistor is built in every LVTTL input. The unused driver inputs should be left floating or connected to ground. The low−level output of an unused enabled driver may oscillate if left floating and should be connected to ground. If the input is floating or connected to ground, the unused Y (non−inverting) output of an enabled driver should be connected to ground. The unused Z (inverting) should be left floating.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65MLVD047AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD047A	Samples
SN65MLVD047ADG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD047A	Samples
SN65MLVD047ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD047A	Samples
SN65MLVD047APW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BUL	Samples
SN65MLVD047APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BUL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

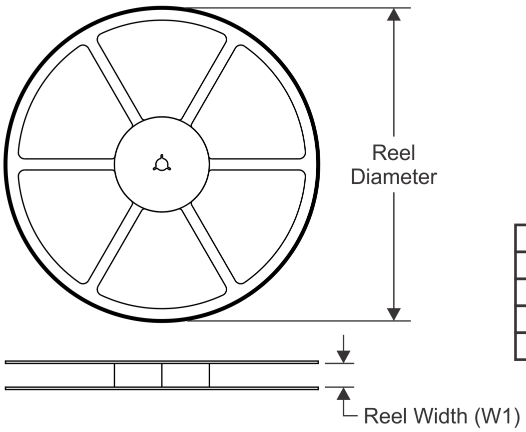
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

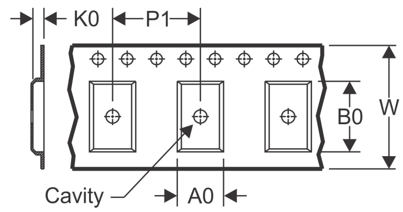
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

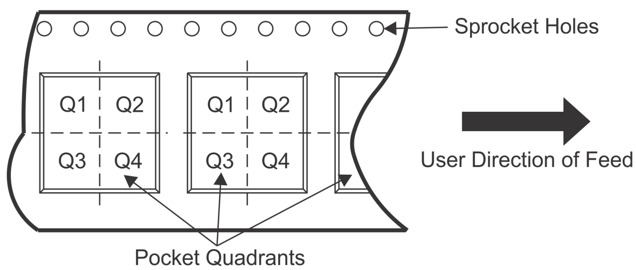


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

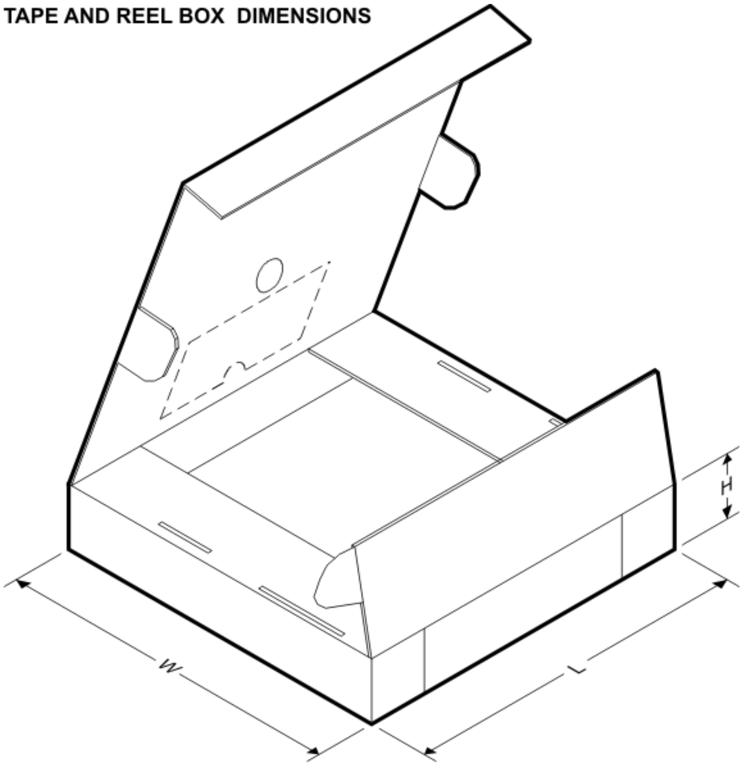
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65MLVD047ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65MLVD047APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

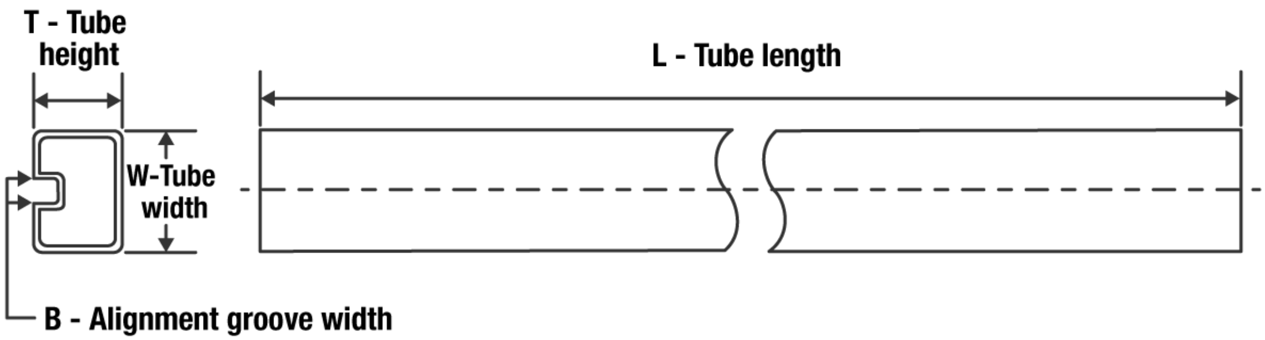
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65MLVD047ADR	SOIC	D	16	2500	350.0	350.0	43.0
SN65MLVD047APWR	TSSOP	PW	16	2000	350.0	350.0	43.0

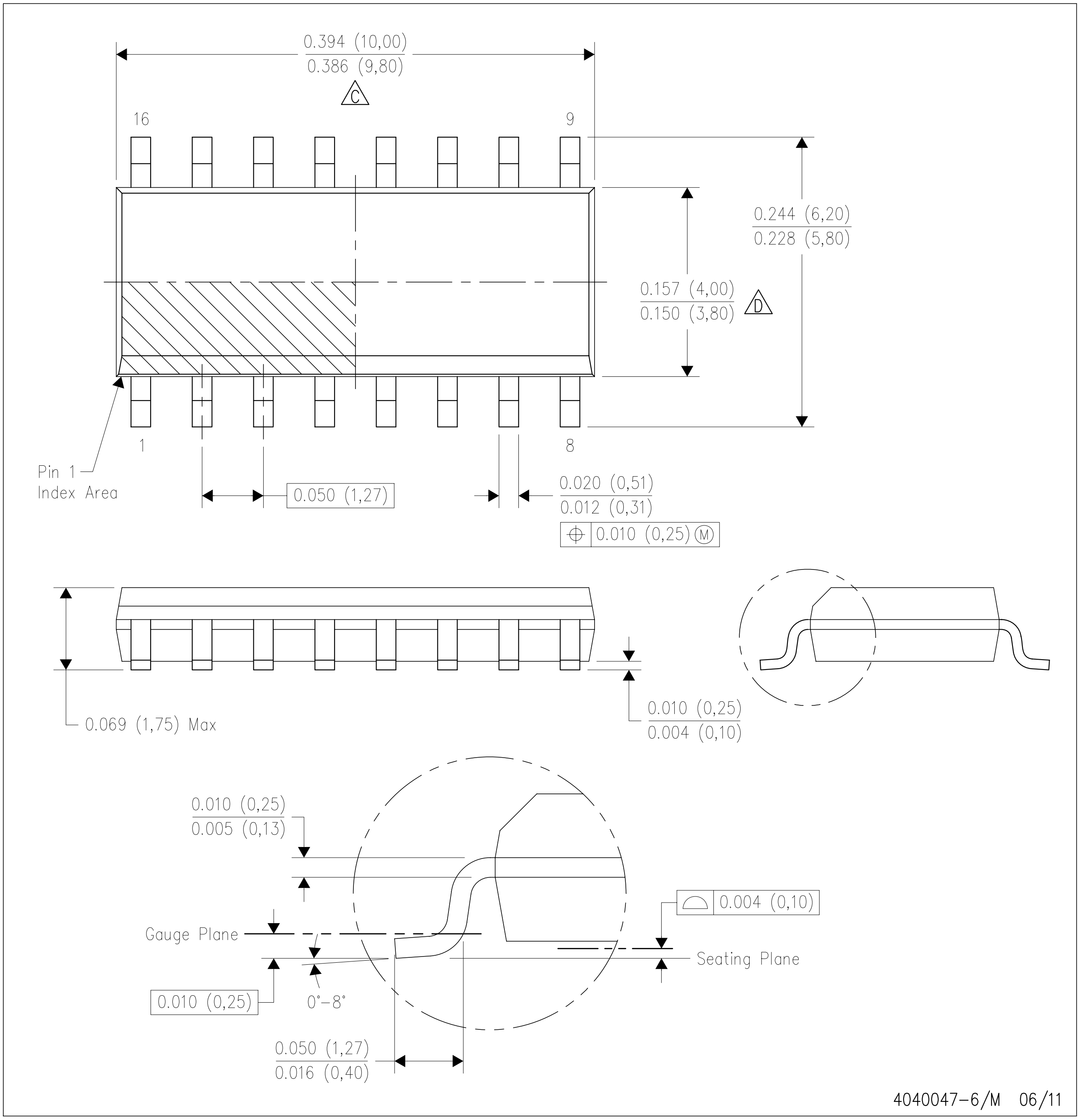
TUBE



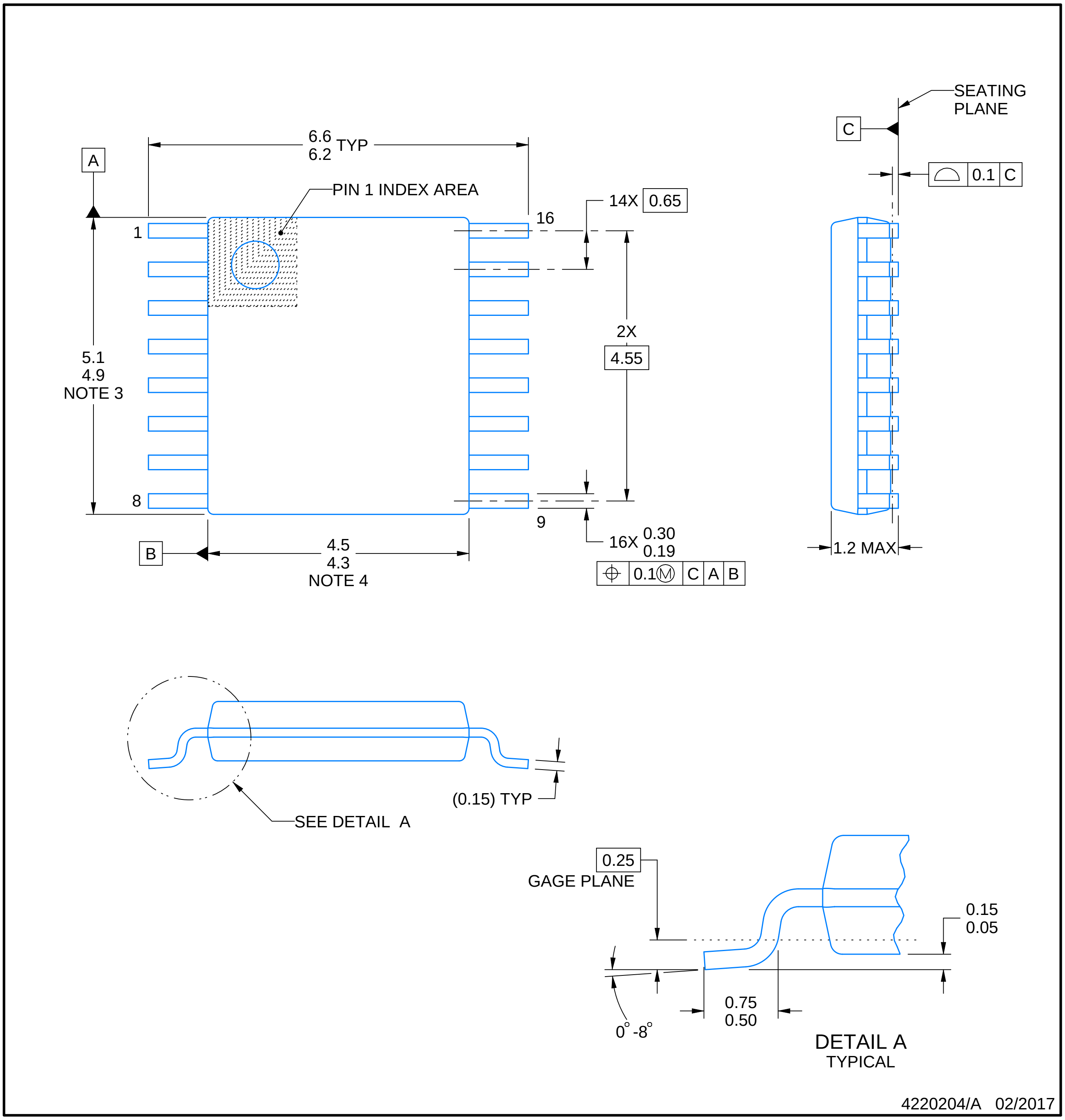
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65MLVD047AD	D	SOIC	16	40	505.46	6.76	3810	4
SN65MLVD047ADG4	D	SOIC	16	40	505.46	6.76	3810	4
SN65MLVD047APW	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R-PDSO-G16) PLASTIC SMALL OUTLINE



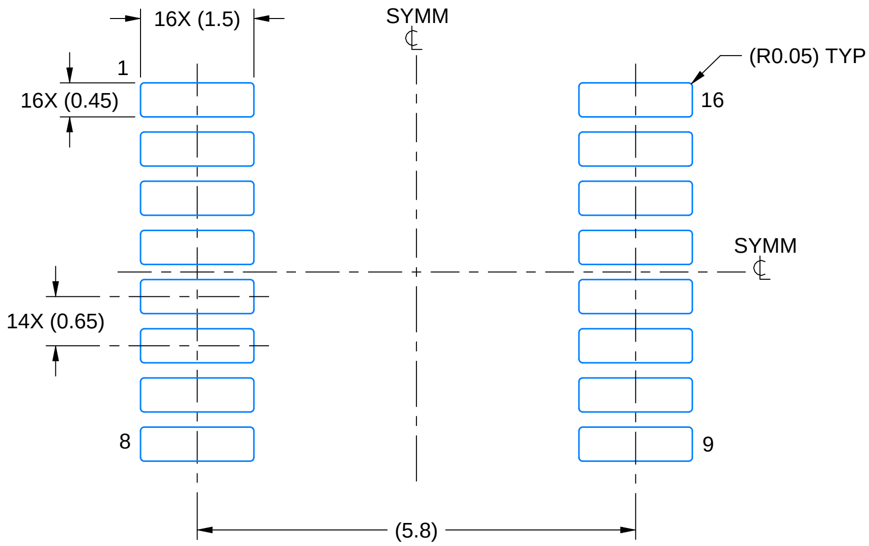
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



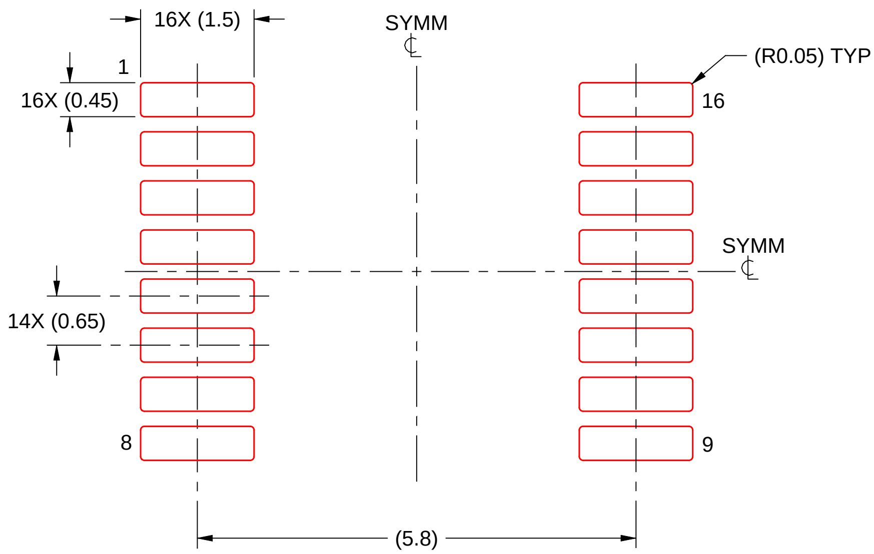
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.