STRUCTURE Silicon Monolithic Integrated Circuit

NAME OF PRODUCT DC-AC Inverter Control IC

TYPE **ＢＤ９２１５Ｆ、ＢＤ９２１５ＦＶ**

FUNCTION
- 36V High voltage process
- 1ch control with Full-Bridge
- Lamp current and voltage sense feed back control
- Sequencing easily achieved with Soft Start Control
- Short circuit protection with Timer Latch
- Under Voltage Lock Out
- Mode-selectable the operating or stand-by mode by stand-by pin
- For master IC, Synchronous operating with BD9898F/FV
- BURST mode controlled by PWM and DC input
- Output liner Control by external DC voltage

○Absolute Maximum Ratings (Ta = 25℃)

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 36 | V |
| BST pin | BST | 40 | V |
| SW pin | SW | 36 | V |
| BST-SW voltage difference | BST-SW | 15 | V |
| Operating Temperature Range | Topr | -40～+85 | ℃ |
| Storage Temperature Range | Tstg | -55～+150 | ℃ |
| Maximum Junction Temperature | Tjmax | +150 | ℃ |
| Power Dissipation | Pd | 749*1 (BD9215F) | mW |
| | | 1062*2 (BD9215FV) | |

*1 Pd derate at 6.0mW/℃ for temperature above Ta = 25℃ (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

*2 Pd derate at 8.5mW/℃ for temperature above Ta = 25℃ (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

○Operating condition

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 16.0～30.0 ※ | V |
| BST voltage | BST | 5.0～37.5 | V |
| BST-SW voltage difference | BST-SW | 5.0～14.0 | V |
| DRIVER frequency | FOUT | 30～110 | kHz |
| BCT oscillation frequency | $f_{BCT}$ | 0.05～1.00 | kHz |

※For Operation condition of Supply voltage, Please see NOTE FOR USE(4page), more information.

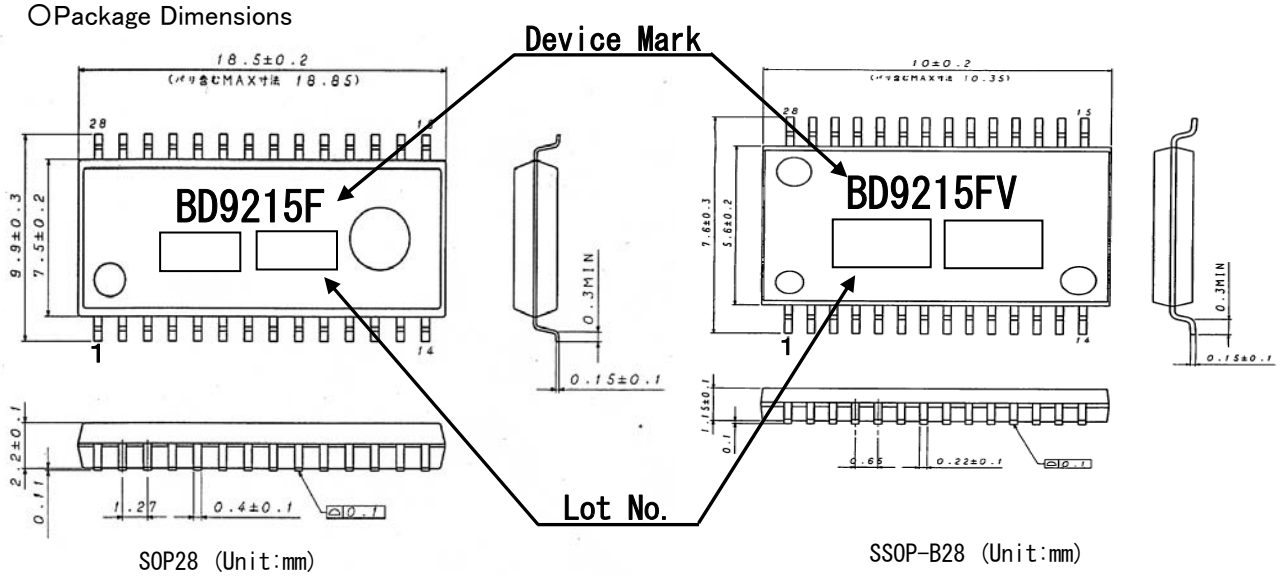
Status of this document
The Japanese version of this document is the official specification.
Please use the translation version of this document as a reference to expedite understanding of the official version.
If these are any uncertainty in translation version of this document, official version takes priority.

## ○Electric Characteristics (Ta=25℃、VCC=24V、STB=UVLO=3.0V)

| Parameter | Symbol | Limits | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | | |
| ((WHOLE DEVICE)) | | | | | | |
| Operating current | Icc1 | — | 5.0 | 9.0 | mA | FOUT=60kHz, FB=GND, BST=OPEN |
| Stand-by current | Icc2 | — | 60 | 140 | μA | |
| ((STAND BY CONTROL)) | | | | | | |
| Stand-by voltage H | VstH | 2 | — | VCC | V | System ON |
| Stand-by voltage L | VstL | -0.3 | — | 0.8 | V | System OFF |
| ((UVLO BLOCK)) | | | | | | |
| Operating voltage (UVLO) | Vuvlo | 2.16 | 2.25 | 2.34 | V | |
| Hesteresis width (UVLO) | ⊿Vuvlo | 0.085 | 0.110 | 0.135 | V | |
| ((REG BLOCK)) | | | | | | |
| REG output voltage | VREG | 7.35 | 7.50 | 7.65 | V | |
| REG source current | IREG | 20 | — | — | mA | |
| ((OSC BLOCK)) | | | | | | |
| RT pin Voltage | VRT | 1.05 | 1.50 | 1.95 | V | |
| Soft start current | ISS | 1.7 | 2.2 | 2.7 | μA | |
| SS operation start Voltage | VSS_ST | 0.18 | 0.20 | 0.22 | V | |
| SS term END Voltage | VSS_ED | 1.35 | 1.50 | 1.65 | V | |
| SRT ON resistance | RSRT | — | 85 | 170 | Ω | |
| ((BOSC BLOCK)) | | | | | | |
| BOSC Max voltage | VBCTH | 1.94 | 2 | 2.06 | V | fBCT=0.3kHz |
| BOSC Min voltage | VBCTL | 0.4 | 0.5 | 0.6 | V | fBCT=0.3kHz |
| BOSC constant current | IBCT | 1.35/BRT | 1.5/BRT | 1.65/BRT | A | VBCT=0.2V |
| BOSC frequency | fBCT | 291 | 300 | 309 | Hz | (BRT=37.8kΩ BCT=0.047μF) |
| ((FEED BACK BLOCK)) | | | | | | |
| IS threshold voltage 1 | VIS1 | 1.225 | 1.25 | 1.275 | V | |
| IS threshold voltage 2 | VIS2 | — | VREFIN | VIS1 | V | VREF applying voltage |
| VS threshold voltage | VVS | 1.22 | 1.25 | 1.28 | V | |
| IS source current 1 | IIS1 | — | — | 0.9 | μA | DUTY=2.2V |
| IS source current 2 | IIS2 | 40 | 50 | 60 | μA | DUTY=0V IS=1.0V |
| VS source current | IVS | — | — | 0.9 | μA | |
| IS COMP detect voltage 1 | VISCOMP1 | 0.606 | 0.625 | 0.644 | V | VREFIN≧1.25V |
| IS COMP detect voltage 2 | VISCOMP2 | — | 0.50 | — | V | VREFIN= 1V |
| VREF input voltage range | VREFIN | 0.6 | — | 1.6 | V | No effect at VREF＞1.25V |
| ((DUTY BLOCK)) | | | | | | |
| High voltage | VDUTY-OUTH | 3.8 | 4.0 | 4.2 | V | |
| Low voltage | VDUTY-OUTL | — | - | 0.5 | V | |
| DUTY-OUT sink resistance | RDUTY-OUT_sink | — | 150 | 300 | Ω | |
| DUTY-OUT source resistance | RDUTY-OUT_source | — | 300 | 600 | Ω | |
| ((OUTPUT BLOCK)) | | | | | | |
| LN output sink resistance | RsinkLN | 1.8 | 3.5 | 7.0 | Ω | |
| LN output source resistance | RsourceLN | 4.5 | 9.0 | 18.0 | Ω | |
| HN output sink resistance | RsinkHN | 1.8 | 3.5 | 7.0 | Ω | VBST-VSW=7.0V |
| HN output source resistance | RsourceLN | 4.5 | 9.0 | 18.0 | Ω | VBST-VSW=7.0V |
| MAX DUTY | MAX DUTY | 46.0 | 48.5 | 49.5 | % | FOUT=60kHz |
| OFF period | TOFF | 100 | 200 | 400 | ns | |
| Drive output frequency | FOUT | 57.9 | 60 | 62.1 | kHz | RT=21k Ω |
| ((TIMER LATCH BLOCK)) | | | | | | |
| Timer Latch setting voltage | VCP | 3.88 | 4.0 | 4.12 | V | |
| Timer Latch setting current | ICP | 1.6 | 2.1 | 2.6 | μA | |
| ((COMP BLOCK)) | | | | | | |
| COMP over voltage detect voltage | VCOMPH | 3.88 | 4.0 | 4.12 | V | VSS＞1.65V |
| Hysterisis width (COMP) | ⊿VCOMPH | 0.15 | 0.20 | 0.25 | V | |
| ((Synchronous Block)) | | | | | | |
| High voltage | VCT_SYNCH | 3.8 | 4.0 | 4.2 | V | |
| Low voltage | VCT_SYNCL | — | — | 0.5 | V | |
| CT_SYNC_OUT sink resistance | RSYNC_OUT_sink | — | 150 | 300 | Ω | |
| CT_SYNC_OUT source resistance | RSYNC_OUT_source | — | 300 | 400 | Ω | |

(This product is not designed to be radiation-resistant.)

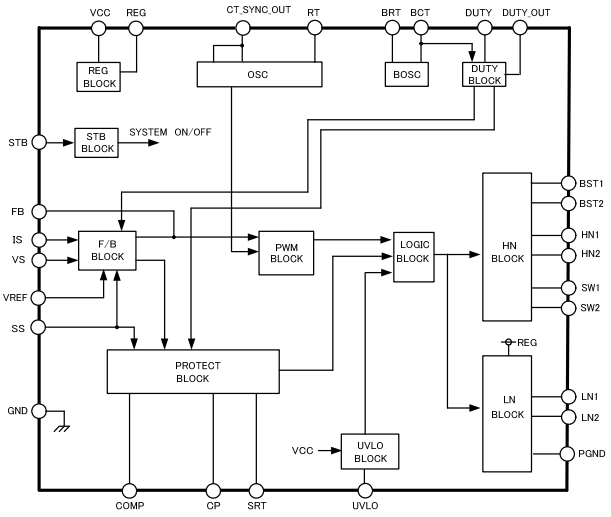
○Package Dimensions




SOP28 (Unit:mm)

SSOP-B28 (Unit:mm)

○Block Diagram




○Pin Description

| PIN No. | PIN NAME | FUNCTION |
|---|---|---|
| 1 | PGND | Ground for FET drivers |
| 2 | LN2 | NMOS FET driver |
| 3 | HN2 | NMOS FET driver |
| 4 | SW2 | Lower rail voltage for HN2 output |
| 5 | BST2 | Boot-Strap input for HN2 output |
| 6 | DUTY_OUT | BURST signal output pin |
| 7 | CT_SYNC_OUT | CT synchronous signal output pin |
| 8 | SRT | External resistor from SRT to RT for adjusting the start-up triangle oscillator |
| 9 | RT | External resistor from RT to GND for adjusting the triangle oscillator |
| 10 | GND | GROUND |
| 11 | BCT | External capacitor from BCT to GND for adjusting the BURST triangle oscillator |
| 12 | BRT | External resistor from BRT to GND for adjusting the BURST triangle oscillator |
| 13 | DUTY | Control PWM mode and BURST mode |
| 14 | STB | Stand-by switch |
| 15 | CP | External capacitor from CP to GND for Timer Latch |
| 16 | VREF | Reference voltage input pin for Error amplifier |
| 17 | VS | Error amplifier input |
| 18 | IS | Error amplifier input |
| 19 | FB | Error amplifier output |
| 20 | SS | External capacitor from SS to GND for Soft Start Control |
| 21 | COMP | Over voltage detect pin |
| 22 | VCC | Supply voltage input |
| 23 | UVLO | External Under Voltage Lock Out |
| 24 | REG | Internal regulator output |
| 25 | BST1 | Boot-Strap input for HN1 output |
| 26 | SW1 | Lower rail voltage for HN1 output |
| 27 | HN1 | NMOS FET driver |
| 28 | LN1 | NMOS FET driver |

○NOTE FOR USE

1. This product is produced with strict quality control, but might be destroyed if used beyond its absolute maximum ratings. Once IC is destroyed, failure mode will be difficult to determine, like short mode or open mode. Therefore, physical protection countermeasure, like fuse is recommended in case operating conditions go beyond the expected absolute maximum ratings.
2. The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however the variation will be small. When it is used in between STB-UVLO Diode short etc., the IC can operate VCC≧9V. Please refer to a Technical Note in detail.
3. Mounting failures, such as misdirection or miscounts, may harm the device.
4. A strong electromagnetic field may cause the IC to malfunction.
5. The GND pin should be the location within ±0.3V compared with the PGND pin. ALL Pin (except BST1, BST2, HN1, HN2,) Voltage should be under VCC voltage +0.3V
6. BD9215F, BD9215FV incorporate a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation of the thermal shutdown circuit is assumed.
7. When modifying the external circuit components, make sure to leave an adequate margin for external components actual value and tolerance as well as dispersion of the IC.
8. About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
9. Under operating CP charge (under error mode) analog dimming and burst dimming are not operate.
10. Under operating Slow Start Control (SS is less than 1.5V), It does not operate Timer Latch.
11. By STB voltage, BD9215F, BD9215FV are changed to 2 states. Therefore, do not input STB pin voltage between one state and the other state (0.8～2.0V).
12. The pin connected a connector need to connect to the resistor for electrical surge destruction.
13. This IC is a monolithic IC which (as shown is Fig-1) has $P^+$ substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows,

    ○(When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)
    ○(When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)

    Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin.

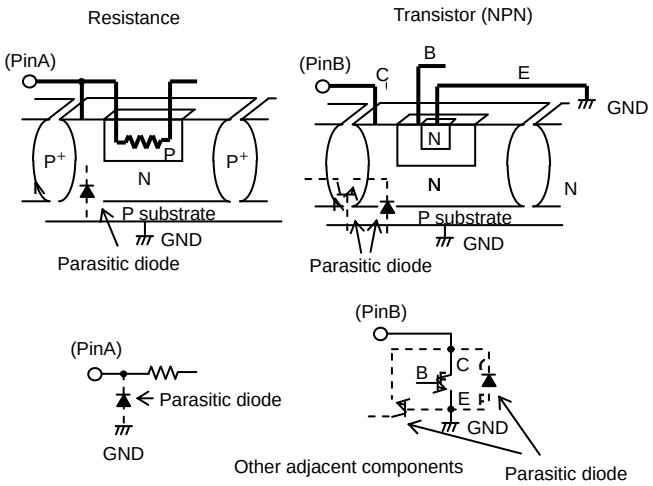



Fig-1 Simplified structure of a Bipolar IC

## Notes

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