bq769x0 3-Series to 15-Series Cell Battery Monitor Family for Li-Ion and Phosphate Applications

ECCN: EAR99

1 Introduction

1.1 Features

- AFE MONITORING FEATURES
  - Pure digital interface
  - Internal ADC measures cell voltage, die temperature, and external thermistor
  - A separate, internal ADC measures pack current (coulomb counter)
  - Directly supports up to three thermistors (103AT)
- HARDWARE PROTECTION FEATURES
  - Overcurrent in discharge (OCD)
  - Short circuit in discharge (SCD)
  - Overvoltage (OV)
  - Undervoltage (UV)
  - Secondary protector fault detection
- ADDITIONAL FEATURES
  - Integrated cell balancing FETs
  - Charge, discharge low-side NCH FET drivers
  - Alert interrupt to host microcontroller
  - 2.5-V or 3.3-V output voltage regulator
  - No EEPROM programming necessary
  - High supply voltage abs max (up to 108 V)
  - Simple I^2C™ compatible interface (CRC option)
  - Random cell connection tolerant

1.2 Applications

- Light Electric Vehicles (LEV): eBikes, eScooters, Pedelec, and Pedal-Assist Bicycles
- Power and Gardening Tools
- Battery Backup and UPS Systems
- Wireless Base Station Backup Systems
- 12-V, 18-V, 24-V, 36-V, and 48-V Battery Packs

1.3 Description

The bq769x0 family of robust analog front-end (AFE) devices serves as part of a complete pack monitoring and protection solution for next-generation, high-power systems, such as light electric vehicles, power tools, and uninterruptible power supplies. The bq769x0 is designed with low power in mind; sub-blocks within the IC may be enabled/disabled to control the overall chip current consumption, and a SHIP mode provides a simple way to put the pack into an ultra-low power state.

The bq76920 device supports up to 5-series cells or typical 18-V packs; the bq76930 handles up to 10-series cells or typical 36-V packs; and the bq76940 works for up to 15-series cells or typical 48-V packs. A variety of battery chemistries may be managed with these AFEs, including Lithium Ion, Lithium iron phosphate, and more.

Via I^2C, a host controller may use the bq769x0 to implement many battery pack management functions, such as monitoring (cell voltages, pack current, pack temperatures), protection (controlling charge/discharge FETs), and balancing. Integrated A/D converters enable a purely digital readout of critical system parameters, with calibration handled in TI's manufacturing process.

For an additional degree of pack reliability, the bq769x0 includes hardware protections for voltage (OV, UV) and current (OCD, SCD). Texas Instruments pre-programs them to specific thresholds and delays, which may be updated by the host microcontroller during pack startup.

For control of power FETs, the bq769x0 provides two low-side FET drivers: charge and discharge. These may be used to directly manipulate low-side power NCH FETs, or as signals that control an external circuit that enables high-side PCH or NCH FETs. A dedicated ALERT input/output pin serves as an interrupt signal to the host microcontroller, quickly informing the microcontroller of an updated status in the AFE. This may include a fault event or that a coulomb counter sample is available for reading. The ALERT pin may also be driven externally by a secondary protector to provide a redundant means of disabling the CHG and DSG signals and higher system visibility.

Table of Contents

1.1 Device Comparison Table

TUBE	TAPE & REEL	CELLS	I²C ADDRESS (7-Bit)	LDO (V)	CRC	PACKAGE
bq7692000PW(1)	bq7692000PWR(1)	3–5	0x08	2.5	No	20-TSSOP (PW)
bq7692001PW(1)	bq7692001PWR(1)				Yes	
bq7692002PW(1)	bq7692002PWR(1)			3.3	No	
bq7692003PW(1)	bq7692003PWR(1)				Yes	
bq7692006PW	bq7692006PWR		0x18		No	
bq7693000DBT(1)	bq7693000DBTR(1)	6–10	0x08	2.5	No	30-TSSOP (DBT)
bq7693001DBT(1)	bq7693001DBTR(1)				Yes	
bq7693002DBT(1)	bq7693002DBTR(1)			3.3	No	
bq7693003DBT	bq7693003DBTR				Yes	
bq7693006DBT	bq7693006DBTR		0x18		No	
bq7694000DBT	bq7694000DBTR	9–15	0x08	2.5	No	44-TSSOP (DBT)
bq7694001DBT	bq7694001DBTR				Yes	
bq7694002DBT	bq7694002DBTR			3.3	No	
bq7694003DBT	bq7694003DBTR				Yes	
bq7694006DBT	bq7694006DBTR		0x18		No	

(1) Product Preview only

Texas Instruments pre-configures the bq769x0 devices for a specific I²C address, LDO voltage, and more. These settings are permanently stored in EEPROM and cannot be further modified.

Contact Texas Instruments for other options not listed above, as well as any options noted as “Product Preview only.”

1.2 Thermal Information

THERMAL METRIC(1)		TSSOP			UNITS
		bq76920xy 20 Pins (PW)	bq76930xy 30 Pins (DBT)	bq76940xy 44 Pins (DBT)	
$R_{\theta JA, High K}$	Junction-to-ambient thermal resistance(2)	93.7	86.5	70.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance(3)	28.7	19.4	17.5	
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	44.6	41.3	33.9	
ψ_{JT}	Junction-to-top characterization parameter(5)	1.3	0.5	0.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	44.1	40.6	33.4	
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance(7)	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

2 Terminal Diagrams and Descriptions

2.3 Versions

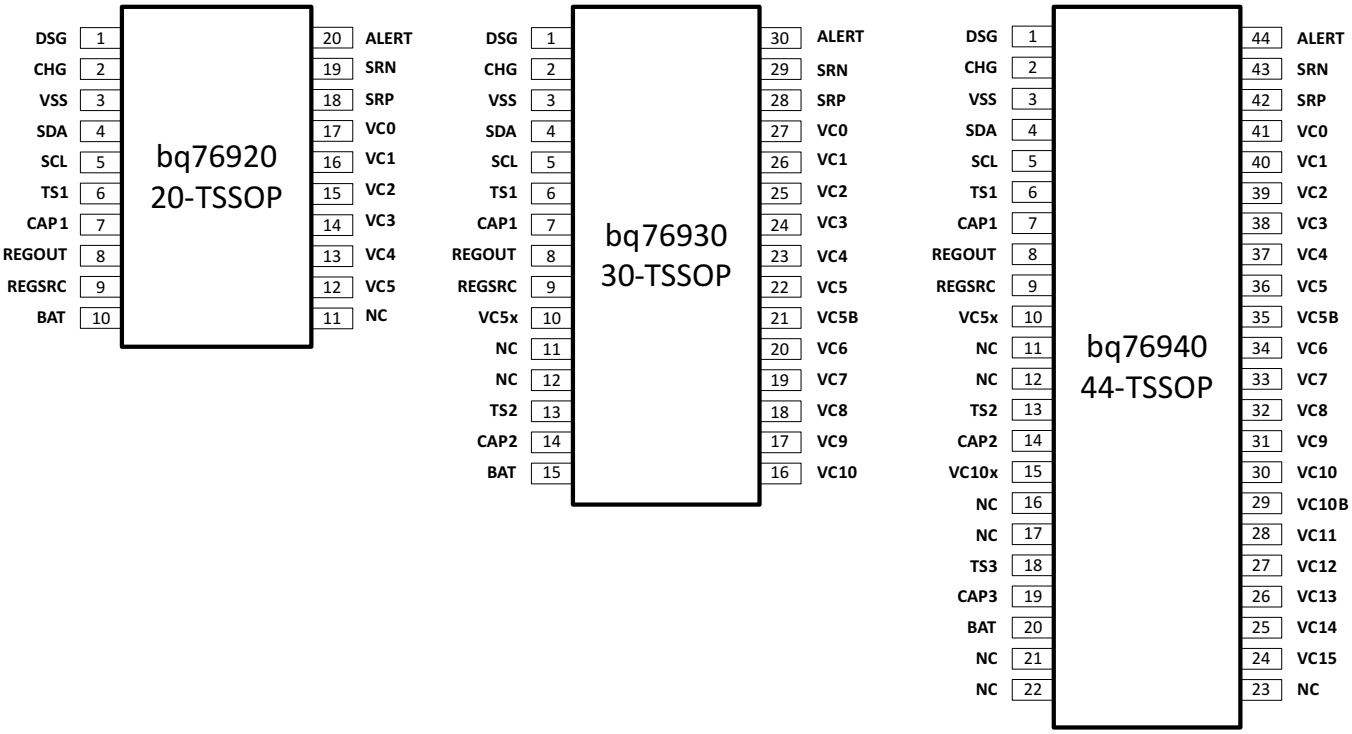


Figure 2-1. Terminal Versions

bq76920: 3-5 Series Cells (20-TSSOP)

- 6.5 mm x 4.4 mm x 1.2 mm

bq76930: 6-10 Series Cells (30-TSSOP)

- 7.8 mm x 4.4 mm x 1.2 mm

bq76940: 9-15 Series Cells (44-TSSOP)

- 11.3 mm x 4.4 mm x 1.2 mm

2.4 bq76920 Terminal Diagram

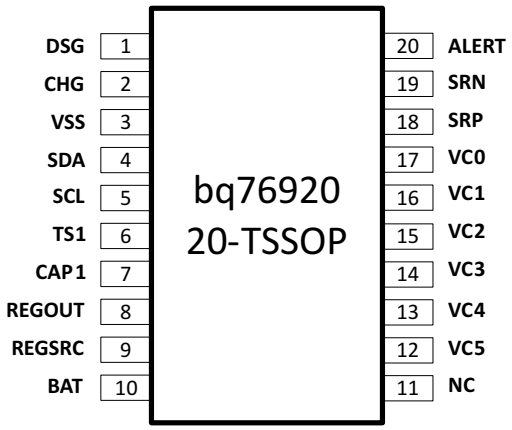


Figure 2-2. bq76920 Terminal Diagram

2.4.1 bq76920 Terminal Map

Table 2-1. bq76920 Terminal Functions

TERMINAL	NAME	TYPE	DESCRIPTION
1	DSG	O	Discharge FET driver
2	CHG	O	Charge FET driver
3	VSS	—	Chip VSS
4	SDA	I/O	I^2C communication to the host controller
5	SCL	I/O	I^2C communication to the host controller
6	TS1	I	Thermistor #1 positive terminal
7	CAP1	O	Capacitor to VSS
8	REGOUT	P	Output LDO
9	REGSRC	I	Input source for output LDO
10	BAT	P	Battery (top-most) terminal
11	NC	—	No connect
12	VC5	I	Sense voltage for 5th cell positive terminal
13	VC4	I	Sense voltage for 4th cell positive terminal
14	VC3	I	Sense voltage for 3rd cell positive terminal
15	VC2	I	Sense voltage for 2nd cell positive terminal
16	VC1	I	Sense voltage for 1st cell positive terminal
17	VC0	I	Sense voltage for 1st cell negative terminal
18	SRP	I	Negative current sense (nearest VSS)
19	SRN	I	Positive current sense
20	ALERT	I/O	Alert output and override input

2.5 bq76930 Terminal Diagram

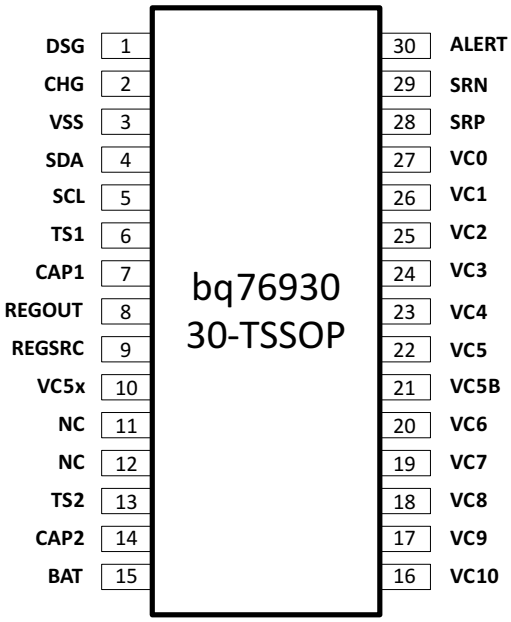


Figure 2-3. bq76930 Terminal Diagram

2.5.1 bq76930 Terminal Map

Table 2-2. bq76930 Terminal Functions

TERMINAL	NAME	TYPE	DESCRIPTION
1	DSG	O	Discharge FET driver
2	CHG	O	Charge FET driver
3	VSS	—	Chip VSS
4	SDA	I/O	I^2C communication to the host controller
5	SCL	I/O	I^2C communication to the host controller
6	TS1	I	Thermistor #1 positive terminal
7	CAP1	O	Capacitor to VSS
8	REGOUT	P	Output LDO
9	REGSRC	I	Input source for output LDO
10	VC5X	I	Thermistor #2 negative terminal
11	NC	—	No connect (short to CAP2)
12	NC	—	No connect (short to CAP2)
13	TS2	I	Thermistor #2 positive terminal
14	CAP2	O	Capacitor to VC5X
15	BAT	P	Battery (top-most) terminal
16	VC10	I	Sense voltage for 10th cell positive terminal
17	VC9	I	Sense voltage for 9th cell positive terminal
18	VC8	I	Sense voltage for 8th cell positive terminal
19	VC7	I	Sense voltage for 7th cell positive terminal
20	VC6	I	Sense voltage for 6th cell positive terminal
21	VC5B	I	Sense voltage for 6th cell negative terminal
22	VC5	I	Sense voltage for 5th cell positive terminal

Table 2-2. bq76930 Terminal Functions (continued)

TERMINAL	NAME	TYPE	DESCRIPTION
23	VC4	I	Sense voltage for 4th cell positive terminal
24	VC3	I	Sense voltage for 3rd cell positive terminal
25	VC2	I	Sense voltage for 2nd cell positive terminal
26	VC1	I	Sense voltage for 1st cell positive terminal
27	VC0	I	Sense voltage for 1st cell negative terminal
28	SRP	I	Negative current sense (nearest VSS)
29	SRN	I	Positive current sense
30	ALERT	I/O	Alert output and override input

2.6 bq76940 Terminal Diagram

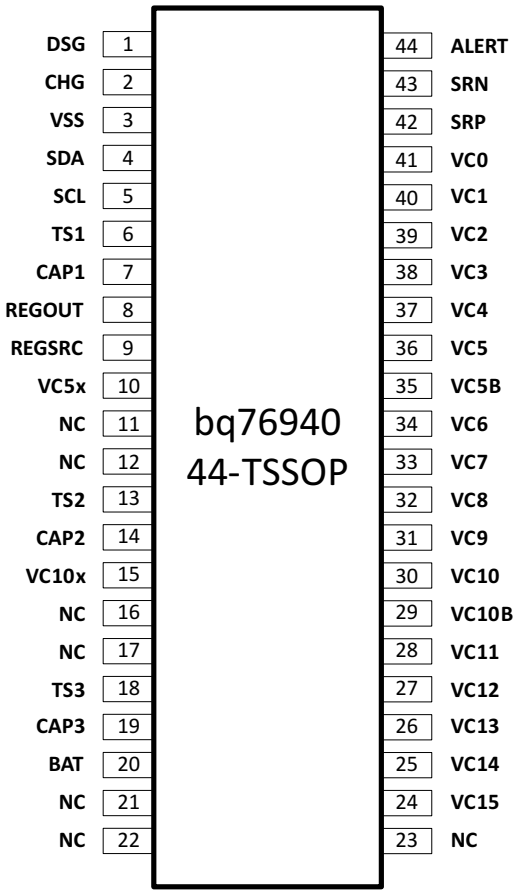


Figure 2-4. bq76940 Terminal Diagram

2.6.1 bq76940 Terminal Map

Table 2-3. bq76940 Terminal Functions

TERMINAL	NAME	TYPE	DESCRIPTION
1	DSG	O	Discharge FET driver
2	CHG	O	Charge FET driver
3	VSS	—	Chip VSS
4	SDA	I/O	I^2C communication to the host controller
5	SCL	I/O	I^2C communication to the host controller
6	TS1	I	Thermistor #1 positive terminal
7	CAP1	O	Capacitor to VSS
8	REGOUT	P	Output LDO
9	REGSRC	I	Input source for output LDO
10	VC5X	I	Thermistor #2 negative terminal
11	NC	—	No connect (short to CAP2)
12	NC	—	No connect (short to CAP2)
13	TS2	I	Thermistor #2 positive terminal
14	CAP2	O	Capacitor to VC5X

Table 2-3. bq76940 Terminal Functions (continued)

TERMINAL	NAME	TYPE	DESCRIPTION
15	VC10X	I	Thermistor #3 negative terminal
16	NC	—	No connect (short to CAP3)
17	NC	—	No connect (short to CAP3)
18	TS3	I	Thermistor #3 positive terminal
19	CAP3	O	Capacitor to VC10X
20	BAT	P	Battery (top-most) terminal
21	NC	—	No connect
22	NC	—	No connect
23	NC	—	No connect
24	VC15	I	Sense voltage for 15th cell positive terminal
25	VC14	I	Sense voltage for 14th cell positive terminal
26	VC13	I	Sense voltage for 13th cell positive terminal
27	VC12	I	Sense voltage for 12th cell positive terminal
28	VC11	I	Sense voltage for 11th cell positive terminal
29	VC10B	I	Sense voltage for 10th cell negative terminal
30	VC10	I	Sense voltage for 10th cell positive terminal
31	VC9	I	Sense voltage for 9th cell positive terminal
32	VC8	I	Sense voltage for 8th cell positive terminal
33	VC7	I	Sense voltage for 7th cell positive terminal
34	VC6	I	Sense voltage for 6th cell positive terminal
35	VC5B	I	Sense voltage for 6th cell negative terminal
36	VC5	I	Sense voltage for 5th cell positive terminal
37	VC4	I	Sense voltage for 4th cell positive terminal
38	VC3	I	Sense voltage for 3rd cell positive terminal
39	VC2	I	Sense voltage for 2nd cell positive terminal
40	VC1	I	Sense voltage for 1st cell positive terminal
41	VC0	I	Sense voltage for 1st cell negative terminal
42	SRP	I	Negative current sense (nearest VSS)
43	SRN	I	Positive current sense
44	ALERT	I/O	Alert output and override input

2.7 Simplified Application Schematics

CAUTION

The external circuitry shown in the following schematics are a minimum requirement to ensure device robustness, during both cell connection to the PCB and normal operation. For more detailed guidance, please refer to the Reference Schematic (when available).

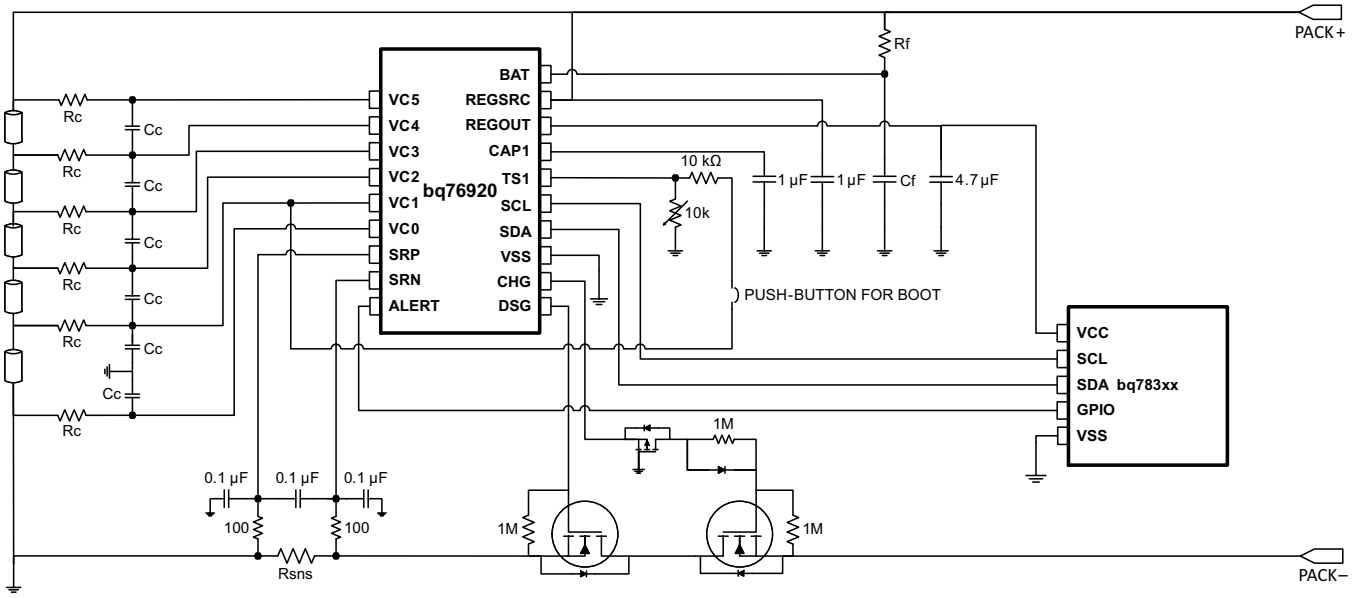


Figure 2-5. bq76920 with bq783xx Companion Controller IC

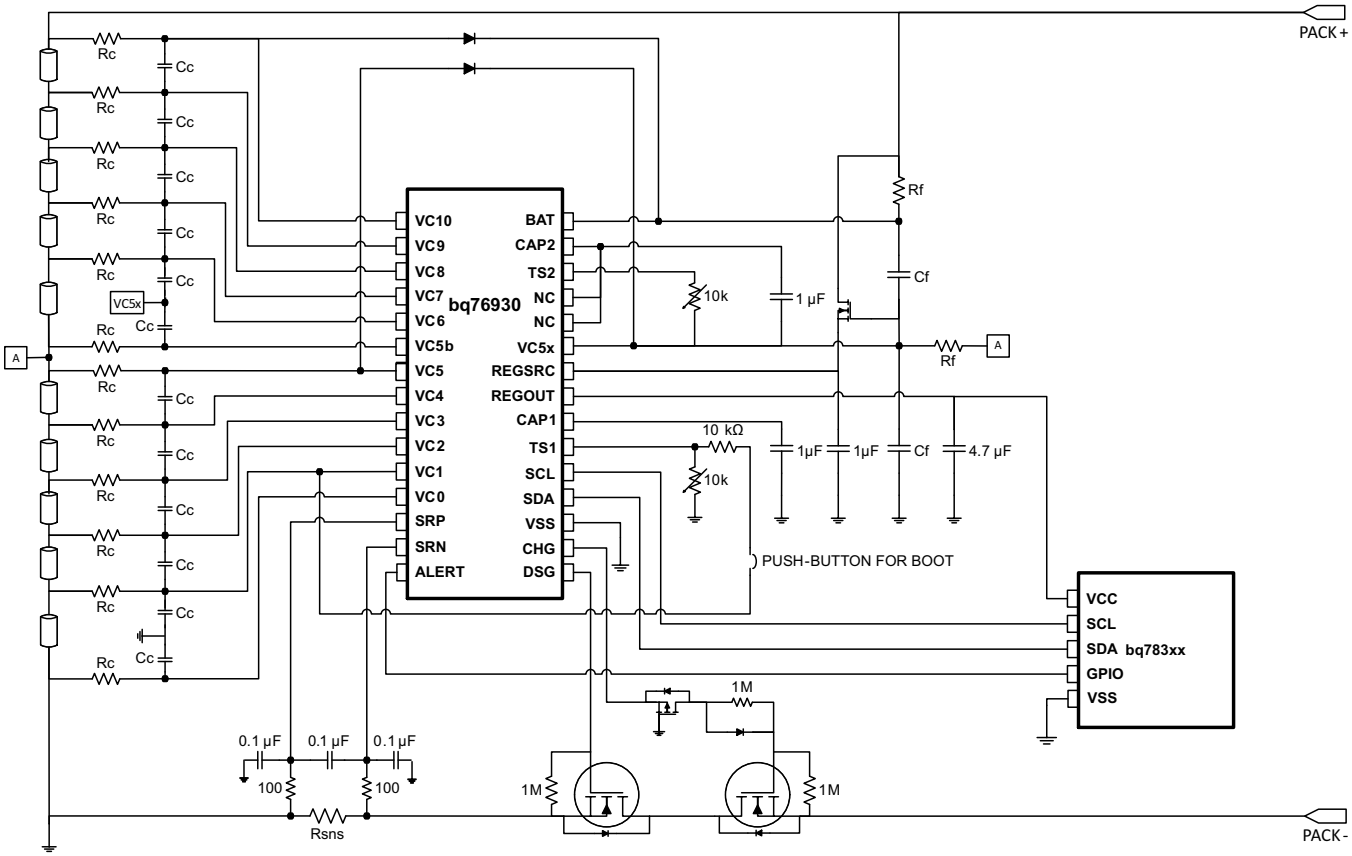


Figure 2-6. bq76930 with bq783xx Companion Controller IC

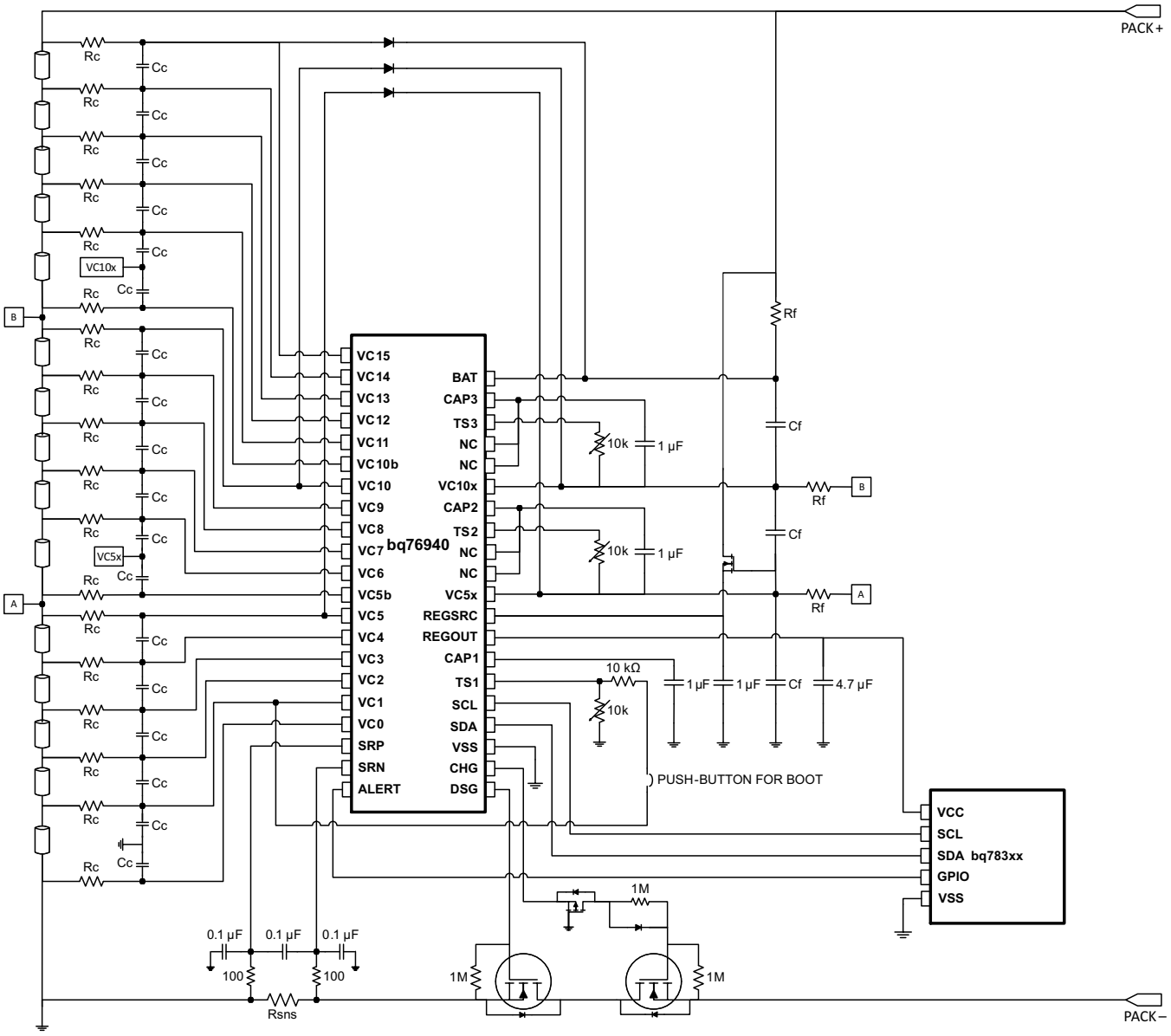
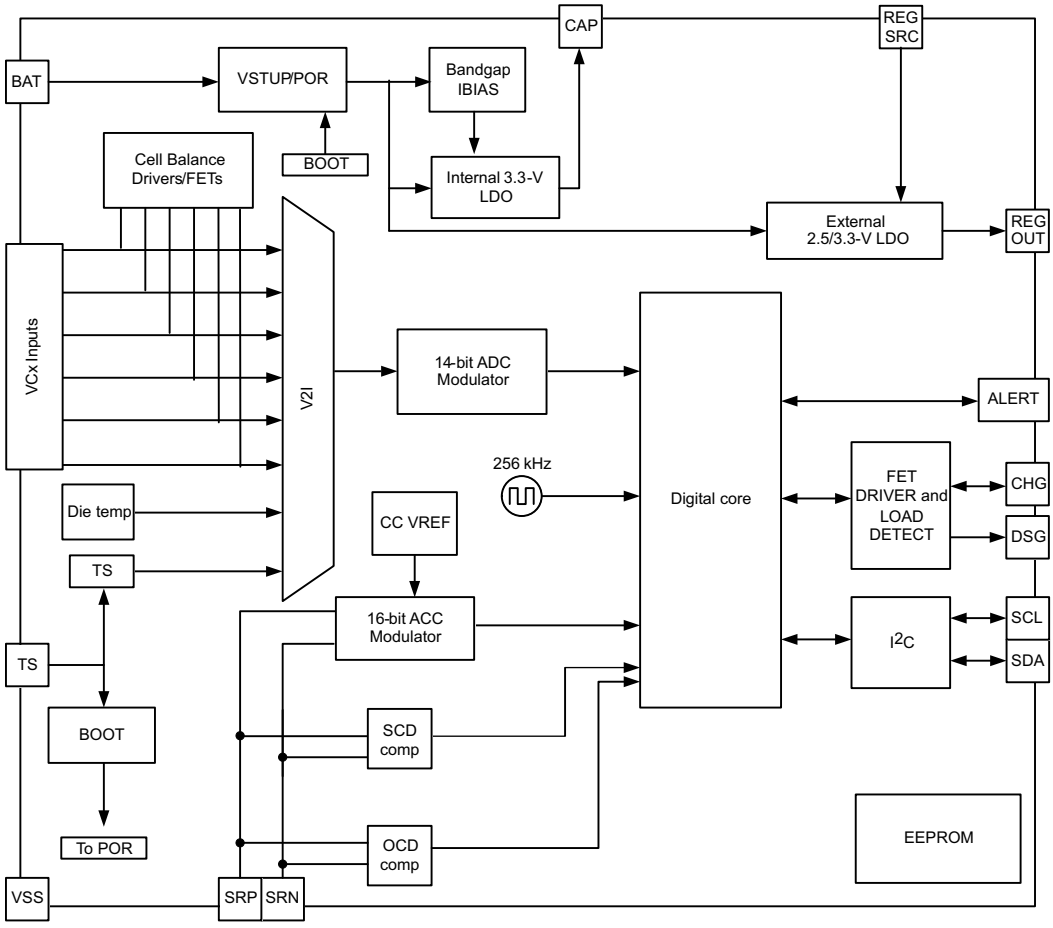


Figure 2-7. bq76940 with bq783xx Companion Controller IC

2.8 Functional Block Diagram



3 Electrical Specifications

3.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

PARAMETER				RANGE (1)
V_{BAT}	Supply voltage range	(BAT–VSS)	bq76920	–0.3 to 36
		(BAT–VC5x), (VC5x–VSS)	bq76930	
		(BAT–VC10x), (VC10x–VC5x), (VC5x–VSS)	bq76940	
V_I	Input voltage range	(VCn–VSS) where n = 1..5	bq76920	–0.3 to (n x 7.2)
		(VCn–VSS) where n = 1..5, (VCn-VC5x) where n = 6..10	bq76930	
		(VCn–VSS) where n = 1..5, (VCn–VC5x) where n = 6..10, (VCn–VC10x) where n = 11..15	bq76940	
		Cell input pins, differential (VCn–VCn–1) where n = 1..15/10/5 (bq76940/bq76930/bq76920, respectively)		–0.3 to 9
		SRN, SRP, SCL, SDA		–0.3 to 3.6
		(VC0–VSS), (CAP1–VSS), (TS1–VSS)	bq76920	
		(VC0–VSS), (VC5b–VC5x), (CAP2–VC5x), (CAP1–VSS), (TS2–VC5x), (TS1–VSS)	bq76930	
		(VC0–VSS), (VC5b–VC5x), (VC10b–VC10x), (CAP3–VC10x), (CAP2–VC5x), (CAP1–VSS), (TS3–VC10x), (TS2–VC5x), (TS1–VSS)	bq76940	
		REGSRC		–0.3 to 36
V_O	Output voltage range	REGOUT, ALERT		–0.3 to 3.6
		DSG		–0.3 to 20
		CHG		–0.3 to $V_{CHGCLAMP}$
ESD (HBM)		All pins		2 kV
ESD (CDM)		All pins		500 V
I_{CB}	Cell balancing current (per cell)		bq76920	70 mA
			bq76930, bq76940	5 mA
I_{DSG}	Discharge terminal input current when disabled (measured into terminal)			7 mA
T_{STG}	Storage temperature range			–65 to 150°C
	Lead temperature (soldering, 10 s)			300°C

3.2 Recommended Operating Conditions

Over-operating free-air temperature range (unless otherwise noted)

NOTE

See Section 6 for more information on cell configurations. All voltages are relative to VSS, except "Cell input differential."

PARAMETER				MIN	TYP	MAX	UNIT
V_{BAT}	Supply voltage range	(BAT–VSS)	bq76920	6		25	V
		(BAT–VC5x), (VC5x–VSS)	bq76930				
		(BAT–VC10x), (VC10x–VC5x), (VC5x–VSS)	bq76940				

Over-operating free-air temperature range (unless otherwise noted)

PARAMETER				MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	Cell input pins, differential (VCn–VCn–1) where n = 1..15/10/5 (bq76940/bq76930/bq76920, respectively), in-use cells only		2		5	V
		(VCn–VSS) where n = 1..5	bq76920	0		5 × n	V
		(VCn–VSS) where n = 1..5, (VCn–VC5x) where n = 6..10	bq76930				
		(VCn–VSS) where n = 1..5, (VCn–VC5x) where n = 6..10, (VCn–VC10x) where n = 11..15	bq76940				
		SRP		–10		10	mV
		(VC0–VSS)	bq76920				
		(VC0–VSS), (VC5b–VC5x)	bq76930				
		(VC0–VSS), (VC5b–VC5x), (VC10b–VC10x)	bq76940				
		SRN		–200		200	mV
		SCL, SDA		0		3.6	V
		(TS1–VSS)	bq76920				
		(TS1–VSS), (TS2–VC5x)	bq76930				
		(TS1–VSS), (TS2–VC5x), (TS3–VC10x)	bq76940				
		REGSRC		6		25	
V_{OUT}	Output voltage range	CHG, DSG		0		16	V
		REGOUT, ALERT		0		3.6	V
		(CAP1–VSS)	bq76920				
		(CAP1–VSS), (CAP2–VC5x)	bq76930				
		(CAP1–VSS), (CAP2–VC5x), (CAP3–VC10x)	bq76940				
I_{CB}	Cell balancing current (internal, per cell)	bq76920		0		50	mA
		bq76930, bq76940		0		5	mA
R_C	External cell input resistance	bq76920		40	100	1K	Ω
		bq76930, bq76940		500	1K	1K	Ω
C_C	External cell input capacitance			0.1	1	10	µF
R_f	External supply filter resistance			40	100	1K	Ω
C_f	External supply filter capacitance			1	10	40	µF
R_{FILT}	Sense resistor filter resistance			100	1K		Ω
R_{ALERT}	ALERT terminal to VSS resistor				1M		Ω
C_L	REGOUT loading capacitance			1	4.7		µF

Over-operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
C_{CAP}	REGSRC, CAP1, CAP2 and CAP3 output capacitance	1			µF
R_{TS}	External thermistor nominal resistance (103AT) at 25ºC	10K			Ω
T_{OPR}	Operating free-air temperature	–40		85	°C

3.3 Electrical Characteristics

Typical conditions are measured at 25ºC with nominal BAT voltages of 18 V (bq76920), 36 V (bq76930), or 48 V (bq76940) with V_{CELL} = 4 V. Min and max values include full recommended operating condition temperature range from –40ºC to +85ºC. Certain characteristics may be shown at different voltage or temperature ranges, as clarified in the Test Condition sections.

PARAMETER	DESCRIPTION	TEST CONDITION	MIN	TYP	MAX	UNITS
SUPPLY CURRENTS						
I_{DD}	NORMAL mode: ADC off, CC off	Sum of ICC_BAT and ICC_REGSRC currents		40	60	µA
	NORMAL mode: ADC on, CC off			60	90	
	NORMAL mode: ADC off, CC on			110	165	
	NORMAL mode: ADC on, CC on			130	195	
I_{CC_BAT}	NORMAL mode: ADC off	Into BAT terminal		30	45	
	NORMAL mode: ADC on			50	75	
I_{CC_REGSRC}	NORMAL mode: CC off	Into REGSRC terminal		10	15	
	NORMAL mode: CC on			80	120	
I_{SHIP}	SHIP/SHUTDOWN mode	Device in full shutdown, only VSTUP/BG and BOOT detector on		0.6	1.8	
LEAKAGE AND OFFSET CURRENTS						
dI_{NOM}	NORMAL mode supply current offset	Measured into VC5x (bq76930, bq76940) and VC10x (bq76940)	–5	±2.5	5	µA
dI_{SHIP}	SHIP mode supply current offset		–1.0	±0.1	1.0	
dI_{ALERT}	Supply current when ALERT active	Measured into VC5x (bq76930, bq76940) or added to BAT (bq76920)		15	25	
dI_{CELL}	Cell measurement input current	Measured into VC0–VC15 except VC5, VC10, VC15	–0.3	±0.1	0.3	
		Measured into VC5, VC10, VC15			0.5	
I_{LKG}	Terminal input leakage				1	
INTERNAL POWER CONTROL (STARTUP and SHUTDOWN)						
V_{PORA}	Analog POR threshold	See Note (1)	4		5	V
V_{SHUT}	Shutdown voltage	See Note (1)			3.6	V
$t_{I2CSTARTUP}$	Time delay after boot signal on TS1 before I^2C communications allowed	Delay after boot sequence when I^2C communication is allowed		1		ms
$t_{BOOTREADY}$	Device boot startup delay	Delay after boot signal when device has completed full boot-up sequence			10	ms
T_{SHUTD}	Thermal shutdown voltage (2)			100	150	°C

(1) bq76920: Measured at (BAT–VSS) bq76930: Measured at (VC5x–VSS) and (BAT–VC5x) bq76940: Measured at (VC5x–VSS), (VC10x–VC5x), and (BAT–VC10x).
(2) Assured by design, not tested in production.

Typical conditions are measured at 25ºC with nominal BAT voltages of 18 V (bq76920), 36 V (bq76930), or 48 V (bq76940) with V_{CELL} = 4 V. Min and max values include full recommended operating condition temperature range from –40ºC to +85ºC. Certain characteristics may be shown at different voltage or temperature ranges, as clarified in the Test Condition sections.

PARAMETER	DESCRIPTION	TEST CONDITION	MIN	TYP	MAX	UNITS
MEASUREMENT SCHEDULE						
t_{VCELL}	Cell voltage measurement interval	bq76920, bq76930, bq76940		250		ms
$t_{INDCELL}$	Individual cell measurement time	Per cell, balancing off		50		ms
		Per cell, balancing on		12.5		ms
t_{CB_RELAX}	Cell balancing relaxation time before cell voltage measured			12.5		ms
t_{TEMP_DEC}	Temperature measurement decimation time	Measurement duration for temperature reading		12.5		ms
t_{BAT}	Pack voltage calculation interval			250		ms
t_{TEMP}	Temperature measurement interval	Period of measurement of either TS1/TS2/TS3 or internal die temp		2		s
14-BIT ADC FOR CELL VOLTAGE AND TEMPERATURE MEASUREMENT						
ADC_{RANGE}	ADC measurement recommend operation range	V_{CELL} measurements	2		5	V
		TS/Temp measurements	0.3		3	V
ADC_{LSB}	ADC LSB value			382		µV
ADC_{25A}	ADC cell voltage accuracy(1)	V_{CELL} = 3.6 – 4.3 V	–40	±10	40	mV
ADC_{25B}		V_{CELL} = 3.2 – 4.6 V	–40	±15	40	mV
ADC_{25C}		V_{CELL} = 2.0 – 5.0 V	–50	±25	50	mV
ADC_{60}	ADC cell voltage accuracy temperature drift adder from 25°C	TA = 0ºC to 60ºC	–10		10	mV
ADC_{TS}	ADC thermistor measurement accuracy	Input from 0.3 to 3.0 V, BAT > 7 V	–35		35	mV
16-BIT CC FOR PACK CURRENT MEASUREMENT						
CC_{RANGE}	CC input voltage range		–200		200	mV
CC_{FSR}	CC full scale range		–270		270	mV
CC_{LSB}	CC LSB value	CC running constantly		8.44		µV
tCC_{READ}	Conversion time	Single conversion		250		ms
CC_{INL}	Integral nonlinearity	16-bit, best fit over input voltage range ± 200 mV		± 2	± 40	LSB
CC_{OFFSET}	Offset error			± 1	± 3	LSB
CC_{GAIN}	Gain error	Over input voltage range		± 0.5	± 1.5	%FSR
$CC_{GAINDRIFT}$	Gain error drift	Over input voltage range			150	PPM / °C
CC_{RIN}	Effective input resistance			2.5		MΩ
THERMISTOR BIAS						
R_{TS}	Pull-up resistance	TA = 25°C	9.85	10	10.15	kΩ
$R_{TSDRIFT}$	Pull-up resistance across temp	TA = –40°C to 85°C	9.7		10.3	kΩ
DIETEMP						
$V_{DIETEMP25}$	Die temperature voltage	TA = 25°C		1.20		V
$V_{DIETEMPDRIFT}$	Die temperature voltage drift			–4.2		mV/°C
INTEGRATED HARDWARE PROTECTIONS						
OV_{RANGE}	OV threshold range(2)		0x2008		0x2FF8	ADC

(1) For tighter MIN and MAX accuracies, refer to Section 5.2.2.1.
(2) See the section on Overvoltage Protection for translating the ADC code into actual OV threshold in volts (Section 5.2).

Typical conditions are measured at 25ºC with nominal BAT voltages of 18 V (bq76920), 36 V (bq76930), or 48 V (bq76940) with V_{CELL} = 4 V. Min and max values include full recommended operating condition temperature range from –40ºC to +85ºC. Certain characteristics may be shown at different voltage or temperature ranges, as clarified in the Test Condition sections.

PARAMETER	DESCRIPTION	TEST CONDITION	MIN	TYP	MAX	UNITS
UV_{RANGE}	UV threshold range(3)		0x1000		0x1FF0	ADC
OV_{UVSTEP}	OV and UV threshold step size			16		LSB
$UV_{MINQUAL}$	UV minimum value to qualify	Below $UV_{MINQUAL}$, cell is shorted (unused)		0x0518		ADC
OV_{DELAY}	OV delay timer options	OV delay = 1 s	0.7	1	1.75	s
		OV delay = 2 s	1.6	2	2.75	
		OV delay = 4 s	3.5	4	5	
		OV delay = 8 s	7	8	10	
UV_{DELAY}	UV delay timer options	UV delay = 1 s	0.7	1	1.75	
		UV delay = 4 s	3.5	4	5	
		UV delay = 8 s	7	8	10	
		UV delay = 16 s	14	16	20	
OCD_{RANGE}	OCD threshold options	Measured across (SRP–SRN)	8		100	mV
OCD_{STEP}	OCD threshold step size	RSNS = 0		2.78		mV
		RSNS = 1		5.56		mV
OCD_{DELAY}	OCD delay options		10		1280	ms
SCD_{RANGE}	SCD threshold options	Measured across (SRP–SRN)	22		200	mV
SCD_{STEP}	SCD threshold step size	RSNS = 0		11.1		mV
		RSNS = 1		22.2		mV
SCD_{DELAY}	SCD delay options		35	70	105	µs
			50	100	150	µs
			140	200	260	µs
			280	400	520	µs
$t_{PROTACC}$	Delay accuracy for OCD		–20		20	%
OC_{OFFSET}	OCD and SCD voltage offset		–2.5		2.5	mV
$OC_{SCALEERR}$	OCD and SCD scale accuracy		–10		10	%
CHARGE AND DISCHARGE DRIVERS						
V_{FETON}	CHG and DSG on	REGSRC ≥ 12 V with load resistance of 10 MΩ	10	12	14	V
		REGSRC < 12 V with load resistance of 10 MΩ	REGSRC –2	REGSRC –1	REGSRC	V
t_{FET_ON}	CHG and DSG ON rise time	CHG/DSG driving an equivalent load capacitance of 10 nF, measured from 10% to 90% of V_{FETON}		200	250	µs
t_{DSG_OFF}	DSG pull-down OFF fall time	DSG driving an equivalent load capacitance of 10 nF, measured from 90% to 10%		60	90	µs
R_{CHG_OFF}	CHG pull-down OFF resistance to VSS	When CHG disabled, CHG held at 12 V	750	1000	1250	kΩ
R_{DSG_OFF}	DSG pull-down OFF resistance to VSS	When DSG disabled, DSG held at 12 V	1.75	2.50	4.25	kΩ
V_{LOAD_DETECT}	Load detection threshold		0.4	0.7	1.0	V
V_{CHG_CLAMP}	CHG clamp voltage	If the CHG terminal externally pulled high (through PACK–, if load applied), 500 µA max sink current into CHG terminal. With CHG_ON bit cleared.	18	20	22	V

(3) See the section on Undervoltage Protection for translating the ADC code into actual UV threshold in volts (Section 5.2).

Typical conditions are measured at 25ºC with nominal BAT voltages of 18 V (bq76920), 36 V (bq76930), or 48 V (bq76940) with V_{CELL} = 4 V. Min and max values include full recommended operating condition temperature range from –40ºC to +85ºC. Certain characteristics may be shown at different voltage or temperature ranges, as clarified in the Test Condition sections.

PARAMETER	DESCRIPTION	TEST CONDITION	MIN	TYP	MAX	UNITS
ALERT TERMINAL						
V_{ALERT_OH}	ALERT output voltage high	I_{OL} = 1 mA	REGOUT x 0.75			V
V_{ALERT_OL}	ALERT output voltage low	Unloaded			REGOUT x 0.25	V
V_{ALERT_IH}	ALERT input high	ALERT externally forced high when internally driven low	1			V
R_{ALERT_PD}	ALERT terminal weak pulldown resistance when driven low	Measured into ALERT terminal with ALERT = REGOUT	0.8	2.5	8	MΩ
CELL BALANCING DRIVER						
R_{DSFET}	Internal cell balancing driver resistance	V_{CELL} = 3.6 V	1	5	10	Ω
X_{BAL}	Cell balancing duty cycle when enabled	Every 250 ms		70		%
EXTERNAL REGULATOR						
V_{EXTLDO}	External LDO voltage options	Nominal values, TI factory programmed, unloaded, across temp	2.45	2.50	2.55	V
			3.20	3.30	3.40	V
V_{EXTLDO_LN}	Line regulation	REGSRC terminal stepped from 6 to 25 V, with 10 mA load, in 100 µs			100	mV
V_{EXTLDO_LD}	Load regulation	IREGOUT = 0 mA to 10 mA	–4		4	%
V_{EXTLDO_DC}	External LDO minimum voltage under DC load	REGOUT = 10 mA DC, 2.5-V version	2.4			V
		REGOUT = 20 mA DC, 2.5-V version	2.3			V
		REGOUT = 10 mA DC, 3.3-V version	3.15			V
		REGOUT = 20 mA DC, 3.3-V version	3.05			V
I_{EXTLDO_LIMIT}	External LDO current limit	REGOUT = 0 V	30	38	45	mA
BOOT DETECTOR						
V_{BOOT}	Boot threshold voltage	Measured at TS1 terminal with device in SHIP mode. Below MIN, device will not boot up. Above MAX, device will be guaranteed to boot up.	300		1000	mV
t_{BOOT_max}	Boot threshold application time	Measured at TS1 terminal. Below MIN, device will not boot up. Above MAX, device will be guaranteed to boot up.	10		2000	µs
I^2C COMPATIBLE INTERFACE						
V_{IL}	Input Low Logic Threshold				REGOUT x 0.25	V
V_{IH}	Input High Logic Threshold		REGOUT x 0.75			V
V_{OL}	Output Low Logic Drive	I_{OL} = 1 mA			0.20	V
t_f	SCL, SDA Fall Time	I_{OL} = 2.5 mA			0.40	
V_{OH}	Output High Logic Drive (Not applicable due to open-drain outputs)		N/A		N/A	V
t_{HIGH}	SCL Pulse Width High		4.0			µs
t_{LOW}	SCL Pulse Width Low		4.7			µs
$t_{SU;STA}$	Setup time for START condition		4.7			µs
$t_{HD;STA}$	START condition hold time after which first clock pulse is generated		4.0			µs
$t_{SU;DAT}$	Data setup time		250			ns

Typical conditions are measured at 25ºC with nominal BAT voltages of 18 V (bq76920), 36 V (bq76930), or 48 V (bq76940) with V_{CELL} = 4 V. Min and max values include full recommended operating condition temperature range from –40ºC to +85ºC. Certain characteristics may be shown at different voltage or temperature ranges, as clarified in the Test Condition sections.

PARAMETER	DESCRIPTION	TEST CONDITION	MIN	TYP	MAX	UNITS
$t_{HD;DAT}$	Data hold time		0			µs
$t_{SU;STO}$	Setup time for STOP condition		4.0			µs
t_{BUF}	Time the bus must be free before new transmission can start		4.7			µs
$t_{VD;DAT}$	Clock Low to Data Out Valid				900	ns
$t_{HD;DAT}$	Data Out Hold Time After Clock Low		0			ns
f_{SCL}	Clock Frequency		0		100	kHz

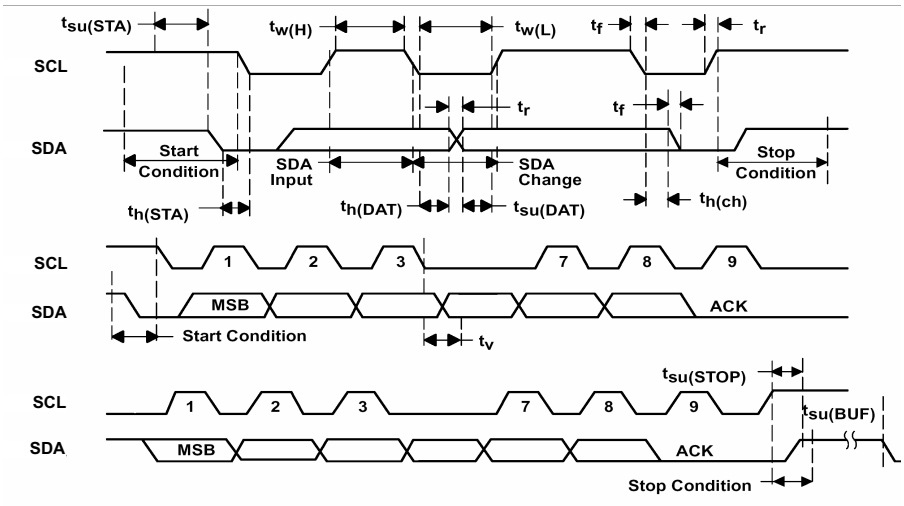


Figure 3-1. I²C Timing

4 Power Modes

4.1 Introduction

Each bq769x0 device supports the following modes of operation.

Table 4-1. Supported Power Modes

Mode	Description
NORMAL	Fully operational state. Both ADC and CC may be on, or disabled by host microcontroller. OV and UV protection enabled if ADC is on. OCD and SCD enabled. ADC and CC may be disabled to reduce power consumption, and CC may be operated in a “1-SHOT” mode for flexible power savings.
SHIP	Lowest possible power state, intended for pack assembly and/or long term pack storage. Must see a BOOT signal (> 1 VBOOT) on TS1 terminal to boot from SHIP → NORMAL. Note that the device always enters SHIP mode upon POR.

4.2 NORMAL Mode

NORMAL mode represents the fully operational mode where all blocks are enabled and the device sees its highest current consumption. In this mode, certain blocks/functions may be disabled to save power—these include the ADC and CC. OV and UV are running continuously as long as the ADC is enabled. The OCD and SCD comparators may not be disabled in this mode.

Transitioning from NORMAL to SHIP mode is also initiated by the host, and requires consecutive writes to two bits in the SYS_CTRL1 register.

4.3 SHIP Mode

SHIP mode is the basic and lowest power mode that bq769x0 supports. SHIP mode is automatically entered during initial pack assembly and after every POR event. When the device is in NORMAL mode, it may enter SHIP by the host controller via a specific sequence of I^2C commands.

In SHIP mode, only a minimum of blocks are turned on, including the VSTUP power supply and primal boot detector. Waking from SHIP mode to NORMAL mode requires pulling the TS1 terminal greater than VBOOT, which triggers the device boot-up sequence.

To enter SHIP mode from NORMAL mode, the *[SHUTA]* and *[SHUTB]* bits in the SYS_CTRL1 register must be written with specific patterns across two consecutive writes:

- Write #1: *[SHUTA]* = 0, *[SHUTB]* = 1
- Write #2: *[SHUTA]* = 1, *[SHUTB]* = 0

Note that *[SHUTA]* and *[SHUTB]* should each be in a 0 state prior to executing the shutdown command above. If this specific sequence is entered into the device, the device transitions into SHIP mode. If any other sequence is written to the *[SHUTA]* and *[SHUTB]* bits or if either of the two patterns is not correctly entered, the device will not enter SHIP mode.

CAUTION

DO NOT OPERATE THE DEVICE BELOW POR. When designing with the bq76940, the intermediate voltages (BAT–VC10x), (VC10x–VC5x) and (VC5x–VSS) must each never fall below VSHUT. When this occurs, a full device reset must be initiated by powering down all three intermediate voltages (BAT–VC10x), (VC10x–VC5x) and (VC5x–VSS) below VSHUT and rebooting by applying the appropriate VBOOT signal to the TS1 terminal. When designing with the bq76930, the intermediate voltages (BAT–VC5x) and (VC5x–VSS) must each never fall below VSHUT. When this occurs, a full device reset must be initiated by powering down both intermediate voltages (BAT–VC5x) and (VC5x–VSS) below VSHUT and rebooting by applying the appropriate VBOOT signal to the TS1 terminal.

The device will also enter SHIP mode during a POR event; however, this is not a recommended method of SHIP mode entry. If any of the supply-side voltages below fall below V_{SHUT} and then back up above VPORA, the device defaults into the SHIP mode state. This is similar to an initial pack assembly condition. In order to exit SHIP mode into NORMAL mode, the device must follow the standard boot sequence by applying a voltage greater than the VBOOT threshold on the TS1 pin.

5 Subsystems

5.1 Introduction

bq769x0 consists of three major subsystems: Measurement, Protection, and Control. These work in harmony to ensure that the fundamental battery pack parameters—voltage, current and temperature—are accurately captured and easily available to a host controller, while ensuring a baseline or secondary level of hardware protection in the event that a host controller is unable or unavailable to manage certain fault conditions.

NOTE

The bq769x0 is intended to serve as an analog front-end (AFE) as part of a chipset system solution: A companion microcontroller is required to oversee and control this AFE.

The Measurement subsystem's core responsibility is to digitize the cell voltages, pack current (integrated into a passed charge calculation), external thermistor temperature, and internal die temperature. It also performs an automatic calculation of the total battery stack voltage, by simply adding up all measured cell voltages.

The Protection subsystem provides a baseline or secondary level of hardware protections to better support a battery pack's FMEA requirements in the event of a loss of host control or simply if a host is unable to respond to a certain fault event in time. Integrated protections include pack-level faults such as OV, UV, OCD, SCD; detection of an external secondary protector fault; and internal "watchdog"-style device fault. Protection events will trigger toggling of the ALERT terminal, as well as automatic disabling of the DSG and/or CHG FET driver (depending on the fault). Recovery from a fault event must be handled by the host microcontroller.

The Control subsystem implements a suite of useful pack features, including direct low-side NCH FET drivers, cell balancing drivers, the ALERT digital output, an external LDO and more.

The following sections describe each subsystem in greater detail, as well as explaining the various power states that are available.

5.2 Measurement Subsystem Overview

The monitoring subsystem ensures that all cell voltages, temperatures, and pack current may be easily measured by the host. All ADCs are trimmed by TI.

ADC and CC data are always returned as atomic values if both high and low registers are read in the same transaction (using address auto-increment).

5.2.1 Data Transfer to the Host Controller

The bq769x0 has a fully digital interface: All information is transferred through I^2C, simply by reading and/or writing to the appropriate register(s) storing the relevant data. Block reads and writes, buffered by an 8-bit CRC code per byte, ensure a fast and robust transmission of data.

5.2.2 14-Bit ADC

Each bq769x0 device measures cell voltages and temperatures using a 14-bit ADC. This ADC measures all differential cell voltages, thermistors and/or die temperature with a nominal full-scale unsigned range of 0–6.275 V and LSB of 382 µV.

To enable the ADC, the *[ADC_EN]* bit in the SYS_CTRL1 register must be set. This bit is set automatically whenever the device enters NORMAL mode. When enabled, the ADC ensures that the integrated OV and UV protections are functional.

For each contiguous set of five cells (VC1 to VC5, VC6 to VC10), when no cells in that particular set are being balanced, each cell is measured over a 50-ms decimation window and a complete update is available every 250 ms. In the bq76930 and bq76940, every set of five cells above the primary five cells is measured in parallel. The 50-ms decimation greatly assists with removing the aliasing effects present in a noisy motor environment.

When any cells in a contiguous set of 5 cells are being balanced, those affected cells are measured in a reduced 12.5-ms decimation period, to allow the cell balancing to function properly without affecting the integrated OV and UV protections. Since cell balancing is typically only performed during pack charge or idle periods, the shortened decimation periods should not impact accuracy as the system noise during these times is greatly reduced. This reduced decimation period is only applied to sets where one of the cells is being balanced.

This is summarized as follows for the bq76920–bq76940:

- VC1 to VC5 measurements are each taken in a 50-ms decimation period when all bits in CELLBAL1 register are 0, and a 12.5-ms decimation period when any bits in CELLBAL1 register are 1.
- VC6 to VC10 measurements are each taken in a 50-ms decimation period when all bits in CELLBAL2 register are 0, and a 12.5-ms decimation period when any bits in CELLBAL2 register are 1.
- VC11 to VC15 measurements are each taken in a 50-ms decimation period when all bits in CELLBAL3 register are 0, and a 12.5-ms decimation period when any bits in CELLBAL3 register are 1.
- Total update interval is 250 ms.

Each differential cell input is factory-trimmed for gain and/or offset, such that the resulting reading via I^2C is always consistent from part-to-part and requires no additional calibration or correction factor application.

The ADC is required to be enabled in order for the integrated OV and UV protections to be operating.

The following shows how to convert the 14-bit ADC reading into an analog voltage. Each device is factory calibrated, with a GAIN and OFFSET stored into EEPROM.

The ADC transfer function is a linear equation defined as follows:

V(cell) = GAIN x ADC(cell) + OFFSET

GAIN is stored in units of µV/LSB, while OFFSET is stored in mV units.

Some example cell voltage calculations are provided in the table below. For illustration purposes, the example uses a hypothetical GAIN of 380 µV/LSB (ADCGAIN<4:0> = 0x0F) and OFFSET of 30 mV (ADCOFFSET<7:0> = 0x1E).

14-Bit ADC Result	ADC Result in Decimal	GAIN (µV/LSB)	OFFSET (mV)	Cell Voltage (mV)
0x1800	6144	380	30	2365
0x1F10	7952	380	30	3052

NOTE

When entering NORMAL mode from SHIP mode, please allow for the following times before reading out initial cell voltage data:

bq76920: 250 ms

bq76930: 400 ms

bq76940: 800 ms

5.2.2.1 Optional Real-time Calibration Using the Host Microcontroller

The performance of the cell voltage values measured by the 14-bit ADC has a factory-calibrated accuracy, as follows:

- +/– 10 mV TYP, +/– 40 mV MIN and MAX from 3.6 to 4.3 V,
- +/– 15 mV TYP, +/– 40 mV MIN and MAX from 3.2 to 4.6 V, and
- +/– 50 mV MIN and MAX from 2.0 to 5.0 V

While this is suitable for the majority of pack protection and basic monitoring applications the bq769x0 AFE family is intended to support, certain systems may require a higher accuracy performance.

To achieve this, use an available ADC channel and general purpose output terminal on the host microcontroller paired with the bq769x0. A simple external circuit consisting of two precision resistors and a small-signal FET is activated by the host microcontroller to determine the total stack voltage, V_{STACK}; this is then compared against the sum of the individual cell voltages as measured by the internal ADC of the bq769x0. The resulting transfer function coefficient, $GAIN_2$, is simply applied to each cell voltage ADC value for improved accuracy.

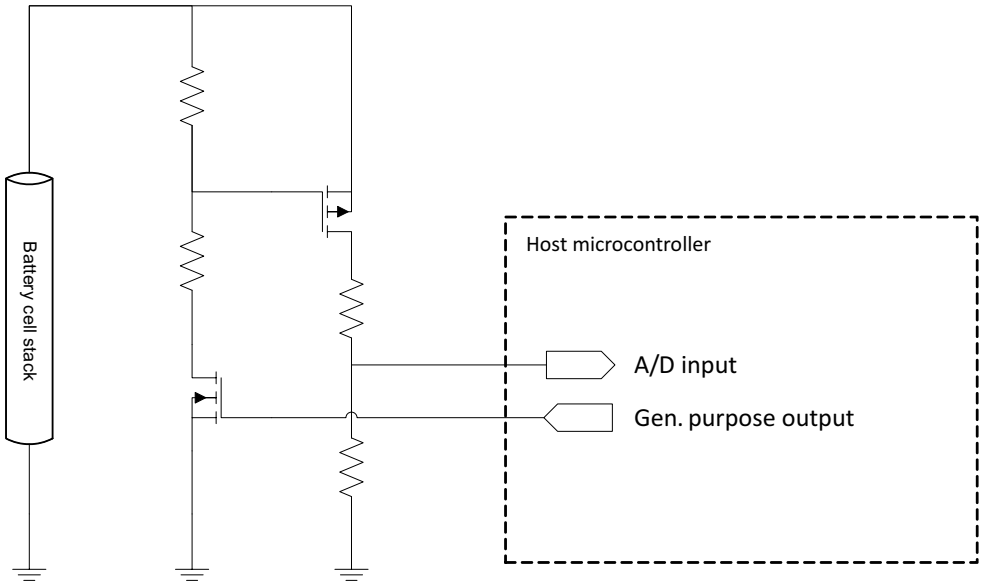


Figure 5-1. External Real-Time Calibration Circuit to Host Microcontroller

The process is as follows:

1. Periodically measure V_{STACK}
   (a) $V_{STACK} = V_{AD} \times (R1 + R2) / R1$
2. Read out all V_{CELL} ADC readings from the bq769x0 and apply the standard GAIN and OFFSET values stored in the bq769x0.
   (a) $V(1) = GAIN \times ADC_1 + OFFSET$, $V(2) = GAIN \times ADC_2 + OFFSET$, and so on
3. Sum up all V_{CELL} values, V_{SUM}
   (a) $V_{SUM} = V(1) + V(2) + V(3) \ldots$
4. Calculate GAIN2
   (a) $GAIN_2 = V_{STACK} / V_{SUM}$

As a general recommendation, a new GAIN2 function should be generated when the cell voltages increase or decrease by more than 100 mV. With $GAIN_2$, each cell voltage calculation becomes:

$V(cell) = GAIN_2 \times (GAIN \times ADC(cell) + OFFSET)$

For systems that do not require this additional in-use calibration function, $GAIN_2$ is simply “1”.

5.2.3 16-Bit CC

A 16-bit integrating ADC, commonly referred to as the coulomb counter (CC), provides measurements of accumulated charge across the current sense resistor. The integration period for this reading is 250 ms.

The CC may be operated in one of two modes: ALWAYS ON and 1-SHOT.

- In ALWAYS ON mode, the CC runs at 100%, gathering a fresh reading every 250 ms. The conclusion of each reading sets the CC_READY bit, which toggles the ALERT terminal high to inform the microcontroller that a new reading is available. To enable Always On mode, set *[CC_EN]* = 1.
- In 1-SHOT mode, the CC performs a single 250-ms reading, and similarly sets the CC_READY bit when completed. This mode is intended for non-gauging usages, where the host simply desires to check the pack current.

  To enable a 1-SHOT reading, ensure [*CC_EN]* = 0 and set *[CC_ONESHOT]* = 1.

The full scale range of the CC is ± 270 mV, with a max recommended input range of ± 200 mV, thus yielding an LSB of approximately 8.44 µV.

The following equation shows how to convert the 16-bit CC reading into an analog voltage if no board-level calibration is performed:

CC Reading (in µV) = ***[16-bit 2's Complement Value] × (8.44 µV/LSB)***

16-Bit CC Result	ADC Result in Decimal	CC Reading (in µV)
0x0001	1	8.44
0x2710	10000	84,400
0x7D00	32000	270,080
0x8300	–32000	–270,080
0xC350	–15536	–131,123.84
0xFFFF	–1	–8.44

5.2.4 External Thermistor

One (bq76920), two (bq76930), or three (bq76940) 10 kΩ NTC 103AT thermistors may be measured by the device. These are measured by applying a factory-trimmed internal 10k pull-up resistance to an internal regulator value of nominally 3.3 V, the result of which can be read out from the TSx (TS1, TS2, TS3) registers.

To select thermistor measurement mode, set *[TEMP_SEL]* = 1.

Thermistor TS1 is connected between TS1 and VSS; TS2 is connected between TS2 and VC5x (bq76930 and bq76940 only); and TS3 is connected between TS3 and VC10x (bq76940 only). These thermistors may be placed in various areas in the battery pack to measure such things as localized cell temperature, FET heating, etc.

The thermistor impedance may be calculated using the 14-bit ADC reading in the TS1/TS2/TS3 registers and 10k internal pull-up resistance as follows:

The following equation shows how to use the 14-bit ADC readings in TS1, TS2, and TS3 to determine the resistance of the external 103AT thermistor:

$$V_{TSX} = \text{(ADC in Decimal)} \times 382\ \mu V/LSB$$

$$R_{TS} = (10{,}000 \times VTSX) \div (3.3 - VTSX)$$

To convert the thermistor resistance into temperature, please refer to the thermistor component manufacturer's datasheet.

5.2.5 Die Temperature Monitor

NOTE

When switching between external and internal temperature monitoring, a 2-s latency may be incurred due to the natural scheduler update interval.

A die temperature block generates a voltage that is proportional to the die temperature, and provides a way of reducing component count if pack thermistors are not used or ensuring that the die power dissipation requirements are observed. The die is measured using the same on-board 14-bit ADC as the cell voltages.

To select internal die temperature measurement mode, set *[TEMP_SEL]* = 0.

For bq76930 and bq76940, multiple die temperature measurements are available; these are stored in TS2 and TS3.

To convert a DIETEMP reading into temperature, refer to the following equation box. If more accurate temperature readings are needed from DIETEMP, the DIETEMP at room temperature value should be stored during production calibration.

The following equation shows how to use the 14-bit ADC readings in TS1, TS2, and TS3 when [TEMPSEL] = 0 to determine the internal die temperature:

$$V_{25} = 1.200\ V\ (nominal)$$
$$V_{TSX} = (ADC\ in\ Decimal) \times 382\ \mu V/LSB$$
$$TEMP_{DIE} = 25° - ((V_{TSX} - V_{25}) \div 0.0042)$$

5.2.6 16-Bit Pack Voltage

Once converted to digital form, each cell voltage is added up and the summation result stored in the BAT registers. This 16-bit value has a nominal LSB of 1.532 mV.

The following shows how to convert the 16-bit pack voltage ADC reading into an analog voltage. This value also uses the GAIN and OFFSET stored into EEPROM.

The ADC transfer function is a linear equation defined as follows:

$$V_{(BAT)} = 4 \times GAIN \times ADC(cell) + (\#Cells \times OFFSET)$$

GAIN is stored in units of µV/LSB, while OFFSET is stored in mV units.

5.2.7 System Scheduler

A master scheduler oversees the monitoring intervals, creating a full update every 250 ms. Temperature measurements are taken every 2 seconds. Pack voltage is calculated every 250 ms.

5.3 Protection Subsystem

5.3.1 Integrated Hardware Protections

Integrated hardware protections are provided as an extra degree of safety and are meant to supplement the standard protection feature set that would be incorporated into the host controller firmware. They should not be used as the sole means of protecting a battery pack, but are useful for FMEA purposes; for example, in the event that a host microcontroller is unable to react to any of the below protection situations. All hardware protection thresholds and delays should be loaded into the AFE by the host microcontroller during system startup. The AFE will also default to pre-defined threshold and delay settings, in case the host microcontroller is unable to or does not wish to program the protection settings.

Overcurrent in Discharge (OCD) and Short Circuit in Discharge (SCD) are implemented using sampled analog comparators that run at 32 kHz, and that continuously monitor the voltage across (SRP–SRN) while the device is in NORMAL mode. Upon detection of a voltage that exceeds the programmed OCD or SCD threshold, a counter begins to count up to a programmed delay setting. If the counter reaches its target value, the SYS_STAT register is updated to indicate the fault condition, the FET state(s) are updated as shown in Table 3, and the ALERT terminal is driven high to interrupt the host.

The protection fault threshold and delay settings for OCD and SCD protections are configured via the PROTECT1 and PROTECT2 registers. See the Register Map section for details about supported values.

Overvoltage (OV) and Undervoltage (UV) protections are handled digitally, by comparing the cell voltage readings against the 8-bit programmed thresholds in the OV and UV registers.

The OV threshold is stored in the OV_TRIP register and is a direct mapping of 8 bits of the 14-bit ADC reading, with the upper 2 MSB preset to “10” and lower 4 LSB preset to “1000”. In other words, the corresponding OV trip level is mapped to “10-XXXX-XXXX–1000”. The programmable range of OV thresholds is approximately 3.15 to 4.7 V, but this is subject to variation of to the (GAIN, OFFSET) linear equation used to map the ADC values.

The UV threshold is stored in the UV_TRIP register and is a direct mapping of 8 bits of the 14-bit ADC reading, with the upper 2 MSB preset to “01” and lower 4 LSB preset to “0000”. In other words, the corresponding OV trip level is mapped to “01-XXXX-XXXX–0000”. The programmable range of UV thresholds is approximately 1.58 to 3.1 V, but this is subject to variation due to the (GAIN, OFFSET) linear equation used to map the ADC values.

Protection	Upper 2 MSB	Middle 8 Bits	Lower 4 LSB
OV	10	Set in OV_TRIP Register	1000
UV	01	Set in UV_TRIP Register	0000

NOTE

To support flexible cell configurations within bq76920, bq76930, and bq76940, UV is ignored on any cells that have a reading under $UV_{MINQUAL}$. This allows cell pins to be shorted in implementations where not all cells are needed (for example, 6-series cells using the bq76930).

Default protection thresholds and delays are shown in the register description at the end of this datasheet. These are loaded into the digital register (RAM) of the device when the device enters NORMAL mode. These RAM values may then be overwritten by the host controller to any other values, which they will retain until a POR event. It is recommended that the host controller reload these values during its standard power-up and/or re-initialization sequence.

To calculate the correct OV_TRIP and UV_TRIP register values for a device, use the following procedure:

1. Determine desired OV.
2. Read out *[ADCGAIN]* and *[ADCOFFSET]* from their corresponding registers. Note that ADCGAIN is stored in units of µV/LSB, while ADCOFFSET is stored in mV.
3. Calculate the full 14-bit ADC value needed to meet the desired OV and UV trip thresholds as follows:
   (a) OV_TRIP_FULL = (OV – ADCOFFSET) ÷ ADCGAIN
   (b) UV_TRIP_FULL = (UV – ADCOFFSET) ÷ ADCGAIN
4. Remove the upper 2 MSB and lower 4 LSB from the full 14-bit value, retaining only the remaining middle 8 bits. This can be done by shifting the OV_TRIP_FULL and UV_TRIP_FULL binary values 4 bits to the right and removing the upper 2 MSB.
5. Write OV_TRIP and UV_TRIP to their corresponding registers.

Both OV and UV protections require the ADC to be enabled. Ensure that the *[ADC_EN]* bit is set to 1 if OV and UV protections are needed.

5.3.2 Reduced Test Time

A special debug and test configuration bit is provided in the SYS_CTRL2 register, called *[DELAY_DIS]*. Setting *[DELAY_DIS]* bypasses the OV/UV protection fault timers and allows a fault condition to be registered within 200 ms after application of such a fault condition.

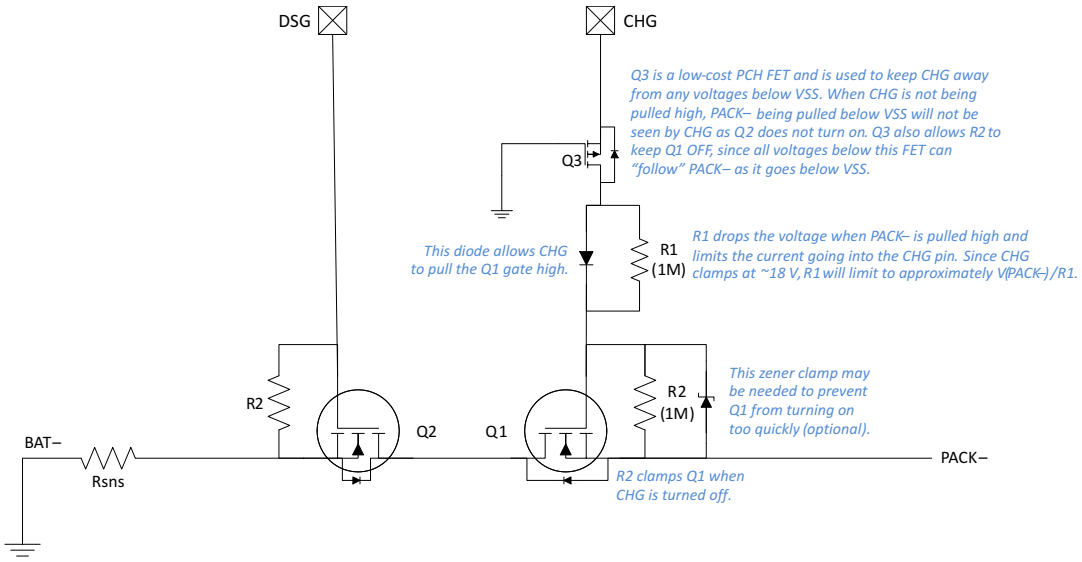
5.4 Control Subsystem

5.4.1 FET Driving (CHG AND DSG)

Each bq769x0 device provides two low-side FET drivers, CHG and DSG, which control NCH power FETs or may be used as a signal to enable various other circuits such as a high-side NCH charge pump circuit.

Both DSG and CHG drivers have a fast pull-up to nominally 12 V when enabled. DSG uses a fast pull-down to VSS when disabled, while CHG utilizes a high impedance (nominally 1 MΩ) pull-down path when disabled.

An additional internal clamp circuit ensures that the CHG terminal does not exceed a maximum of 20 V.



The power path for the CHG and DSG pull-up circuit originates from the REGSRC terminal, instead of BAT.

To enable the CHG fet, set the [CHG_ON] register bit to 1; to disable, set [CHG_ON] = 0. The discharge FET may be similarly controlled via the [DSG_ON] register bit.

Certain fault conditions or power state transitions will clear the state of the CHG/DSG FET controls. Table 5-1 shows what action, if any, are taken to [CHG_ON] and [DSG_ON] in response to various system events:

Table 5-1. CHG, DSG Response Under Various System Events

EVENT	[CHG_ON]	[DSG_ON]
OV Fault	Set to 0	—
UV Fault	—	Set to 0
OCD Fault	—	Set to 0
SCD Fault	—	Set to 0
ALERT Override	Set to 0	Set to 0
DEVICE_XREADY gets set	Set to 0	Set to 0
Enter SHIP mode from NORMAL	Set to 0	Set to 0

NOTE

All protection recovery must be initiated by the host microcontroller. In order to resume FET operation after a fault condition has occurred, the host microcontroller must first clear the corresponding status bit in the SYS_STAT register, which will clear the ALERT terminal, and then manually re-enable the CHG and/or DSG bit. Certain faults, such as OV or UV, may immediately re-toggle if such a condition still persists. Refer to Table 7-1 for details on clearing status bits.

There are no conditions under which the bq769x0 automatically sets either *[CHG_ON]* or *[DSG_ON]* to 1.

5.4.2 Load Detection

A load detection circuit is present on the CHG terminal and activated whenever the CHG FET is disabled ([CHG_ON] = 0). This circuit detects if the CHG terminal is externally pulled high when the high impedance (approximately 1 MΩ) pull-down path should actually be holding the CHG terminal to VSS, and is useful for determining if the PACK– terminal (outside of the AFE) is being held at a high voltage—for example, if the load is present while the power FETs are off. The state of the load detection circuit is read from the *[LOAD_PRESENT]* bit of the SYS_CTRL1 register.

After an OCD or SCD fault has occurred, the DSG FET will be disabled ([DSG_ON] cleared), and the CHG FET must similarly be explicitly disabled to activate the load detection circuit. The host microcontroller may periodically poll the *[LOAD_PRESENT]* bit to determine the state of the PACK– terminal and determine when the load is removed (*[LOAD_PRESENT]* = 0).

5.4.3 Cell Balancing

Both internal and external passive cell balancing options are fully supported by the bq76920, while external cell balancing is recommended for bq76930 and bq76940. It is left to the host controller to determine the exact balancing algorithm to be used in any given system; each bq769x0 device provides the cell voltages and balancing drivers to enable this. If using the internal cell balance drivers, up to 50 mA may be balanced per cell. If using external cell balancing, much higher balancing currents may be employed.

To activate a particular cell balancing channel, simply set the corresponding bit for that cell in the CELLBAL1, CELLBAL2, or CELLBAL3 register. For example, VC1–VC0 is enabled by setting *[CB1]*, while VC12–VC11 is set via *[CB12]*.

Multiple cells may be simultaneously balanced; it is left to the user's discretion to determine the ideal number of cells to concurrently balance. Adjacent cells should not be balanced simultaneously; this may cause cell pins to exceed their absolute maximum conditions and is also not recommended for external balancing implementations. Additionally, if internal balancing is used, care should be taken to avoid exceeding package power dissipation ratings.

NOTE

The host controller must ensure that no two adjacent cells are balanced simultaneously within each set of the following:

- VC1–VC5
- VC6–VC10
- VC11–VC15

The total duty cycle devoted to balancing is approximately 70% per 250 ms. This is because a portion of the 250 ms is allotted for normal cell voltage measurements via the ADC.

If *[ADC_EN]* =1, OV and UV protections are not affected by cell balancing, since the cell balancing is temporarily suspended for a small slice of time every 250 ms during which the cell voltage readings are taken. This ensures that the OV and UV protections do not accidentally trigger, or miss an actual OV/UV condition on the cells while balancing is enabled.

NOTE

All cell balancing control bits in CELLBAL1, CELLBAL2, and CELLBAL3 are automatically cleared under the following events, and must be explicitly re-written by the host microcontroller following clearing of the event:

- DEVICE_XREADY gets set
- Enters NORMAL mode from SHIP mode

5.4.4 Alert

The ALERT terminal serves as an active high digital interrupt signal that can be connected to a GPIO port of the host microcontroller. This signal is an OR of all bits in the SYS_STAT register.

In order to clear the ALERT signal, the source bit in the SYS_STAT register must first be cleared by writing a “1” to that bit. This will cause an automatic clear of the ALERT terminal once all bits are cleared.

The ALERT terminal may also be driven by an external source; for example, the pack may include a secondary overvoltage protector IC. When the ALERT terminal is forced high externally while low, the device will recognize this as an OVRD_ALERT fault and set the *[OVRD_ALERT]* bit. This triggers automatic disabling of both CHG and DSG FET drivers. The device cannot recognize the ALERT signal input high when it is already forcing the ALERT signal high from another condition.

An external pull-down resistor of 500 kΩ–1 MΩ from ALERT to VSS is highly recommended.

5.4.5 Output LDO

An adjustable output voltage regulator LDO is provided as a simple way to provide power to additional components in the battery pack, such as the host microcontroller or LEDs. The LDO is configured in EEPROM by TI during the production test process, and can support 2.5-V or 3.3-V options.

A cascode small-signal FET must be added in the external path between BAT and REGSRC. This helps drop most of the power dissipation outside of the package and cuts down on package power dissipation.

5.4.6 I^2C Communications

The AFE implements a standard 100-kHz I^2C interface and acts as a slave device. The I^2C device address is 7-bits and is factory programmed; consult the “ORDERING INFO” section of this datasheet for more information.

A write transaction is shown in Figure 5-2. Block writes are allowed by sending additional data bytes before the Stop. The I^2C block will auto-increment the register address after each data byte. When enabled, the CRC is calculated over the
register address and data. Block writes are achieved by sending additional data and CRC byte pairs, where each subsequent CRC is calculated only over the byte being sent. The CRC polynomial is $x^8 + x^2 + x + 1$.

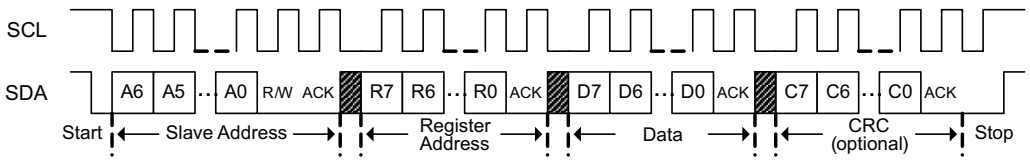


Figure 5-2. I^2C Write

Figure 5-3 shows a read transaction using a Repeated Start.

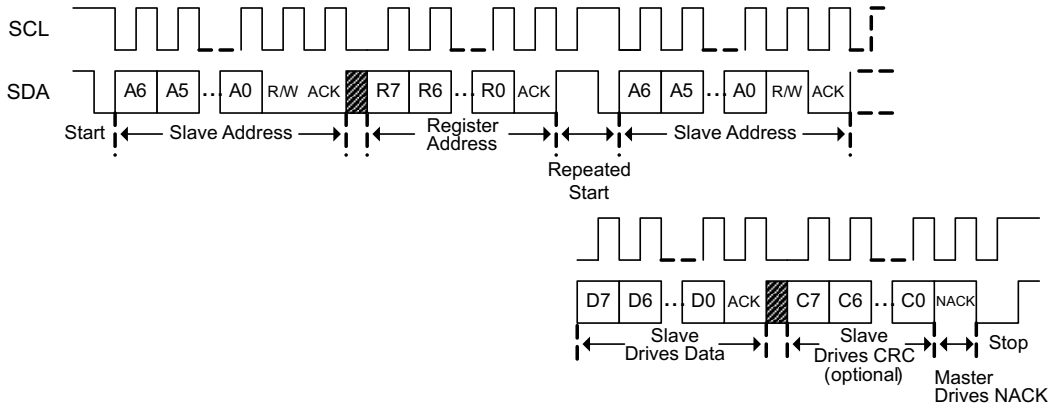


Figure 5-3. I²C Read with Repeated Start

Figure 5-4 shows a read transaction where a Repeated Start is not used, for example if not available in hardware. For a block read the master ACK's each data byte except the last and continues to clock the interface. The I²C block will auto-increment the register address after each data byte. When enabled, the CRC is calculated only over the second slave address and data. Similar to a block write, in a block read with CRC enabled each additional read byte is followed by a CRC byte calculated over only that byte.

When detecting a bad CRC, the I²C Slave will NACK the CRC and go to an idle state.

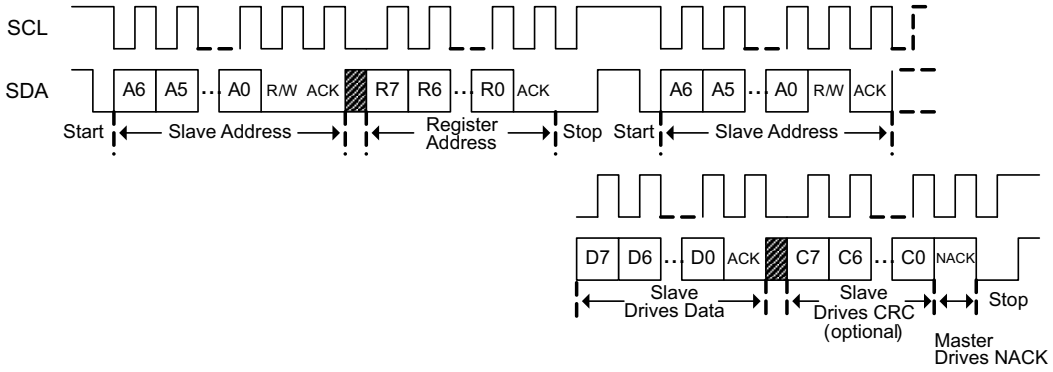


Figure 5-4. I²C Read Without Repeated Start

6 Configuring Alternative Cell Counts

6.1 Introduction

Each bq769x0 IC supports a variety of cell counts. The following tables provide guidance on which input pins to use, depending on the number of cells in the pack.

Table 6-1. Cell Connections for bq76920

Cell Input	3 Cells	4 Cells	5 Cells
VC5–VC4	CELL 3	CELL 4	CELL 5
VC4–VC3	short	short	CELL 4
VC3–VC2	short	CELL 3	CELL 3
VC2–VC1	CELL 2	CELL 2	CELL 2
VC1–VC0	CELL 1	CELL 1	CELL 1

Table 6-2. Cell Connections for bq76930

Cell Input	6 Cells	7 Cells	8 Cells	9 Cells	10 Cells
VC10–VC9	CELL 6	CELL 7	CELL 8	CELL 9	CELL 10
VC9–VC8	short	short	short	short	CELL 9
VC8–VC7	short	short	CELL 7	CELL 8	CELL 8
VC7–VC6	CELL 5	CELL 6	CELL 6	CELL 7	CELL 7
VC6–VC5b	CELL 4	CELL 5	CELL 5	CELL 6	CELL 6
VC5–VC4	CELL 3	CELL 4	CELL 4	CELL 5	CELL 5
VC4–VC3	short	short	short	CELL 4	CELL 4
VC3–VC2	short	CELL 3	CELL 3	CELL 3	CELL 3
VC2–VC1	CELL 2	CELL 2	CELL 2	CELL 2	CELL 2
VC1–VC0	CELL 1	CELL 1	CELL 1	CELL 1	CELL 1

Table 6-3. Cell Connections for bq76940

Cell Input	9 Cells	10 Cells	11 Cells	12 Cells	13 Cells	14 Cells	15 Cells
VC15–VC14	CELL 9	CELL 10	CELL 11	CELL 12	CELL 13	CELL 14	CELL 15
VC14–VC13	short	short	short	short	short	short	CELL 14
VC13–VC12	short	short	short	CELL 11	CELL 12	CELL 13	CELL 13
VC12–VC11	CELL 8	CELL 9	CELL 10	CELL 10	CELL 11	CELL 12	CELL 12
VC11–VC10b	CELL 7	CELL 8	CELL 9	CELL 9	CELL 10	CELL 11	CELL 11
VC10–VC9	CELL 6	CELL 7	CELL 8	CELL 8	CELL 9	CELL 10	CELL 10
VC9–VC8	short	short	short	short	short	CELL 9	CELL 9
VC8–VC7	short	short	CELL 7	CELL 7	CELL 8	CELL 8	CELL 8
VC7–VC6	CELL 5	CELL 6	CELL 6	CELL 6	CELL 7	CELL 7	CELL 7
VC6–VC5b	CELL 4	CELL 5	CELL 5	CELL 5	CELL 6	CELL 6	CELL 6
VC5–VC4	CELL 3	CELL 4	CELL 4	CELL 4	CELL 5	CELL 5	CELL 5
VC4–VC3	short	short	short	short	CELL 4	CELL 4	CELL 4
VC3–VC2	short	CELL 3	CELL 3	CELL 3	CELL 3	CELL 3	CELL 3
VC2–VC1	CELL 2	CELL 2	CELL 2	CELL 2	CELL 2	CELL 2	CELL 2
VC1–VC0	CELL 1	CELL 1	CELL 1	CELL 1	CELL 1	CELL 1	CELL 1

7 Register Set

7.1 Registers

Name	Addr	D7	D6	D5	D4	D3	D2	D1	D0
READ/WRITE									
SYS_STAT	0x00	CC_READY	RSVD	DEVICE_XREADY	OVRD_ALERT	UV	OV	SCD	OCD
CELLBAL1	0x01				CB<5:1>				
CELLBAL2(1)	0x02				CB<10:6>				
CELLBAL3(2)	0x03				CB<15:11>				
SYS_CTRL1	0x04	LOAD_PRESENT			ADC_EN	TEMP_SEL	RSVD	SHUT_A	SHUT_B
SYS_CTRL2	0x05	DELAY_DIS	CC_EN	CC_ONESHOT	RSVD			DSG_ON	CHG_ON
PROTECT1	0x06	RSNS			SCD_DELAY		SCD_THRESH		
PROTECT2	0x07	OCD_DELAY				OCD_THRESH			
PROTECT3	0x08	UV_DELAY		OV_DELAY		RSVD			
OV_TRIP	0x09	OV_THRESH							
UV_TRIP	0x0A	UV_THRESH							
CC_CFG	0x0B			Must be programmed to 0x19					
READ-ONLY									
VC1_HI	0x0C			<13:8>					
VC1_LO	0x0D	<7:0>							
VC2_HI	0x0E			<13:8>					
VC2_LO	0x0F	<7:0>							
VC3_HI	0x10			<13:8>					
VC3_LO	0x11	<7:0>							
VC4_HI	0x12			<13:8>					
VC4_LO	0x13	<7:0>							
VC5_HI	0x14			<13:8>					
VC5_LO	0x15	<7:0>							
VC6_HI(1)	0x16			<13:8>					
VC6_LO(1)	0x17	<7:0>							
VC7_HI(1)	0x18			<13:8>					
VC7_LO(1)	0x19	<7:0>							
VC8_HI(1)	0x1A			<13:8>					
VC8_LO(1)	0x1B	<7:0>							
VC9_HI(1)	0x1C			<13:8>					
VC9_LO(1)	0x1D	<7:0>							
VC10_HI(1)	0x1E			<13:8>					
VC10_LO(1)	0x1F	<7:0>							
VC11_HI(2)	0x20			<13:8>					
VC11_LO(2)	0x21	<7:0>							
VC12_HI(2)	0x22			<13:8>					
VC12_LO(2)	0x23	<7:0>							
VC13_HI(2)	0x24			<13:8>					
VC13_LO(2)	0x25	<7:0>							
VC14_HI(2)	0x26			<13:8>					
VC14_LO(2)	0x27	<7:0>							
VC15_HI(2)	0x28			<13:8>					
VC15_LO(2)	0x29	<7:0>							
BAT_HI	0x2A	<15:8>							
BAT_LO	0x2B	<7:0>							

(1) These registers are only valid for bq76930 and bq76940.
(2) These registers are only valid for bq76940.

Name	Addr	D7	D6	D5	D4	D3	D2	D1	D0
TS1_HI	0x2C			<13:8>					
TS1_LO	0x2D	<7:0>							
TS2_HI(1)	0x2E			<13:8>					
TS2_LO(1)	0x2F	<7:0>							
TS3_HI(2)	0x30			<13:8>					
TS3_LO(2)	0x31	<7:0>							
CC_HI	0x32	<15:8>							
CC_LO	0x33	<7:0>							
ADCGAIN1	0x50	RSVD				ADCGAIN<4:3>		RSVD	
ADCOFFSET	0x51	ADCOFFSET<7:0>							
ADCGAIN2	0x59	ADCGAIN<2:0>			RSVD				

7.1.1 Detailed Information

Table 7-1. SYS_STAT (0x00)

BIT	7	6	5	4	3	2	1	0
NAME	CC_READY	RSVD	DEVICE_XREADY	OVRD_ALERT	UV	OV	SCD	OCD
RESET	0	0	0	0	0	0	0	0
ACCESS	RW	RW	RW	RW	RW	RW	RW	RW

NOTE

Bits in SYS_STAT may be cleared by writing a "1" to the corresponding bit.

Writing a "0" does not change the state of the corresponding bit.

CC_READY (Bit 7): Indicates that a fresh coulomb counter reading is available. Note that if this bit is not cleared between two adjacent CC readings becoming available, the bit remains latched to 1. This bit may only be cleared (and not set) by the host.

0 = Fresh CC reading not yet available or bit is cleared by host microcontroller.

1 = Fresh CC reading is available. Remains latched high until cleared by host.

RSVD (Bit 6): Reserved. Do not use.

DEVICE_XREADY (Bit 5): Internal chip fault indicator. When this bit is set to 1, it should be cleared by the host. May be set due to excessive system transients. This bit may only be cleared (and not set) by the host.

0 = Device is OK.

1 = Internal chip fault detected, recommend that host microcontroller clear this bit after waiting a few seconds. Remains latched high until cleared by the host.

OVRD_ALERT (Bit 4): External pull-up on the ALERT terminal indicator. Only active when ALERT terminal isn't already being driven high by the AFE itself.

0 = No external override detected

1 = External override detected. Remains latched high until cleared by the host.

UV (Bit 3): Undervoltage fault event indicator.

0 = No UV fault is detected.

1 = UV fault is detected. Remains latched high until cleared by the host.

OV (Bit 2): Overvoltage fault event indicator.

0 = No OV fault is detected.

1 = OV fault is detected. Remains latched high until cleared by the host.

SCD (Bit 1): Short circuit in discharge fault event indicator.

0 = No SCD fault is detected.

1 = SCD fault is detected. Remains latched high until cleared by the host.

OCD (Bit 0): Over current in discharge fault event indicator.

0 = No OCD fault is detected.

1 = OCD fault is detected. Remains latched high until cleared by the host.

Table 7-2. CELLBAL1 (0x01) for bq76920, bq76930, and bq76940

BIT	7	6	5	4	3	2	1	0
NAME	—	—	—	CB5	CB4	CB3	CB2	CB1
RESET	0	0	0	0	0	0	0	0
ACCESS	R	R	R	RW	RW	RW	RW	RW

CBx (Bits 4–0):

0 = Cell balancing on Cell “x” is disabled.

1 = Cell balancing on Cell “x” is enabled.

Table 7-3. CELLBAL2 (0x02) for bq76930 and bq76940

BIT	7	6	5	4	3	2	1	0
NAME	—	—	—	CB10	CB9	CB8	CB7	CB6
RESET	0	0	0	0	0	0	0	0
ACCESS	R	R	R	RW	RW	RW	RW	RW

CBx (Bits 4–0):

0 = Cell balancing on Cell “x” is disabled.

1 = Cell balancing on Cell “x” is enabled.

Table 7-4. CELLBAL3 (0x03) for bq76940

BIT	7	6	5	4	3	2	1	0
NAME	—	—	—	CB15	CB14	CB13	CB12	CB11
RESET	0	0	0	0	0	0	0	0
ACCESS	R	R	R	RW	RW	RW	RW	RW

CBx (Bits 4–0):

0 = Cell balancing on Cell “x” is disabled.

1 = Cell balancing on Cell “x” is enabled.

Table 7-5. SYS_CTRL1 (0x04)

BIT	7	6	5	4	3	2	1	0
NAME	LOAD_ PRESENT	—	—	ADC_EN	TEMP_SEL	RSVD	SHUT_A	SHUT_B
RESET	0	0	0	0	0	0	0	0

Table 7-5. SYS_CTRL1 (0x04) (continued)

BIT	7	6	5	4	3	2	1	0
ACCESS	R	R	R	RW	RW	RW	RW	RW

LOAD_PRESENT (Bit 7): Valid only when [CHG_ON] = 0. Is high if CHG terminal is detected to exceed VLOAD_DETECT while CHG_ON = 0, which suggests that external load is present. Note this bit is read-only and automatically clears when load is removed.

0 = CHG terminal < VLOAD_DETECT or [CHG_ON] = 1.

1 = CHG terminal >VLOAD_DETECT, while [CHG_ON] = 0.

ADC_EN (Bit 4): ADC enable command

0 = Disable voltage and temperature ADC readings (also disables OV protection)

1 = Enable voltage and temperature ADC readings (also enables OV protection)

TEMP_SEL (Bit 3): TSx_HI and TSx_LO temperature source

0 = Store internal die temperature voltage reading in TSx_HI and TSx_LO

1 = Store thermistor reading in TSx_HI and TSx_LO (all thermistor ports)

RSVD (Bit 2): Reserved, do not set to 1.

SHUT_A, SHUT_B (Bits 1–0): Shutdown command from host microcontroller. Must be written in a specific sequence, shown below.

00 then non-01 then 01 then 10 = Device powers down and enters SHIP mode.

Other = Device ignores the command.

Table 7-6. SYS_CTRL2 (0x05)

BIT	7	6	5	4	3	2	1	0
NAME	DELAY_DIS	CC_EN	CC_ ONESHOT	RSVD	RSVD	RSVD	DSG_ON	CHG_ON
RESET	0	0	0	0	0	0	0	0
ACCESS	RW	RW	RW	RW	RW	RW	RW	RW

DELAY_DIS (Bit 7): Disable OV, UV, OCD, and SCD delays for faster customer production testing.

0 = Normal delay settings

1 = OV, UV, OCD and SCD delay circuit is bypassed, creating zero delay (approximately 250 ms).

CC_EN (Bit 6): Coulomb counter continuous operation enable command. If set high, *[CC_ONESHOT]* bit is ignored.

0 = Disable CC continuous readings

1 = Enable CC continuous readings and ignore *[CC_ONESHOT]* state

CC_ONESHOT (Bit 5): Coulomb counter single 250-ms reading trigger command. If set to 1, the coulomb counter will be activated for a single 250-ms reading, and then turned back off. *[CC_ONESHOT]* will also be cleared at the conclusion of this reading, while *[CC_READY]* bit will be set to 1.

0 = No action

1 = Enable single CC reading (only valid if *[CC_EN]* = 0), and *[CC_READY]* = 0)

RSVD (Bit 4–2): Reserved. Do not use.

DSG_ON (Bit 1): Discharge FET driver (low side NCH) or discharge signal control

0 = DSG is off.

1 = DSG is on.

CHG_ON (Bit 0): Discharge FET driver (low side NCH) or discharge signal control

0 = CHG is off.

1 = CHG is on.

Table 7-7. PROTECT1 (0x06)

BIT	7	6	5	4	3	2	1	0
NAME	RSNS	—	RSVD	SCD_D1	SCD_D0	SCD_T2	SCD_T1	SCD_T0
RESET	TBD	0	0	TBD	TBD	TBD	TBD	TBD
ACCESS	RW	R	RW	RW	RW	RW	RW	RW

RSNS (Bit 7): Allows for doubling the OCD and SCD thresholds simultaneously

0 = OCD and SCD thresholds at lower input range

1 = OCD and SCD thresholds at upper input range

RSVD (Bit 5): Reserved, do not set to 1.

SCD_D2:0 (Bits 4–3): Short circuit in discharge delay setting. A 400-µs setting is recommended only in systems using maximum cell measurement input resistance, Rc, of 1 kΩ (which corresponds to minimum internal cell balancing current or external cell balancing configuration).

Code	(in µs)
0x0	70
0x1	100
0x2	200
0x3	400

SCD_T2:0 (Bits 2–0): Short circuit in discharge threshold setting

Code	RSNS = 1 (in mV)	RSNS = 0 (in mV)
0x0	44	22
0x1	67	33
0x2	89	44
0x3	111	56
0x4	133	67
0x5	155	78
0x6	178	89
0x7	200	100

Table 7-8. PROTECT2 (0x07)

BIT	7	6	5	4	3	2	1	0
NAME	—	OCD_D2	OCD_D1	OCD_D0	OCD_T3	OCD_T2	OCD_T1	OCD_T0
RESET	0	TBD	TBD	TBD	TBD	TBD	TBD	TBD
ACCESS	R	RW	RW	RW	RW	RW	RW	RW

OCD_D2:0 (Bits 6–4): Overcurrent in discharge delay setting

Code	(in ms)
0x0	10
0x1	20
0x2	40
0x3	80
0x4	160
0x5	320
0x6	640

Code	(in ms)
0x7	1280

OCD_T3:0 (Bits 3–0): Overcurrent in discharge threshold setting.

Code	RSNS = 1 (in mV)	(RSNS = 0 (in mV)
0x0	17	8
0x1	22	11
0x2	28	14
0x3	33	17
0x4	39	19
0x5	44	22
0x6	50	25
0x7	56	28
0x8	61	31
0x9	67	33
0xA	72	36
0xB	78	39
0xC	83	42
0xD	89	44
0xE	94	47
0xF	100	50

Table 7-9. PROTECT3 (0x08)

BIT	7	6	5	4	3	2	1	0
NAME	UV_D1	UV_D0	OV_D1	OV_D0	RSVD	RSVD	RSVD	RSVD
RESET	0	0	0	0	1	0	0	0
ACCESS	RW	RW	RW	RW	RW	RW	RW	RW

UV_D1:0 (Bits 7–6): Undervoltage delay setting

Code	(in s)
0x0	1
0x1	4
0x2	8
0x3	16

OV_D1:0 (Bits 5–4): Overvoltage delay setting

Code	(in s)
0x0	1
0x1	2
0x2	4
0x3	8

RSVD (Bits 3–0): These bits are for TI internal debug use only and must be configured to the default settings indicated.

Table 7-10. OV_TRIP (0x09)

BIT	7	6	5	4	3	2	1	0
NAME	OV_T7	OV_T6	OV_T5	OV_T4	OV_T3	OV_T2	OV_T1	OV_T0
RESET	1	0	1	0	1	1	0	0
ACCESS	RW	RW	RW	RW	RW	RW	RW	RW

OV_T7:0 (Bits 7–0): Middle 8 bits of the direct ADC mapping of the desired OV protection threshold, with upper 2 MSB set to 10 and lower 2 LSB set to 1000. The equivalent OV threshold is mapped to: 10-OV_T<7:0>1000.

By default, OV_TRIP is configured to a 0xAC setting.

Note that OV_TRIP is based on the ADC voltage, which requires back-calculation using the GAIN and OFFSET values stored in ADCGAIN<4:0>and ADCOFFSET<7:0>.

Table 7-11. UV_TRIP (0x0A)

BIT	7	6	5	4	3	2	1	0
NAME	UV_T7	UV_T6	UV_T5	UV_T4	UV_T3	UV_T2	UV_T1	UV_T0
RESET	1	0	0	1	0	1	1	1
ACCESS	RW	RW	RW	RW	RW	RW	RW	RW

UV_T7:0 (Bits 7–0): Middle 8 bits of the direct ADC mapping of the desired UV protection threshold, with upper 2 MSB set to 01 and lower 4 LSB set to 0000. In other words, the equivalent OV threshold is mapped to: 01-UV_T<7:0>–0000.

By default, UV_TRIP is configured to a 0x97 setting. .

Note that UV_TRIP is based on the ADC voltage, which requires back-calculation using the GAIN and OFFSET values stored in ADCGAIN<4:0>and ADCOFFSET<7:0>.

Table 7-12. CC_CFG REGISTER (0x0B)

BIT	7	6	5	4	3	2	1	0
NAME	—	—	CC_CFG5	CC_CFG4	CC_CFG3	CC_CFG2	CC_CFG1	CC_CFG0
RESET	0	0	0	0	0	0	0	0
ACCESS	R	R	RW	RW	RW	RW	RW	RW

CC_CFG5:0 (Bits 5–0): For optimal performance, these bits should be programmed to 0x19 upon device startup.

7.2 Read-Only Registers

Table 7-13. ALL REGISTERS

VC1_HI, _LO (0x0C–0x0D), VC2_HI, _LO (0x0E–0x0F), VC3_HI, _LO (0x10–0x11), VC4_HI, _LO (0x12–0x13), VC5_HI, _LO (0x14–0x15) / bq76930, bq76940: VC6_HI, _LO (0x16–0x17), VC7_HI, _LO (0x18–0x19), VC8_HI, _LO (0x1A–0x1B), VC9_HI, _LO (0x1C–0x1D), VC10_HI, _LO (0x1E–0x1F) / bq76940: VC11_HI, _LO (0x20–0x21), VC12_HI, _LO (0x22–0x23), VC13_HI, _LO (0x24–0x25), VC14_HI, _LO (0x26–0x27), VC15_HI, _LO (0x28–0x29)								
BIT	7	6	5	4	3	2	1	0
NAME	—	—	D13	D12	D11	D10	D9	D8
RESET	0	0	0	0	0	0	0	0

Table 7-13. ALL REGISTERS (continued)

VC1_HI, _LO (0x0C–0x0D), VC2_HI, _LO (0x0E–0x0F), VC3_HI, _LO (0x10–0x11), VC4_HI, _LO (0x12–0x13), VC5_HI, _LO (0x14–0x15) / bq76930, bq76940: VC6_HI, _LO (0x16–0x17), VC7_HI, _LO (0x18–0x19), VC8_HI, _LO (0x1A–0x1B), VC9_HI, _LO (0x1C–0x1D), VC10_HI, _LO (0x1E–0x1F) / bq76940: VC11_HI, _LO (0x20–0x21), VC12_HI, _LO (0x22–0x23), VC13_HI, _LO (0x24–0x25), VC14_HI, _LO (0x26–0x27), VC15_HI, _LO (0x28–0x29)							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	D7	D6	D5	D4	D3	D2	D1	D0
RESET	0	0	0	0	0	0	0	0

D11:8 (Bits 3–0): Cell “x” ADC reading, upper 6 MSB. Always returned as an atomic value if both high and low registers are read in the same transaction (using address auto-increment).

D7:0 (Bits 7–0): Cell ”x” ADC reading, lower 8 LSB.

Table 7-14. BAT_HI (0x2A) and BAT_LO (0x2B)

BIT	7	6	5	4	3	2	1	0
NAME	D15	D14	D13	D12	D11	D10	D9	D8
RESET	0	0	0	0	0	0	0	0
NAME	D7	D6	D5	D4	D3	D2	D1	D0
RESET	0	0	0	0	0	0	0	0

D15:8 (Bits 7–0):

BAT calculation based on adding up Cells 1–15, upper 8 MSB. Always returned as an atomic value if both high and low registers are read in the same transaction (using address auto-increment).

D7:0 (Bits 7–0):

BAT calculation based on adding up Cells 1–15, lower 8 LSB

Table 7-15. TS1_HI (0x2C) and TS1_LO (0x2D)

BIT	7	6	5	4	3	2	1	0
NAME	—	—	D13	D12	D11	D10	D9	D8
RESET	0	0	0	0	0	0	0	0
NAME	D7	D6	D5	D4	D3	D2	D1	D0
RESET	0	0	0	0	0	0	0	0

D11:8 (Bits 3–0): TS1 or DIETEMP ADC reading, upper 6 MSB. Always returned as an atomic value if both high and low registers are read in the same transaction (using address auto-increment).

D7:0 (Bits 7–0): TS1 or DIETEMP ADC reading, lower 8 LSB

Table 7-16. TS2_HI (0x2E) and TS2_LO (0x2F)

BIT	7	6	5	4	3	2	1	0
NAME	—	—	D13	D12	D11	D10	D9	D8
RESET	0	0	0	0	0	0	0	0
NAME	D7	D6	D5	D4	D3	D2	D1	D0
RESET	0	0	0	0	0	0	0	0

D11:8 (Bits 3–0): TS2 ADC reading, upper 6 MSB. Always returned as an atomic value if both high and low registers are read in the same transaction (using address auto-increment).

D7:0 (Bits 7–0): TS2 ADC reading, lower 8 LSB

Table 7-17. TS3_HI (0x30) and TS3_LO (0x31)

BIT	7	6	5	4	3	2	1	0
NAME	—	—	D13	D12	D11	D10	D9	D8
RESET	0	0	0	0	0	0	0	0
NAME	D7	D6	D5	D4	D3	D2	D1	D0
RESET	0	0	0	0	0	0	0	0

D11:8 (Bits 3–0): TS3 ADC reading, upper 6 MSB. Always returned as an atomic value if both high and low registers are read in the same transaction (using address auto-increment).

D7:0 (Bits 7–0): TS3 ADC reading, lower 8 LSB

Table 7-18. CC_HI (0x32) and CC_LO (0x33)

BIT	7	6	5	4	3	2	1	0
NAME	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8
RESET	0	0	0	0	0	0	0	0
NAME	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
RESET	0	0	0	0	0	0	0	0

CC15:8 (Bits 7–0): Coulomb counter upper 8 MSB. Always returned as an atomic value if both high and low registers are read in the same transaction (using address auto-increment).

CC7:0 (Bits 7–0): Coulomb counter lower 8 LSB

Table 7-19. ADCGAIN1 (0x50)

BIT	7	6	5	4	3	2	1	0
NAME	—	—	—	—	ADCGAIN4	ADCGAIN3	—	—
RESET	—	—	—	—	—	—	—	—
ACCESS	R	R	R	R	R	R	R	R

Table 7-20. ADCGAIN2 (0x59)

BIT	7	6	5	4	3	2	1	0
NAME	ADCGAIN2	ADCGAIN1	ADCGAIN0	—	—	—	—	—
RESET	—	—	—	—	—	—	—	—
ACCESS	R	R	R	R	R	R	R	R

ADCGAIN4:3 (Bits 3–2, address 0x50):

ADC offset upper 2 MSB

ADCOFFSET2:0 (Bits 7–5, address 0x59):

ADC offset lower 3 LSB

ADCGAIN<4:0> is a production-trimmed value for the ADC transfer function, in units of µV/LSB. The range is 365 µV/LSB to 396 µV/LSB, in steps of 1 µV/LSB, and may be calculated as follows:

GAIN = 365 µV/LSB + (ADCGAIN<4:0>in decimal) x (1 µV/LSB)

Alternately, a conversion table is provided below:

ADC GAIN	Gain (µV/LSB)	ADC GAIN	Gain (µV/LSB)
0x00	365	0x10	381
0x01	366	0x11	382
0x02	367	0x12	383
0x03	368	0x13	384
0x04	369	0x14	385
0x05	370	0x15	386
0x06	371	0x16	387
0x07	372	0x17	388
0x08	373	0x18	389
0x09	374	0x19	390
0x0A	375	0x1A	391
0x0B	376	0x1B	392
0x0C	377	0x1C	393
0x0D	378	0x1D	394
0x0E	379	0x1E	395
0x0F	380	0x1F	396

Table 7-21. ADCOFFSET (0x51)

BIT	7	6	5	4	3	2	1	0
NAME	ADC OFFSET7	ADC OFFSET6	ADC OFFSET5	ADC OFFSET4	ADC OFFSET3	ADC OFFSET2	ADC OFFSET1	ADC OFFSET0
RESET	—	—	—	—	—	—	—	—
ACCESS	R	R	R	R	R	R	R	R

ADCOFFSET7:0 (Bits 7–0):

ADC offset, stored in 2's complement format in mV units. Positive full-scale range corresponds to 0x7F and negative full-scale corresponds to 0x80. The full-scale input range is –128 mV to 127 mV, with an LSB of 1 mV.

Some example offsets are shown in the table below.

ADCOFFSET	Offset (mV)
0x00	0
0x01	1
0x7F	127
0x80	–128
0x81	–127
0xFF	–1

8 Device and Documentation Support

8.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
bq76920	Click here	Click here	Click here	Click here	Click here
bq76930	Click here	Click here	Click here	Click here	Click here
bq76940	Click here	Click here	Click here	Click here	Click here

8.2 Related Documentation

For related documentation, see the following: *bq76920 Evaluation Module User 's Guide* (SLVU924).

8.3 Trademarks

I^2C is a trademark of NXP B.V. Corporation.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from Disclosing party under this Agreement, or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2013) to Revision A	Page
• Changed some devices from Product Preview to Production Data	3
• Changed bq76940 with bq783xx Companion Controller IC Schematic	11
• Changed the $t_{INDCELL}$ test condition	16
• Deleted duplicate CELLBAL3 table	35

Changes from Revision A (December 2013) to Revision B	Page
• Changed title of the data manual	1
• Changed Ordering Information table to Device Comparison table	3
• Changed some devices to Product Preview	3
• Changed R_f max value	14
• Changed verbiage in I^2C Communications	30
• Changed SYS_STAT D6 bit name	33

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ7692000PW	PREVIEW	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7692000	
BQ7692000PWR	PREVIEW	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7692000	
BQ7692003PW	PREVIEW	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7692003	
BQ7692003PWR	PREVIEW	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7692003	
BQ7692006PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7692006	Samples
BQ7692006PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7692006	Samples
BQ7693000DBT	PREVIEW	TSSOP	DBT	30		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7693000	
BQ7693000DBTR	PREVIEW	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7693000	
BQ7693003DBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7693003	Samples
BQ7693003DBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7693003	Samples
BQ7693006DBT	PREVIEW	TSSOP	DBT	30		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7693006	
BQ7693006DBTR	PREVIEW	TSSOP	DBT	30		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7693006	
BQ7694000DBT	ACTIVE	TSSOP	DBT	44	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7694000	Samples
BQ7694000DBTR	ACTIVE	TSSOP	DBT	44	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7694000	Samples
BQ7694001DBT	ACTIVE	TSSOP	DBT	44	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7694001	Samples
BQ7694001DBTR	ACTIVE	TSSOP	DBT	44	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7694001	Samples
BQ7694002DBT	ACTIVE	TSSOP	DBT	44	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7694002	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ7694002DBTR	ACTIVE	TSSOP	DBT	44	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7694002	Samples
BQ7694003DBT	ACTIVE	TSSOP	DBT	44	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7694003	Samples
BQ7694003DBTR	ACTIVE	TSSOP	DBT	44	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7694003	Samples
BQ7694006DBT	ACTIVE	TSSOP	DBT	44	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7694006	Samples
BQ7694006DBTR	ACTIVE	TSSOP	DBT	44	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7694006	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

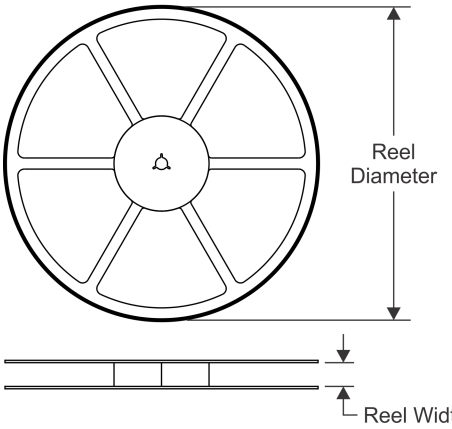
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

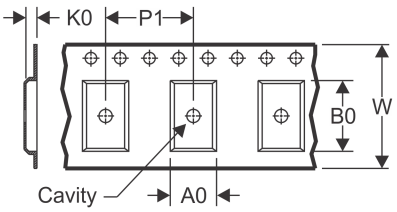
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

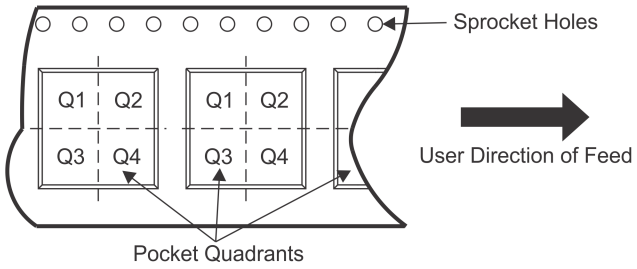


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

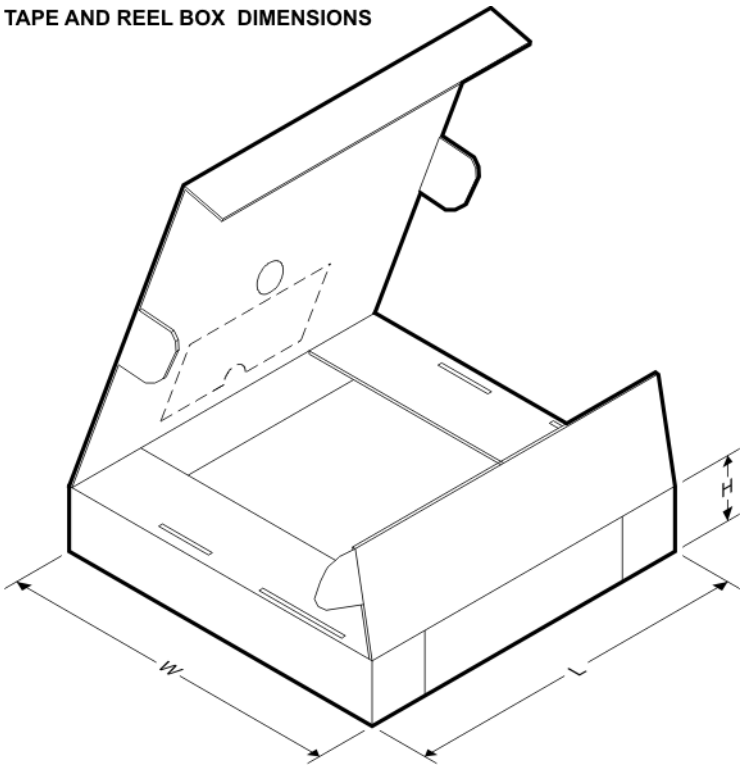
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ7692006PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

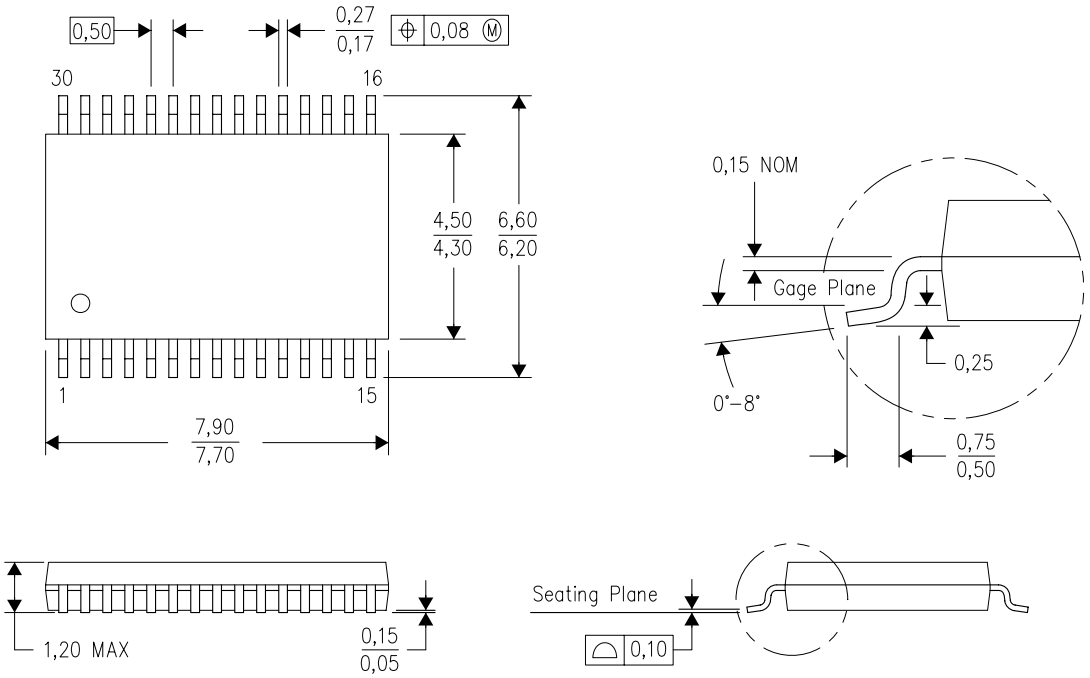
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ7692006PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

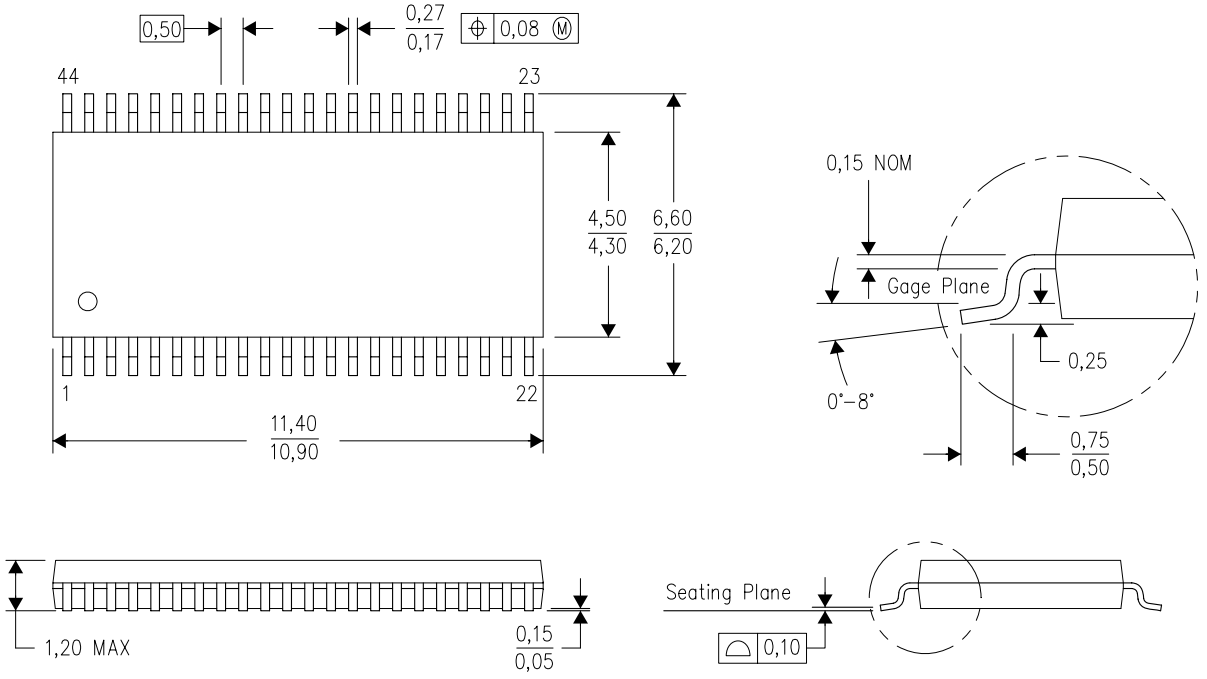
DBT (R–PDSO–G30) PLASTIC SMALL OUTLINE



4073252–5/I 03/11

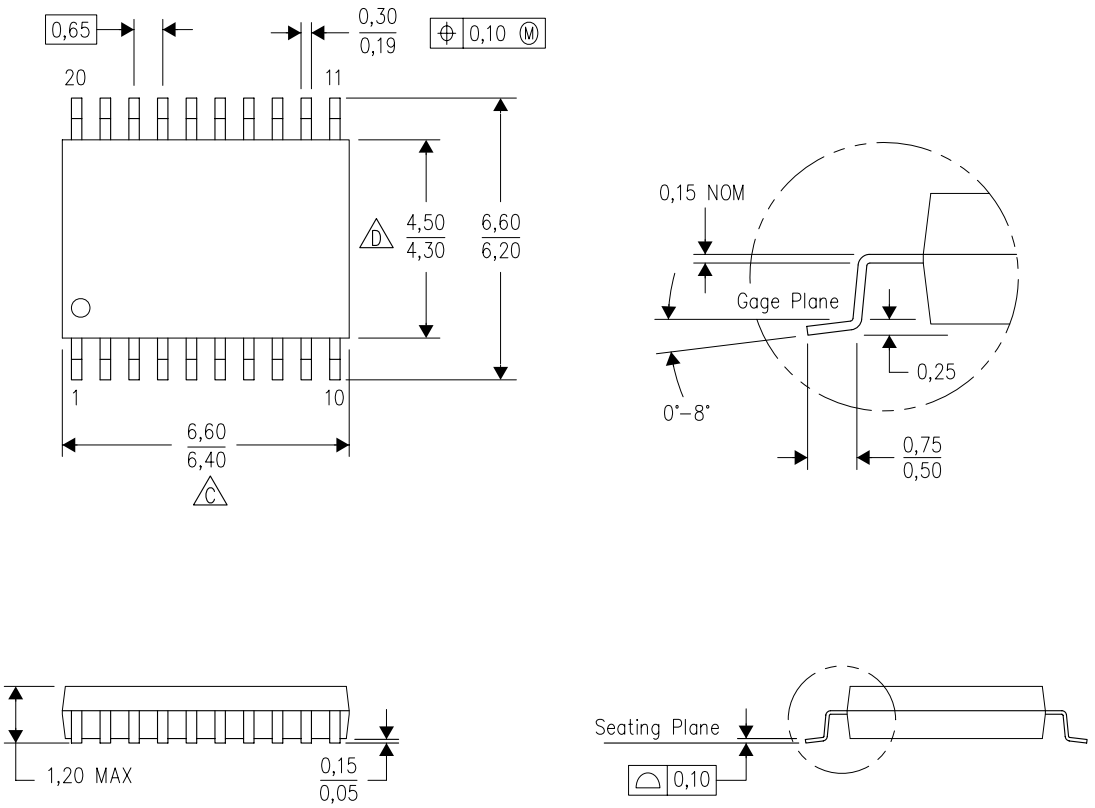
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–153.

DBT (R–PDSO–G44) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

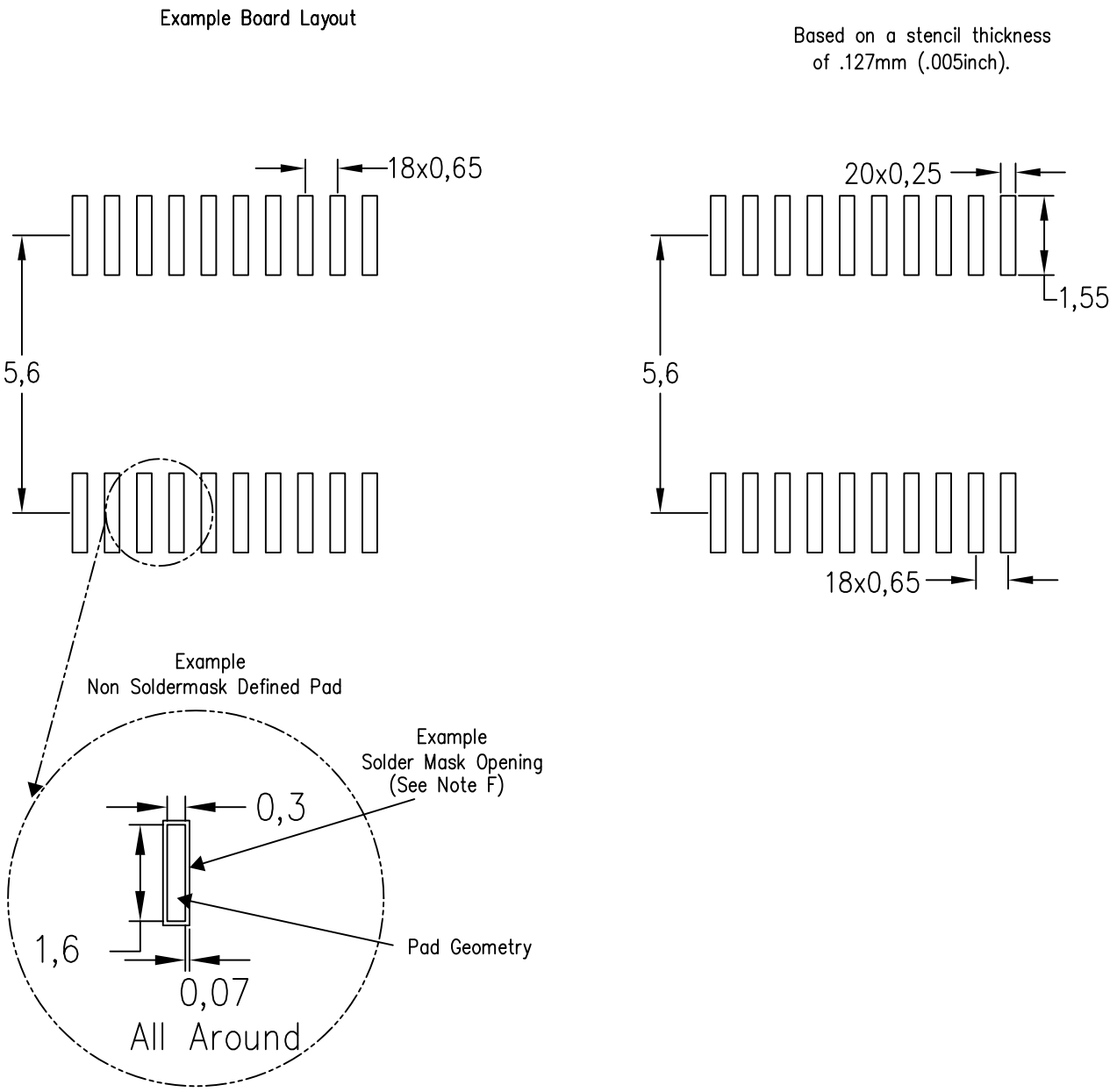
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265