DRV8833 Dual H-Bridge Motor Driver

1 Features

- Dual-H-Bridge Current-Control Motor Driver
  - Can Drive Two DC Motors or One Stepper Motor
  - Low MOSFET ON-Resistance: HS + LS 360 mΩ
- Output Current (at V_M = 5 V, 25°C)
  - 1.5-A RMS, 2-A Peak per H-Bridge in PWP and RTY Package Options
  - 500-mA RMS, 2-A Peak per H-Bridge in PW Package Option
- Outputs can be in Parallel for
  - 3-A RMS, 4-A Peak (PWP and RTY)
  - 1-A RMS, 4-A Peak (PW)
- Wide Power Supply Voltage Range: 2.7 to 10.8 V
- PWM Winding Current Regulation and Current Limiting
- Thermally Enhanced Surface-Mount Packages

2 Applications

- Battery-Powered Toys
- POS Printers
- Video Security Cameras
- Office Automation Machines
- Gaming Machines
- Robotics

3 Description

The DRV8833 device provides a dual bridge motor driver solution for toys, printers, and other mechatronic applications.

The device has two H-bridge drivers, and can drive two DC brush motors, a bipolar stepper motor, solenoids, or other inductive loads.

The output driver block of each H-bridge consists of N-channel power MOSFETs configured as an H-bridge to drive the motor windings. Each H-bridge includes circuitry to regulate or limit the winding current.

Internal shutdown functions with a fault output pin are provided for overcurrent protection, short-circuit protection, undervoltage lockout, and overtemperature. A low-power sleep mode is also provided.

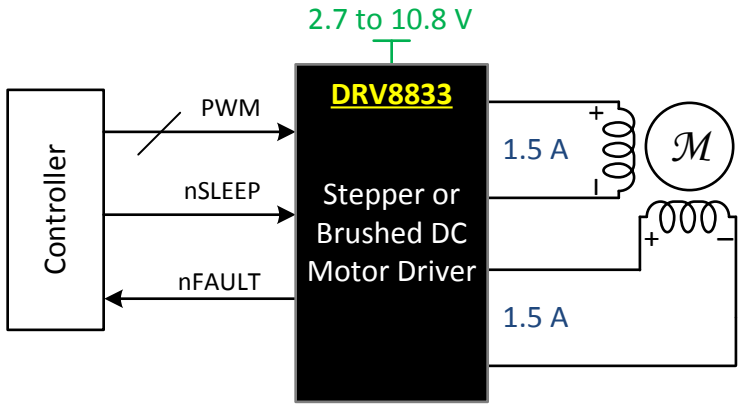
The DRV8833 is packaged in a 16-pin WQFN package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8833	TSSOP (16)	5.00 mm × 4.40 mm
	HTSSOP (16)	5.00 mm × 4.40 mm
	WQFN (16)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2015) to Revision E — **Page**

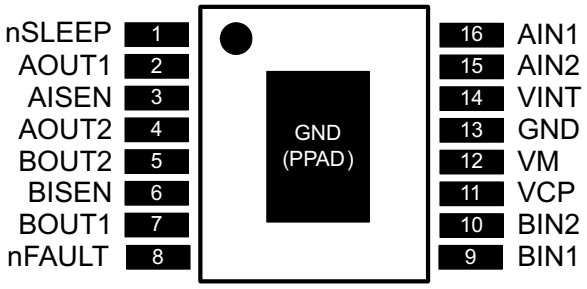
- Updated *Features* bullets to include specifications for other packages ... 1
- Added note back to *Pin Functions* regarding the different I/O types ... 3
- Corrected the device name and current regulation description in *Overview* ... 8
- Corrected output current to 1.5-A RMS from 700-mA RMS ... 8

Changes from Revision C (January 2013) to Revision D — **Page**

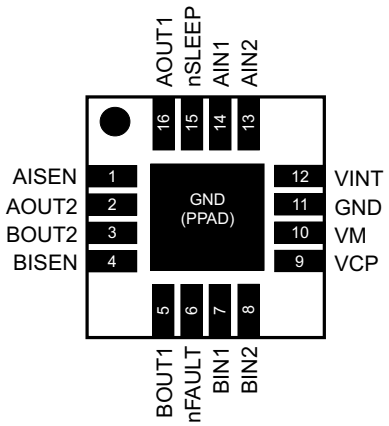
- Added *ESD Ratings table*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

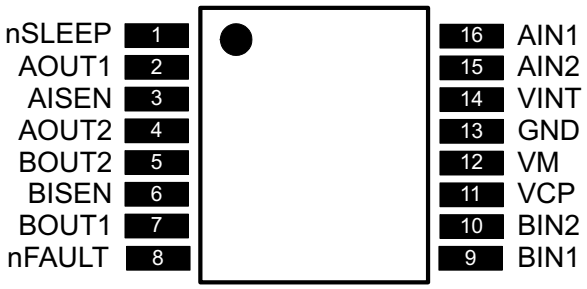
PWP Package
16-Pin HTSSOP
Top View



RTY Package
16-Pin WQFN
Top View



PW Package
16-Pin TSSOP
Top View



Pin Functions

PIN			I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	WQFN	HTSSOP, TSSOP			
POWER AND GROUND					
GND	11 PPAD	13	—	Device ground. HTSSOP package has PowerPAD.	Both the GND pin and device PowerPAD must be connected to ground.
VINT	12	14	—	Internal supply bypass	Bypass to GND with 2.2-µF, 6.3-V capacitor.
VM	10	12	—	Device power supply	Connect to motor supply. A 10-µF (minimum) ceramic bypass capacitor to GND is recommended.
VCP	9	11	IO	High-side gate drive voltage	Connect a 0.01-µF, 16-V (minimum) X7R ceramic capacitor to VM.
CONTROL					
AIN1	14	16	I	Bridge A input 1	Logic input controls state of AOUT1. Internal pulldown.
AIN2	13	15	I	Bridge A input 2	Logic input controls state of AOUT2. Internal pulldown.
BIN1	7	9	I	Bridge B input 1	Logic input controls state of BOUT1. Internal pulldown.
BIN2	8	10	I	Bridge B input 2	Logic input controls state of BOUT2. Internal pulldown.
nSLEEP	15	1	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode and reset all internal logic. Internal pulldown.

(1) I = Input, O = Output, OZ = Tri-state output, OD = Open-drain output, IO = Input/output

Pin Functions (continued)

PIN			I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	WQFN	HTSSOP, TSSOP			
STATUS					
nFAULT	6	8	OD	Fault output	Logic low when in fault condition (overtemperature, overcurrent)
OUTPUT					
AISEN	1	3	IO	Bridge A ground / I_{SENSE}	Connect to current sense resistor for bridge A, or GND if current control not needed
BISEN	4	6	IO	Bridge B ground / I_{SENSE}	Connect to current sense resistor for bridge B, or GND if current control not needed
AOUT1	16	2	O	Bridge A output 1	Connect to motor winding A
AOUT2	2	4	O	Bridge A output 2	
BOUT1	5	7	O	Bridge B output 1	Connect to motor winding B
BOUT2	3	5	O	Bridge B output 2	

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
VM	Power supply voltage	–0.3	11.8	V
	Digital input pin voltage	–0.5	7	V
	xISEN pin voltage	–0.3	0.5	V
	Peak motor drive output current	Internally limited		A
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_A = 25°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range(1)	2.7		10.8	V
V_{DIGIN}	Digital input pin voltage range	–0.3		5.75	V
I_{OUT}	RTY package continuous RMS or DC output current per bridge(2)			1.5	A

(1) $R_{DS(ON)}$ increases and maximum output current is reduced at VM supply voltages below 5 V.
(2) V_M = 5 V, power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC(1)		DRV8833			UNIT
		PWP (HTSSOP)	RTY (WQFN)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.5	37.2	103.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.9	34.3	38	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.8	15.3	48.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	0.3	3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.5	15.4	47.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.8	3.5	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{VM}	VM operating supply current	V_M = 5 V, xIN1 = 0 V, xIN2 = 0 V		1.7	3	mA
I_{VMQ}	VM sleep mode supply current	V_M = 5 V		1.6	2.5	µA
V_{UVLO}	VM undervoltage lockout voltage	V_M falling			2.6	V
V_{HYS}	VM undervoltage lockout hysteresis			90		mV
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage	nSLEEP			0.5	V
		All other pins			0.7	
V_{IH}	Input high voltage	nSLEEP	2.5			V
		All other pins	2			
V_{HYS}	Input hysteresis			0.4		V
R_{PD}	Input pulldown resistance	nSLEEP		500		kΩ
		All except nSLEEP		150		
I_{IL}	Input low current	VIN = 0			1	µA
I_{IH}	Input high current	VIN = 3.3 V, nSLEEP		6.6	13	µA
		VIN = 3.3 V, all except nSLEEP		16.5	33	
t_{DEG}	Input deglitch time			450		ns
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
H-BRIDGE FETs						
$R_{DS(ON)}$	HS FET on resistance	V_M = 5 V, I_O = 500 mA, T_J = 25°C		200		mΩ
		V_M = 5 V, I_O = 500 mA, T_J = 85°C			325	
		V_M = 2.7 V, I_O = 500 mA, T_J = 25°C		250		
		V_M = 2.7 V, I_O = 500 mA, T_J = 85°C			350	
	LS FET on resistance	V_M = 5 V, I_O = 500 mA, T_J = 25°C		160		
		V_M = 5 V, I_O = 500 mA, T_J = 85°C			275	
		V_M = 2.7 V, I_O = 500 mA, T_J = 25°C		200		
		V_M = 2.7 V, I_O = 500 mA, T_J = 85°C			300	
I_{OFF}	Off-state leakage current	V_M = 5 V, T_J = 25°C, V_{OUT} = 0 V	–1		1	µA
MOTOR DRIVER						
f_{PWM}	Current control PWM frequency	Internal PWM frequency		50		kHz
t_R	Rise time	V_M = 5 V, 16 Ω to GND, 10% to 90% V_M		180		ns
t_F	Fall time	V_M = 5 V, 16 Ω to GND, 10% to 90% V_M		160		ns
t_{PROP}	Propagation delay INx to OUTx	V_M = 5 V		1.1		µs
t_{DEAD}	Dead time(1)	V_M = 5 V		450		ns
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		2	3.3		A
t_{DEG}	OCP Deglitch time		4			µs
t_{OCP}	Overcurrent protection period			1.35		ms
t_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C

(1) Internal dead time. External implementation is not necessary.

Electrical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CONTROL						
V_{TRIP}	xISEN trip voltage		160	200	240	mV
t_{BLANK}	Current sense blanking time			3.75		µs
SLEEP MODE						
t_{WAKE}	Start-up time	nSLEEP inactive high to H-bridge on			1	ms

6.6 Typical Characteristics

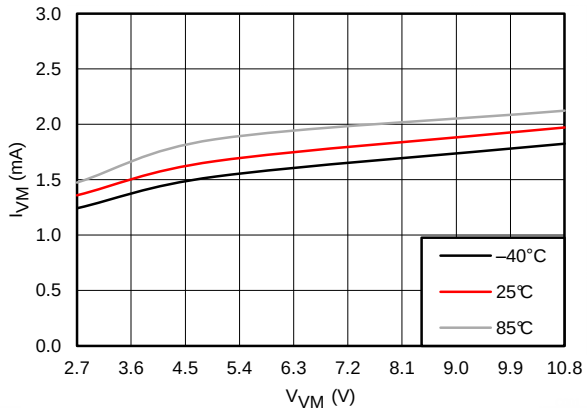


Figure 1. Operating Current

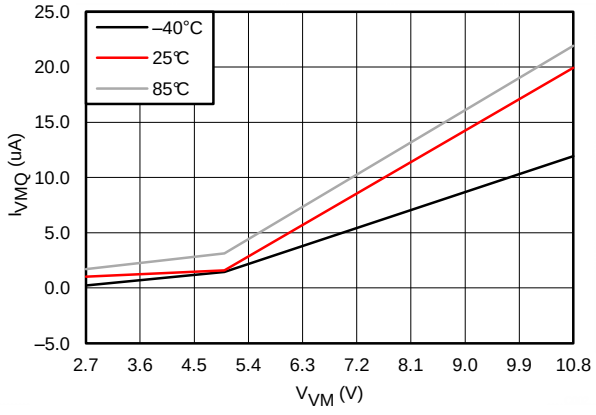


Figure 2. Sleep Current

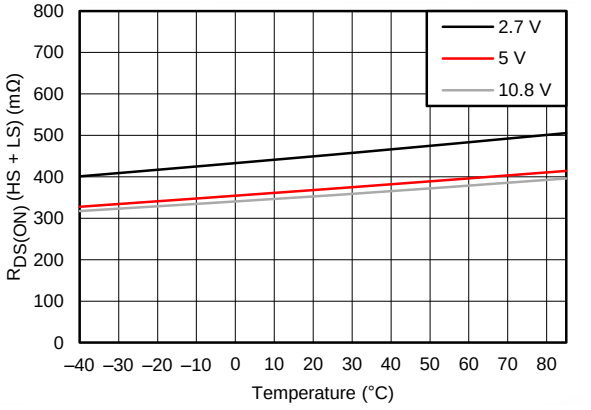


Figure 3. $R_{DS(on)}$ (HS + LS)

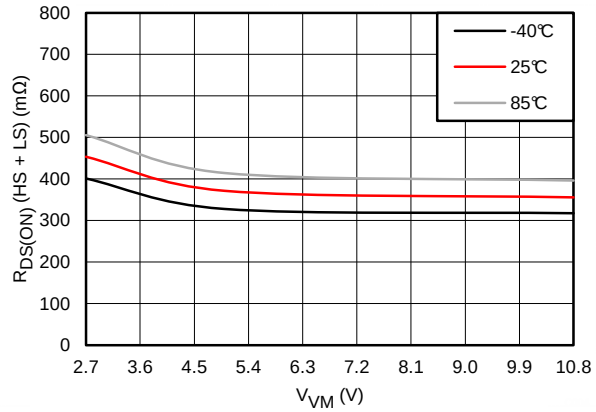


Figure 4. $R_{DS(on)}$ (HS + LS)

7 Detailed Description

7.1 Overview

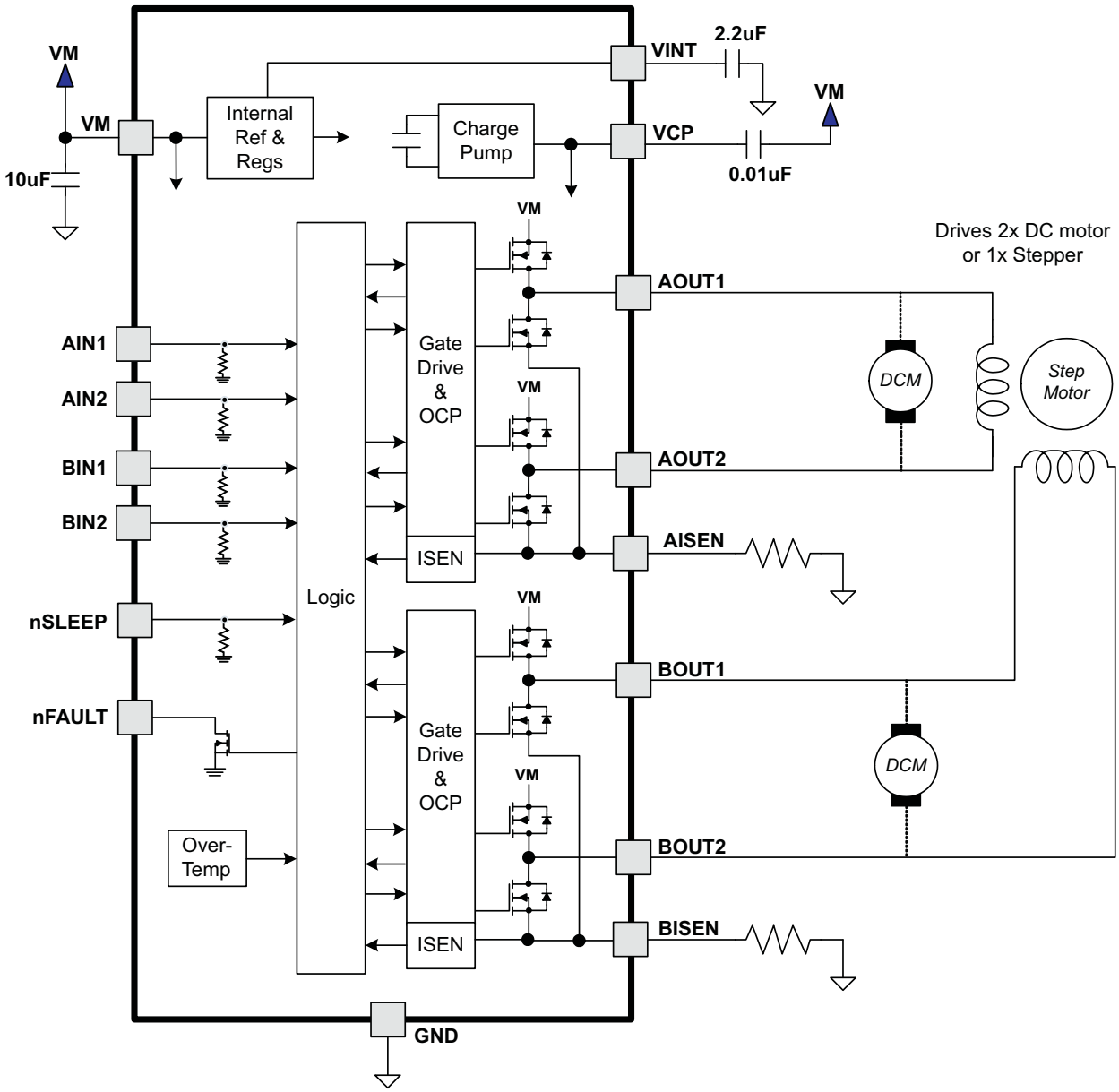
The DRV8833 device is an integrated motor driver solution for brushed DC or bipolar stepper motors. The device integrates two NMOS H-bridges and current regulation circuitry. The DRV8833 can be powered with a supply voltage from 2.7 to 10.8 V and can provide an output current up to 1.5-A RMS.

A simple PWM interface allows easy interfacing to the controller circuit.

The current regulation is a fixed frequency PWM slow decay.

The device includes a low-power sleep mode, which lets the system save power when not driving the motor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed-Frequency PWM Motor Drivers

DRV8833 contains two identical H-bridge motor drivers with current-control PWM circuitry. Figure 5 shows a block diagram of the circuitry.

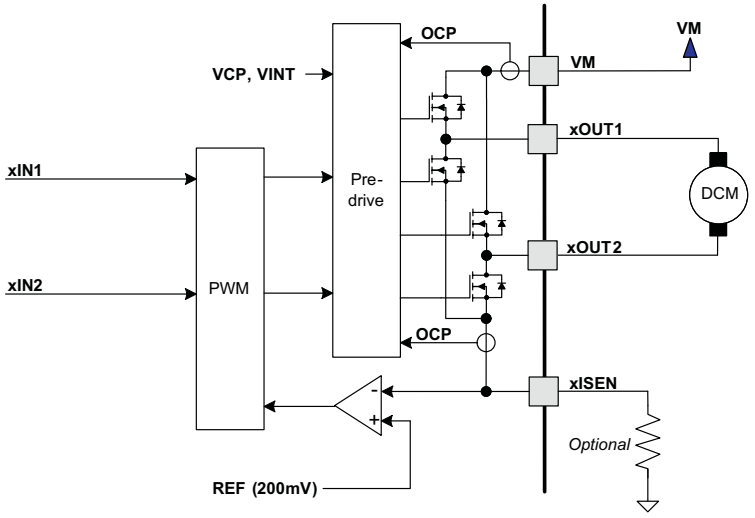


Figure 5. Motor Control Circuitry

7.3.2 Bridge Control and Decay Modes

The AIN1 and AIN2 input pins control the state of the AOUT1 and AOUT2 outputs; similarly, the BIN1 and BIN2 input pins control the state of the BOUT1 and BOUT2 outputs. Table 1 shows the logic.

Table 1. H-Bridge Logic

xIN1	xIN2	xOUT1	xOUT2	FUNCTION
0	0	Z	Z	Coast/fast decay
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake/slow decay

The inputs can also be used for PWM control of the motor speed. When controlling a winding with PWM, when the drive current is interrupted, the inductive nature of the motor requires that the current must continue to flow. This is called recirculation current. To handle this recirculation current, the H-bridge can operate in two different states: fast decay or slow decay. In fast decay mode, the H-bridge is disabled and recirculation current flows through the body diodes; in slow decay, the motor winding is shorted.

To PWM using fast decay, the PWM signal is applied to one xIN pin while the other is held low; to use slow decay, one xIN pin is held high.

Table 2. PWM Control of Motor Speed

xIN1	xIN2	FUNCTION
PWM	0	Forward PWM, fast decay
1	PWM	Forward PWM, slow decay
0	PWM	Reverse PWM, fast decay
PWM	1	Reverse PWM, slow decay

Figure 6 shows the current paths in different drive and decay modes.

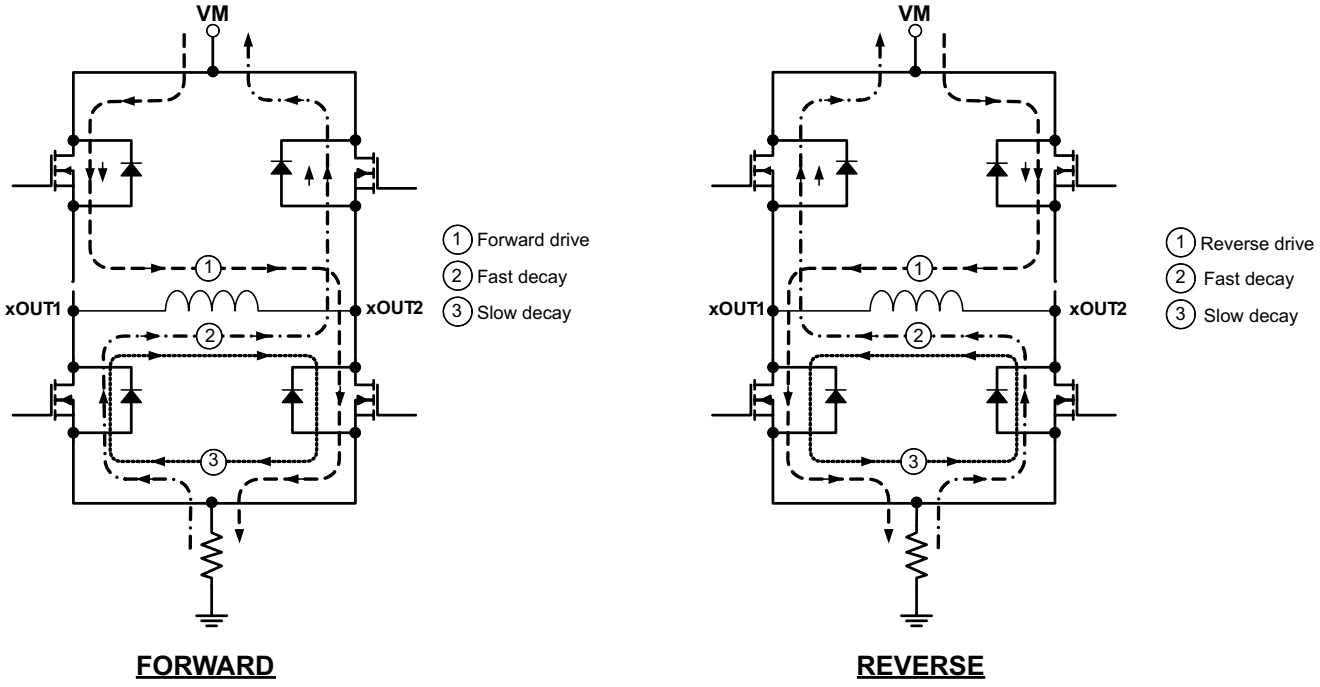


Figure 6. Drive and Decay Modes

7.3.3 Current Control

The current through the motor windings may be limited, or controlled, by a fixed-frequency PWM current regulation, or current chopping. For DC motors, current control is used to limit the start-up and stall current of the motor. For stepper motors, current control is often used at all times.

When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. If the current reaches the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle. Immediately after the current is enabled, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 µs. This blanking time also sets the minimum on time of the PWM when operating in current chopping mode.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pins with a reference voltage. The reference voltage is fixed at 200 mV.

The chopping current is calculated in Equation 1.

$$I_{CHOP} = \frac{200\ mV}{R_{ISENSE}} \quad (1)$$

Example: If a 1-Ω sense resistor is used, the chopping current will be 200 mV/1 Ω = 200 mA.

Once the chopping current threshold is reached, the H-bridge switches to slow decay mode. Winding current is recirculated by enabling both of the low-side FETs in the bridge. This state is held until the beginning of the next fixed-frequency PWM cycle.

If current control is not needed, the xISEN pins should be connected directly to ground.

7.3.4 nSLEEP Operation

Driving nSLEEP low will put the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, all internal logic is reset, and all internal clocks are stopped. All inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (up to 1 ms) needs to pass before the motor driver becomes fully operational. To make the board design simple, the nSLEEP can be pulled up to the supply (VM). TI recommends using a pullup resistor when this is done. This resistor limits the current to the input in case VM is higher than 6.5 V. Internally, the nSLEEP pin has a 500-kΩ resistor to GND. It also has a clamping Zener diode that clamps the voltage at the pin at 6.5 V. Currents greater than 250 µA can cause damage to the input structure. Hence the recommended pullup resistor would be between 20 kΩ and 75 kΩ.

7.3.5 Protection Circuits

The DRV8833 is fully protected against undervoltage, overcurrent and overtemperature events.

7.3.5.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The driver will be re-enabled after the OCP retry period (t_{OCP}) has passed. nFAULT becomes high again at this time. If the fault condition is still present, the cycle repeats. If the fault is no longer present, normal operation resumes and nFAULT remains deasserted. Please note that only the H-bridge in which the OCP is detected will be disabled while the other bridge will function normally.

Overcurrent conditions are detected independently on both high- and low-side devices; that is, a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Overcurrent protection does not use the current sense circuitry used for PWM current control, so it functions even without presence of the xISEN resistors.

7.3.5.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level, operation will automatically resume.

7.3.5.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and all internal logic will be reset. Operation will resume when VM rises above the UVLO threshold. nFAULT is driven low in the event of an undervoltage condition.

Table 3. Device Protection

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
VM undervoltage (UVLO)	V_M < 2.5 V	None	Disabled	Disabled	V_M > 2.7 V
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	FAULTn	Disabled	Operating	OCP
Thermal Shutdown (TSD)	$T_J > T_{TSD}$	FAULTn	Disabled	Operating	$T_J < T_{TSD} – T_{HYS}$

7.4 Device Functional Modes

The DRV8833 is active unless the nSLEEP pin is brought logic low. In sleep mode, the H-bridge FETs are disabled (Hi-Z). The DRV8833 is brought out of sleep mode automatically if nSLEEP is brought logic high. tWAKE must elapse before the outputs change state after wakeup.

Table 4. Modes of Operation

FAULT	CONDITION	H-BRIDGE	INTERNAL CIRCUITS
Operating	nSLEEP pin high	Operating	Operating
Sleep mode	nSLEEP pin low	Disabled	Disabled
Fault encountered	Any fault condition met	Disabled	See Table 3

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8833 is used in brushed DC or stepper motor control. The following design procedure can be used to configure the DRV8833 in a brushed DC motor application. The inputs and outputs are connected in parallel to achieve higher current.

8.2 Typical Application

The two H-bridges in the DRV8833 can be connected in parallel for double the current of a single H-bridge. The internal dead time in the DRV8833 prevents any risk of cross-conduction (shoot-through) between the two bridges due to timing differences between the two bridges. Figure 7 shows the connections.

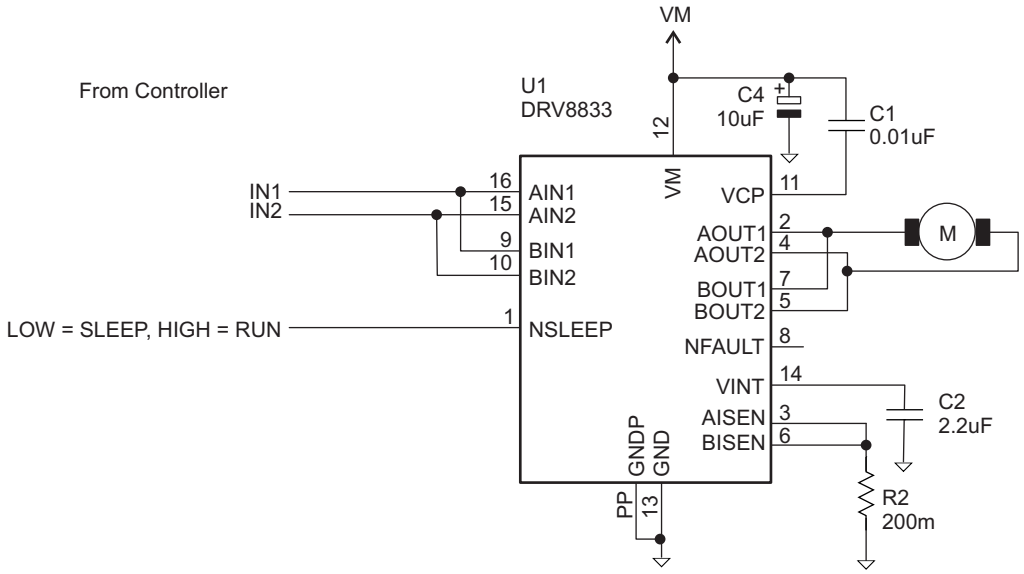


Figure 7. Parallel Mode

8.2.1 Design Requirements

Table 5. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	V_M	10 V
Motor RMS current	I_{RMS}	0.8 A
Motor start-up current	I_{START}	2 A
Motor current trip point	I_{TRIP}	2.5 A

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.2.2 Motor Current Trip Point

When the voltage on pin xISEN exceeds V_{TRIP} (0.2 V), current regulation is activated. The R_{ISENSE} resistor should be sized to set the desired I_{CHOP} level.

$$R_{ISENSE} = 0.2\ V / I_{CHOP} \quad (2)$$

To set I_{CHOP} to 1 A, R_{SENSE} = 0.2 V / 1 A = 0.2 Ω.

8.2.2.3 Sense Resistor

For optimal performance, it is important for the sense resistor to be:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{RMS}^2 \times R$. For example, if peak motor current is 3 A, RMS motor current is 2 A, and a 0.05-Ω sense resistor is used, the resistor will dissipate 2 $A^2\times$ 0.05 Ω = 0.2 W. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. For best practice, measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, the common practice is to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.

8.2.3 Application Curve

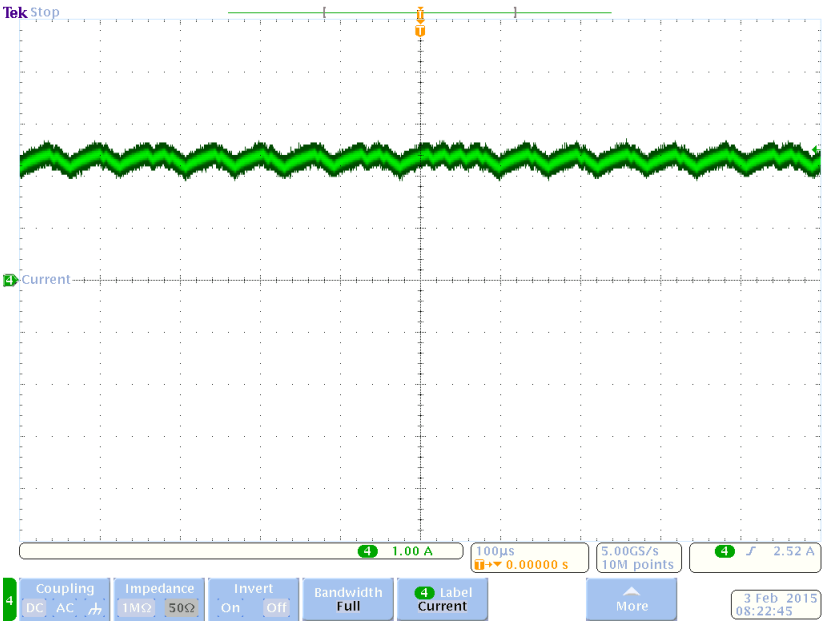


Figure 8. Current Regulation

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

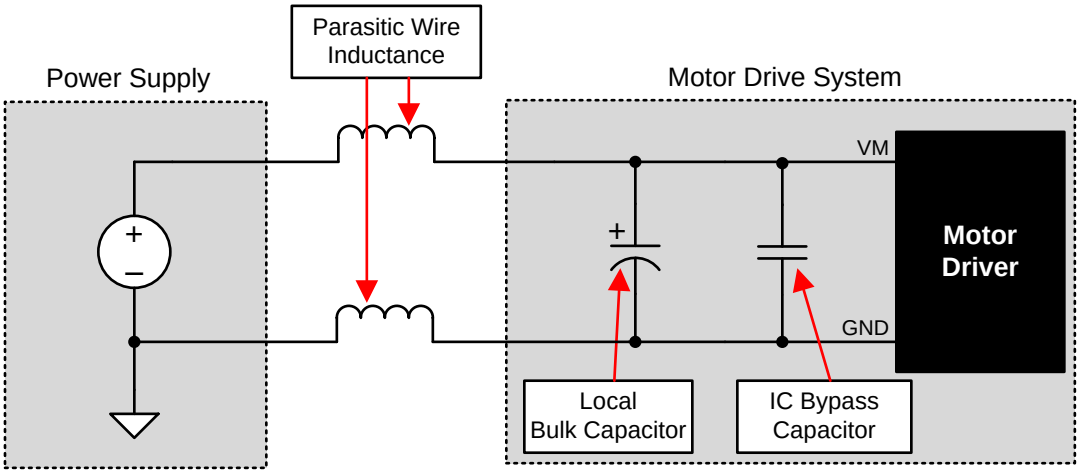


Figure 9. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

9.2 Power Supply and Logic Sequencing

There is no specific sequence for powering up the DRV8833. The presence of digital input signals is acceptable before VM is applied. After VM is applied to the DRV8833, the device begins operation based on the status of the control pins.

10 Layout

10.1 Layout Guidelines

The VM pin should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 10-µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. TI recommends a value of 0.01-µF rated for 16 V. Place this component as close to the pins as possible.

Bypass VINT to ground with a 2.2-µF ceramic capacitor rated 6.3 V. Place this bypass capacitor as close to the pin as possible.

10.1.1 Heatsinking

The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multilayer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report, *PowerPAD™ Thermally Enhanced Package* (SLMA002) and TI application brief, *PowerPAD™ Made Easy* (SLMA004), available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

NOTE

The PW package option is not thermally enhanced and TI recommends adhering to the power dissipation limits.

10.2 Layout Example

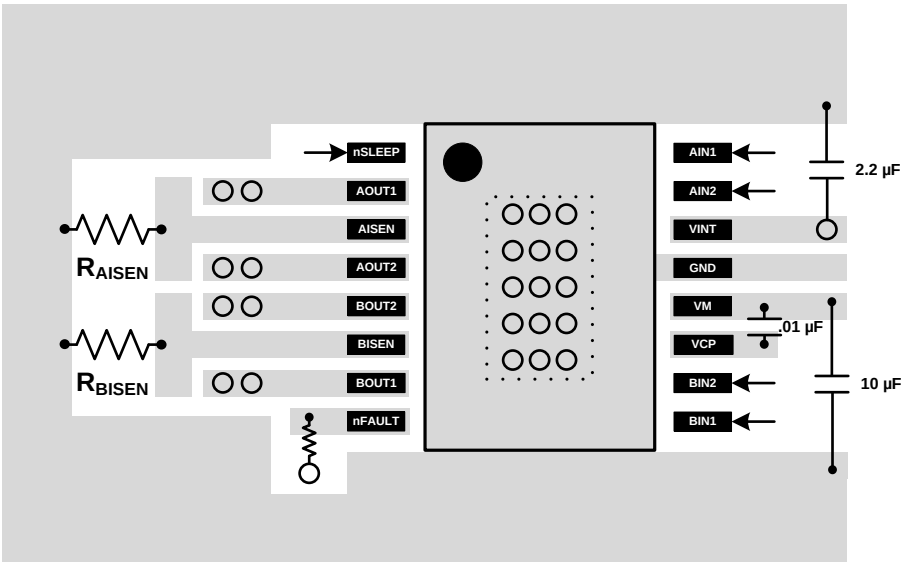


Figure 10. Recommended Layout Example

10.3 Thermal Considerations

10.3.1 Maximum Output Current

In actual operation, the maximum output current achievable with a motor driver is a function of die temperature. This, in turn, is greatly affected by ambient temperature and PCB design. Basically, the maximum motor current will be the amount of current that results in a power dissipation level that, along with the thermal resistance of the package and PCB, keeps the die at a low enough temperature to stay out of thermal shutdown.

The dissipation ratings given in the data sheet can be used as a guide to calculate the approximate maximum power dissipation that can be expected to be possible without entering thermal shutdown for several different PCB constructions. However, for accurate data, the actual PCB design must be analyzed through measurement or thermal simulation.

10.3.2 Thermal Protection

The DRV8833 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops by 45°C.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.4 Power Dissipation

Power dissipation in the DRV8833 is dominated by the DC power dissipated in the output FET resistance, or $R_{DS(ON)}$. There is additional power dissipated due to PWM switching losses, which are dependent on PWM frequency, rise and fall times, and VM supply voltages. These switching losses are typically on the order of 10% to 30% of the DC power dissipation.

The DC power dissipation of one H-bridge can be roughly estimated by Equation 3.

$$P_{TOT} = \left(HS - R_{DS(ON)} \times I_{OUT(RMS)}^{2}\right) + \left(LS - R_{DS(ON)} \times I_{OUT(RMS)}^{2}\right)$$

where

- P_{TOT} is the total power dissipation
- HS - $R_{DS(ON)}$ is the resistance of the high-side FET
- LS - $R_{DS(ON)}$ is the resistance of the low-side FET
- $I_{OUT(RMS)}$ is the RMS output current being applied to the motor (3)

$R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *PowerPAD™ Thermally Enhanced Package*, SLMA002
- *PowerPAD™ Made Easy*, SLMA004
- *Current Recirculation and Decay Modes*, SLVA321
- *Calculating Motor Driver Power Dissipation*, SLVA504
- *Understanding Motor Driver Current Ratings*, SLVA505

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8833PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	8833PW	Samples
DRV8833PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8833	Samples
DRV8833PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8833	Samples
DRV8833PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	8833PW	Samples
DRV8833RTYR	ACTIVE	QFN	RTY	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8833	Samples
DRV8833RTYT	ACTIVE	QFN	RTY	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8833	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

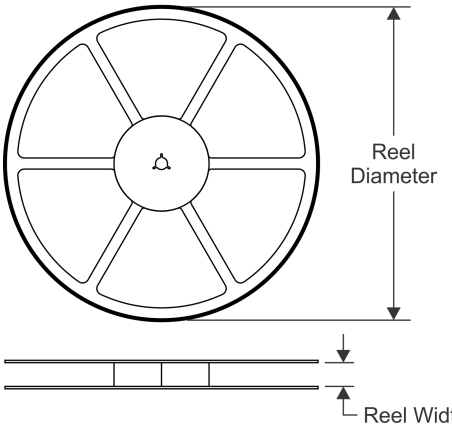
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

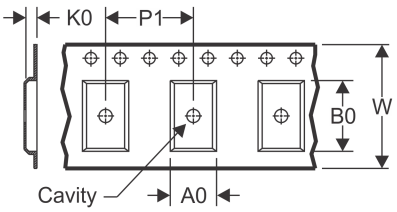
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

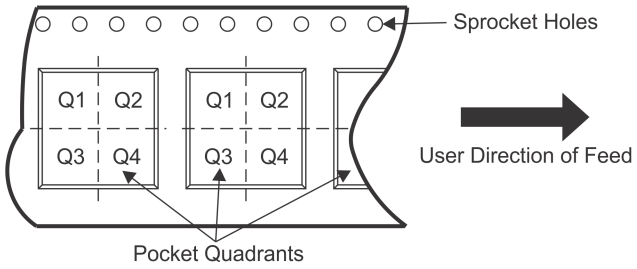


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

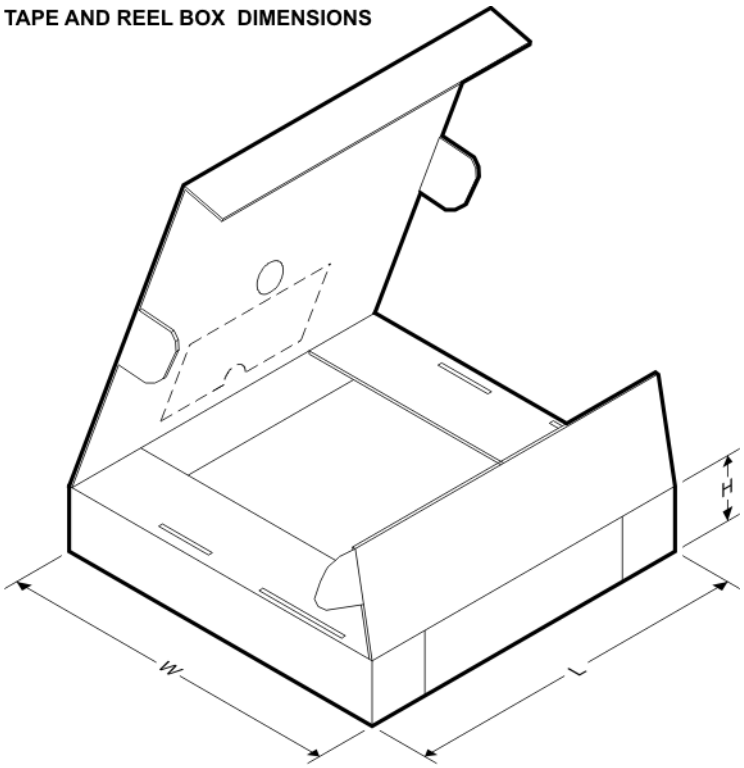
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8833PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV8833PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV8833RTYR	QFN	RTY	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV8833RTYT	QFN	RTY	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

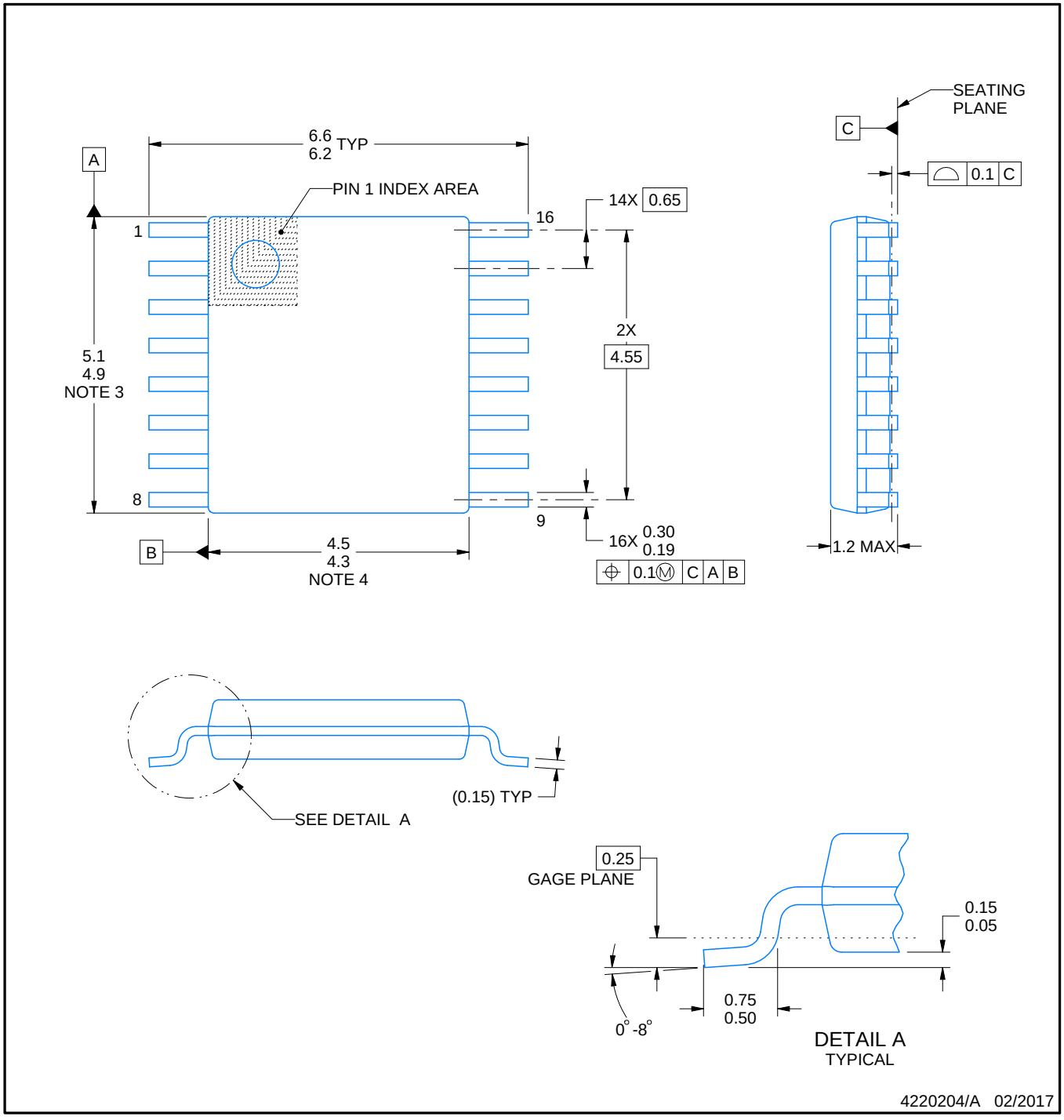
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8833PWPR	HTSSOP	PWP	16	2000	367.0	367.0	35.0
DRV8833PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
DRV8833RTYR	QFN	RTY	16	3000	367.0	367.0	35.0
DRV8833RTYT	QFN	RTY	16	250	210.0	185.0	35.0

PACKAGE OUTLINE

PW0016A

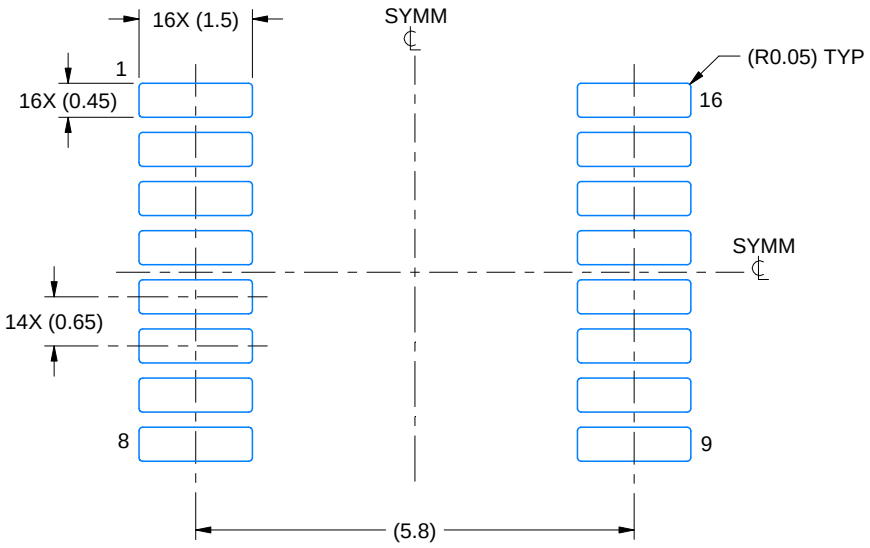
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

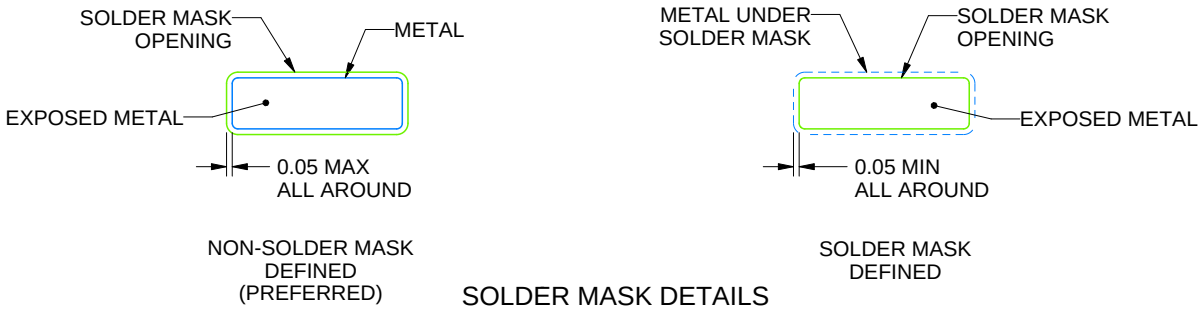


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

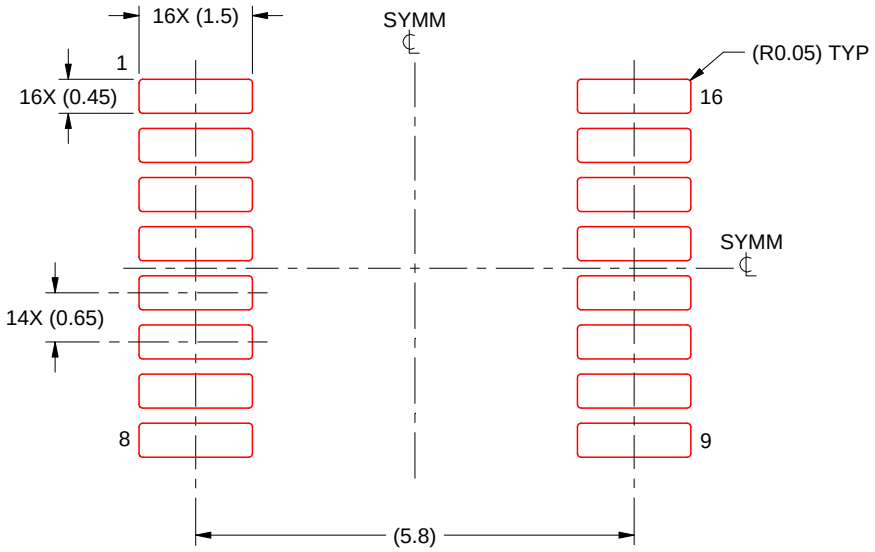


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

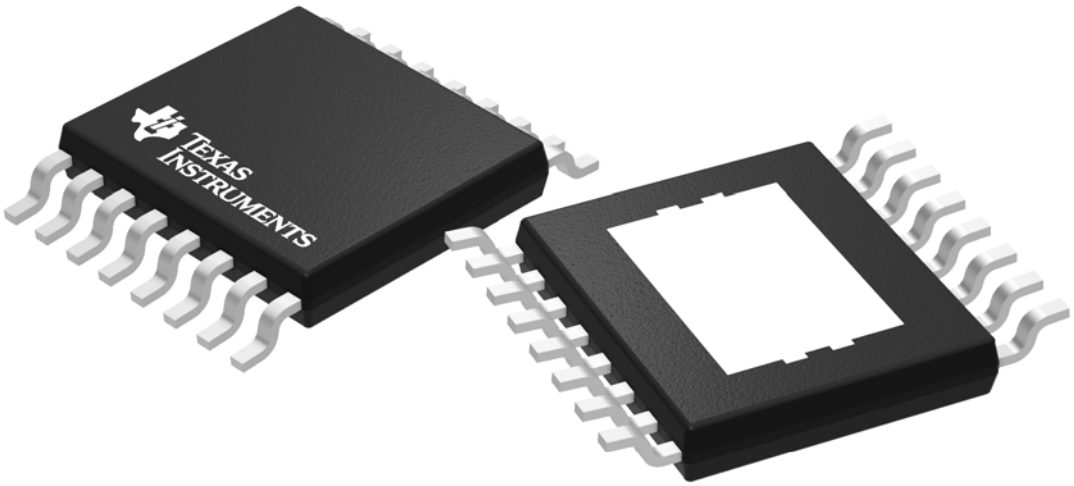
4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

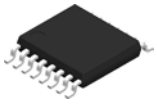
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

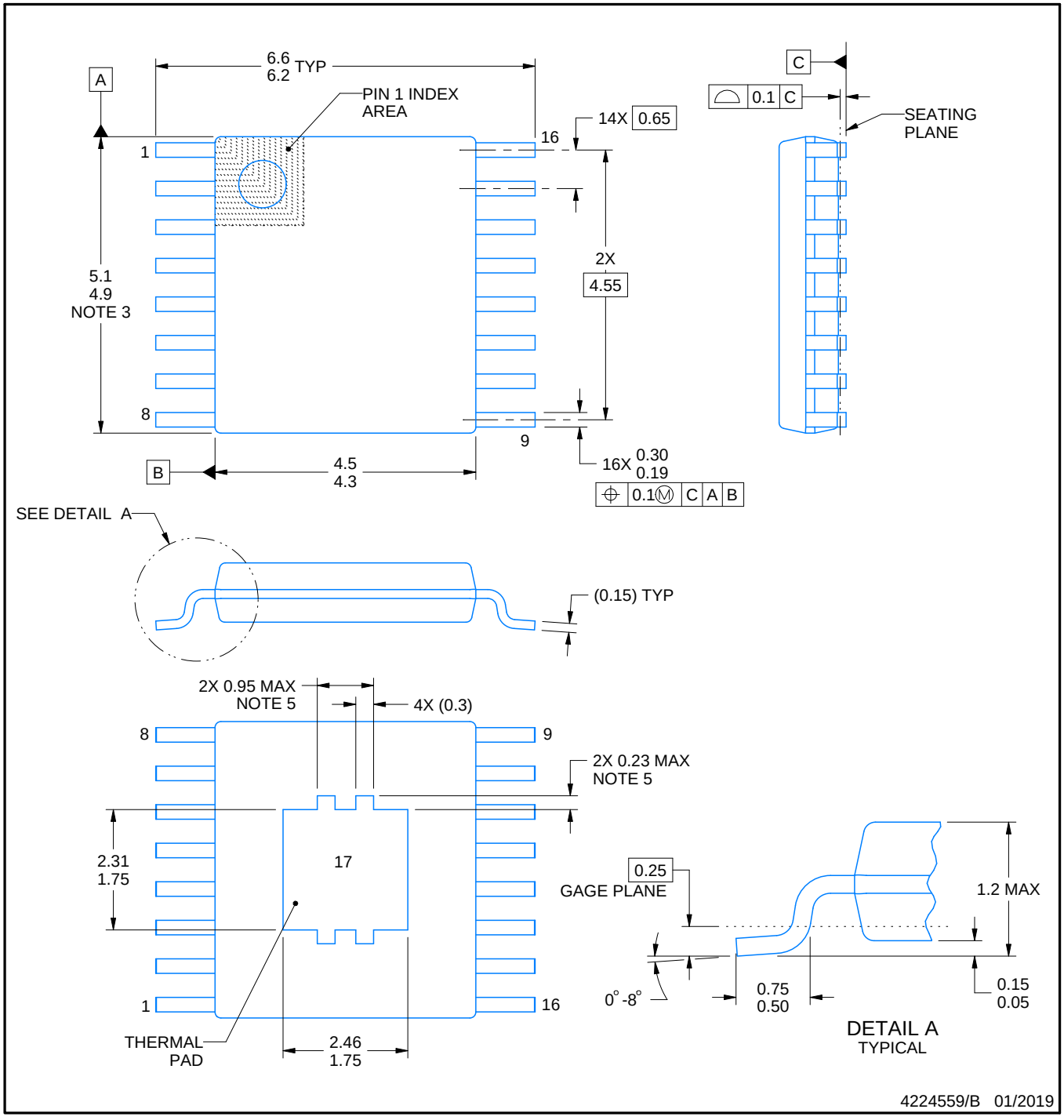
PACKAGE OUTLINE

PWP0016C



PowerPAD™ TSSOP - 1.2 mm max height

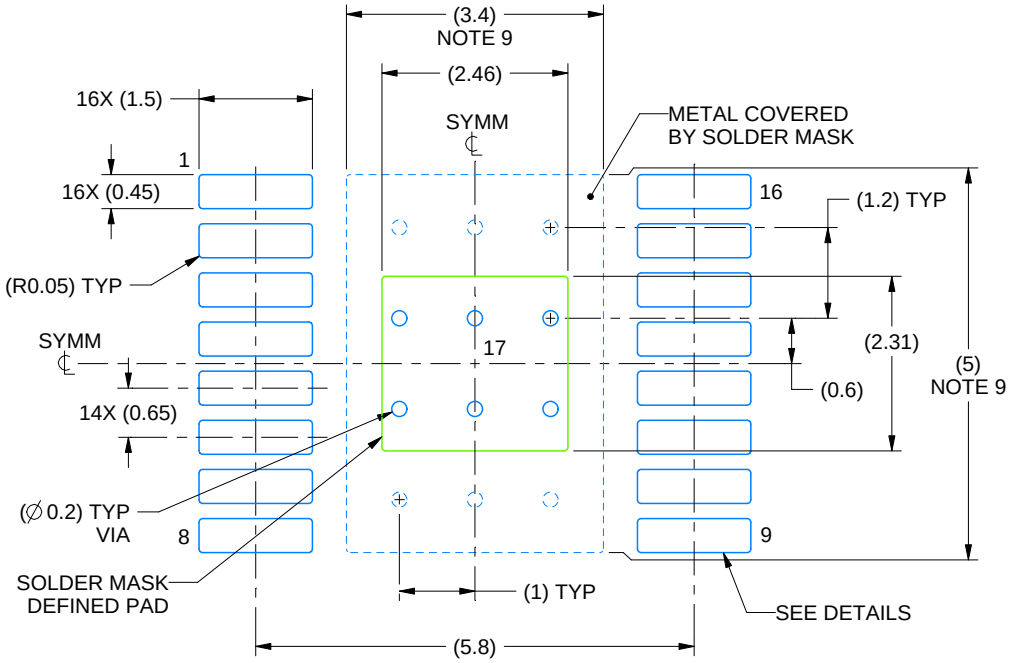
SMALL OUTLINE PACKAGE



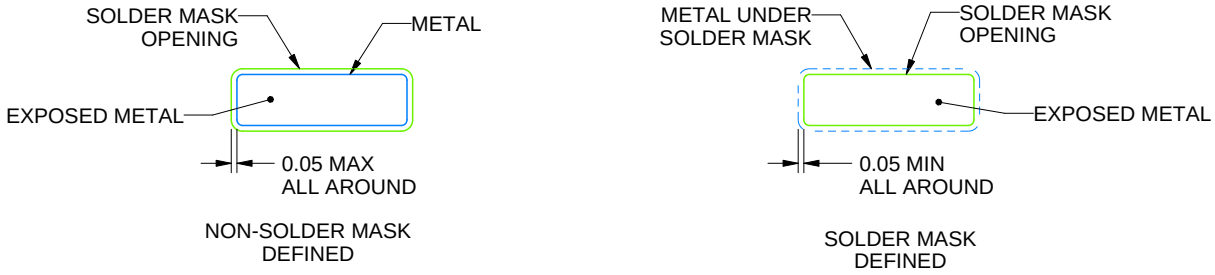
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

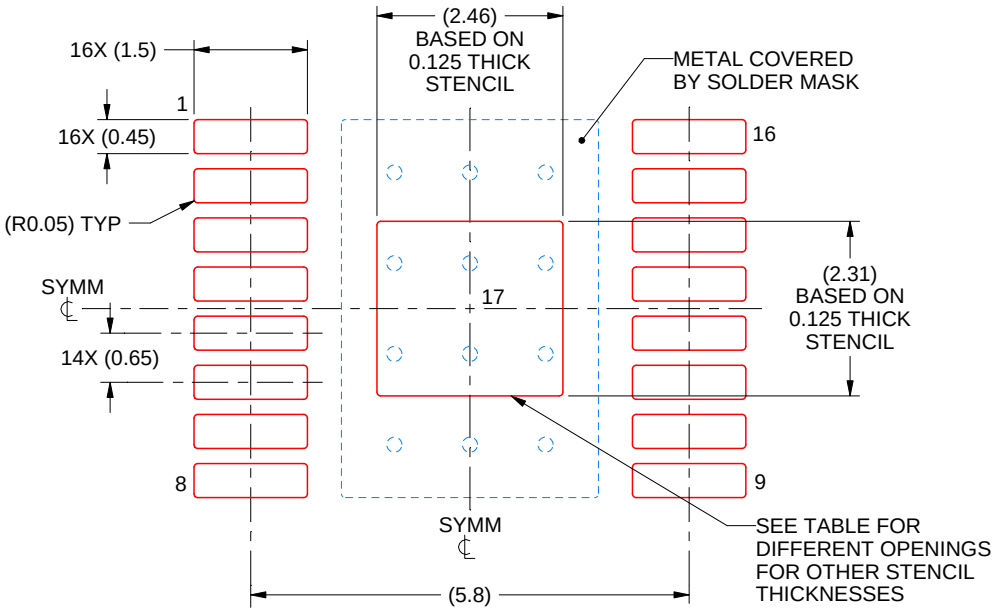


SOLDER MASK DETAILS

4224559/B 01/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

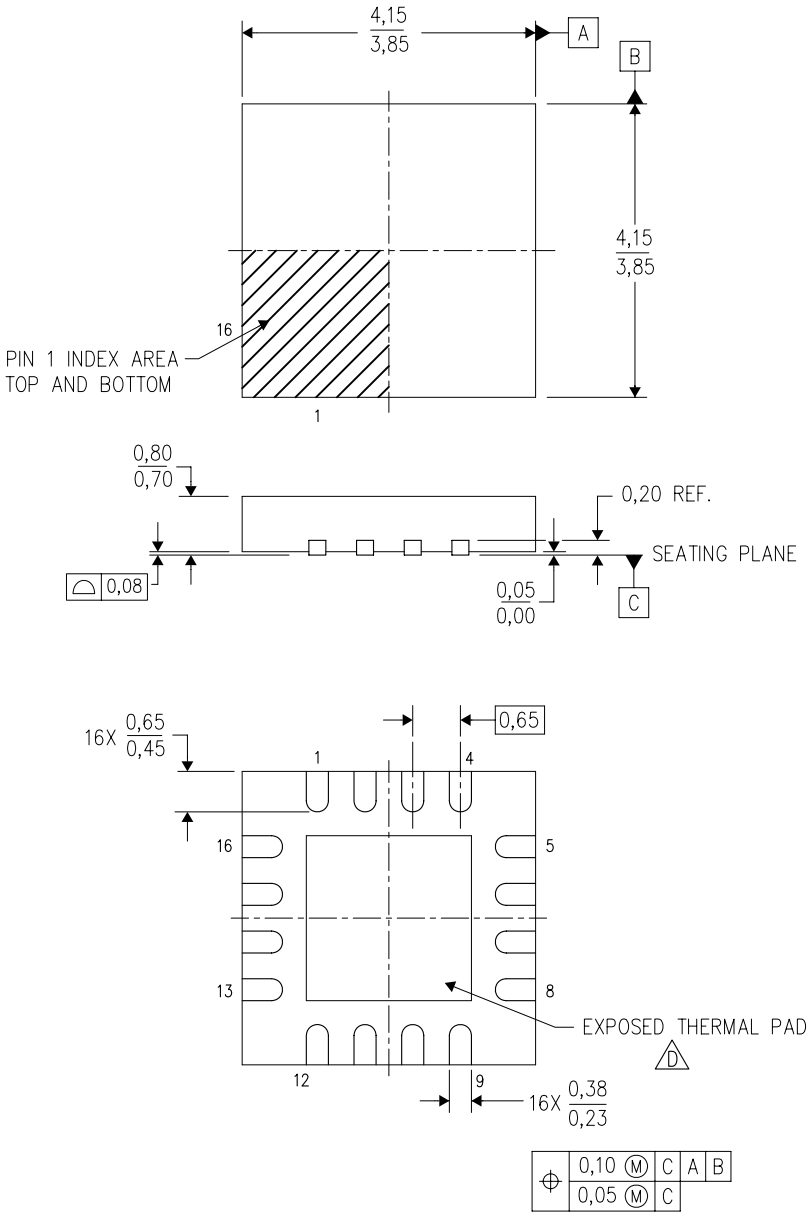
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 2.58
0.125	2.46 X 2.31 (SHOWN)
0.15	2.25 X 2.11
0.175	2.08 X 1.95

4224559/B 01/2019

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

RTY (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



4206276/B 03/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

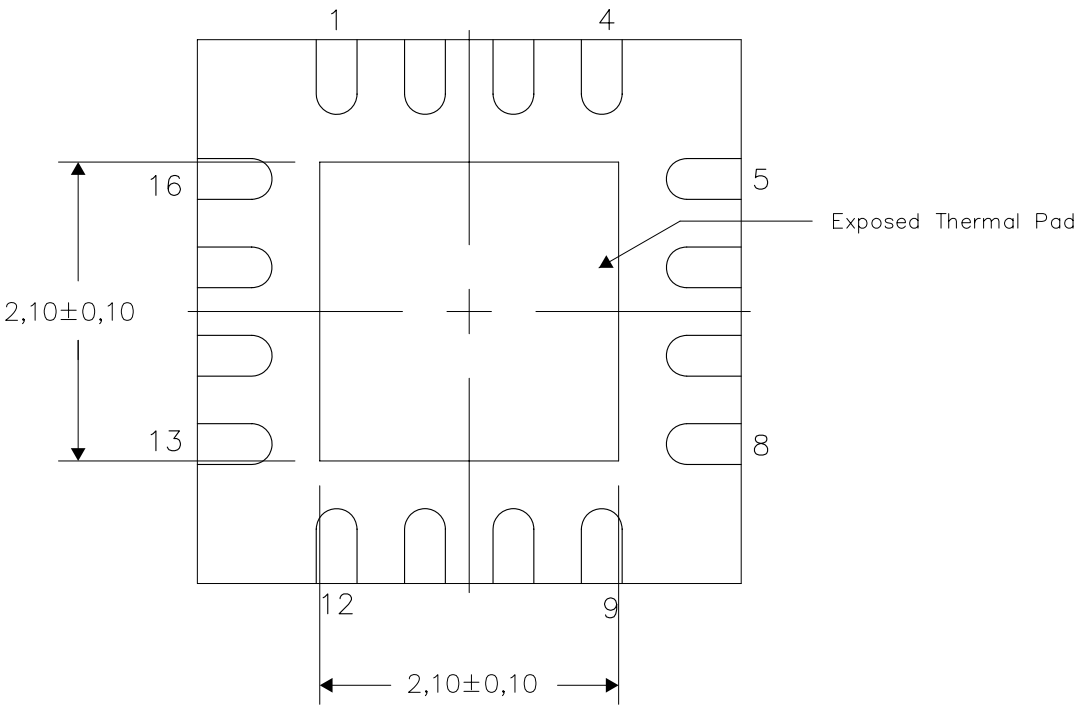
RTY (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



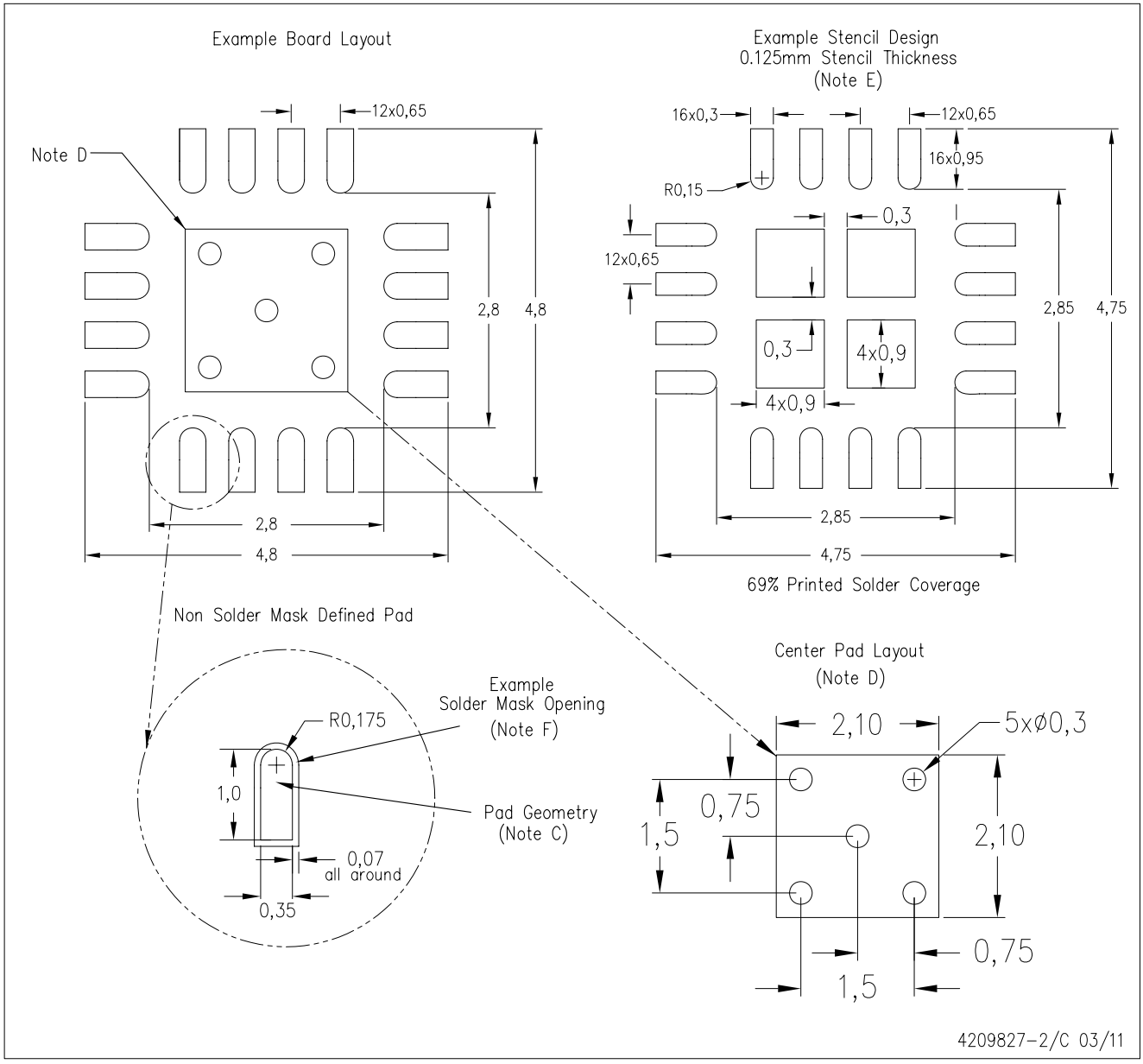
Bottom View

Exposed Thermal Pad Dimensions

4206277–2/E 03/11

NOTE: A. All linear dimensions are in millimeters

RTY (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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