



SANYO Semiconductors

## DATA SHEET

# LA6567H

Monolithic Linear IC  
 For MD and CD Player  
**Five-Channel Motor Driver**  
 (four BTL channels plus one H bridge channel)

## Overview

The LA6567H is a motor driver IC for MD and CD players with four BTL channels and one H bridge channel. The LA6567H features a separate power supply for the H bridge block, an output adjustment pin, and a 5V regulator to support a wide range of applications.

## Functions

- Power amplifier 4-channel (BTL) and 1-channel (H bridge) built-in.
- $I_O$  max 700mA (Each channel)
- Level shift circuit built-in (BTL AMP).
- Overheat protection circuit (thermal shutdown) built-in.
- With loading output voltage setting function
- 5V regulator built-in.

## Specifications

### Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}$ max		14	V
Allowable power dissipation	$P_d$ max	Mounted on a specified board*	2.0	W
Maximum output current	$I_O$ max	Each output for channel 1 to 5.	0.7	A
Maximum input voltage	$V_{INB}$		13	V
MUTE pin voltage	VMUTE		13	V
Operating temperature	$T_{opr}$		-30 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

\* Mounted on a specified board : 76.1×114.3×1.6mm<sup>3</sup>, glass epoxy board.

### Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}$		5.6 to 13	V

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**Electrical Characteristics** at  $T_a = 25^\circ\text{C}$ ,  $V_{CC1} = V_{CC2} = 8\text{V}$ ,  $V_{REF} = 1.65\text{V}$ , unless especially specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Overall Characteristics]						
No-load current drain ON	$I_{CC}$	All outputs ON, FWD = REV = 0V *1		30	50	mA
VREF input voltage range	VREF-IN		1		$V_{CC-1}$	V
[BTL Amplifier Block]						
Output offset voltage	VOFF	Voltage difference between outputs for BTL AMP, each channel.	-50		50	mV
Input voltage range	$V_{IN}$	Input voltage range	0		$V_{CC}$	V
Output voltage	$V_O$	Each voltage between $V_{O+}$ and $V_{O-}$ when $R_L = 8\Omega$ . *2	4	5		V
Closed-circuit voltage gain	VG	Input and output gain.	3.7	4	4.3	deg
Slew rate	SR	AMP Independent Multiply 2 between outputs. *3		0.5		V/ $\mu\text{s}$
[H Bridge Block]						
Output voltage	$V_{O-LOAD}$	$V_{CONT} = 8\text{V}$ *2	5.45	6		V
Input low level	$V_{IN-L}$				1	V
Input high level	$V_{IN-H}$		2			V
Output setting voltage	VCONT	$V_{CONT} = 8\text{V}$ *2	3.0	3.5	4.0	V
[Regulator Block] (PNP transistor : 2SB632K-use)						
Output voltage	Vreg	$I_L = 100\text{mA}$	4.75	5	5.25	V
Output load fluctuation	$\Delta V_{RL}$	$I_L = 0$ to $200\text{mA}$	-50	0	10	mV
Supply voltage fluctuation	$\Delta V_{V_{CC}}$	$V_{CC} = 6$ to $12\text{V}$ , $I_L = 100\text{mA}$	-15	21	60	mV

Note \*1 : Current dissipation that is a sum of  $V_{CC1}$  and  $V_{CC2}$  at no load.

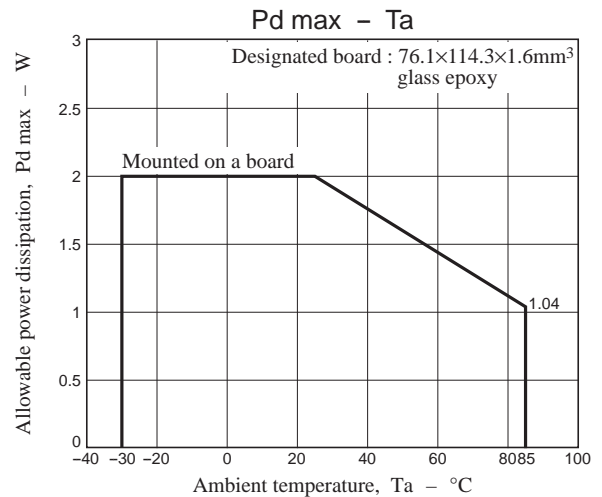
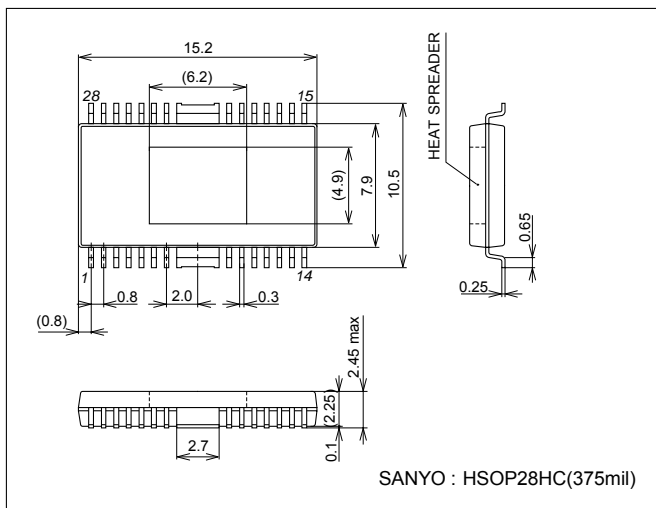
\*2 : Voltage difference between both ends of load ( $8\Omega$ ). Output saturated.

\*3 : Design guarantee value

## Package Dimensions

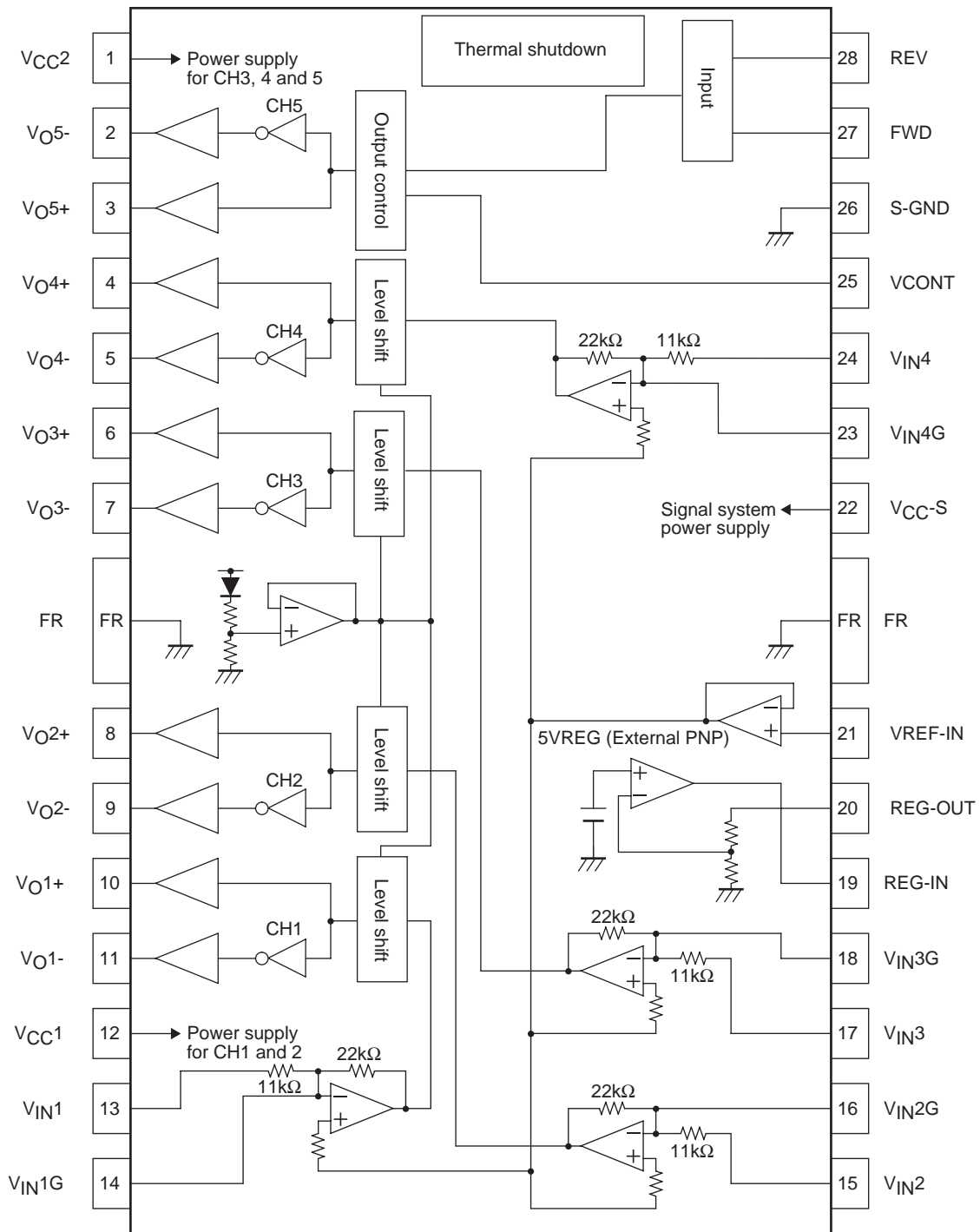
unit : mm (typ)

3234B



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## Block Diagram



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## Pin Functions

Pin No.	Symbol	Pin descriptions
1	V <sub>CC2</sub>	CH3, 4, and 5 power supplies (Used while being short-circuited to V <sub>CC1</sub> and V <sub>CC-S</sub> )
2	V <sub>O5-</sub>	Loading output (-)
3	V <sub>O5+</sub>	Loading output (+)
4	V <sub>O4+</sub>	Output pin (+) for channel 4
5	V <sub>O4-</sub>	Output pin (-) for channel 4
6	V <sub>O3+</sub>	Output pin (+) for channel 3
7	V <sub>O3-</sub>	Output pin (-) for channel 3
8	V <sub>O2+</sub>	Output pin (+) for channel 2
9	V <sub>O2-</sub>	Output pin (-) for channel 2
10	V <sub>O1+</sub>	Output pin (+) for channel 1
11	V <sub>O1-</sub>	Output pin (-) for channel 1
12	V <sub>CC1</sub>	CH1 and 2(BTL) power supplies (Used while being short-circuited to V <sub>CC-S</sub> and V <sub>CC2</sub> )
13	V <sub>IN1</sub>	Input pin for channel 1
14	V <sub>IN1G</sub>	Input pin for channel 1 (for gain adjustment)
15	V <sub>IN2</sub>	Input pin for channel
16	V <sub>IN2G</sub>	Input pin for channel 2 (for gain adjustment)
17	V <sub>IN3</sub>	Input pin for channel 3
18	V <sub>IN3G</sub>	Input pin for channel 3 (for gain adjustment)
19	REG-IN	Regulator pin (external PNP base)
20	REG-OUT	Regulator pin (external PNP collector)
21	VREF-IN	Reference voltage input pin
22	V <sub>CC-S</sub>	Signal system supply (Used while being short-circuited to V <sub>CC1</sub> and V <sub>CC2</sub> )
23	V <sub>IN4G</sub>	Input pin for channel 4 (for gain adjustment)
24	V <sub>IN4</sub>	Input pin for channel 4
25	VCONT	5CH (VLO) output voltage setting pin
26	S-GND	Signal system GND
27	FWD	5CH(VLO) Output change pin (FWD), logic input for loading block.
28	REV	5CH(VLO) Output change pin (REV), logic input for loading block.

Note : • Center frame (FR) becomes GND for the power system (P-GND). Set this to the minimum potential together with S-GND.

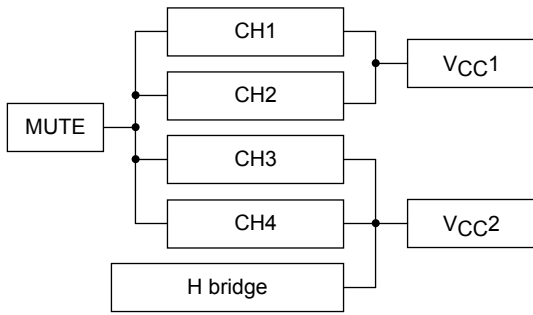
- Short-circuit power system pins, V<sub>CC-S</sub>, V<sub>CC1</sub>, and V<sub>CC2</sub> externally for use.

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## Pin Description

Pin No.	Symbol	Pin function	Description	Equivalent circuit
13 14 15 16 17 18 23 24	$V_{IN}$ $V_{ING}$	Input	Each input pin	
4 5 6 7 8 9 10 11	$V_O$	Output	Each output	
2 3 25	$V_{O5+}$ $V_{O5-}$ $V_{CONT}$	$V_{O5}$ Output set for loading block	H bridge output Output setting voltage pin	
27 28	FWD	FWD	H bridge input	

Relation of MUTE and Power (V<sub>CC</sub>\*)



\* Connect V<sub>CC</sub>1 and V<sub>CC</sub>2 externally.

H bridge block

FWD	REV	V <sub>O</sub> 5+	V <sub>O</sub> 5-	Mode
L	L	OFF	OFF	Open *1
L	H	H	L	Forward
H	L	L	H	Reversed
H	H	L	L	Break *2

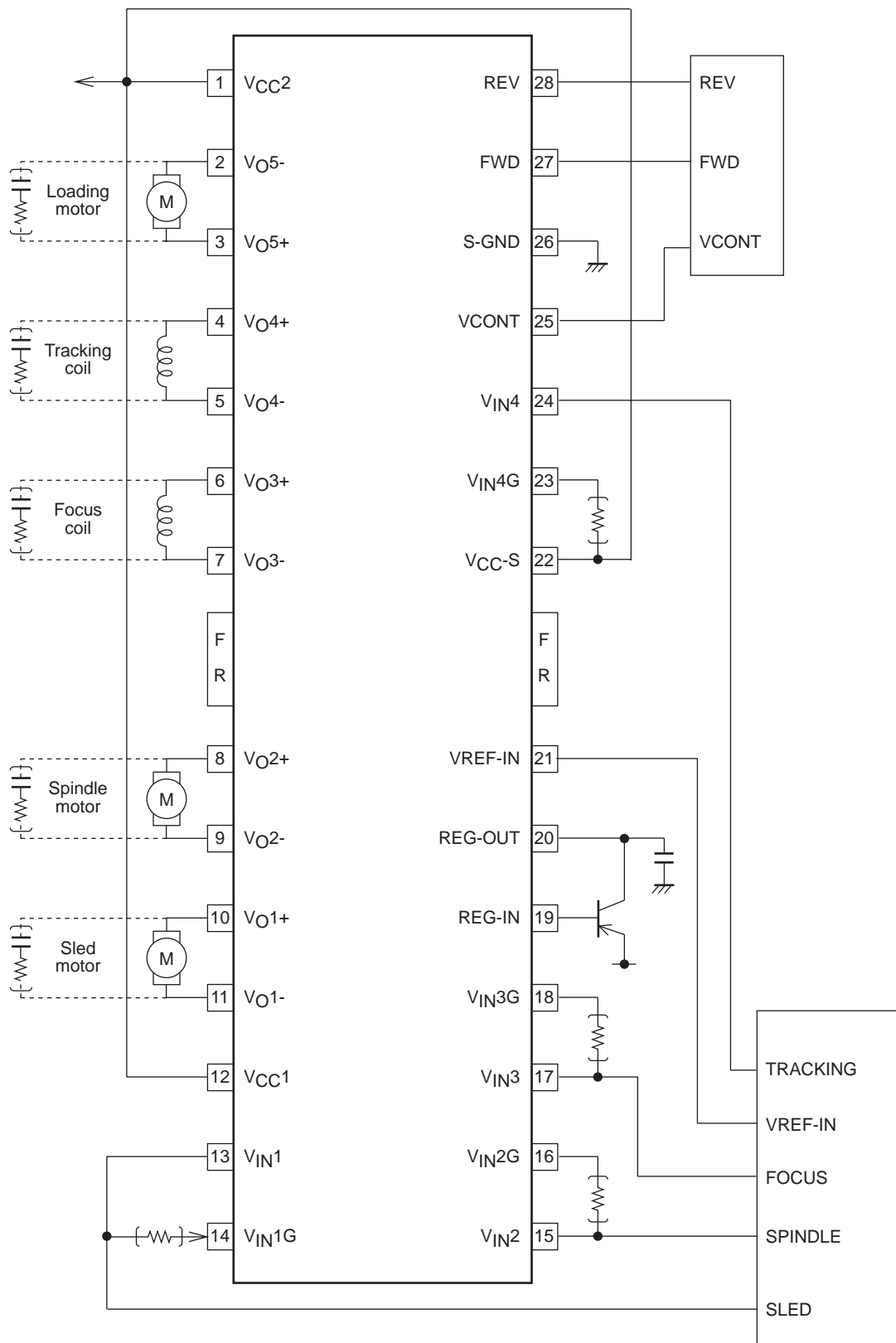
Note \*1 : The output has a high Impedance.

\*2 : At brake, the SINK side transistor is ON (short brake).

V<sub>LO</sub>+ and V<sub>LO</sub>- are approximately on the GND level.

\*3 : V<sub>CONT</sub> (output setting voltage pin) and V<sub>LO</sub> can be related as V<sub>LO</sub> = V<sub>CONT</sub>-1V (typ).

Sample Application Circuit



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