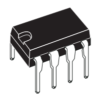
TS512, TS512A

Precision dual operational amplifier

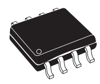
Datasheet — production data

Features

- Low input offset voltage: 500 µV max. (A version)
- Low power consumption
- Short-circuit protection
- Low distortion, low noise
- High gain bandwidth product: 3 MHz
- High channel separation
- ESD protection 2 kV
- Macromodel included in this specification

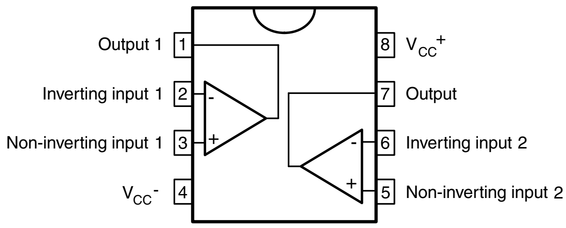


N
DIP8
(plastic package)



D
SO-8
(plastic micropackage)

Pin connections
(top view)



Description

The TS512 device is a high-performance dual operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation in voltage follower configurations, in spite of its high gain bandwidth product.

The circuit presents very stable electrical characteristics over the entire supply voltage range and it is particularly intended for professional and telecom applications (such as active filtering).

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	±18	V
V_{in}	Input voltage	$\pm V_{CC}$	
V_{id}	Differential input voltage	$\pm(V_{CC} - 1)$	
R_{thja}	Thermal resistance junction-to-ambient(1) DIP8 SO-8	 85 125	°C/W
R_{thjc}	Thermal resistance junction-to-case(1) DIP8 SO-8	 41 40	°C/W
T_j	Junction temperature	+ 150	°C
T_{stg}	Storage temperature range	-65 to +150	°C
ESD	HBM: human body model(2)	2	kV
	MM: machine model(3)	200	V
	CDM: charged device model(4)	1.5	kV

1. Short-circuits can cause excessive heating and destructive dissipation. R_{th} are typical values.
2. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
3. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
4. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to ground through only one pin. This is done for all pins.

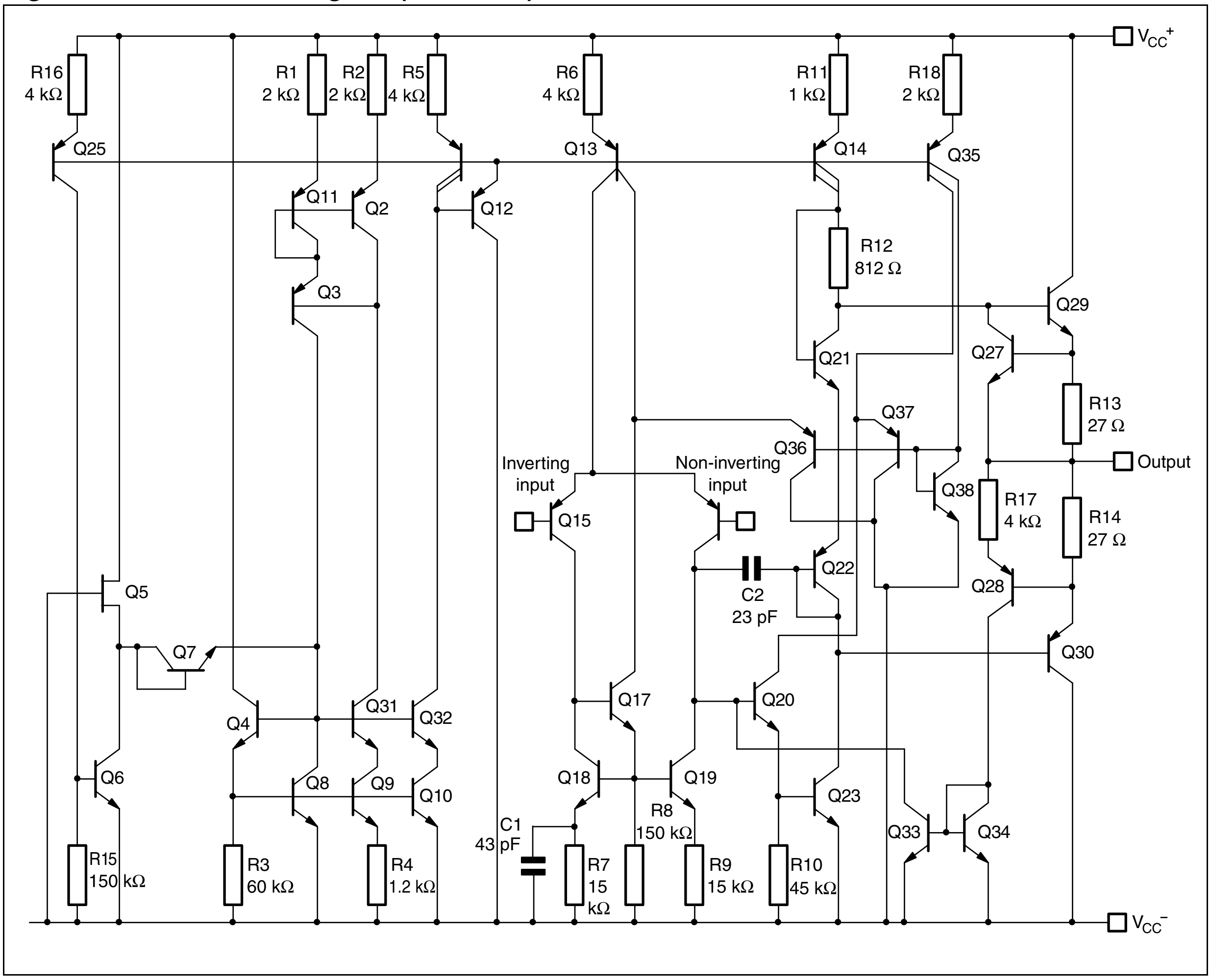
Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	6 to 30V	V
V_{icm}	Common mode input voltage range	V_{CC-}+1.5 to V_{CC+}-1.5	V
T_{oper}	Operating free air temperature range	-40 to +125	°C

1. Value with respect to V_{CC-} pin.

2 Schematic diagram

Figure 1. Schematic diagram (1/2 TS512)



3 Electrical characteristics

Table 3. $V_{CC} = \pm 15$ V, $T_{amb} = 25$ °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current (per operator) $T_{min} \leq T_{amb} \leq T_{max}$		0.5	0.6 0.75	mA
I_{ib}	Input bias current $T_{min} \leq T_{amb} \leq T_{max}$		50	150 300	nA
R_{in}	Input resistance, f = 1 kHz		1		MΩ
V_{io}	Input offset voltage TS512 TS512A $T_{min} \leq T_{amb} \leq T_{max}$ TS512 TS512A		0.5	2.5 0.5 3.5 1.5	mV
ΔV_{io}	Input offset voltage drift $T_{min} \leq T_{amb} \leq T_{max}$		2		µV/°C
I_{io}	Input offset current $T_{min} \leq T_{amb} \leq T_{max}$		5	20 40	nA
ΔI_{io}	Input offset current drift $T_{min} \leq T_{amb} \leq T_{max}$		0.08		$\frac{nA}{°C}$
I_{os}	Output short-circuit current		23		mA
A_{vd}	Large signal voltage gain $R_L = 2$ kΩ, $V_{CC} = \pm 15$ V, $T_{min} \leq T_{amb} \leq T_{max}$ $V_{CC} = \pm 4$ V	90	100 95		dB
GBP	Gain bandwidth product, f = 100 kHz	1.8	3		MHz
e_n	Equivalent input noise voltage, f = 1 kHz Rs = 50 Ω Rs = 1 kΩ Rs = 10 kΩ		8 10 18		$\frac{nV}{\sqrt{Hz}}$
THD	Total harmonic distortion $A_v = 20$ dB, $R_L = 2$ kΩ $V_o = 2\ V_{pp}$, f = 1 kHz		0.03		%
$\pm V_{opp}$	Output voltage swing $R_L = 2$ kΩ, $V_{CC} = \pm 15$ V, $T_{min} \leq T_{amb} \leq T_{max}$ $V_{CC} = \pm 4$ V	±13	 ±3		V
V_{opp}	Large signal voltage swing $R_L = 10$ kΩ, f = 10 kHz		28		V_{pp}
SR	Slew rate Unity gain, $R_L = 2$ kΩ	0.8	1.5		V/µs
CMR	Common mode rejection ratio CMR = 20 log ($\Delta V_{ic}/\Delta V_{io}$) ($V_{ic} = -10$ V to 10 V, $V_{out} = V_{CC}/2$, $R_L > 1$ MΩ)	90			dB

Table 3. V_{CC} = ±15 V, T_{amb} = 25 °C (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$) ($V_{CC}$ = ±4 V to ±15 V, $V_{out} = V_{icm} = V_{CC}/2$)	90			dB
V_{o1}/V_{o2}	Channel separation, f = 1 kHz		120		dB

Figure 2. V_{io} distribution at V_{CC} = ±15 V and T = 25 °C

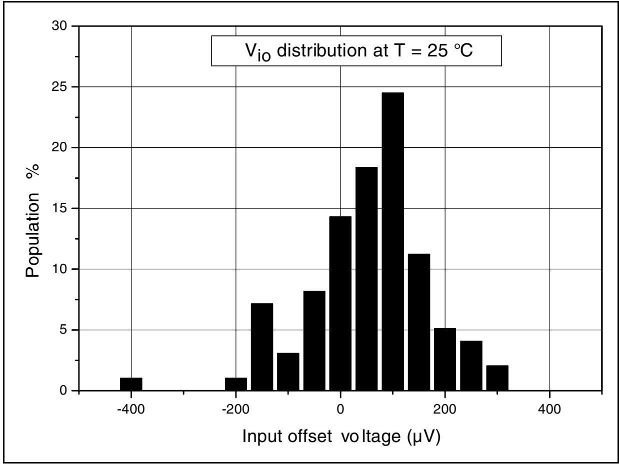


Figure 3. V_{io} distribution at V_{CC} = ±15 V and T = 125 °C

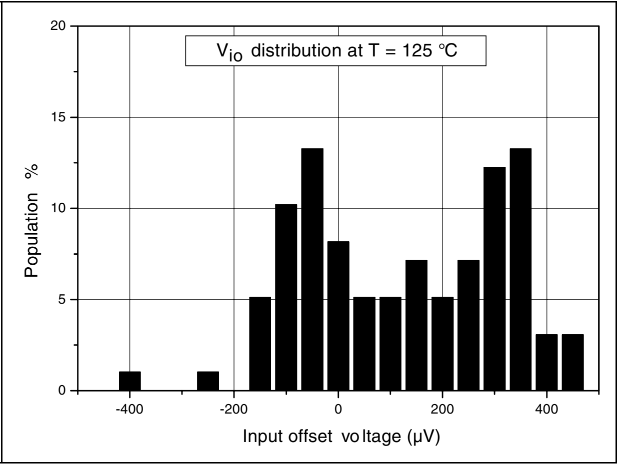


Figure 4. Input offset voltage vs. input common mode voltage at V_{CC} =10 V

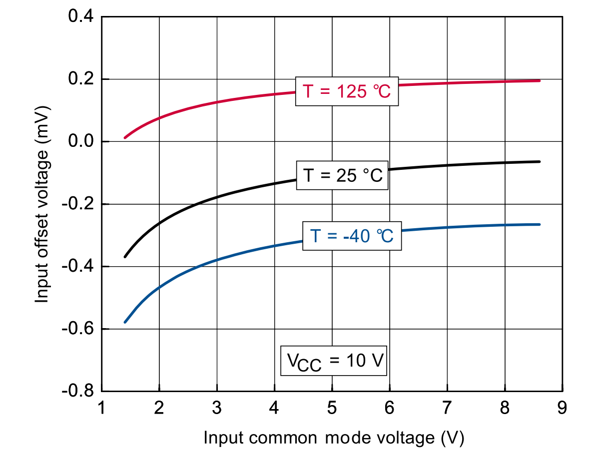


Figure 5. Input offset voltage vs. input common mode voltage at V_{CC} = 30 V

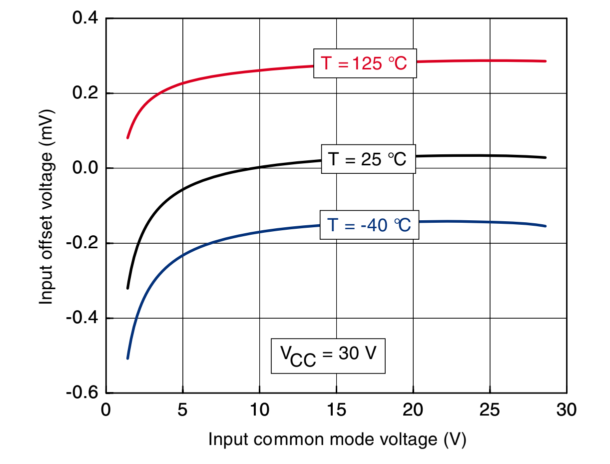


Figure 6. Supply current (per operator) vs. supply voltage at V_{icm} = V_{CC}/2

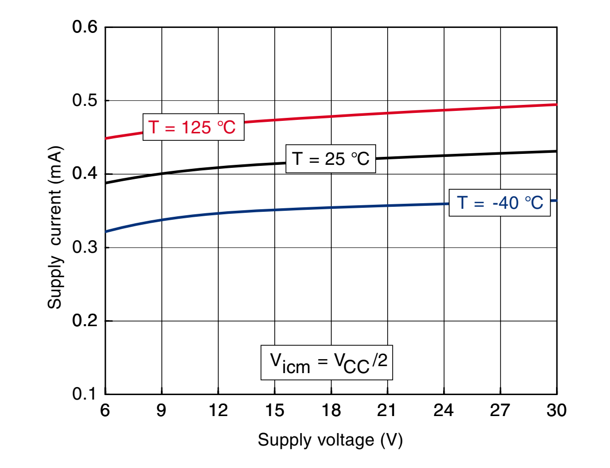


Figure 7. Supply current (per operator) vs. input common mode voltage at V_{CC} = 6 V

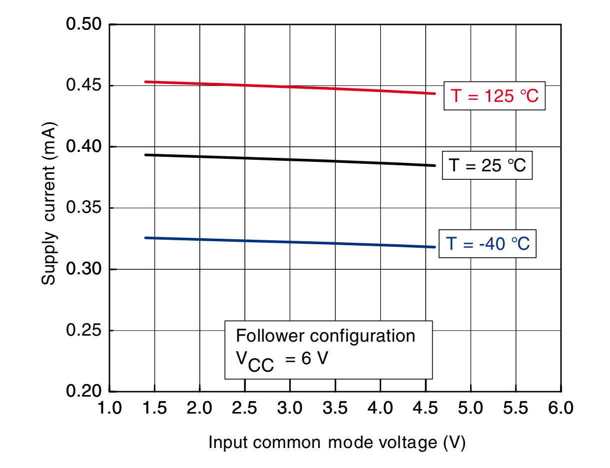


Figure 8. Supply current (per operator) vs. input common mode voltage at V_{CC} = 10 V

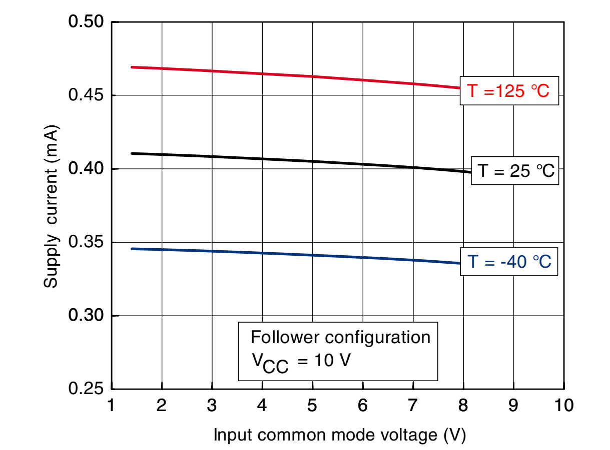


Figure 9. Supply current (per operator) vs. input common mode voltage at V_{CC} = 30 V

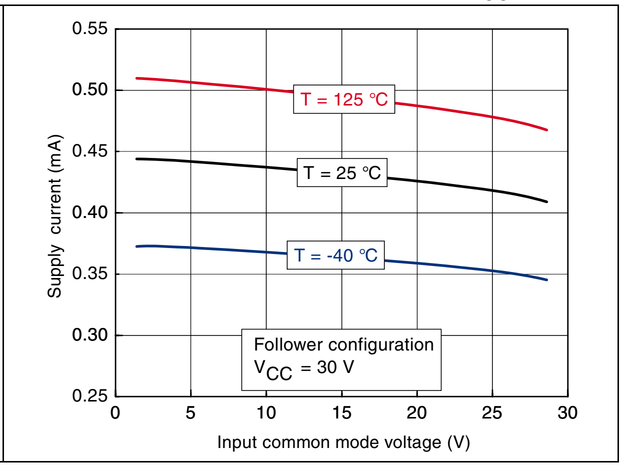


Figure 10. Output current vs. supply voltage at V_{icm} = V_{CC}/2

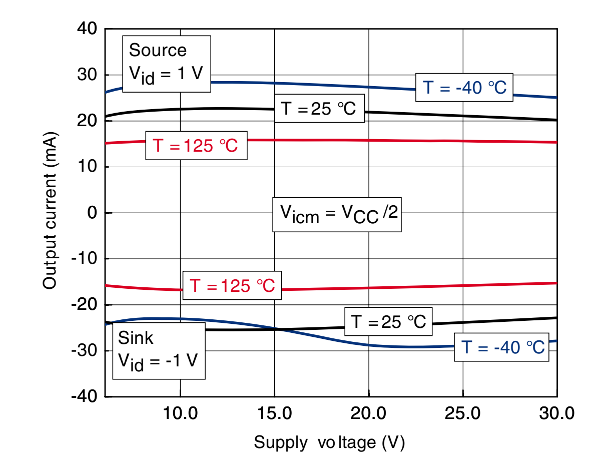


Figure 11. Output current vs. output voltage at V_{CC} = 5 V

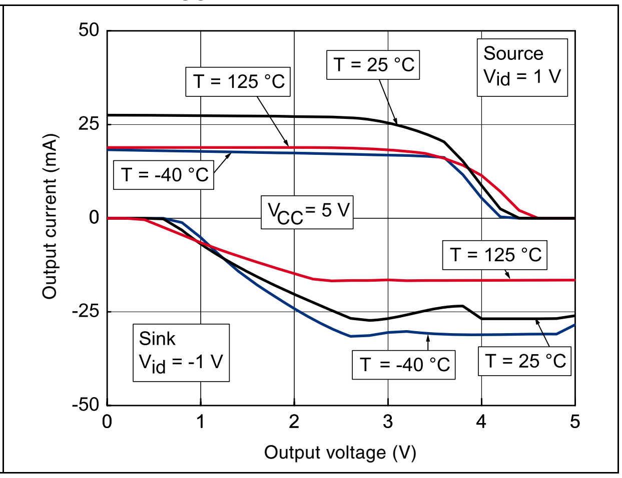


Figure 12. Output current vs. output voltage at V_{CC} = 30 V

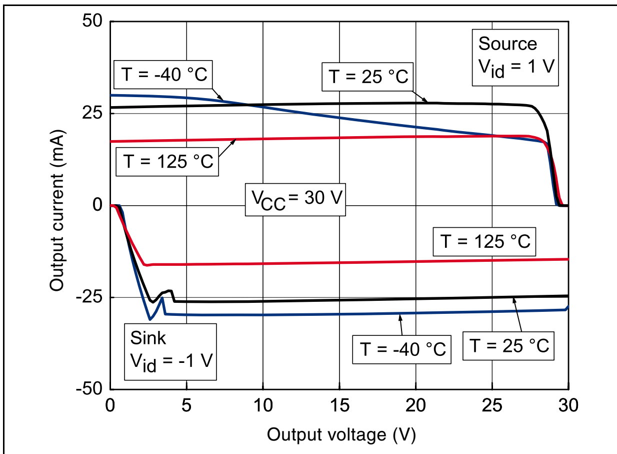


Figure 13. Voltage gain and phase for different capacitive loads at V_{CC} = 6 V, V_{icm} = 3 V and T = 25 °C

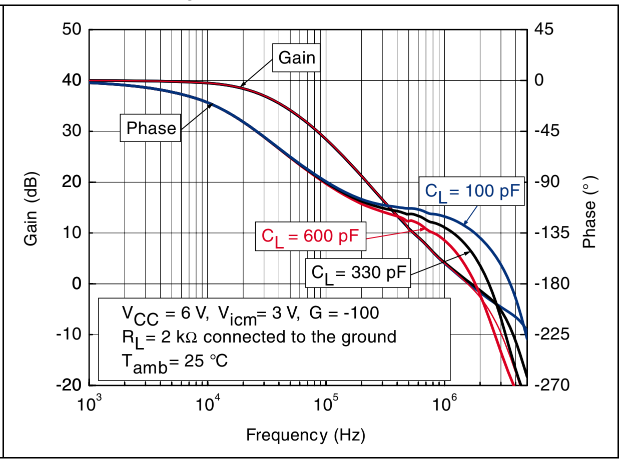


Figure 14. Voltage gain and phase for different capacitive loads at V_{CC} = 10 V, V_{icm} = 5 V and T = 25 °C

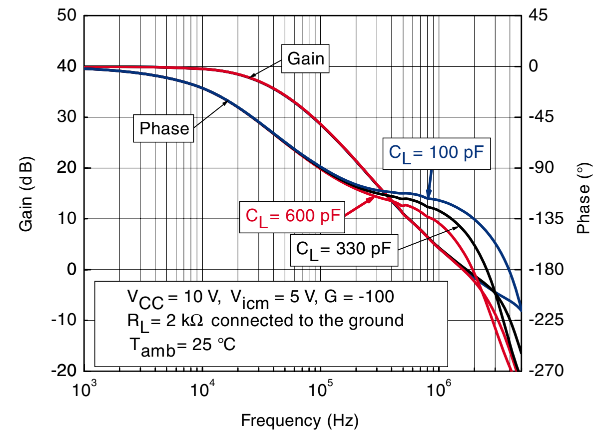


Figure 15. Voltage gain and phase for different capacitive loads at V_{CC} = 30 V, V_{icm} = 15 V and T = 25 °C

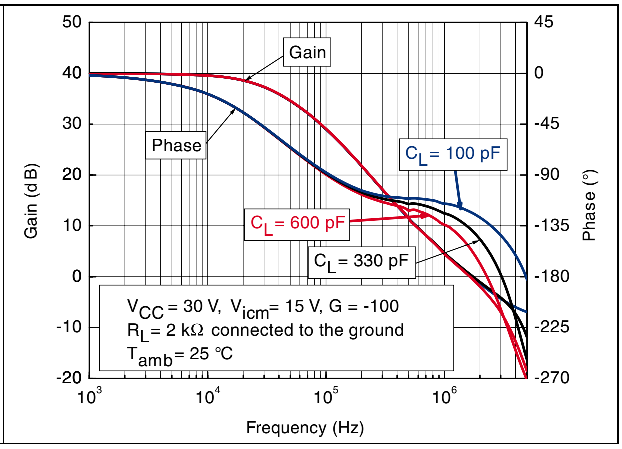


Figure 16. Frequency response for different capacitive loads at V_{CC} = 6 V, V_{icm} = 3 V and T = 25 °C

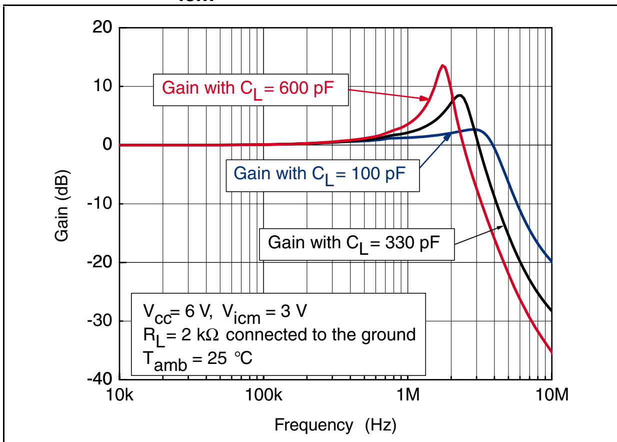


Figure 17. Frequency response for different capacitive loads at V_{CC} = 10 V, V_{icm} = 5 V and T = 25 °C

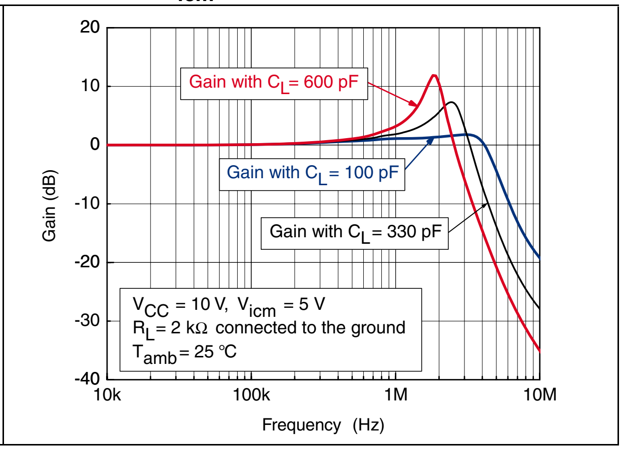


Figure 18. Frequency response for different capacitive loads at V_{CC} = 30 V, V_{icm} = 15 V and T = 25 °C

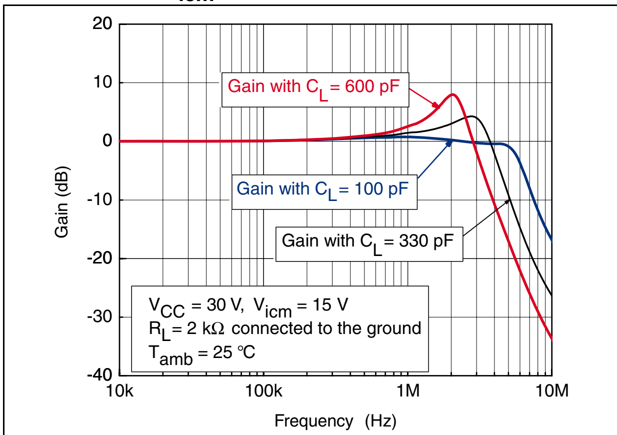


Figure 19. Phase margin vs. output current, at V_{CC} = 6 V, V_{icm} = 3 V and T = 25 °C

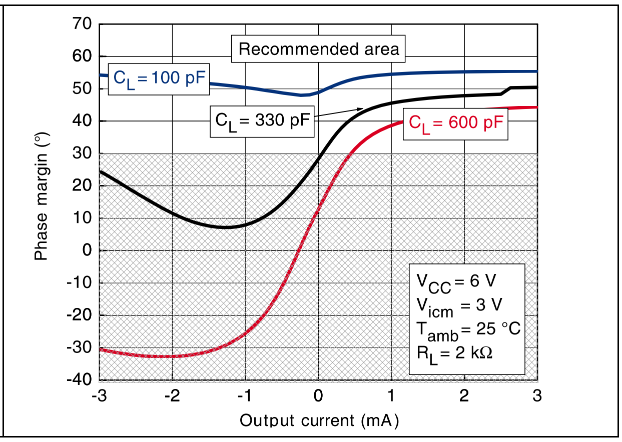


Figure 20. Phase margin vs. output current, at V_{CC} = 10 V, V_{icm} = 5 V and T = 25 °C

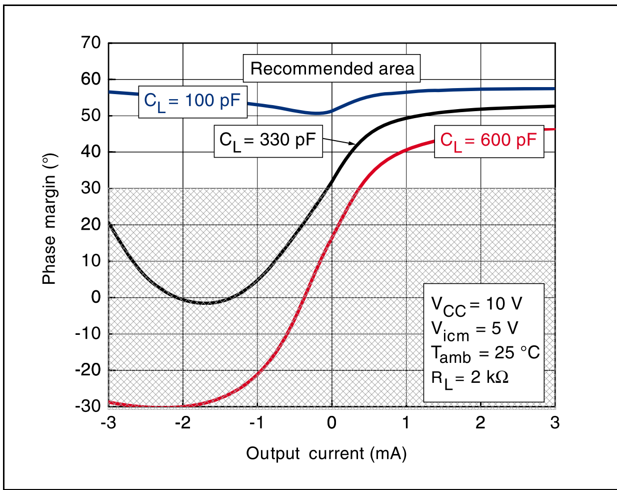
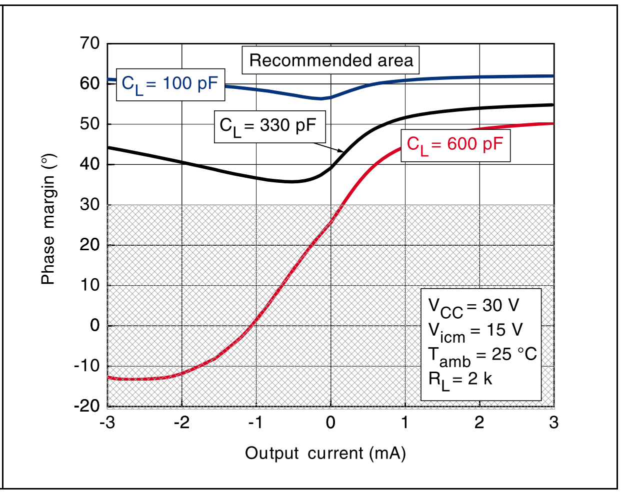


Figure 21. Phase margin vs. output current, at V_{CC} = 30 V, V_{icm} = 15 V and T = 25 °C



4 Macromodel

4.1 Important notes concerning this macromodel

- All models are a trade-off between accuracy and complexity (i.e. simulation time).
- Macromodels are not a substitute to breadboarding; rather, they confirm the validity of a design approach and help to select surrounding component values.
- A macromodel emulates the **nominal** performance of a **typical** device within **specified operating conditions** (temperature, supply voltage, for example). Thus the macromodel is often not as exhaustive as the datasheet, its purpose is to illustrate the main parameters of the product.

Data derived from macromodels used outside of the specified conditions (V_{CC}, temperature, for example) or even worse, outside of the device operating conditions (V_{CC}, V_{icm}, for example), is not reliable in any way.

4.2 Macromodel code

```
** Standard Linear Ics Macromodels, 1993.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY

.SUBCKT TS512 1 3 2 4 5
********************************************************
.MODEL MDTH D IS=1E-8 KF=6.565195E-17 CJO=10F
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 2.600000E+01
RIN 15 16 2.600000E+01
RIS 11 15 1.061852E+02
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0
VOFN 13 14 DC 0
IPOL 13 5 1.000000E-05
CPS 11 15 12.47E-10
DINN 17 13 MDTH 400E-12
VIN 17 5 1.500000e+00
DINR 15 18 MDTH 400E-12
```

```
VIP 4 18 1.500000E+00
FCP 4 5 VOFP 3.400000E+01
FCN 5 4 VOFN 3.400000E+01
FIBP 2 5 VOFN 1.000000E-02
FIBN 5 1 VOFP 1.000000E-02
* AMPLIFYING STAGE
FIP 5 19 VOFP 9.000000E+02
FIN 5 19 VOFN 9.000000E+02
RG1 19 5 1.727221E+06
RG2 19 4 1.727221E+06
CC 19 5 6.000000E-09
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 6.521739E+03
VIPM 28 4 1.500000E+02
HONM 21 27 VOUT 6.521739E+03
VINM 5 27 1.500000E+02
GCOMP 5 4 4 5 6.485084E-04
RPM1 5 80 1E+06
RPM2 4 80 1E+06
GAVPH 5 82 19 80 2.59E-03
RAVPHGH 82 4 771
RAVPHGB 82 5 771
RAVPHDH 82 83 1000
RAVPHDB 82 84 1000
CAVPHH 4 83 0.331E-09
CAVPHB 5 84 0.331E-09
EOUT 26 23 82 5 1
VOUT 23 5 0
ROUT 26 3 6.498455E+01
COUT 3 5 1.000000E-12
DOP 19 25 MDTH 400E-12
VOP 4 25 1.742230E+00
DON 24 19 MDTH 400E-12
VON 24 5 1.742230E+00
.ENDS
```

Table 4. $V_{CC} = \pm 15$ V, $T_{amb} = 25$ °C (unless otherwise specified)

Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	$R_L = 2$ kΩ	100	V/mV
I_{CC}	No load, per operator	350	µA
V_{icm}		-13.4 to 14	V
V_{OH}	$R_L = 2$ kΩ	+14	V
V_{OL}	$R_L = 2$ kΩ	-14	V
I_{sink}	$V_o = 0$ V	27.5	mA
I_{source}	$V_o = 0$ V	27.5	mA
GBP	$R_L = 2$ kΩ, $C_L = 100$ pF	2.5	MHz
SR	$R_L = 2$ kΩ	1.4	V/µs
∅m	$R_L = 2$ kΩ, $C_L = 100$ pF	55	Degrees

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 22. DIP8 package outline

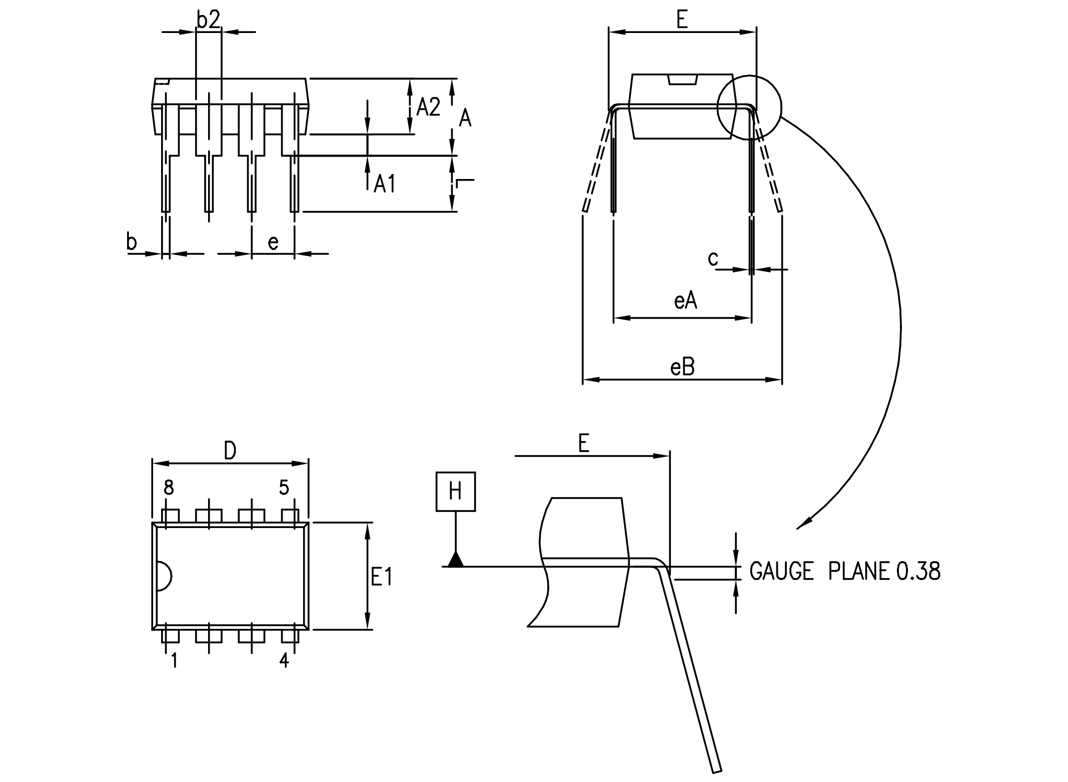


Table 5. DIP8 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
e		2.54			0.100	
eA		7.62			0.300	
eB			10.92			0.430
L	2.92	3.30	3.81	0.115	0.130	0.150

Figure 23. SO-8 package outline

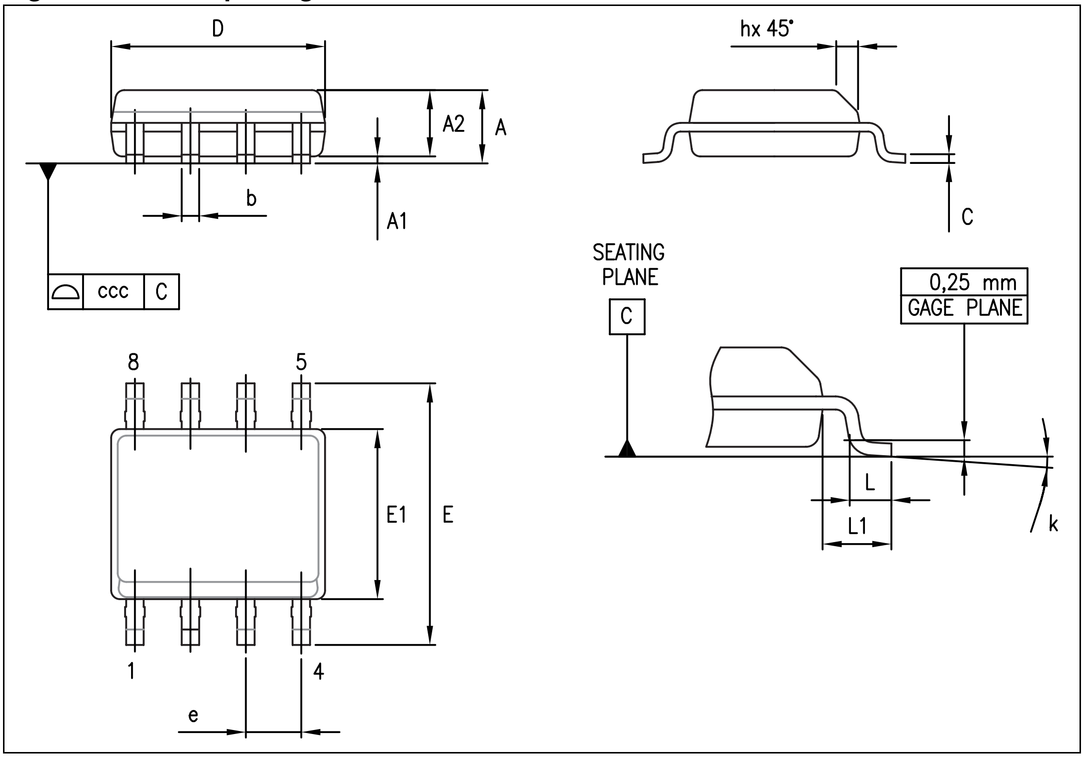


Table 6. SO-8 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0		8°	1°		8°
ccc			0.10			0.004

6 Ordering information

Table 7. Order codes

<table>
<tr><th>Order code</th><th>Temperature range</th><th>Package</th><th>Packaging</th><th>Marking</th></tr>
<tr><td>TS512IN</td><td rowspan="6">-40 °C, + 125 °C</td><td rowspan="2">DIP8</td><td rowspan="2">Tube</td><td>512IN</td></tr>
<tr><td>TS512AIN</td><td>512AIN</td></tr>
<tr><td>TS512ID
TS512IDT</td><td rowspan="2">SO-8</td><td rowspan="2">Tube or
tape and reel</td><td>512I</td></tr>
<tr><td>TS512AID
TS512AIDT</td><td>512AI</td></tr>
<tr><td>TS512IYDT(1)</td><td rowspan="2">SO-8
(automotive grade)</td><td>Tube or
tape and reel</td><td>512IY</td></tr>
<tr><td>TS512AIYDT(1)</td><td>Tape and reel</td><td>512AIY</td></tr>
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1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q 002 or equivalent are ongoing.

7 Revision history

Table 8. Document revision history

Date	Revision	Changes
21-Nov-2001	1	Initial release.
23-Jun-2005	2	PPAP references inserted in the datasheet, see *Table 7: Order codes*.
05-May-2008	3	AC and DC performance characteristics curves added for V_{CC}= 6V, V_{CC}= 10V and V_{CC}= 30V. Modified I_{CC} typ, added parameters over temperature range in electrical characteristics table. Corrected macromodel information.
04-Feb-2010	4	Updated document format. Added TS512A and related parameters. Modified footnote *1* under *Table 2*. Removed *Figure 11*. Modified *Figure 12* and *Figure 13*. Removed TS512AIYD order code from *Table 7*.
12-Sep-2012	5	Updated CMR and SVR test conditions in *Table 3*. Removed TS512IYD order code from *Table 7*. Minor corrections throughout document.