1. Cyclone III Device Datasheet: DC and Switching Characteristics

CIII52001-1.3

Electrical Characteristics

Operating Conditions

When Cyclone® III devices are implemented in a system, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Cyclone III devices, system designers must consider the operating requirements within this document. Cyclone III devices are offered in both commercial and industrial grades. Commercial devices are offered in –6 (fastest), –7, and –8 speed grades.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Cyclone III devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Conditions beyond those listed in Table 1–1 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device. All parameters representing voltages are measured with respect to ground.

Table 1–1. Cyclone III Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	–0.5	1.8	V
V_{CCIO}	Supply voltage for output buffers	–0.5	3.9	V
V_{CCA}	Supply (analog) voltage for PLL regulator	–0.5	3.75	V
V_{CCD_PLL}	Supply (digital) voltage for PLL	–0.5	1.8	V
V_I	DC input voltage	–0.5	3.95	V
I_{OUT}	DC output current, per pin	–25	40	mA
V_{ESDHBM}	Electrostatic discharge voltage using the human body model	NA	±2000	V
V_{ESDCDM}	Electrostatic discharge voltage using the charged device model	NA	±500	V
T_{STG}	Storage temperature	–65	150	°C
T_J	Operating junction temperature	–40	125	°C

Note to Table 1–1:
(1) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.

Maximum Allowed Overshoot/Undershoot Voltage
During transitions, input signals may overshoot to the voltage shown in Table 1–2 and undershoot to –2.0 V for input currents less than 100 mA and for periods shorter than 20 ns.

Table 1–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as percentage of high-time over the lifetime of the device.

A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.2 V can only be at 4.2 V for 10.74% over the lifetime of the device; for device lifetime of 10 years, this amounts to 10.74/10ths of a year. Figure 1–1 shows the way to determine the overshoot duration.

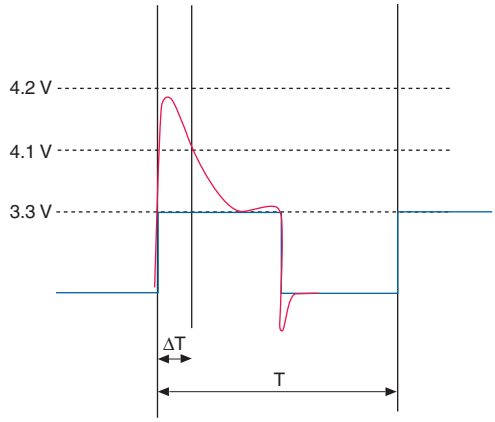
Table 1–2. Maximum Allowed Overshoot During Transitions over 10-Year Time Frame

Symbol	Parameter	Condition	Overshoot Duration as % of High Time	Unit
Vi	AC Input Voltage	V_I = 3.95 V	100	%
		V_I = 4.0 V	95.67	%
		V_I = 4.05 V	55.24	%
		V_I = 4.10 V	31.97	%
		V_I = 4.15 V	18.52	%
		V_I = 4.20 V	10.74	%
		V_I = 4.25 V	6.23	%
		V_I = 4.30 V	3.62	%
		V_I = 4.35 V	2.1	%
		V_I = 4.40 V	1.22	%
		V_I = 4.45 V	0.71	%
		V_I = 4.50 V	0.41	%
		V_I = 4.60 V	0.14	%
		V_I = 4.70 V	0.047	%

Note to Table 1–2:

(1) Figure 1–1 shows the methodology to determine the overshoot duration. In the example in Figure 1–1, overshoot voltage is shown in red and is present on the Cyclone III input pin at over 4.1 V but below 4.2 V. From Table 1–1, for an overshoot of 4.1 V the percentage of high time for the overshoot can be as high as 31.97 % over a 10-year period. Percentage of high time is calculated as ((delta T)/T) × 100. This 10-year period assumes the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations where the device is in an idle state, lifetimes are increased.

Figure 1–1. Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Cyclone III devices. The steady-state voltage and current values expected from Cyclone III devices are provided in the Table 1–3. All supplies must be strictly monotonic without plateaus.

Table 1–3. Recommended Operating Conditions *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCINT} *(3)*	Supply voltage for internal logic and input buffers	—	1.15	1.2	1.25	V
V_{CCIO} *(3)*	Supply voltage for output buffers, 3.3-V operation	—	3.15	3.3	3.45	V
	Supply voltage for output buffers, 3.0-V operation	—	2.85	3	3.15	V
	Supply voltage for output buffers, 2.5-V operation	—	2.375	2.5	2.625	V
	Supply voltage for output buffers, 1.8-V operation	—	1.71	1.8	1.89	V
	Supply voltage for output buffers, 1.5-V operation	—	1.425	1.5	1.575	V
	Supply voltage for output buffers, 1.2-V operation	—	1.14	1.2	1.26	V
V_{CCA} *(3)*	Supply (analog) voltage for PLL regulator	—	2.375	2.5	2.625	V
V_{CCD_PLL} *(3)*	Supply (digital) voltage for PLL	—	1.15	1.2	1.25	V
V_I	Input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	–40	—	100	°C
tRAMP	Power supply ramptime	Standard POR *(4)*	50 µs	—	50 ms	—
		Fast POR *(5)*	50 µs	—	3 ms	—

Notes to Table 1–3:

(1) V_{CCIO} for all I/O banks should be powered up during device operation. All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used), and must be powered-up and powered-down at the same time.
(2) V_{CCD_PLL} must always be connected to V_{CCINT} through a decoupling capacitor and ferrite bead.
(3) The V_{CC} must rise monotonically.
(4) POR time for Standard POR will range between 50 – 200 ms. All supplies must be up and stable within 50 ms.
(5) POR time for Fast POR will range between 3 – 9 ms. All supplies must be up and stable within 3 ms.

DC Characteristics

This section lists the I/O leakage currents, pin capacitance, on chip termination tolerance and and bus hold specifications for Cyclone III devices.

Supply Current

Standby current is the current the device draws after the device is configured with no inputs/outputs toggling and no activity in the device. Since these currents vary largely with resources used, use the Excel based Early Power Estimator to get supply current estimates for your design. Table 1–4 lists I/O pin leakage current for Cyclone III.

Table 1–4. Cyclone III I/O Pin Leakage Current *Notes (1), (2)* **(Part 1 of 2)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input Pin Leakage Current	$V_I = V_{CCIOMAX}$ to 0 V	–10	—	10	µA
I_{OZ}	Tri-stated I/O Pin Leakage Current	$V_O = V_{CCIOMAX}$ to 0 V	–10	—	10	µA

Table 1–4. Cyclone III I/O Pin Leakage Current Notes (1), (2) (Part 2 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CCINT0}	V_{CCINT} supply current (standby)	V_I = ground, no load, no toggling inputs, T_J= 25C	EP3C5	1.7	(3)	mA
			EP3C10	1.7		mA
			EP3C16	3.0		mA
			EP3C25	3.5		mA
			EP3C40	4.3		mA
			EP3C55	5.2		mA
			EP3C80	6.5		mA
			EP3C120	8.4		mA
I_{CCA0}	V_{CCA} supply current (standby)	V_I = ground, no load, no toggling inputs, T_J = 25C	EP3C5	11.3	(3)	mA
			EP3C10	11.3		mA
			EP3C16	11.4		mA
			EP3C25	18.4		mA
			EP3C40	18.6		mA
			EP3C55	18.7		mA
			EP3C80	18.9		mA
			EP3C120	19.2		mA
I_{CCD_PLL0}	V_{CCD_PLL} supply current (standby)	V_I = ground, no load, no toggling inputs, T_J = 25C	EP3C5	4.1	(3)	mA
			EP3C10	4.1		mA
			EP3C16	8.2		mA
			EP3C25	8.2		mA
			EP3C40	8.2		mA
			EP3C55	8.2		mA
			EP3C80	8.2		mA
			EP3C120	8.2		mA
I_{CCIO0}	V_{CCIO} supply current (standby)	V_I = ground, no load, no toggling inputs, T_J = 25C	EP3C5	0.6	(3)	mA
			EP3C10	0.6		mA
			EP3C16	0.9		mA
			EP3C25	0.9		mA
			EP3C40	1.3		mA
			EP3C55	1.3		mA
			EP3C80	1.3		mA
			EP3C120	1.2		mA

Notes to Table 1–4:

(1) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 3.0, 2.5, 1.8, 1.5 and 1.2 V).

(2) 10 µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be the observed when the diode is on.

(3) Maximum values depend on the actual T_J and design utilization. Refer to the Excel-based PowerPlay Early Power Estimator (available at **www.altera.com/support/devices/estimator/cy3-estimator/cy3-power_estimator.html**) or the Quartus II PowerPlay Power Analyzer feature for maximum values. Refer to the "Power Consumption" on page 1–11" for more information.

Bus Hold

Bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode. Table 1–5 lists bus hold specifications for Cyclone III. Also listed are the input pin capacitances and on-chip termination tolerance specifications.

Table 1–5. Cyclone III Bus Hold Parameter *Note (1)*

Parameter	Condition	V_{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold low, sustaining current	$V_{IN} > V_{IL}$ (maximum)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus-hold high, sustaining current	$V_{IN} < V_{IL}$ (minimum)	–8	—	–12	—	–30	—	–50	—	–70	—	–70	—	µA
Bus-hold low, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus-hold high, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	–125	—	–175	—	–200	—	–300	—	–500	—	–500	µA
Bus-hold trip point	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

Note to Table 1–5:
(1) The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

On-Chip Termination (OCT) Specifications

Table 1–6 lists variation of uncalibrated OCT across process, temperature and voltage.

Table 1–6. Uncalibrated On-Chip Series Termination Specifications **Preliminary**

Symbol	V_{CCIO} (V)	Resistance Tolerance				Unit
		Commercial		Industrial		
		Min	Max	Min	Max	
Series Termination without calibration	3.0	–30	+30	*(1)*	*(1)*	%
	2.5	–30	+30	*(1)*	*(1)*	%
	1.8	–30	+30	*(1)*	*(1)*	%
	1.5	–30	+30	*(1)*	*(1)*	%
	1.2	–40	+40	*(1)*	*(1)*	%

Note to Table 1–6:
(1) Pending silicon characterization

OCT calibration is automatically performed at power up for OCT enabled I/Os.

Table 1–7 lists the OCT calibration accuracy at power up.

Table 1–7. On-Chip Series Termination Power-up Calibration Specifications				Preliminary
Symbol	V_{CCIO} (V)	Calibration Accuracy		Unit
		Commercial Max	Industrial Max	
Series Termination with power-up calibration	3.0	±10%	*(1)*	%
	2.5	±10%	*(1)*	%
	1.8	±10%	*(1)*	%
	1.5	±10%	*(1)*	%
	1.2	±10%	*(1)*	%

Note to Table 1–7:
(1) Pending silicon characterization

Table 1–8 lists the percentage change of the OCT resistance with voltage and temperature. Use Table 1–8 and Equation 1–1 to determine OCT variation after power-up calibration.

Table 1–8. On-Chip Termination Variation After Power-up Calibration		
Nominal Voltage	dR/dT (%ΔOhm/°C)	dR/dmV (%ΔOhm/mV)
3.0	0.262	–0.026
2.5	0.234	–0.039
1.8	0.219	–0.086
1.5	0.199	–0.136
1.2	0.161	–0.288

Note to Table 1–8:
(1) This table is needed to calculate the final OCT resistance with the variation of temperature and voltage.

Equation 1–1. *Notes (1), (2), (3), (4), (5), (6), (7), (8), (9), (10), (11), (12)*

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dmV \text{ ----- (1)}$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT \text{ ----- (2)}$$

$$\text{For } \Delta R_x < 0;\ MF_x = 1/\ (|\Delta R_x|\ /100 + 1) \text{ ----- (3)}$$

$$\text{For } \Delta R_x > 0;\ MF_x = \Delta R_x/100 + 1 \text{ ----- (4)}$$

$$MF = MF_V \times MF_T \text{ ----- (5)}$$

$$R_{final} = R_{initial} \times MF \text{ ----- (6)}$$

Notes to Equation 1–1:

(1) ΔR_V is variation of resistance with voltage.
(2) ΔR_T is variation of resistance with temperature.
(3) dR/dT is the percentage change of resistance with temperature.
(4) dR/dmV is the percentage change of resistance with voltage.
(5) V_2 is final voltage.
(6) V_1 is the initial voltage.
(7) T_2 is the final temperature.
(8) T_1 is the initial temperature.
(9) MF is multiplication factor.
(10) R_{final} is final resistance.
(11) $R_{initial}$ is initial resistance.
(12) Subscript x refers to both $_V$ and $_T$.

For example, to calculate the change of 50 Ω I/O impedance from 25° C at 3.0 V to 85° C at 3.15 V,

$$\Delta R_V = (3.15 - 3) \times 1000 \times -0.026 = -3.83$$
$$\Delta R_T = (85 - 25) \times 0.262 = 15.72$$

Since ΔR_V is negative,

$$MF_V = 1\ /\ (3.83/100 + 1) = 0.963$$

Since ΔR_T is positive,

$$MF_T = 15.72/100 + 1 = 1.157$$

$$MF = 0.963 \times 1.157 = 1.114$$

$$R_{final} = 50 \times 1.114 = \underline{55.71}\ \Omega$$

Pin Capacitance

Table 1–9 shows the Cyclone III device family pin capacitance.

Table 1–9. Cyclone III Device Pin Capacitance *Note (1)* ***(Part 1 of 2)*** **Preliminary**

Symbol	Parameter	Typical – QFP	Typical – FBGA	Unit
C_{IOTB}	Input capacitance on top/bottom I/O pins	7	6	pF
C_{IOLR}	Input capacitance on left/right I/O pins	6	5	pF
C_{LVDSLR}	Input capacitance on left/right I/O pins with Dedicated LVDS output	8	7	pF
C_{VREFLR}	Input capacitance on left/right I/O pins with V_{REF}	21	21	pF
C_{VREFTB}	Input capacitance on top/bottom I/O pins with V_{REF}	21 *(2)*	21 *(2)*	pF
C_{CLKTB}	Input capacitance on top/bottom dedicated clock input pins	7	6	pF

Table 1–9. Cyclone III Device Pin Capacitance Note (1) (Part 2 of 2)				Preliminary
Symbol	**Parameter**	**Typical – QFP**	**Typical – FBGA**	**Unit**
C_{CLKLR}	Input capacitance on left/right dedicated clock input pins	6	5	pF

Notes to Table 1–9:
(1) Pending silicon characterization.
(2) C_{VREFTB} for EP3C25 is 30 pF.

Internal Weak Pull-up and Weak Pull-down Resistor

Table 1–10 lists the weak pull-up and pull-down resistor values for Cyclone III devices.

Table 1–10. Cyclone III Internal Weak Pull-Up / Weak Pull-Down Resistor Note (1)						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
R_{CONF_PU} (2)	Value of I/O pin pull-up resistor before and during configuration	V_I = 0 V, V_{CCIO} = 3.3 V ± 5% (3), (4)	7	25	41	KΩ
		V_I = 0 V, V_{CCIO} = 3.0 V ± 5% (3), (4)	7	28	47	KΩ
		V_I = 0 V, V_{CCIO} = 2.5 V ± 5% (3), (4)	8	35	61	KΩ
		V_I = 0 V, V_{CCIO} = 1.8 V ± 5% (3), (4)	10	57	108	KΩ
		V_I = 0 V, V_{CCIO} = 1.5 V ± 5% (3), (4)	13	82	163	KΩ
		V_I = 0 V, V_{CCIO} = 1.2 V ± 5% (3), (4)	19	143	351	KΩ
R_{CONF_PD} (2)	Value of I/O pin pull-down resistor before and during configuration	V_I = 0 V, V_{CCIO} = 3.3 V ± 5% (3), (4)	6	19	30	KΩ
		V_I = 0 V, V_{CCIO} = 3.0 V ± 5% (3), (4)	6	22	36	KΩ
		V_I = 0 V, V_{CCIO} = 2.5 V ± 5% (3), (4)	6	25	43	KΩ
		V_I = 0 V, V_{CCIO} = 1.8 V ± 5% (3), (4)	7	35	71	KΩ
		V_I = 0 V, V_{CCIO} = 1.5 V ± 5% (3), (4)	8	50	112	KΩ

Notes to Table 1–10:
(1) All I/O pins have an option to enable weak pull-up except configuration, test and JTAG pin. Weak pull-down feature is only available for JTAG TCK.
(2) R_{CONF} values are based on characterization. $R_{CONF} = V_{CCIO}/I_{RCONF}$. R_{CONF} values may be different if V_I value is not 0 V. V_I refers to the input voltage at the I/O pin.
(3) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
(4) Minimum condition at –40° C and high V_{CC}, typical condition at 25° C and nominal V_{CC} and maximum condition at 125° C and low V_{CC} for R_{CONF} values.

Hot Socketing

Table 1–11 lists the hot-socketing specifications for Cyclone III devices.

Table 1–11. Cyclone III Hot Socketing Specifications		
Symbol	**Parameter**	**Maximum**
$I_{IOPIN(DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN(AC)}$	AC current per I/O pin	8 mA (1)

Note to Table 1–11:
(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |IIOPIN| = C dv/dt, where C is I/O pin capacitance and *dv/dt* is the slew rate.

I/O Standard Specifications

The following tables list input voltage sensitivities (V_{IH} and V_{IL}), and output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Cyclone III devices. Table 1–12 to Table 1–17 show the Cyclone III device family I/O standard specifications. Refer to "Single-ended Voltage referenced I/O Standard" in "Glossary" for voltage referenced receiver input waveform and explanation of terms used in Table 1–12.

Table 1–12. Single-Ended I/O Standard Specifications *Note (1)*

I/O Standard	V_{CCIO}(V)			V_{IL}(V)		V_{IH}(V)		V_{OL}(V)	V_{OH}(V)	I_{OL} *(3)* (mA)	I_{OH} *(3)* (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTL *(2)*	3.15	3.3	3.45	—	0.8	1.7	3.6	0.45	2.4	4	–4
3.3-V LVCMOS *(2)*	3.15	3.3	3.45	—	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	2	–2
3.0-V LVTTL *(2)*	2.85	3.0	3.15	–0.3	0.8	1.7	V_{CCIO} + 0.3	0.45	2.4	4	–4
3.0-V LVCMOS *(2)*	2.85	3.0	3.15	–0.3	0.8	1.7	V_{CCIO} + 0.3	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5-V LVTTL and LVCMOS *(2)*	2.375	2.5	2.625	–0.3	0.7	1.7	V_{CCIO} + 0.3	0.2	2.1	0.1	–0.1
								0.4	2.0	1	–1
								0.7	1.7	2	–2
1.8-V LVTTL and LVCMOS	1.71	1.8	1.89	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	2.25	0.45	V_{CCIO} – 0.45	2	–2
1.5-V LVCMOS	1.425	1.5	1.575	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	–2
1.2-V LVCMOS	1.14	1.2	1.26	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	–2
PCI and PCI-X	2.85	3.0	3.15	—	0.3 * V_{CCIO}	0.5 * V_{CCIO}	V_{CCIO} + 0.3	0.1 * V_{CCIO}	0.9 * V_{CCIO}	1.5	–0.5

Notes to Table 1–12:

(1) AC load CL = 10 pF.

(2) For more detail of interfacing Cyclone III devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O standards, refer to AN 447: Interfacing Cyclone III Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems.

(3) Specified I_{OL} and I_{OH} are valid with lowest current strength setting available for respective I/O standards. I_{OL} and I_{OH} values correspond to the selected current strength settings value. For example, current drive characteristics for 3.3-V LVTTL with 8 mA current strength setting are 8 mA (I_{OL}) and –8 mA (I_{OH}) at 0.45 V (V_{OL}) and 2.4 V (V_{OH}), respectively.

Refer to "Glossary" for explanation of terms used in Table 1–13.

Table 1–13. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications

I/O Standard	V_{CCIO}(V)			V_{REF}(V)			V_{TT}(V) *(3)*		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 * V_{CCIO} *(1)*	0.5 * V_{CCIO} *(1)*	0.52 * V_{CCIO} *(1)*	—	0.5 * V_{CCIO}	—
				0.47 * V_{CCIO} *(2)*	0.5 * V_{CCIO} *(2)*	0.53 * V_{CCIO} *(2)*			

Notes to Table 1–13:

(1) Value shown refers to DC input reference voltage, $V_{REF(DC)}$.

(2) Value shown refers to AC input reference voltage, $V_{REF(AC)}$.

(3) V_{TT} of transmitting device must track V_{REF} of the receiving device.

Table 1–14. Single-Ended SSTL and HSTL I/O Standards Signal Specifications

I/O Standard	$V_{IL(DC)}$(V)		$V_{IH(DC)}$(V)		$V_{IL(AC)}$(V)		$V_{IH(AC)}$(V)		V_{OL}(V)	V_{OH}(V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
SSTL-2 Class I	—	V_{REF} – 0.18	V_{REF} + 0.18	—	—	V_{REF} – 0.35	V_{REF} + 0.35	—	V_{TT} – 0.57	V_{TT} + 0.57	8.1	–8.1
SSTL-2 Class II	—	V_{REF} – 0.18	V_{REF} + 0.18	—	—	V_{REF} – 0.35	V_{REF} + 0.35	—	V_{TT} – 0.76	V_{TT} + 0.76	16.4	–16.4
SSTL-18 Class I	—	V_{REF} – 0.125	V_{REF} + 0.125	—	—	V_{REF} – 0.25	V_{REF} + 0.25	—	V_{TT} – 0.475	V_{TT} + 0.475	6.7	–6.7
SSTL-18 Class II	—	V_{REF} – 0.125	V_{REF} + 0.125	—	—	V_{REF} – 0.25	V_{REF} + 0.25	—	0.28	V_{CCIO} – 0.28	13.4	–13.4
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	–0.24	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	–0.24	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 × V_{CCIO}	0.75 × V_{CCIO}	14	–14

For more illustrations of receiver input and transmitter output waveforms, and for other differential I/O standards, refer to the *High-Speed Differential Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook.*

Table 1–15. Differential SSTL I/O Standard Specifications

I/O Standard	V_{CCIO}(V)			$V_{Swing(DC)}$(V)		$V_{X(DC)}$(V)			$V_{Swing(AC)}$(V)		$V_{OX(AC)}$(V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V_{CCIO}	V_{CCIO}/2 – 0.2	—	V_{CCIO}/2 + 0.2	0.7	V_{CCIO}	*(1)*	—	*(1)*
SSTL-18 Class I, II	1.7	1.8	1.90	0.25	V_{CCIO}	V_{CCIO}/2 – 0.175	—	V_{CCIO}/2 + 0.175	0.5	V_{CCIO}	V_{CCIO}/2 – 0.125	—	V_{CCIO}/2 + 0.125

Note to Table 1–15:
(1) Pending silicon characterization.

Table 1–16. Differential HSTL I/O Standard Specifications

I/O Standard	V_{CCIO}(V)			$V_{DIF(DC)}$(V)		$V_{X(AC)}$(V)			$V_{CM(DC)}$(V)			$V_{DIF(AC)}$(V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO}	0.48 * V_{CCIO}	—	0.52 * V_{CCIO}	0.48 * V_{CCIO}	—	0.52 * V_{CCIO}	0.3	0.48 * V_{CCIO}

Refer to "Transmitter Output Waveform" in "Glossary" for an explanation of terms used in Table 1–17.

Table 1–17. Differential I/O Standard Specifications

I/O Standard	V_{CCIO}(V)			V_{TH}(mV)			V_{IN}(V)			V_{OD}(mV) *(1)*			V_{OS}(V) *(1)*		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL (Row I/Os) *(2)*	2.375	2.5	2.625	–100	V_{CM} = 1.25V	100	0	D_{MAX} ≤500 Mbps	1.85	247	—	600	1.125	1.25	1.375
							0.5	500 Mbps ≤D_{MAX} ≤700 Mbps	1.85						
							1	D_{MAX} > 700 Mbps	1.6						
LVPECL (Column I/Os) *(2)*	2.375	2.5	2.625	–100	V_{CM} = 1.25V	100	0	D_{MAX} ≤500 Mbps	1.85	247	—	600	1.125	1.25	1.375
							0.5	500 Mbps ≤D_{MAX} ≤700 Mbps	1.85						
							1	D_{MAX} > 700 Mbps	1.6						
LVDS (Row I/Os)	2.375	2.5	2.625	–100	V_{CM} =1.25V	100	0	D_{MAX} ≤500 Mbps	1.85	247	—	600	1.125	1.25	1.375
							0.5	500 Mbps ≤D_{MAX} ≤700 Mbps	1.85						
							1	D_{MAX} > 700 Mbps	1.6						
LVDS (Column I/Os)	2.375	2.5	2.625	–100	V_{CM} = 1.25V	100	0	D_{MAX} ≤500 Mbps	1.85	247	—	600	1.125	1.25	1.375
							0.5	500 Mbps ≤D_{MAX} ≤700 Mbps	1.85						
							1	D_{MAX} > 700 Mbps	1.6						
mini-LVDS (Row I/Os) *(3)*	2.375	2.5	2.625	—	—	—	—	—	—	300	—	600	1.0	1.2	1.4
mini-LVDS (Column I/Os) *(3)*	2.375	2.5	2.625	—	—	—	—	—	—	300	—	600	1.0	1.2	1.4
RSDS® (Row I/Os)*(3) (4)*	2.375	2.5	2.625	—	—	—	—	—	—	100	200	600	0.5	1.2	1.5
RSDS (Column I/Os) *(3)*	2.375	2.5	2.625	—	—	—	—	—	—	100	200	600	0.5	1.2	1.5
PPDS® (Row I/Os) *(3) (4)*	2.375	2.5	2.625	—	—	—	—	—	—	100	200	600	0.5	1.2	1.4
PPDS (Column I/Os) *(3)*	2.375	2.5	2.625	—	—	—	—	—	—	100	200	600	0.5	1.2	1.4

Notes to Table 1–17:

(1) R_L range : 90 ≤R_L ≤110 Ω

(2) LVPECL input standard is only supported at clock input. Output standard is not supported.

(3) Mini-LVDS, RSDS and PPDS standards are only supported at output pins of Cyclone III devices.

(4) RSDS and PPDS are registered trademarks of National Semiconductor.

Power Consumption

Altera® offers two ways to estimate power for a design: the Excel-based Early Power Estimator and the Quartus® II **PowerPlay Power Analyzer** feature.

The interactive Excel-based Early Power Estimator is typically used prior to designing the device in order to get a magnitude estimate of the device power. The Quartus II **PowerPlay Power Analyzer** provides better quality estimates based on the specifics of the design after place-and-route is complete. The **PowerPlay Power Analyzer** can apply a combination of user-entered, simulation-derived, and estimated signal activities which, combined with detailed circuit models, can yield very accurate power estimates.

For more information on power estimation tools, refer to the *Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapters in the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of the Cyclone III core and periphery blocks for commercial grade devices.

These characteristics can be designated as Preliminary and Final. Each designation is defined below.

Preliminary	Final
Preliminary characteristics are created using simulation results, process data, and other known parameters.	Final numbers are based on actual silicon characterization and testing. These numbers reflect the actual performance of the device under worst-case silicon process, voltage and junction temperature conditions.

The upper-right hand corner of a table shows the designation as '***Preliminary***' or '***Final***'.

Core Performance Specifications

Clock Tree Specifications

Table 1–18 lists the clock tree specifications for Cyclone III devices.

Table 1–18. Cyclone III Clock Tree Performance — **Preliminary**

Device	Performance			Unit
	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	
EP3C5	500	*(2)*	*(2)*	MHz
EP3C10	500	*(2)*	*(2)*	MHz
EP3C16	500	*(2)*	*(2)*	MHz
EP3C25	500	*(2)*	*(2)*	MHz
EP3C40	500	*(2)*	*(2)*	MHz
EP3C55	500	*(2)*	*(2)*	MHz
EP3C80	500	*(2)*	*(2)*	MHz
EP3C120	*(1)*	437.5	*(2)*	MHz

Notes to Table 1–18:
(1) EP3C120 offered in –7 and –8 speed grades only.
(2) Pending silicon characterization.

PLL Specifications

Table 1–19 describes the Cyclone III PLL specifications when operating in both the commercial junction temperature range (0° C to 85° C) and the industrial junction temperature range (–40° C to 100° C). For more information on PLL Block, refer to "PLL Block" in "Glossary".

Table 1–19. Cyclone III PLL Specifications *Note (5)* ***(Part 1 of 2)*** — **Preliminary**

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN} *(1)*	Input clock frequency (–6 speed grade)	5	—	472.5	MHz
	Input clock frequency (–7 speed grade)	5	—	472.5	MHz
	Input clock frequency (–8 speed grade)	5	—	472.5	MHz
f_{INPFD}	PFD input frequency (–6 speed grade)	5	—	325	MHz
	PFD input frequency (–7 speed grade)	5	—	325	MHz
	PFD input frequency (–8 speed grade)	5	—	325	MHz

Table 1–19. Cyclone III PLL Specifications Note (5) (Part 2 of 2)					Preliminary
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
f_{VCO}	PLL internal VCO operating range	600	—	1300	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$t_{INJITTER}$	Input clock period jitter	—	200	—	ps
f_{OUT_EXT} (external clock output) (1)	PLL output frequency (–6 speed grade)	5	—	472.5	MHz
	PLL output frequency (–7 speed grade)	5	—	472.5	MHz
	PLL output frequency (–8 speed grade)	5	—	472.5	MHz
f_{OUT} (to global clock)	PLL output frequency (–6 speed grade)	5	—	472.5	MHz
	PLL output frequency (–7 speed grade)	5	—	450	MHz
	PLL output frequency (–8 speed grade)	5	—	402.5	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{LOCK}	Time required to lock from end of device configuration	—	—	100 (2)	µs
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
$t_{OU\ TJIT\ TE\ R\_DEDCLK}$	Dedicated clock output period jitter	—	—	300	ps
$t_{OU\ TJIT\ TE\ R\_IO}$	Regular I/O period jitter	—	—	(4)	ps
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±60	ps
t_{ARESET}	Minimum pulse width on areset signal.	10	—	—	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for PLLs	—	3.5 (3)	—	SCANCLK cycles
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz

Notes to Table 1–19:
(1) This parameter is limited in Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
(2) For extended temperature devices, the maximum lock time is 500 µs.
(3) With 100 MHz `scanclk` frequency.
(4) Pending silicon characterization.
(5) V_{CCD_PLL} should always be connected to V_{CCINT} through decoupling capacitor and ferrite bead.

Embedded Multiplier Specifications

Table 1–20 describes the Cyclone III embedded multiplier specifications.

Table 1–20. Cyclone III Embedded Multiplier Specifications					Preliminary
Mode	**Resources Used**	**Performance**			**Unit**
	Number of Multipliers	**–6 Speed Grade**	**–7 Speed Grade**	**–8 Speed Grade**	
9 × 9-bit multiplier	1	260	223	180	MHz
18 × 18-bit multiplier	1	260	223	180	MHz

Memory Block Specifications

Table 1–21 describes the Cyclone III M9K Memory block specifications.

Table 1–21. Cyclone III Memory Block Performance Specifications Note (1) — Preliminary

Memory	Mode	Resources Used		Performance	
		LEs	M9K Memory	–6 Speed Grade	Unit
M9K Block	FIFO 256×36	47	1	260	MHz
	Single-port 256×36	0	1	260	MHz
	Simple dual-port 256×36 CLK	0	1	260	MHz
	True dual port 512×18 single CLK	0	1	260	MHz

Note to Table 1–21:
(1) Values for device speed grade –7 and –8 will be available after characterization.

Configuration and JTAG Specifications

Table 1–22 lists the Cyclone III Configuration Mode Specifications.

Table 1–22. Cyclone III Configuration Mode Specifications — Preliminary

Programming Mode	DCLK F_{max}	Unit
Passive Serial (PS)	133	MHz
Fast Passive Parallel (FPP) *(1)*	100	MHz

Note to Table 1–22:
(1) EP3C25 and smaller family members support 133 MHz.

Table 1–23 lists the Cyclone III Active Configuration Mode Specifications.

Table 1–23. Cyclone III Active Configuration Mode Specifications — Preliminary

Programming Mode	DCLK Range	Unit
Active Parallel (AP)	20 – 40	MHz
Active Serial (AS)	20 – 40	MHz

Table 1–24 shows the JTAG timing parameters and values for Cyclone III. For more information, refer to "JTAG Waveform" in "Glossary".

Table 1–24. Cyclone III JTAG Timing Parameters (Part 1 of 2) — Preliminary

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	40	—	ns
t_{JCH}	TCK clock high time	20	—	ns
t_{JCL}	TCK clock low time	20	—	ns
t_{JPSU_TDI}	JTAG port setup time for TDI *(1)*	1	—	ns
t_{JPSU_TMS}	JTAG port setup time for TMS *(1)*	3	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output *(1)*	—	15	ns
t_{JPZX}	JTAG port high impedance to valid output *(1)*	—	15	ns

Table 1–24. Cyclone III JTAG Timing Parameters (Part 2 of 2)				Preliminary
Symbol	**Parameter**	**Min**	**Max**	**Unit**
t_{JPXZ}	JTAG port valid output to high impedance *(1)*	—	15	ns
t_{JSSU}	Capture register setup time *(1)*	5	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Note to Table 1–24:
(1) The specification is shown for 3.3 V, 3.0 V and 2.5 V LVTTL/LVCMOS operation of JTAG pins. For 1.8- V LVTTL/LVCMOS and 1.5- V LVCMOS, the JTAG port clock to output time is 16 ns.

Periphery Performance

High-Speed I/O Specification

Table 1–25 to Table 1–34 show the high-speed I/O timing for Cyclone III devices. Refer to "Glossary" for definitions of high-speed timing specifications.

Table 1–25. Dedicated RSDS Transmitter Timing Specification *Notes (2), (3)*					
Symbol	**Modes**	**–6 Speed Grade**			**Unit**
		Min	**Typ**	**Max**	
f_{HSCLK} (input clock frequency)	×10	10	—	180	MHz
	×8	10	—	180	MHz
	×7	10	—	180	MHz
	×4	10	—	180	MHz
	×2	10	—	180	MHz
	×1	10	—	360	MHz
Device operation in Mbps	×10	100	—	360	Mbps
	×8	80	—	360	Mbps
	×7	70	—	360	Mbps
	×4	40	—	360	Mbps
	×2	20	—	360	Mbps
	×1	10	—	360	Mbps
t_{DUTY}	—	*(1)*	—	*(1)*	%
TCCS	—	—	—	*(1)*	ns
Output jitter (peak to peak)	—	—	—	*(1)*	ps
t_{RISE}	20 – 80%	—	*(1)*	—	ps
t_{FALL}	80 – 20%	—	*(1)*	—	ps
t_{LOCK}	—	—	—	*(1)*	ms

Notes to Table 1–25:
(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) Dedicated RSDS is only supported at output pin of Row I/O (Banks 1, 2, 5, and 6).

Table 1–26. Single-Resistor RSDS Transmitter Timing Specification Notes (2), (3)

Symbol	Modes	–6 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	85	MHz
	×8	10	—	85	MHz
	×7	10	—	85	MHz
	×4	10	—	85	MHz
	×2	10	—	85	MHz
	×1	10	—	85	MHz
Device operation in Mbps	×10	100	—	(1)	Mbps
	×8	80	—	(1)	Mbps
	×7	70	—	(1)	Mbps
	×4	40	—	(1)	Mbps
	×2	20	—	(1)	Mbps
	×1	10	—	(1)	Mbps
t_{DUTY}	—	(1)	—	(1)	%
TCCS	—	—	—	(1)	ps
Output jitter (peak to peak)	—	—	—	(1)	ps
t_{RISE}	20 – 80%	—	(1)	—	ps
t_{FALL}	80 – 20%	—	(1)	—	ps
t_{LOCK}	—	—	—	(1)	ms

Notes to Table 1–26:
(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) Single-resistor RSDS is only supported at output pin of Column I/O (Banks 3, 4, 7, and 8).

Table 1–27. Three-Resistor RSDS Transmitter Timing Specification Notes (2), (3) (Part 1 of 2)

Symbol	Modes	–6 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	155.5	MHz
	×8	10	—	155.5	MHz
	×7	10	—	155.5	MHz
	×4	10	—	155.5	MHz
	×2	10	—	155.5	MHz
	×1	10	—	155.5	MHz
Device operation in Mbps	×10	100	—	(1)	Mbps
	×8	80	—	(1)	Mbps
	×7	70	—	(1)	Mbps
	×4	40	—	(1)	Mbps
	×2	20	—	(1)	Mbps
	×1	10	—	(1)	Mbps
t_{DUTY}	—	(1)	—	(1)	%
TCCS	—	—	—	(1)	ps
Output jitter (peak to peak)	—	—	—	(1)	ps
t_{RISE}	20 – 80%	—	(1)	—	ps

Table 1–27. Three-Resistor RSDS Transmitter Timing Specification Notes (2), (3) (Part 2 of 2)

Symbol	Modes	–6 Speed Grade			Unit
		Min	Typ	Max	
t_{FALL}	80 – 20%	—	(1)	—	ps
t_{LOCK}	—	—	—	(1)	ms

Notes to Table 1–27:
(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) Three-resistor RSDS is only supported at output pin of Column I/O (Banks 3, 4, 7, and 8).

Table 1–28. Dedicated PPDS Transmitter Timing Specification Notes (2), (3)

Symbol	Modes	–6 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	(1)	MHz
	×8	10	—	(1)	MHz
	×7	10	—	(1)	MHz
	×4	10	—	(1)	MHz
	×2	10	—	(1)	MHz
	×1	10	—	(1)	MHz
Device operation in Mbps	×10	100	—	(1)	Mbps
	×8	80	—	(1)	Mbps
	×7	70	—	(1)	Mbps
	×4	40	—	(1)	Mbps
	×2	20	—	(1)	Mbps
	×1	10	—	(1)	Mbps
t_{DUTY}	—	(1)	—	(1)	%
TCCS	—	—	—	(1)	ps
Output jitter (peak to peak)	—	—	—	(1)	ps
t_{RISE}	20 – 80%	—	(1)	—	ps
t_{FALL}	80 – 20%	—	(1)	—	ps
t_{LOCK}	—	—	—	(1)	ms

Notes to Table 1–28:
(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) Dedicated PPDS is only supported at output pin of Row I/O (Banks 1, 2, 5, and 6).

Table 1–29. Three-Resistor PPDS Transmitter Timing Specification Notes (2), (3) (Part 1 of 2)

Symbol	Modes	–6 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	(1)	MHz
	×8	10	—	(1)	MHz
	×7	10	—	(1)	MHz
	×4	10	—	(1)	MHz
	×2	10	—	(1)	MHz
	×1	10	—	(1)	MHz

Table 1–29. Three-Resistor PPDS Transmitter Timing Specification Notes (2), (3) (Part 2 of 2)

Symbol	Modes	–6 Speed Grade			Unit
		Min	Typ	Max	
Device operation in Mbps	×10	100	—	(1)	Mbps
	×8	80	—	(1)	Mbps
	×7	70	—	(1)	Mbps
	×4	40	—	(1)	Mbps
	×2	20	—	(1)	Mbps
	×1	10	—	(1)	Mbps
t_{DUTY}	—	(1)	—	(1)	%
TCCS	—	—	—	(1)	ps
Output jitter (peak to peak)	—	—	—	(1)	ps
t_{RISE}	20 – 80%	—	(1)	—	ps
t_{FALL}	80 – 20%	—	(1)	—	ps
t_{LOCK}	—	—	—	(1)	ms

Notes to Table 1–29:
(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) Three-resistor PPDS is only supported at output pin of Column I/O (Banks 3, 4, 7, and 8).

Table 1–30. Dedicated Mini-LVDS Transmitter Timing Specification Notes (2), (3)

Symbol	Modes	–6 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	200	MHz
	×8	10	—	200	MHz
	×7	10	—	200	MHz
	×4	10	—	200	MHz
	×2	10	—	200	MHz
	×1	10	—	400	MHz
Device operation in Mbps	×10	100	—	400	Mbps
	×8	80	—	400	Mbps
	×7	70	—	400	Mbps
	×4	40	—	400	Mbps
	×2	20	—	400	Mbps
	×1	10	—	400	Mbps
t_{DUTY}	—	(1)	—	(1)	%
TCCS	—	—	—	1.30	ns
Output jitter (peak to peak)	—	—	—	(1)	ps
t_{RISE}	20 – 80%	—	(1)	—	ps
t_{FALL}	80 – 20%	—	(1)	—	ps
t_{LOCK}	—	—	—	(1)	ms

Notes to Table 1–30:
(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) Dedicated mini-LVDS is only supported at output pin of Row I/O (Banks 1, 2, 5, and 6).

Table 1–31. Three-Resistor mini-LVDS Transmitter Timing Specification Notes (2), (3)

Symbol	Modes	–6 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	155.5	MHz
	×8	10	—	155.5	MHz
	×7	10	—	155.5	MHz
	×4	10	—	155.5	MHz
	×2	10	—	155.5	MHz
	×1	10	—	155.5	MHz
Device operation in Mbps	×10	100	—	(1)	Mbps
	×8	80	—	(1)	Mbps
	×7	70	—	(1)	Mbps
	×4	40	—	(1)	Mbps
	×2	20	—	(1)	Mbps
	×1	10	—	(1)	Mbps
t_{DUTY}	—	(1)	—	(1)	%
TCCS	—	—	—	(1)	ps
Output jitter (peak to peak)	—	—	—	(1)	ps
t_{RISE}	20 – 80%	—	(1)	—	ps
t_{FALL}	80 – 20%	—	(1)	—	ps
t_{LOCK}	—	—	—	(1)	ms

Notes to Table 1–31:
(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) Three-resistor mini-LVDS is only supported at output pin of Column I/O (Banks 3, 4, 7, and 8).

Table 1–32. Dedicated LVDS Transmitter Timing Specification Notes (2), (5) (Part 1 of 2)

Symbol	Modes	–6 Speed Grade				Unit
		Min	Typ	Max (3)	Max (4)	
f_{HSCLK} (input clock frequency)	×10	10	—	420	(1)	MHz
	×8	10	—	420	(1)	MHz
	×7	10	—	420	(1)	MHz
	×4	10	—	420	(1)	MHz
	×2	10	—	420	(1)	MHz
	×1	10	—	420	(1)	MHz
HSIODR	×10	100	—	840	(1)	Mbps
	×8	80	—	840	(1)	Mbps
	×7	70	—	840	(1)	Mbps
	×4	40	—	840	(1)	Mbps
	×2	20	—	840	(1)	Mbps
	×1	10	—	420	(1)	Mbps
t_{DUTY}	—	(1)	—	(1)	(1)	%
TCCS	—	—	—	248		ps
Output jitter (peak to peak)	—	—	—	(1)	—	ps

Table 1–32. Dedicated LVDS Transmitter Timing Specification Notes (2), (5) (Part 2 of 2)

Symbol	Modes	–6 Speed Grade				Unit
		Min	Typ	Max (3)	Max (4)	
t_{RISE}	20 – 80%	(1)	(1)	(1)	(1)	ps
t_{FALL}	80 – 20%	(1)	(1)	(1)	(1)	ps
t_{LOCK}	—	—	—	(1)	—	ms

Notes to Table 1–32:
(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) The maximum data rate that complies with duty cycle distortion of 45–55%.
(4) The maximum data rate when taking duty cycle in absolute ps into consideration that may not comply with 45–55% duty cycle distortion. If the downstream receiver can handle duty cycle distortion beyond the 45–55% range, you may use the higher data rate values from this column. You can calculate the duty cycle distortion as a percentage using the absolute ps value. For example, for a data rate of 640 Mbps (UI = 1625 ps) and a tDUTY of 250 ps, the duty cycle distortion is: tDUTY/(UI*2) *100% = 250 ps/(1625 *2) * 100% = 7.7%, which gives you a duty cycle distortion of 42.3–57.7%.
(5) Dedicated LVDS transmitter is only supported at output pin of Row I/O (Banks 1, 2, 5, and 6).

Table 1–33. Three-Resistor LVDS Transmitter Timing Specification Notes (2), (5) (Part 1 of 2)

Symbol	Modes	–6 Speed Grade				Unit
		Min	Typ	Max (3)	Max (4)	
f_{HSCLK} (input clock frequency)	×10	10	—	320	320	MHz
	×8	10	—	320	320	MHz
	×7	10	—	320	320	MHz
	×4	10	—	320	320	MHz
	×2	10	—	320	320	MHz
	×1	10	—	402.5	402.5	MHz
HSIODR	×10	(1)	—	(1)	(1)	Mbps
	×8	(1)	—	(1)	(1)	Mbps
	×7	(1)	—	(1)	(1)	Mbps
	×4	(1)	—	(1)	(1)	Mbps
	×2	(1)	—	(1)	(1)	Mbps
	×1	(1)	—	(1)	(1)	Mbps
t_{DUTY}	—	(1)	—	(1)	(1)	%
TCCS	—	—	—	(1)	(1)	ps
Output jitter (peak to peak)	—	—	—	(1)	(1)	ps
t_{RISE}	20 – 80%	(1)	(1)	(1)	(1)	ps
t_{FALL}	80 – 20%	(1)	(1)	(1)	(1)	ps

Table 1–33. Three-Resistor LVDS Transmitter Timing Specification Notes (2), (5) (Part 2 of 2)

Symbol	Modes	–6 Speed Grade				Unit
		Min	Typ	Max (3)	Max (4)	
t_{LOCK}	—	—	—	(1)	—	ms

Notes to Table 1–33:
(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) The maximum data rate that complies with duty cycle distortion of 45–55%.
(4) The maximum data rate when taking duty cycle in absolute ps into consideration that may not comply with 45–55% duty cycle distortion. If the downstream receiver can handle duty cycle distortion beyond the 45–55% range, you may use the higher data rate values from this column. You can calculate the duty cycle distortion as a percentage using the absolute ps value. For example, for a data rate of 640 Mbps (UI = 1625 ps) and a t_{DUTY} of 250 ps, the duty cycle distortion is $t_{DUTY}/(UI*2)$ *100% = 250 ps/(1625 *2) * 100% = 7.7%, which gives you a duty cycle distortion of 42.3–57.7%.
(5) Three-resistor LVDS is only supported at output pin of Column I/O (Banks 3, 4, 7, and 8).

Table 1–34. Dedicated LVDS Receiver Timing Specification Notes (2), (3)

Symbol	Modes	–6 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	437.5	MHz
	×8	10	—	437.5	MHz
	×7	10	—	437.5	MHz
	×4	10	—	437.5	MHz
	×2	10	—	437.5	MHz
	×1	10	—	437.5	MHz
HSIODR	×10	100	—	875	Mbps
	×8	80	—	875	Mbps
	×7	70	—	875	Mbps
	×4	40	—	875	Mbps
	×2	20	—	875	Mbps
	×1	10	—	437.5	Mbps
SW	—	—	—	400	ps
Input jitter tolerance	—	—	—	(1)	ps
t_{LOCK}	—	—	—	(1)	ps

Notes to Table 1–34:
(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) Dedicated LVDS Receiver is supported at all banks.

External Memory Interface Specifications

Cyclone III devices support external memory interfaces up to 200 MHz. Cyclone III external memory interfaces are auto-calibrating and easy to implement. Table 1–35 to Table 1–38 list the External Memory Interface Specifications for the Cyclone III device family.

Use the following tables for memory interface timing analysis.

Table 1–35. Cyclone III Maximum Clock Rate Support for External Memory Interfaces Notes (1) (5)

Memory Standard	I/O Standard	Commercial					
		–6 Speed Grade (MHz)		–7 Speed Grade (MHz)		–8 Speed Grade (MHz)	
		Column I/Os	Row I/Os	Column I/Os	Row I/Os	Column I/Os	Row I/Os
DDR2 SDRAM (2)	SSTL-18 class I	200	167	167	150	167	133
	SSTL-18 class II	133	125	125	(3)	(3)	(3)
DDR SDRAM (2)	SSTL-2 class I	167	150	150	133	133	125
	SSTL-2 class II	133	125	125	100	100	(3)
QDRII SRAM (4)	1.8-V HSTL class I	167	150	150	133	133	125
	1.8V HSTL class II	100	(3)	(3)	(3)	(3)	(3)

Notes to Table 1–35:
(1) These numbers are preliminary until characterization is final.
(2) The values apply for interfaces with both modules and components.
(3) Support will be evaluated after characterization.
(4) QDRII SRAM also supports the 1.5-V HSTL I/O standard. However, Altera recommends using the 1.8-V HSTL I/O standard for maximum performance because of the higher I/O Current Strength.
(5) Column I/Os refer to Top and Bottom I/Os. Row I/Os refer to Right and Left I/Os.

Table 1–36. FPGA Sampling Window (SW) Requirement – Read Side Note (1) **Preliminary**

Memory Standards	–6 Speed Grade				–7 Speed Grade				–8 Speed Grade				Units
	Column I/Os		Row I/Os		Column I/Os		Row I/Os		Column I/Os		Row I/Os		
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	
DDR2 SDRAM	620	620	745	745	755	755	840	840	790	790	945	945	ps
DDR SDRAM	595	595	730	730	728	728	843	843	850	850	975	975	ps
QDRII SRAM	695	695	780	780	790	790	885	885	895	895	970	970	ps

Note to Table 1–36:
(1) Column I/Os refer to Top and Bottom I/Os. Row I/Os refer to Right and Left I/Os.

Table 1–37. Transmitter Channel-to-Channel Skew (TCCS) – Write Side Note (1) — **Preliminary**

Memory Standards	–6 Speed Grade				–7 Speed Grade				–8 Speed Grade				Units
	Column I/Os		Row I/Os		Column I/Os		Row I/Os		Column I/Os		Row I/Os		
	Lead	Lag	Lead	Lag	Lead	Lag	Lead	Lag	Lead	Lag	Lead	Lag	
DDR2 SDRAM	585	585	645	645	595	595	650	650	595	595	660	660	ps
DDR SDRAM	610	610	670	670	620	620	680	680	630	630	685	685	ps
QDRII SRAM	670	670	725	725	675	675	735	735	685	685	740	740	ps

Note to Table 1–37:
(1) Column I/Os refer to Top and Bottom I/Os. Row I/Os refer to Right and Left I/Os.

Table 1–38. DDIO Outputs Half-Period Jitter

Name	Description	Max	Unit
$t_{OUTFULLJITTER}$	Half-period jitter (PLL driving DDIO outputs)	(1)	ps

Note to Table 1–38:
(1) Pending silicon characterization.

DCD Specifications

Table 1–39 lists the worst case duty cycle distortion for Cyclone III devices. Detailed information on duty cycle distortion will be published after characterization.

Table 1–39. **Duty Cycle Distortion on Cyclone III I/O Pins** *Notes (1) (2)*

Symbol	–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	40	60	%

Notes to Table 1–39:
(1) Preliminary DCD specification applies to clock outputs from PLLs, global clock tree and IOE driving dedicated and general purpose I/O pins.
(2) Detailed DCD specification pending silicon characterization.

I/O Timing

Timing Model

The DirectDrive™ technology and MultiTrack™ interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Cyclone III device densities and speed grades. This section describes and specifies the performance of I/Os and internal timing.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

The timing numbers listed in the tables of this section are extracted from the Quartus II software version 7.0 Build 31.

Preliminary, Correlated and Final Timing

Timing models can have either preliminary, correlated, or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. Table 1–40 shows the status of the Cyclone III device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Correlated numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Final timing numbers are based on complete correlation to actual devices and addressing any minor deviations from the correlated timing model. When the timing models are final, all or most of the Cyclone III family devices have been completely characterized and no further changes to the timing model are expected.

Table 1–40. Cyclone III Device Timing Model Status

Device	Preliminary	Correlated	Final
EP3C5	*(1)*	—	—
EP3C10	✓	—	—
EP3C16	✓	—	—
EP3C25	✓	—	—
EP3C40	✓	—	—
EP3C55	✓	—	—
EP3C80	✓	—	—
EP3C120	✓	—	—

Note to Table 1–40:
(1) Timing model for EP3C5 will be available in Quartus II software 7.1.

I/O Timing Measurement Methodology

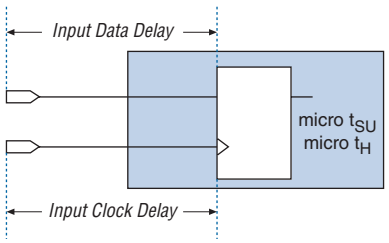
Altera characterizes timing delays at the worst-case process, minimum voltage, and maximum temperature for input register setup time (t_{SU}) and hold time (t_H). The Quartus II software uses the following equations to calculate t_{SU} and t_H timing for Cyclone III devices input signals:

t_{SU} = + data delay from input pin to input register
+ micro setup time of the input register
– clock delay from input pin to input register

t_H = – data delay from input pin to input register
+ micro hold time of the input register
+ clock delay from input pin to input register

Figure 1–2 shows the setup and hold timing diagram for input registers.

Figure 1–2. Input Register Setup and Hold Timing Diagram



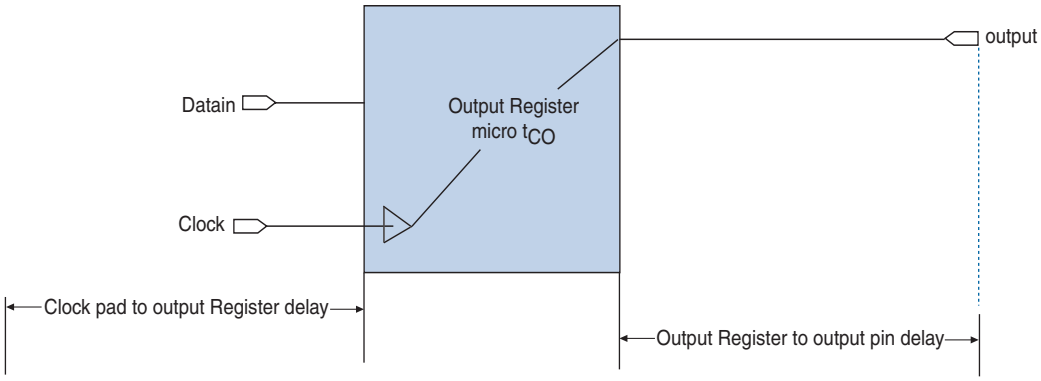
For output timing, different I/O standards require different baseline loading techniques for reporting timing delays. Altera characterizes timing delays with the required termination for each I/O standard and with 0 pF (except for PCI and PCI-X which use 10 pF) loading and the timing is specified up to the output pin of the FPGA device. The Quartus II software calculates the I/O timing for each I/O standard with a default baseline loading as specified by the I/O standards.

The following measurements are made during device characterization. Altera measures clock-to-output delays (t_{CO}) at worst-case process, minimum voltage, and maximum temperature (PVT) for default loading conditions shown in Table 1–41. Use the following equations to calculate clock pin to output pin timing for Cyclone III devices.

t_{CO} from clock pin to I/O pin =

- + delay from clock pad to I/O output register
- + IOE output register clock-to-output delay
- + delay from output register to output pin

Figure 1–3. Output Register Clock to Output Timing Diagram



Simulation using IBIS models is required to determine the delays on the PCB traces in addition to the output pin delay timing reported by the Quartus II software and the timing model in the device handbook.

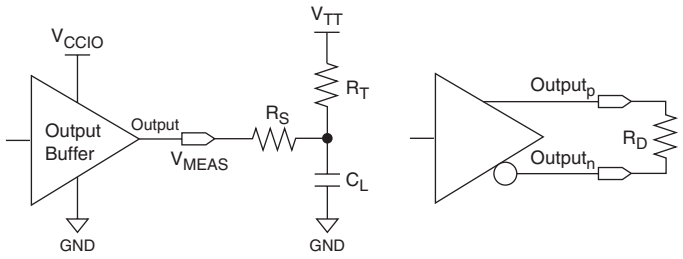
1. Simulate the output driver of choice into the generalized test setup, using values from Table 1–41.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.

4. Record the time to V_{MEAS}.

5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Standard Output Adder delays to yield the actual worst-case propagation delay (clock-to-output) of the PCB trace.

The Quartus II software reports the timing with the conditions shown in Table 1–41 using the above equation. Figure 1–4 shows the model of the circuit that is represented by the output timing of the Quartus II software.

Figure 1–4. Output Delay Timing Reporting Setup Modeled by Quartus II Notes (1), (2)



Notes to Figure 1–4:
(1) Output pin timing is reported at the output pin of the FPGA device. Additional delays for loading and board trace delay need to be accounted for with IBIS model simulations.
(2) V_{CCINT} is 1.10 V unless otherwise specified.

Figure 1–5 and Figure 1–6 show the I/O interface with single and multiple external output resistors.

Figure 1–5. I/O Interface with Single External Output Resistor

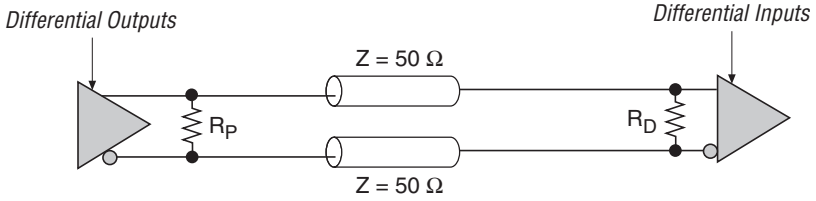


Figure 1–6. I/O Interface with Three External Output Resistor Network

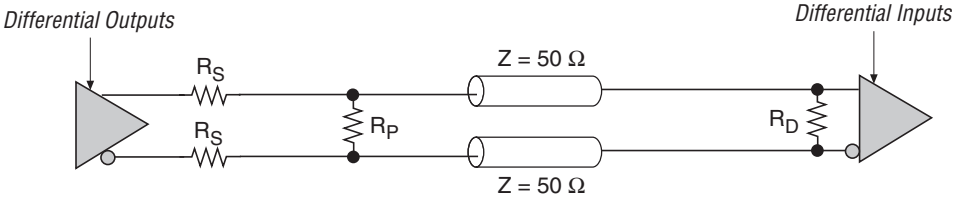


Table 1–41. Output Timing Measurement Methodology for Output Pins Notes (1), (2), (4), (5) **Preliminary**

I/O Standard	Loading and Termination							Measurement Point
	R_S (Ω)	R_T (Ω)	R_D (Ω)	R_P (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
3.3-V LVTTL	—	—	—	—	3.135	—	0	1.5675
3.3-V LVCMOS	—	—	—	—	3.135	—	0	1.5675
3.0-V LVTTL	—	—	—	—	2.85	—	0	1.425
3.0-V LVCMOS	—	—	—	—	2.85	—	0	1.425
2.5-V LVTTL/LVCMOS	—	—	—	—	2.375	—	0	1.1875
1.8-V LVTTL/LVCMOS	—	—	—	—	1.71	—	0	0.855
1.5-V LVCMOS	—	—	—	—	1.425	—	0	0.7125
1.2-V LVCMOS	—	—	—	—	1.15	—	0	0.575
3.0-V PCI	—	—	—	—	2.85	—	10	1.425
3.0-V PCI-X	—	—	—	—	2.85	—	10	1.425
SSTL-2 Class I	25	50	—	—	2.375	1.1875	0	1.1875
SSTL-2 Class II	25	25	—	—	2.375	1.1875	0	1.1875
SSTL-18 Class I	25	50	—	—	1.71	0.855	0	0.855
SSTL-18 Class II	25	25	—	—	1.71	0.855	0	0.855
1.8-V HSTL Class I	50	50	—	—	1.71	0.855	0	0.855
1.8-V HSTL Class II	25	25	—	—	1.71	0.855	0	0.855
1.5-V HSTL Class I	50	50	—	—	1.425	0.7125	0	0.7125
1.5-V HSTL Class II	—	25	—	—	1.425	0.7125	0	0.7125
1.2-V HSTL CLASS I	—	50	—	—	1.15	0.575	0	0.575
1.2-V HSTL CLASS II	—	25 (50 || 50)	—	—	1.15	0.575	0	0.575
LVDS	—	—	100	—	2.375	—	0	1.1875
LVDS_E_3R	120 *(6)*	—	100	170 *(6)*	2.375	—	0	1.1875
mini-LVDS	—	—	100	—	2.375	—	0	1.1875
mini-LVDS_E_3R	120 *(6)*	—	100	170 *(6)*	2.375	—	0	1.1875
PPDS	—	—	100	—	2.375	—	0	1.1875
PPDS_E_3R	120 *(6)*	—	100	170 *(6)*	2.375	—	0	1.1875
RSDS	—	—	100	—	2.375	—	0	1.1875
RSDS_E_1R	—	—	100	100 *(6)*	2.375	—	0	1.1875
RSDS_E_3R	120 *(6)*	—	100	170 *(6)*	2.375	—	0	1.1875

Notes to Table 1–41:

(1) Input measurement point at internal node is 0.5 × V_{CCINT}.
(2) Output measuring point for V_{MEAS} at buffer output is 0.5 × V_{CCIO}.
(3) Input stimulus edge rate is 0 to V_{CC} in 0.2 ns (internal signal) from the driver preceding the I/O buffer.
(4) Less than 50-mV ripple on V_{CCIO}. V_{CCINT} = 1.10 V with less than 30-mV ripple.
(5) The interface has to use external termination RT. The termination voltage V_{TT} may either be supplied by an independent power supply or created through a Thevenin equivalent circuit.
(6) Pending silicon characterization.

I/O Default Capacitive Loading

Refer to Table 1–42 for default capacitive loading of different I/O standards.

Table 1–42. Default Loading of Different I/O Standards for Cyclone III — Preliminary

I/O Standard	Capacitive Load	Unit
3.3-V LVTTL	0	pF
3.3-V LVCMOS	0	pF
3.0-V LVTTL	0	pF
3.0-V LVCMOS	0	pF
2.5-V LVTTL/LVCMOS	0	pF
1.8-V LVTTL/LVCMOS	0	pF
1.5-V LVCMOS	0	pF
1.2-V LVCMOS	0	pF
3.0-V PCI	10	pF
3.0-V PCI-X	10	pF
SSTL-2 Class I	0	pF
SSTL-2 Class II	0	pF
SSTL-18 Class I	0	pF
SSTL-18 Class II	0	pF
1.8-V HSTL Class I	0	pF
1.8-V HSTL Class II	0	pF
1.5-V HSTL Class I	0	pF
1.5-V HSTL Class II	0	pF
1.2-V HSTL CLASS I	0	pF
1.2-V HSTL CLASS II	0	pF
Differential SSTL-2 Class I	0	pF
Differential SSTL-2 Class II	0	pF
Differential SSTL-18 Class I	0	pF
Differential SSTL-18 Class II	0	pF
1.2-V Differential HSTL Class I	0	pF
1.2-V Differential HSTL Class II	0	pF
1.5-V Differential HSTL Class I	0	pF
1.5-V Differential HSTL Class II	0	pF
1.8-V Differential HSTL Class I	0	pF
1.8-V Differential HSTL Class II	0	pF
LVDS	0	pF
LVDS_E_3R	0	pF
mini-LVDS	0	pF
mini-LVDS_E_3R	0	pF
PPDS	0	pF
PPDS_E_3R	0	pF
RSDS	0	pF
RSDS_E_1R	0	pF
RSDS_E_3R	0	pF

Maximum Input and Output Clock Toggle Rate

The maximum clock toggle rate is defined as the maximum frequency achievable for a clock type signal at an I/O pin. The I/O pin can be a regular I/O pin or a dedicated clock I/O pin.

The maximum clock toggle rate is different from the maximum data bit rate. If the maximum clock toggle rate on a regular I/O pin is 300 MHz, the maximum data bit rate for dual data rate (DDR) could be potentially as high as 600 Mbps on the same I/O pin.

Table 1–43 specifies the maximum input clock toggle rates. Table 1–44 specifies the maximum output clock toggle rates at 0 pF load. Table 1–45 specifies the derating factors for the output clock toggle rate for a non 0 pF load.

To calculate the output toggle rate for a non 0 pF load, use this formula:

The toggle rate for a non 0 pF load

= 1000 / (1000/ toggle rate at 0 pF load + derating factor * load value in pF /1000)

For example, the output toggle rate at 0 pF load for SSTL-18 Class II 16 µA I/O standard is 260 MHz on a –6 device clock output pin. The derating factor is 26 ps/pF. For a 10 pF load the toggle rate is calculated as:

1000 / (1000/260 + 26 × 10 /1000) = 243 (MHz)

Table 1–43 through Table 1–45 show the I/O toggle rates for Cyclone III devices.

Table 1–43. Maximum Input Toggle Rate on Cyclone III Devices (Part 1 of 2) — **Preliminary**

I/O Standard	Maximum Input Toggle Rate on CIII Devices (MHz)								
	Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
3.3-V LVTTL	450	405	360	450	405	360	450	405	360
3.3-V LVCMOS	450	405	360	450	405	360	450	405	360
3.0-V LVTTL	450	405	360	450	405	360	450	405	360
3.0-V LVCMOS	450	405	360	450	405	360	450	405	360
2.5-V LVTTL/LVCMOS	450	405	360	450	405	360	450	405	360
1.8-V LVTTL/LVCMOS	450	405	360	450	405	360	450	405	360
1.5-V LVCMOS	300	270	240	300	270	240	300	270	240
1.2-V LVCMOS	300	270	240	300	270	240	300	270	240
SSTL_2_CLASS_I	500	500	500	500	500	500	500	500	500
SSTL_2_CLASS_II	500	500	500	500	500	500	500	500	500
SSTL_18_CLASS_I	500	500	500	500	500	500	500	500	500
SSTL_18_CLASS_II	500	500	500	500	500	500	500	500	500
1.8 V_HSTL_CLASS_I	500	500	500	500	500	500	500	500	500
1.8 V_HSTL_CLASS_II	500	500	500	500	500	500	500	500	500
1.5 V_HSTL_CLASS_I	500	500	500	500	500	500	500	500	500
1.5 V_HSTL_CLASS_II	500	500	500	500	500	500	500	500	500
1.2 V_HSTL_CLASS_I	500	500	500	500	500	500	500	500	500
1.2 V_HSTL_CLASS_II	500	500	500	*(1)*	*(1)*	*(1)*	500	500	500
3.0-V PCI	350	315	280	350	315	280	350	315	280

Table 1–43. Maximum Input Toggle Rate on Cyclone III Devices (Part 2 of 2) — Preliminary

I/O Standard	Maximum Input Toggle Rate on CIII Devices (MHz)								
	Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
3.0-V PCI-X	350	315	280	350	315	280	350	315	280
DIFFERENTIAL_SSTL_2_CLASS_I	(2)	(2)	(2)	(2)	(2)	(2)	500	500	500
DIFFERENTIAL_SSTL_2_CLASS_II	(2)	(2)	(2)	(2)	(2)	(2)	500	500	500
DIFFERENTIAL_SSTL_18_CLASS_I	(2)	(2)	(2)	(2)	(2)	(2)	500	500	500
DIFFERENTIAL_SSTL_18_CLASS_II	(2)	(2)	(2)	(2)	(2)	(2)	500	500	500
1.8 V_DIFFERENTIAL_HSTL_CLASS_I	(2)	(2)	(2)	(2)	(2)	(2)	500	500	500
1.8 V_DIFFERENTIAL_HSTL_CLASS_II	(2)	(2)	(2)	(2)	(2)	(2)	500	500	500
1.5 V_DIFFERENTIAL_HSTL_CLASS_I	(2)	(2)	(2)	(2)	(2)	(2)	500	500	500
1.5 V_DIFFERENTIAL_HSTL_CLASS_II	(2)	(2)	(2)	(2)	(2)	(2)	500	500	500
1.2 V_DIFFERENTIAL_HSTL_CLASS_I	(2)	(2)	(2)	(2)	(2)	(2)	500	500	500
1.2 V_DIFFERENTIAL_HSTL_CLASS_II	(2)	(2)	(2)	(2)	(2)	(2)	500	500	500
LVPECL	(3)	(3)	(3)	(3)	(3)	(3)	403	403	403
LVDS	403	403	403	438	438	438	403	403	403

Notes to Table 1–43:
(1) The 1.2 V_HSTL_CLASS_II is only supported on column I/O pins.
(2) Input differential standard is only supported on GCLK pin.
(3) Input LVPECL is only supported on GCLK pin.

Table 1–44. Maximum Output Toggle Rate on Cyclone III Devices (Part 1 of 4) — Preliminary

I/O Standard		Maximum Output Toggle Rate on CIII Devices (MHz)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
3.3-V LVTTL	4 mA	120	100	80	120	100	80	120	100	80
	8 mA	200	170	140	200	170	140	200	170	140
3.3-V LVCMOS	2 mA	120	100	80	120	100	80	120	100	80
3.0-V LVTTL	4 mA	185	155	125	100	86	70	185	155	125
	8 mA	220	190	150	170	145	120	220	190	150
	12 mA	300	245	200	240	200	160	300	245	200
	16 mA	311	260	215	250	205	170	311	260	215
3.0-V LVCMOS	4 mA	280	233	190	195	165	130	280	233	190
	8 mA	280	233	190	220	180	150	280	233	190
	12 mA	300	250	205	240	200	165	300	250	205
	16 mA	311	260	210	250	210	170	311	260	210

Table 1–44. Maximum Output Toggle Rate on Cyclone III Devices (Part 2 of 4) — **Preliminary**

I/O Standard		Maximum Output Toggle Rate on CIII Devices (MHz)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
2.5-V LVTTL/LVCMOS	4 mA	200	166	133	100	83	66	200	166	133
	8 mA	200	166	133	155	130	100	200	166	133
	12 mA	305	255	210	245	205	165	305	255	210
	16 mA	311	280	240	250	225	195	311	280	240
1.8-V LVTTL/LVCMOS	2 mA	210	170	140	85	70	60	210	170	140
	4 mA	255	210	170	130	110	85	255	210	170
	6 mA	285	233	195	160	130	110	285	233	195
	8 mA	250	210	166	170	140	115	250	210	166
	10 mA	266	220	185	215	180	150	266	220	185
	12 mA	311	260	210	250	210	170	311	260	210
	16 mA	311	260	210	250	210	170	311	260	210
1.5-V LVCMOS	2 mA	290	145	120	60	45	36	290	145	120
	4 mA	225	190	155	93	80	66	225	190	155
	6 mA	245	200	166	129	110	86	245	200	166
	8 mA	240	195	166	166	136	115	240	195	166
	10 mA	266	220	185	215	180	150	266	220	185
	12 mA	311	260	210	250	210	170	311	260	210
	16 mA	311	260	210	250	210	170	311	260	210
1.2-V LVCMOS	2 mA	190	145	120	66	50	40	190	145	120
	4 mA	225	190	155	110	90	75	225	190	155
	6 mA	245	200	166	150	125	100	245	200	166
	8 mA	240	197	166	192	160	133	240	197	166
	10 mA	266	220	185	250	210	175	266	220	185
	12 mA	311	260	210	*(2)*	*(2)*	*(2)*	311	260	210
SSTL_2_CLASS_I	8 mA	300	255	210	250	210	175	300	255	210
	12 mA	300	255	210	250	210	175	300	255	210
SSTL_2_CLASS_II	16 mA	300	250	205	250	205	170	300	250	205
SSTL_18_CLASS_I	8 mA	320	270	220	280	233	190	320	270	220
	10 mA	320	260	215	290	233	290	320	260	215
	12 mA	333	270	225	300	250	200	333	270	225
SSTL_18_CLASS_II	12 mA	333	280	233	266	233	190	333	280	233
	16 mA	333	280	233	300	250	210	333	280	233
1.8 V_HSTL_CLASS_I	8 mA	290	245	200	270	230	190	290	245	200
	10 mA	310	260	220	310	260	220	310	260	220
	12 mA	333	280	230	333	280	230	333	280	230
1.8 V_HSTL_CLASS_II	16 mA	333	275	233	300	250	210	333	275	233
1.5 V_HSTL_CLASS_I	8 mA	320	260	210	275	220	180	320	260	210
	10 mA	320	260	220	285	235	195	320	260	220
	12 mA	333	275	233	300	250	210	333	275	233
1.5 V_HSTL_CLASS_II	16 mA	333	270	222	300	240	200	333	270	222

Table 1–44. Maximum Output Toggle Rate on Cyclone III Devices (Part 3 of 4) — Preliminary

I/O Standard		Maximum Output Toggle Rate on CIII Devices (MHz)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
1.2 V_HSTL_CLASS_I	8 mA	240	190	160	250	205	160	240	190	160
	10 mA	240	195	160	250	205	160	240	195	160
	12 mA	250	210	175	*(2)*	*(2)*	*(2)*	250	210	175
1.2 V_HSTL_CLASS_II	14 mA	250	200	166	*(2)*	*(2)*	*(2)*	250	200	166
3.0-V PCI	—	133	120	106	133	120	105	133	120	106
3.0-V PCI-X	—	133	120	106	133	120	105	133	120	106
DIFFERENTIAL_SSTL_2_CLASS_I	8 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	400	340	280
	12 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	400	340	280
DIFFERENTIAL_SSTL_2_CLASS_II	16 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	350	290	240
DIFFERENTIAL_SSTL_18_CLASS_I	8 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	260	220	180
	10 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	270	220	180
	12 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	280	230	190
DIFFERENTIAL_SSTL_18_CLASS_II	16 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	260	220	180
1.8 V_DIFFERENTIAL_HSTL_CLASS_I	8 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	260	220	180
	10 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	300	250	210
	12 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	320	270	220
1.8 V_DIFFERENTIAL_HSTL_CLASS_II	16 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	230	190	160
1.5 V_DIFFERENTIAL_HSTL_CLASS_I	8 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	210	170	140
	10 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	220	180	150
	12 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	230	190	160
1.5 V_DIFFERENTIAL_HSTL_CLASS_II	16 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	210	170	140
1.2 V_DIFFERENTIAL_HSTL_CLASS_I	8 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	210	170	140
	10 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	220	180	150
	12 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	230	190	160
1.2 V_DIFFERENTIAL_HSTL_CLASS_II	14 mA	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	210	170	140
LVDS	—	*(6)*	*(6)*	*(6)*	438	370	305	438	370	305
LVDS_E_3R	—	350	300	245	*(5)*	*(5)*	*(5)*	438	370	305
mini-LVDS	—	*(4)*	*(4)*	*(4)*	200	170	140	200	170	140
mini-LVDS_E_3R	—	200	170	140	*(5)*	*(5)*	*(5)*	200	170	140
PPDS	—	*(4)*	*(4)*	*(4)*	220	187	154	220	187	154
PPDS_E_3R	—	220	187	154	*(5)*	*(5)*	*(5)*	220	187	154
RSDS	—	*(4)*	*(4)*	*(4)*	180	153	126	180	153	126
RSDS_E_1R	—	180	153	126	*(5)*	*(5)*	*(5)*	180	153	126
RSDS_E_3R	—	180	153	126	*(5)*	*(5)*	*(5)*	180	153	126
3.0-V LVTTL/LVCMOS	OCT_25_OHMS	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*
	OCT_50_OHMS	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*

Table 1–44. Maximum Output Toggle Rate on Cyclone III Devices (Part 4 of 4) — Preliminary

I/O Standard		Maximum Output Toggle Rate on CIII Devices (MHz)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
2.5-V LVTTL/LVCMOS	OCT_25_OHMS	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
	OCT_50_OHMS	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
1.8-V LVTTL/LVCMOS	OCT_25_OHMS	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
	OCT_50_OHMS	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
1.2-V LVTTL/LVCMOS	OCT_25_OHMS	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
	OCT_50_OHMS	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)

Notes to Table 1–44:
(1) The current version of the Quartus II software does not have the information for the standard.
(2) The 1.2 V (12 mA) and 1.2 V_HSTL_CLASS_I / II (12 mA and 14 mA respectively) are only supported on column I/O pins.
(3) Output differential standard is only supported on PLLCLKOUT pin.
(4) Dedicated differential standards are supported at row I/O pins.
(5) Differential standards with external resistor network are supported at column I/O pins.
(6) Output dedicated LVDS is only supported on row I/O pins. Input dedicated LVDS is supported at all I/O pins.

Table 1–45. Maximum Output Clock Toggle Rate Derating Factors on Cyclone III Devices (Part 1 of 3) — Preliminary

I/O Standard	Current Strength or OCT Setting	Maximum Output Clock Toggle Rate Derating Factors (ps/pf)					
		Column I/O Pins			Row I/O Pins		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
3.3-V LVTTL	4 mA	117	123	123	116	122	122
	8 mA	50	52	52	50	52	52
3.3V LVCMOS	2 mA	(1)	(1)	(1)	(1)	(1)	(1)
3.0-V LVTTL	4 mA	(1)	(1)	(1)	(1)	(1)	(1)
	8 mA	(1)	(1)	(1)	(1)	(1)	(1)
	12 mA	(1)	(1)	(1)	(1)	(1)	(1)
	16 mA	(1)	(1)	(1)	(1)	(1)	(1)
3.0-V LVCMOS	4 mA	(1)	(1)	(1)	(1)	(1)	(1)
	8 mA	(1)	(1)	(1)	(1)	(1)	(1)
	12 mA	(1)	(1)	(1)	(1)	(1)	(1)
	16 mA	(1)	(1)	(1)	(1)	(1)	(1)

Table 1–45. Maximum Output Clock Toggle Rate Derating Factors on Cyclone III Devices (Part 2 of 3) — Preliminary

I/O Standard	Current Strength or OCT Setting	Maximum Output Clock Toggle Rate Derating Factors (ps/pf)					
		Column I/O Pins			Row I/O Pins		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
2.5-V LVTTL/LVCMOS	4 mA	36	37	37	35	37	37
	8 mA	30	32	32	30	32	32
	12 mA	27	28	28	(1)	(1)	(1)
	16 mA	26	27	27	(1)	(1)	(1)
1.8-V LVTTL/LVCMOS	2 mA	115	121	121	116	121	121
	4 mA	93	97	97	91	96	96
	6 mA	48	50	50	47	50	50
	8 mA	39	41	41	39	41	41
	10 mA	36	37	37	35	37	37
	12 mA	33	35	35	33	34	34
	16 mA	(1)	(1)	(1)	(1)	(1)	(1)
1.5-V LVCMOS	2 mA	164	172	172	164	172	172
	4 mA	92	96	96	91	96	96
	6 mA	44	46	46	43	45	45
	8 mA	37	39	39	(1)	(1)	(1)
	10 mA	(1)	(1)	(1)	(1)	(1)	(1)
	12 mA	(1)	(1)	(1)	(1)	(1)	(1)
	16 mA	(1)	(1)	(1)	(1)	(1)	(1)
1.2-V LVCMOS	2 mA	(1)	(1)	(1)	(1)	(1)	(1)
	4 mA	(1)	(1)	(1)	(1)	(1)	(1)
	6 mA	(1)	(1)	(1)	(1)	(1)	(1)
	8 mA	(1)	(1)	(1)	(1)	(1)	(1)
	10 mA	(1)	(1)	(1)	(1)	(1)	(1)
	12 mA	(1)	(1)	(1)	(2)	(2)	(2)
SSTL_2_CLASS_I	8 mA	26	27	27	25	27	27
	12 mA	25	26	26	25	26	26
SSTL_2_CLASS_II	16 mA	28	29	29	27	28	28
SSTL_18_CLASS_I	8 mA	24	25	25	23	24	24
	10 mA	23	24	24	24	25	25
	12 mA	24	25	25	(1)	(1)	(1)
SSTL_18_ CLASS_II	16 mA	26	27	27	(1)	(1)	(1)
	18 mA	26	27	27	(1)	(1)	(1)
1.8 V_HSTL_ CLASS_I	8 mA	24	25	25	25	26	26
	10 mA	26	27	27	23	24	24
	12 mA	26	28	28	25	26	26
1.8 V_HSTL_ CLASS_II	12 mA	(1)	(1)	(1)	(1)	(1)	(1)
	16 mA	30	31	31	(1)	(1)	(1)

Table 1–45. Maximum Output Clock Toggle Rate Derating Factors on Cyclone III Devices (Part 3 of 3) — Preliminary

I/O Standard	Current Strength or OCT Setting	Maximum Output Clock Toggle Rate Derating Factors (ps/pf)					
		Column I/O Pins			Row I/O Pins		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
1.5 V_HSTL_ CLASS_I	8 mA	26	28	28	25	26	26
	10 mA	25	27	27	(1)	(1)	(1)
	12 mA	25	26	26	(1)	(1)	(1)
1.5 V_HSTL_ CLASS_II	16 mA	31	33	33	(1)	(1)	(1)
1.2 V_HSTL_ CLASS_I	8 mA	(1)	(1)	(1)	(1)	(1)	(1)
	10 mA	(1)	(1)	(1)	(1)	(1)	(1)
	12 mA	(1)	(1)	(1)	(2)	(2)	(2)
1.2 V_HSTL_ CLASS_II	14 mA	(1)	(1)	(1)	(2)	(2)	(2)
3.0-V PCI	—	(1)	(1)	(1)	(1)	(1)	(1)
3.0-V PCI-X	—	(1)	(1)	(1)	(1)	(1)	(1)
LVDS	—	(6)	(6)	(6)	39	41	41
LVDS_E_3R	—	(1)	(1)	(1)	(5)	(5)	(5)
mini-LVDS	—	(4)	(4)	(4)	(1)	(1)	(1)
mini-LVDS_E_3R	—	(1)	(1)	(1)	(5)	(5)	(5)
PPDS	—	(4)	(4)	(4)	(1)	(1)	(1)
PPDS_E_3R	—	(1)	(1)	(1)	(5)	(5)	(5)
RSDS	—	(4)	(4)	(4)	(1)	(1)	(1)
RSDS_E_1R	—	(1)	(1)	(1)	(5)	(5)	(5)
RSDS_E_3R	—	(1)	(1)	(1)	(5)	(5)	(5)
3.0-V	OCT_25_OHMS	(1)	(1)	(1)	(1)	(1)	(1)
	OCT_50_OHMS	(1)	(1)	(1)	(1)	(1)	(1)
2.5-V LVTTL/LVCMOS	OCT_25_OHMS	(1)	(1)	(1)	(1)	(1)	(1)
	OCT_50_OHMS	240	200	160	240	200	160
1.8-V LVTTL/LVCMOS	OCT_25_OHMS	(1)	(1)	(1)	(1)	(1)	(1)
	OCT_50_OHMS	290	240	200	290	240	200
1.2-V LVCMOS	OCT_25_OHMS	(1)	(1)	(1)	(1)	(1)	(1)
	OCT_50_OHMS	(1)	(1)	(1)	(1)	(1)	(1)

Notes to Table 1–45:

(1) Current version of Quartus II software does not have the information for the standard.
(2) The 1.2 V (12 mA) and 1.2 V_HSTL_CLASS_I/II (12 mA and 14 mA, respectively) are only supported on column I/O pins.
(3) Output differential standard is only supported on `PLLCLKOUT` pin.
(4) Dedicated differential standards are supported at row I/O pins.
(5) Differential standards with external resistor network are supported at column I/O pins.
(6) Output dedicated LVDS is only supported on row I/O pins. Input dedicated LVDS is supported at all I/O pins.
(7) Indicate the lowest value of derating factor.

IOE Programmable Delay

Table 1–46 and Table 1–47 show IOE programmable delay for Cyclone III devices.

Table 1–46. Cyclone III IOE Programmable Delay on Column Pins Notes (1), (2)

Parameter	Paths Affected	Number of Settings	Fast Corner (3)		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input Delay from Pin to Internal Cells	Pad to I/O dataout to core	7	0	1.369	0	2.267	0	2.413	0	2.526	ns
Input Delay from Pin to Input Register	Pad to I/O input register	8	0	1.528	0	2.446	0	2.571	0	2.696	ns
Delay from Output Register to Output Pin	I/O output register to Pad	2	0	0.582	0	1	0	1.098	0	1.199	ns

Notes to Table 1–46:
(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.
(2) The minimum and maximum offset timing numbers are in reference to setting "0" as available in the Quartus II software.
(3) The fast model timing parameter is for commercial devices.

Table 1–47. Cyclone III IOE Programmable Delay on Row Pins Notes (1), (2)

Parameter	Paths Affected	Number of Settings	Fast Corner (3)		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input Delay from Pin to Internal Cells	Pad to I/O dataout to core	7	0	1.369	0	2.244	0	2.39	0	2.495	ns
Input Delay from Pin to Input Register	Pad to I/O input register	8	0	1.538	0	2.459	0	2.586	0	2.716	ns
Delay from Output Register to Output Pin	I/O output register to Pad	2	0	0.62	0	1.065	0	1.171	0	1.277	ns

Notes to Table 1–47:
(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.
(2) The minimum and maximum offset timing numbers are in reference to setting "0" as available in the Quartus II software.
(3) The fast model timing parameter is for commercial devices.

Typical Design Performance

User I/O Pin Timing Parameters

Table 1–48 to Table 1–95 show user I/O pin timing for Cyclone III devices. I/O buffer t_{SU}, t_H and t_{CO} are reported for the cases when clock is driven by global clock and a PLL.

The 12 µA programmable current strength for 1.2 V and 1.2-V HSTL Class I I/O standard is not supported at row I/Os. The 1.2-V HSTL Class II standard is only supported at column I/Os. PCI and PCI-X do not support programmable current strength.

For more information about programmable current strength, refer to the *Cyclone III Device I/O Features* chapter of the *Cyclone III Handbook*.

Dedicated LVDS, mini-LVDS, PPDS, and RSDS I/O standards are supported at row I/Os. External resistor networks are required if the differential standards are used as output pins at column banks. LVDS I/O standard is supported at both input and output pins. PPDS, RSDS, and mini-LVDS standards are only supported at output pins.

For more information about the differential I/O interface, refer to *High-Speed Differential Interfaces in Cyclone III Devices* of the *Cyclone III Handbook*.

EP3C5 I/O Timing Parameters

Table 1–48 through Table 1–53 show the maximum I/O timing parameters for EP3C5 devices.

Table 1–48. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
	8 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
	8 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
	12 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
	16 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
	8 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns

Table 1–48. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	12 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
	16 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
2.5V	4 mA	GCLK	t_{SU}	1.066	1.111	1.135	ns
			t_H	–0.786	–0.794	–0.782	ns
		GCLK PLL	t_{SU}	2.912	3.133	3.336	ns
			t_H	–2.632	–2.816	–2.983	ns
	8 mA	GCLK	t_{SU}	1.066	1.111	1.135	ns
			t_H	–0.786	–0.794	–0.782	ns
		GCLK PLL	t_{SU}	2.912	3.133	3.336	ns
			t_H	–2.632	–2.816	–2.983	ns
	12 mA	GCLK	t_{SU}	1.066	1.111	1.135	ns
			t_H	–0.786	–0.794	–0.782	ns
		GCLK PLL	t_{SU}	2.912	3.133	3.336	ns
			t_H	–2.632	–2.816	–2.983	ns
	16 mA	GCLK	t_{SU}	1.066	1.111	1.135	ns
			t_H	–0.786	–0.794	–0.782	ns
		GCLK PLL	t_{SU}	2.912	3.133	3.336	ns
			t_H	–2.632	–2.816	–2.983	ns
1.8V	2 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.847	3.094	3.323	ns
			t_H	–2.569	–2.778	–2.969	ns
	4 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.847	3.094	3.323	ns
			t_H	–2.569	–2.778	–2.969	ns
	6 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.847	3.094	3.323	ns
			t_H	–2.569	–2.778	–2.969	ns
	8 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.847	3.094	3.323	ns
			t_H	–2.569	–2.778	–2.969	ns

Table 1–48. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	10 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.847	3.094	3.323	ns
			t_H	–2.569	–2.778	–2.969	ns
	12 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.847	3.094	3.323	ns
			t_H	–2.569	–2.778	–2.969	ns
	16 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.847	3.094	3.323	ns
			t_H	–2.569	–2.778	–2.969	ns
1.5V	2 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.916	3.186	3.440	ns
			t_H	–2.636	–2.868	–3.084	ns
	4 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.916	3.186	3.440	ns
			t_H	–2.636	–2.868	–3.084	ns
	6 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.916	3.186	3.440	ns
			t_H	–2.636	–2.868	–3.084	ns
	8 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.916	3.186	3.440	ns
			t_H	–2.636	–2.868	–3.084	ns
	10 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.916	3.186	3.440	ns
			t_H	–2.636	–2.868	–3.084	ns
	12 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.916	3.186	3.440	ns
			t_H	–2.636	–2.868	–3.084	ns
	16 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.916	3.186	3.440	ns
			t_H	–2.636	–2.868	–3.084	ns

Table 1–48. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	2 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.068	3.366	3.646	ns
			t_H	–2.786	–3.044	–3.286	ns
	4 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.068	3.366	3.646	ns
			t_H	–2.786	–3.044	–3.286	ns
	6 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.068	3.366	3.646	ns
			t_H	–2.786	–3.044	–3.286	ns
	8 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.068	3.366	3.646	ns
			t_H	–2.786	–3.044	–3.286	ns
	10 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.068	3.366	3.646	ns
			t_H	–2.786	–3.044	–3.286	ns
	12 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.068	3.366	3.646	ns
			t_H	–2.786	–3.044	–3.286	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	1.057	1.133	1.188	ns
			t_H	–0.777	–0.816	–0.833	ns
		GCLK PLL	t_{SU}	2.901	3.151	3.385	ns
			t_H	–2.621	–2.834	–3.030	ns
	12 mA	GCLK	t_{SU}	1.057	1.133	1.188	ns
			t_H	–0.777	–0.816	–0.833	ns
		GCLK PLL	t_{SU}	2.901	3.151	3.385	ns
			t_H	–2.621	–2.834	–3.030	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	1.057	1.133	1.188	ns
			t_H	–0.777	–0.816	–0.833	ns
		GCLK PLL	t_{SU}	2.901	3.151	3.385	ns
			t_H	–2.621	–2.834	–3.030	ns

Table 1–48. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.118	1.222	1.303	ns
			t_H	–0.838	–0.903	–0.946	ns
		GCLK PLL	t_{SU}	2.962	3.240	3.500	ns
			t_H	–2.682	–2.921	–3.143	ns
	10 mA	GCLK	t_{SU}	1.118	1.222	1.303	ns
			t_H	–0.838	–0.903	–0.946	ns
		GCLK PLL	t_{SU}	2.962	3.240	3.500	ns
			t_H	–2.682	–2.921	–3.143	ns
	12 mA	GCLK	t_{SU}	1.118	1.222	1.303	ns
			t_H	–0.838	–0.903	–0.946	ns
		GCLK PLL	t_{SU}	2.962	3.240	3.500	ns
			t_H	–2.682	–2.921	–3.143	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.118	1.222	1.303	ns
			t_H	–0.838	–0.903	–0.946	ns
		GCLK PLL	t_{SU}	2.962	3.240	3.500	ns
			t_H	–2.682	–2.921	–3.143	ns
	16 mA	GCLK	t_{SU}	1.118	1.222	1.303	ns
			t_H	–0.838	–0.903	–0.946	ns
		GCLK PLL	t_{SU}	2.962	3.240	3.500	ns
			t_H	–2.682	–2.921	–3.143	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.118	1.222	1.303	ns
			t_H	–0.838	–0.903	–0.946	ns
		GCLK PLL	t_{SU}	2.962	3.240	3.500	ns
			t_H	–2.682	–2.921	–3.143	ns
	10 mA	GCLK	t_{SU}	1.118	1.222	1.303	ns
			t_H	–0.838	–0.903	–0.946	ns
		GCLK PLL	t_{SU}	2.962	3.240	3.500	ns
			t_H	–2.682	–2.921	–3.143	ns
	12 mA	GCLK	t_{SU}	1.118	1.222	1.303	ns
			t_H	–0.838	–0.903	–0.946	ns
		GCLK PLL	t_{SU}	2.962	3.240	3.500	ns
			t_H	–2.682	–2.921	–3.143	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.118	1.222	1.303	ns
			t_H	–0.838	–0.903	–0.946	ns
		GCLK PLL	t_{SU}	2.962	3.240	3.500	ns
			t_H	–2.682	–2.921	–3.143	ns

Table 1–48. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	1.074	1.182	1.269	ns
			t_H	–0.794	–0.864	–0.913	ns
		GCLK PLL	t_{SU}	2.918	3.200	3.466	ns
			t_H	–2.638	–2.882	–3.110	ns
	10 mA	GCLK	t_{SU}	1.074	1.182	1.269	ns
			t_H	–0.794	–0.864	–0.913	ns
		GCLK PLL	t_{SU}	2.918	3.200	3.466	ns
			t_H	–2.638	–2.882	–3.110	ns
	12 mA	GCLK	t_{SU}	1.074	1.182	1.269	ns
			t_H	–0.794	–0.864	–0.913	ns
		GCLK PLL	t_{SU}	2.918	3.200	3.466	ns
			t_H	–2.638	–2.882	–3.110	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	1.074	1.182	1.269	ns
			t_H	–0.794	–0.864	–0.913	ns
		GCLK PLL	t_{SU}	2.918	3.200	3.466	ns
			t_H	–2.638	–2.882	–3.110	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.206	1.341	1.453	ns
			t_H	–0.924	–1.019	–1.093	ns
		GCLK PLL	t_{SU}	3.050	3.359	3.650	ns
			t_H	–2.768	–3.037	–3.290	ns
	10 mA	GCLK	t_{SU}	1.206	1.341	1.453	ns
			t_H	–0.924	–1.019	–1.093	ns
		GCLK PLL	t_{SU}	3.050	3.359	3.650	ns
			t_H	–2.768	–3.037	–3.290	ns
	12 mA	GCLK	t_{SU}	1.206	1.341	1.453	ns
			t_H	–0.924	–1.019	–1.093	ns
		GCLK PLL	t_{SU}	3.050	3.359	3.650	ns
			t_H	–2.768	–3.037	–3.290	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	1.206	1.341	1.453	ns
			t_H	–0.924	–1.019	–1.093	ns
		GCLK PLL	t_{SU}	3.050	3.359	3.650	ns
			t_H	–2.768	–3.037	–3.290	ns
3.0-V PCI	—	GCLK	t_{SU}	1.119	1.152	1.162	ns
			t_H	–0.839	–0.834	–0.808	ns
	—	GCLK PLL	t_{SU}	2.965	3.174	3.363	ns
			t_H	–2.685	–2.856	–3.009	ns
3.0-V PCI-X	—	GCLK	t_{SU}	1.119	1.152	1.162	ns
			t_H	–0.839	–0.834	–0.808	ns
	—	GCLK PLL	t_{SU}	2.965	3.174	3.363	ns
			t_H	–2.685	–2.856	–3.009	ns

Table 1–49. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
	8 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
	8 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
	12 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
	16 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
	8 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns

Table 1–49. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	12 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
	16 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
2.5V	4 mA	GCLK	t_{SU}	1.091	1.142	1.176	ns
			t_H	–0.811	–0.825	–0.822	ns
		GCLK PLL	t_{SU}	2.940	3.222	3.435	ns
			t_H	–2.660	–2.905	–3.081	ns
	8 mA	GCLK	t_{SU}	1.091	1.142	1.176	ns
			t_H	–0.811	–0.825	–0.822	ns
		GCLK PLL	t_{SU}	2.940	3.222	3.435	ns
			t_H	–2.660	–2.905	–3.081	ns
	12 mA	GCLK	t_{SU}	1.091	1.142	1.176	ns
			t_H	–0.811	–0.825	–0.822	ns
		GCLK PLL	t_{SU}	2.940	3.222	3.435	ns
			t_H	–2.660	–2.905	–3.081	ns
	16 mA	GCLK	t_{SU}	1.091	1.142	1.176	ns
			t_H	–0.811	–0.825	–0.822	ns
		GCLK PLL	t_{SU}	2.940	3.222	3.435	ns
			t_H	–2.660	–2.905	–3.081	ns

Table 1–49. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	2 mA	GCLK	t_{SU}	1.012	1.088	1.147	ns
			t_H	–0.734	–0.772	–0.792	ns
		GCLK PLL	t_{SU}	2.876	3.183	3.421	ns
			t_H	–2.598	–2.867	–3.066	ns
	4 mA	GCLK	t_{SU}	1.012	1.088	1.147	ns
			t_H	–0.734	–0.772	–0.792	ns
		GCLK PLL	t_{SU}	2.876	3.183	3.421	ns
			t_H	–2.598	–2.867	–3.066	ns
	6 mA	GCLK	t_{SU}	1.012	1.088	1.147	ns
			t_H	–0.734	–0.772	–0.792	ns
		GCLK PLL	t_{SU}	2.876	3.183	3.421	ns
			t_H	–2.598	–2.867	–3.066	ns
	8 mA	GCLK	t_{SU}	1.012	1.088	1.147	ns
			t_H	–0.734	–0.772	–0.792	ns
		GCLK PLL	t_{SU}	2.876	3.183	3.421	ns
			t_H	–2.598	–2.867	–3.066	ns
	10 mA	GCLK	t_{SU}	1.012	1.088	1.147	ns
			t_H	–0.734	–0.772	–0.792	ns
		GCLK PLL	t_{SU}	2.876	3.183	3.421	ns
			t_H	–2.598	–2.867	–3.066	ns
	12 mA	GCLK	t_{SU}	1.012	1.088	1.147	ns
			t_H	–0.734	–0.772	–0.792	ns
		GCLK PLL	t_{SU}	2.876	3.183	3.421	ns
			t_H	–2.598	–2.867	–3.066	ns
	16 mA	GCLK	t_{SU}	1.012	1.088	1.147	ns
			t_H	–0.734	–0.772	–0.792	ns
		GCLK PLL	t_{SU}	2.876	3.183	3.421	ns
			t_H	–2.598	–2.867	–3.066	ns
1.5V	2 mA	GCLK	t_{SU}	1.081	1.181	1.265	ns
			t_H	–0.801	–0.863	–0.909	ns
		GCLK PLL	t_{SU}	2.945	3.276	3.539	ns
			t_H	–2.665	–2.958	–3.183	ns
	4 mA	GCLK	t_{SU}	1.081	1.181	1.265	ns
			t_H	–0.801	–0.863	–0.909	ns
		GCLK PLL	t_{SU}	2.945	3.276	3.539	ns
			t_H	–2.665	–2.958	–3.183	ns
	6 mA	GCLK	t_{SU}	1.081	1.181	1.265	ns
			t_H	–0.801	–0.863	–0.909	ns
		GCLK PLL	t_{SU}	2.945	3.276	3.539	ns
			t_H	–2.665	–2.958	–3.183	ns

Table 1–49. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	8 mA	GCLK	t_{SU}	1.081	1.181	1.265	ns
			t_H	–0.801	–0.863	–0.909	ns
		GCLK PLL	t_{SU}	2.945	3.276	3.539	ns
			t_H	–2.665	–2.958	–3.183	ns
	10 mA	GCLK	t_{SU}	1.081	1.181	1.265	ns
			t_H	–0.801	–0.863	–0.909	ns
		GCLK PLL	t_{SU}	2.945	3.276	3.539	ns
			t_H	–2.665	–2.958	–3.183	ns
	12 mA	GCLK	t_{SU}	1.081	1.181	1.265	ns
			t_H	–0.801	–0.863	–0.909	ns
		GCLK PLL	t_{SU}	2.945	3.276	3.539	ns
			t_H	–2.665	–2.958	–3.183	ns
	16 mA	GCLK	t_{SU}	1.081	1.181	1.265	ns
			t_H	–0.801	–0.863	–0.909	ns
		GCLK PLL	t_{SU}	2.945	3.276	3.539	ns
			t_H	–2.665	–2.958	–3.183	ns
1.2V	2 mA	GCLK	t_{SU}	1.234	1.361	1.472	ns
			t_H	–0.952	–1.039	–1.111	ns
		GCLK PLL	t_{SU}	3.098	3.456	3.746	ns
			t_H	–2.816	–3.134	–3.385	ns
	4 mA	GCLK	t_{SU}	1.234	1.361	1.472	ns
			t_H	–0.952	–1.039	–1.111	ns
		GCLK PLL	t_{SU}	3.098	3.456	3.746	ns
			t_H	–2.816	–3.134	–3.385	ns
	6 mA	GCLK	t_{SU}	1.234	1.361	1.472	ns
			t_H	–0.952	–1.039	–1.111	ns
		GCLK PLL	t_{SU}	3.098	3.456	3.746	ns
			t_H	–2.816	–3.134	–3.385	ns
	8 mA	GCLK	t_{SU}	1.234	1.361	1.472	ns
			t_H	–0.952	–1.039	–1.111	ns
		GCLK PLL	t_{SU}	3.098	3.456	3.746	ns
			t_H	–2.816	–3.134	–3.385	ns
	10 mA	GCLK	t_{SU}	1.234	1.361	1.472	ns
			t_H	–0.952	–1.039	–1.111	ns
		GCLK PLL	t_{SU}	3.098	3.456	3.746	ns
			t_H	–2.816	–3.134	–3.385	ns

Table 1–49. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-2 Class I	8 mA	GCLK	t_{SU}	1.081	1.161	1.224	ns
			t_H	–0.801	–0.843	–0.868	ns
		GCLK PLL	t_{SU}	2.930	3.184	3.480	ns
			t_H	–2.650	–2.866	–3.124	ns
	12 mA	GCLK	t_{SU}	1.081	1.161	1.224	ns
			t_H	–0.801	–0.843	–0.868	ns
		GCLK PLL	t_{SU}	2.930	3.184	3.480	ns
			t_H	–2.650	–2.866	–3.124	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	1.081	1.161	1.224	ns
			t_H	–0.801	–0.843	–0.868	ns
		GCLK PLL	t_{SU}	2.930	3.184	3.480	ns
			t_H	–2.650	–2.866	–3.124	ns
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.128	1.235	1.326	ns
			t_H	–0.848	–0.916	–0.968	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.597	ns
			t_H	–2.712	–2.954	–3.239	ns
	10 mA	GCLK	t_{SU}	1.128	1.235	1.326	ns
			t_H	–0.848	–0.916	–0.968	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.597	ns
			t_H	–2.712	–2.954	–3.239	ns
	12 mA	GCLK	t_{SU}	1.128	1.235	1.326	ns
			t_H	–0.848	–0.916	–0.968	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.597	ns
			t_H	–2.712	–2.954	–3.239	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.128	1.235	1.326	ns
			t_H	–0.848	–0.916	–0.968	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.597	ns
			t_H	–2.712	–2.954	–3.239	ns
	16 mA	GCLK	t_{SU}	1.128	1.235	1.326	ns
			t_H	–0.848	–0.916	–0.968	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.597	ns
			t_H	–2.712	–2.954	–3.239	ns

Table 1–49. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.128	1.235	1.326	ns
			t_H	–0.848	–0.916	–0.968	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.597	ns
			t_H	–2.712	–2.954	–3.239	ns
	10 mA	GCLK	t_{SU}	1.128	1.235	1.326	ns
			t_H	–0.848	–0.916	–0.968	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.597	ns
			t_H	–2.712	–2.954	–3.239	ns
	12 mA	GCLK	t_{SU}	1.128	1.235	1.326	ns
			t_H	–0.848	–0.916	–0.968	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.597	ns
			t_H	–2.712	–2.954	–3.239	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.128	1.235	1.326	ns
			t_H	–0.848	–0.916	–0.968	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.597	ns
			t_H	–2.712	–2.954	–3.239	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	1.083	1.194	1.289	ns
			t_H	–0.803	–0.876	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.232	3.560	ns
			t_H	–2.667	–2.914	–3.203	ns
	10 mA	GCLK	t_{SU}	1.083	1.194	1.289	ns
			t_H	–0.803	–0.876	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.232	3.560	ns
			t_H	–2.667	–2.914	–3.203	ns
	12 mA	GCLK	t_{SU}	1.083	1.194	1.289	ns
			t_H	–0.803	–0.876	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.232	3.560	ns
			t_H	–2.667	–2.914	–3.203	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	1.083	1.194	1.289	ns
			t_H	–0.803	–0.876	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.232	3.560	ns
			t_H	–2.667	–2.914	–3.203	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.214	1.352	1.474	ns
			t_H	–0.932	–1.030	–1.114	ns
		GCLK PLL	t_{SU}	3.078	3.390	3.745	ns
			t_H	–2.796	–3.068	–3.385	ns
	10 mA	GCLK	t_{SU}	1.214	1.352	1.474	ns
			t_H	–0.932	–1.030	–1.114	ns
		GCLK PLL	t_{SU}	3.078	3.390	3.745	ns
			t_H	–2.796	–3.068	–3.385	ns

Table 1–49. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V PCI	—	GCLK	t_{SU}	1.144	1.182	1.201	ns
			t_{H}	–0.864	–0.864	–0.846	ns
	—	GCLK PLL	t_{SU}	2.993	3.262	3.460	ns
			t_{H}	–2.713	–2.944	–3.105	ns
3.0-V PCI-X	—	GCLK	t_{SU}	1.144	1.182	1.201	ns
			t_{H}	–0.864	–0.864	–0.846	ns
	—	GCLK PLL	t_{SU}	2.993	3.262	3.460	ns
			t_{H}	–2.713	–2.944	–3.105	ns

Table 1–50. EP3C5 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.365	5.861	6.384	ns
		GCLK PLL	t_{CO}	3.516	3.838	4.183	ns
	8 mA	GCLK	t_{CO}	5.365	5.861	6.384	ns
		GCLK PLL	t_{CO}	3.516	3.838	4.183	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.324	5.642	5.986	ns
		GCLK PLL	t_{CO}	3.475	3.619	3.785	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.075	5.564	6.082	ns
		GCLK PLL	t_{CO}	3.226	3.541	3.881	ns
	8 mA	GCLK	t_{CO}	4.804	5.280	5.783	ns
		GCLK PLL	t_{CO}	2.955	3.257	3.582	ns
	12 mA	GCLK	t_{CO}	4.707	5.179	5.679	ns
		GCLK PLL	t_{CO}	2.858	3.156	3.478	ns
	16 mA	GCLK	t_{CO}	4.660	5.127	5.621	ns
		GCLK PLL	t_{CO}	2.811	3.104	3.420	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.802	5.277	5.780	ns
		GCLK PLL	t_{CO}	2.953	3.254	3.579	ns
	8 mA	GCLK	t_{CO}	4.661	5.129	5.625	ns
		GCLK PLL	t_{CO}	2.812	3.106	3.424	ns
	12 mA	GCLK	t_{CO}	4.624	5.089	5.582	ns
		GCLK PLL	t_{CO}	2.775	3.066	3.381	ns
	16 mA	GCLK	t_{CO}	4.608	5.074	5.567	ns
		GCLK PLL	t_{CO}	2.759	3.051	3.366	ns

Table 1–50. EP3C5 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
2.5V	4 mA	GCLK	t_{CO}	5.133	5.650	6.196	ns
		GCLK PLL	t_{CO}	3.284	3.627	3.995	ns
	8 mA	GCLK	t_{CO}	4.890	5.397	5.932	ns
		GCLK PLL	t_{CO}	3.041	3.374	3.731	ns
	12 mA	GCLK	t_{CO}	4.792	5.291	5.819	ns
		GCLK PLL	t_{CO}	2.943	3.268	3.618	ns
	16 mA	GCLK	t_{CO}	4.753	5.251	5.778	ns
		GCLK PLL	t_{CO}	2.904	3.228	3.577	ns
1.8V	2 mA	GCLK	t_{CO}	6.244	6.903	7.594	ns
		GCLK PLL	t_{CO}	4.395	4.880	5.393	ns
	4 mA	GCLK	t_{CO}	5.717	6.358	7.030	ns
		GCLK PLL	t_{CO}	3.868	4.335	4.829	ns
	6 mA	GCLK	t_{CO}	5.492	6.100	6.738	ns
		GCLK PLL	t_{CO}	3.643	4.077	4.537	ns
	8 mA	GCLK	t_{CO}	5.389	5.983	6.609	ns
		GCLK PLL	t_{CO}	3.540	3.960	4.408	ns
	10 mA	GCLK	t_{CO}	5.337	5.935	6.563	ns
		GCLK PLL	t_{CO}	3.488	3.912	4.362	ns
	12 mA	GCLK	t_{CO}	5.280	5.868	6.488	ns
		GCLK PLL	t_{CO}	3.431	3.845	4.287	ns
	16 mA	GCLK	t_{CO}	5.226	5.809	6.423	ns
		GCLK PLL	t_{CO}	3.377	3.786	4.222	ns
1.5V	2 mA	GCLK	t_{CO}	6.632	7.465	8.333	ns
		GCLK PLL	t_{CO}	4.783	5.442	6.132	ns
	4 mA	GCLK	t_{CO}	6.157	6.904	7.685	ns
		GCLK PLL	t_{CO}	4.308	4.881	5.484	ns
	6 mA	GCLK	t_{CO}	5.987	6.721	7.488	ns
		GCLK PLL	t_{CO}	4.138	4.698	5.287	ns
	8 mA	GCLK	t_{CO}	5.899	6.608	7.350	ns
		GCLK PLL	t_{CO}	4.050	4.585	5.149	ns
	10 mA	GCLK	t_{CO}	5.840	6.548	7.289	ns
		GCLK PLL	t_{CO}	3.991	4.525	5.088	ns
	12 mA	GCLK	t_{CO}	5.807	6.507	7.239	ns
		GCLK PLL	t_{CO}	3.958	4.484	5.038	ns
	16 mA	GCLK	t_{CO}	5.693	6.365	7.069	ns
		GCLK PLL	t_{CO}	3.844	4.342	4.868	ns

Table 1–50. EP3C5 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	2 mA	GCLK	t_{CO}	7.805	8.993	10.222	ns
		GCLK PLL	t_{CO}	5.956	6.970	8.021	ns
	4 mA	GCLK	t_{CO}	7.360	8.467	9.615	ns
		GCLK PLL	t_{CO}	5.511	6.444	7.414	ns
	6 mA	GCLK	t_{CO}	7.211	8.286	9.401	ns
		GCLK PLL	t_{CO}	5.362	6.263	7.200	ns
	8 mA	GCLK	t_{CO}	7.142	8.206	9.311	ns
		GCLK PLL	t_{CO}	5.293	6.183	7.110	ns
	10 mA	GCLK	t_{CO}	7.006	8.024	9.080	ns
		GCLK PLL	t_{CO}	5.157	6.001	6.879	ns
	12 mA	GCLK	t_{CO}	6.978	7.998	9.058	ns
		GCLK PLL	t_{CO}	5.129	5.975	6.857	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.752	5.244	5.764	ns
		GCLK PLL	t_{CO}	2.900	3.217	3.559	ns
	12 mA	GCLK	t_{CO}	4.730	5.220	5.741	ns
		GCLK PLL	t_{CO}	2.878	3.193	3.536	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.670	5.158	5.675	ns
		GCLK PLL	t_{CO}	2.818	3.131	3.470	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.186	5.757	6.359	ns
		GCLK PLL	t_{CO}	3.334	3.730	4.154	ns
	10 mA	GCLK	t_{CO}	5.161	5.726	6.322	ns
		GCLK PLL	t_{CO}	3.309	3.699	4.117	ns
	12 mA	GCLK	t_{CO}	5.149	5.712	6.305	ns
		GCLK PLL	t_{CO}	3.297	3.685	4.100	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.120	5.683	6.277	ns
		GCLK PLL	t_{CO}	3.268	3.656	4.072	ns
	16 mA	GCLK	t_{CO}	5.107	5.670	6.263	ns
		GCLK PLL	t_{CO}	3.255	3.643	4.058	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.148	5.709	6.301	ns
		GCLK PLL	t_{CO}	3.296	3.682	4.096	ns
	10 mA	GCLK	t_{CO}	5.137	5.702	6.297	ns
		GCLK PLL	t_{CO}	3.285	3.675	4.092	ns
	12 mA	GCLK	t_{CO}	5.128	5.688	6.277	ns
		GCLK PLL	t_{CO}	3.276	3.661	4.072	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.063	5.622	6.211	ns
		GCLK PLL	t_{CO}	3.211	3.595	4.006	ns

Table 1–50. EP3C5 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.662	6.330	7.032	ns
		GCLK PLL	t_{CO}	3.810	4.303	4.827	ns
	10 mA	GCLK	t_{CO}	5.665	6.330	7.027	ns
		GCLK PLL	t_{CO}	3.813	4.303	4.822	ns
	12 mA	GCLK	t_{CO}	5.653	6.322	7.023	ns
		GCLK PLL	t_{CO}	3.801	4.295	4.818	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.591	6.254	6.948	ns
		GCLK PLL	t_{CO}	3.739	4.227	4.743	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.875	7.868	8.899	ns
		GCLK PLL	t_{CO}	5.023	5.841	6.694	ns
	10 mA	GCLK	t_{CO}	6.813	7.779	8.783	ns
		GCLK PLL	t_{CO}	4.961	5.752	6.578	ns
	12 mA	GCLK	t_{CO}	6.815	7.785	8.792	ns
		GCLK PLL	t_{CO}	4.963	5.758	6.587	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.770	7.732	8.732	ns
		GCLK PLL	t_{CO}	4.918	5.705	6.527	ns
3.0-V PCI	—	GCLK	t_{CO}	4.955	5.421	5.916	ns
		GCLK PLL	t_{CO}	3.106	3.398	3.715	ns
3.0-V PCI-X	—	GCLK	t_{CO}	4.955	5.421	5.916	ns
		GCLK PLL	t_{CO}	3.106	3.398	3.715	ns

Table 1–51. EP3C5 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.305	5.794	6.309	ns
		GCLK PLL	t_{CO}	3.471	3.786	4.122	ns
	8 mA	GCLK	t_{CO}	5.305	5.794	6.309	ns
		GCLK PLL	t_{CO}	3.471	3.786	4.122	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.305	5.620	5.959	ns
		GCLK PLL	t_{CO}	3.471	3.612	3.772	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.019	5.501	6.010	ns
		GCLK PLL	t_{CO}	3.185	3.493	3.823	ns
	8 mA	GCLK	t_{CO}	4.762	5.234	5.733	ns
		GCLK PLL	t_{CO}	2.928	3.226	3.546	ns
	12 mA	GCLK	t_{CO}	4.673	5.139	5.631	ns
		GCLK PLL	t_{CO}	2.839	3.131	3.444	ns
	16 mA	GCLK	t_{CO}	4.627	5.088	5.576	ns
		GCLK PLL	t_{CO}	2.793	3.080	3.389	ns

Table 1–51. EP3C5 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.760	5.232	5.731	ns
		GCLK PLL	t_{CO}	2.926	3.224	3.544	ns
	8 mA	GCLK	t_{CO}	4.627	5.089	5.579	ns
		GCLK PLL	t_{CO}	2.793	3.081	3.392	ns
	12 mA	GCLK	t_{CO}	4.592	5.053	5.540	ns
		GCLK PLL	t_{CO}	2.758	3.045	3.353	ns
	16 mA	GCLK	t_{CO}	4.577	5.037	5.523	ns
		GCLK PLL	t_{CO}	2.743	3.029	3.336	ns
2.5V	4 mA	GCLK	t_{CO}	5.117	5.615	6.140	ns
		GCLK PLL	t_{CO}	3.283	3.607	3.953	ns
	8 mA	GCLK	t_{CO}	4.882	5.371	5.886	ns
		GCLK PLL	t_{CO}	3.048	3.363	3.699	ns
	12 mA	GCLK	t_{CO}	4.783	5.266	5.776	ns
		GCLK PLL	t_{CO}	2.949	3.258	3.589	ns
	16 mA	GCLK	t_{CO}	4.742	5.224	5.733	ns
		GCLK PLL	t_{CO}	2.908	3.216	3.546	ns
1.8V	2 mA	GCLK	t_{CO}	6.226	6.866	7.535	ns
		GCLK PLL	t_{CO}	4.377	4.843	5.333	ns
	4 mA	GCLK	t_{CO}	5.713	6.338	6.991	ns
		GCLK PLL	t_{CO}	3.864	4.315	4.789	ns
	6 mA	GCLK	t_{CO}	5.492	6.084	6.704	ns
		GCLK PLL	t_{CO}	3.643	4.061	4.502	ns
	8 mA	GCLK	t_{CO}	5.391	5.970	6.578	ns
		GCLK PLL	t_{CO}	3.542	3.947	4.376	ns
	10 mA	GCLK	t_{CO}	5.340	5.921	6.532	ns
		GCLK PLL	t_{CO}	3.491	3.898	4.330	ns
	12 mA	GCLK	t_{CO}	5.285	5.858	6.459	ns
		GCLK PLL	t_{CO}	3.436	3.835	4.257	ns
	16 mA	GCLK	t_{CO}	5.242	5.811	6.410	ns
		GCLK PLL	t_{CO}	3.393	3.788	4.208	ns
1.5V	2 mA	GCLK	t_{CO}	6.620	7.433	8.280	ns
		GCLK PLL	t_{CO}	4.771	5.410	6.078	ns
	4 mA	GCLK	t_{CO}	6.164	6.889	7.647	ns
		GCLK PLL	t_{CO}	4.315	4.866	5.445	ns
	6 mA	GCLK	t_{CO}	5.997	6.711	7.456	ns
		GCLK PLL	t_{CO}	4.148	4.688	5.254	ns
	8 mA	GCLK	t_{CO}	5.921	6.618	7.346	ns
		GCLK PLL	t_{CO}	4.072	4.595	5.144	ns

Table 1–51. EP3C5 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	10 mA	GCLK	t_{CO}	5.861	6.555	7.280	ns
		GCLK PLL	t_{CO}	4.012	4.532	5.078	ns
	12 mA	GCLK	t_{CO}	5.827	6.512	7.229	ns
		GCLK PLL	t_{CO}	3.978	4.489	5.027	ns
	16 mA	GCLK	t_{CO}	5.730	6.404	7.110	ns
		GCLK PLL	t_{CO}	3.881	4.381	4.908	ns
1.2V	2 mA	GCLK	t_{CO}	7.808	8.973	10.176	ns
		GCLK PLL	t_{CO}	5.959	6.950	7.974	ns
	4 mA	GCLK	t_{CO}	7.373	8.459	9.584	ns
		GCLK PLL	t_{CO}	5.524	6.436	7.382	ns
	6 mA	GCLK	t_{CO}	7.245	8.305	9.405	ns
		GCLK PLL	t_{CO}	5.396	6.282	7.203	ns
	8 mA	GCLK	t_{CO}	7.173	8.223	9.310	ns
		GCLK PLL	t_{CO}	5.324	6.200	7.108	ns
	10 mA	GCLK	t_{CO}	7.042	8.060	9.115	ns
		GCLK PLL	t_{CO}	5.193	6.037	6.913	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.721	5.208	5.724	ns
		GCLK PLL	t_{CO}	2.864	3.178	3.515	ns
	12 mA	GCLK	t_{CO}	4.702	5.189	5.703	ns
		GCLK PLL	t_{CO}	2.845	3.159	3.494	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.647	5.132	5.643	ns
		GCLK PLL	t_{CO}	2.790	3.102	3.434	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.170	5.738	6.334	ns
		GCLK PLL	t_{CO}	3.298	3.693	4.110	ns
	10 mA	GCLK	t_{CO}	5.157	5.720	6.313	ns
		GCLK PLL	t_{CO}	3.285	3.675	4.089	ns
	12 mA	GCLK	t_{CO}	5.144	5.705	6.295	ns
		GCLK PLL	t_{CO}	3.272	3.660	4.071	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.114	5.676	6.267	ns
		GCLK PLL	t_{CO}	3.242	3.631	4.043	ns
	16 mA	GCLK	t_{CO}	5.106	5.670	6.262	ns
		GCLK PLL	t_{CO}	3.234	3.625	4.038	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.134	5.692	6.279	ns
		GCLK PLL	t_{CO}	3.262	3.647	4.055	ns
	10 mA	GCLK	t_{CO}	5.129	5.688	6.276	ns
		GCLK PLL	t_{CO}	3.257	3.643	4.052	ns
	12 mA	GCLK	t_{CO}	5.122	5.681	6.269	ns
		GCLK PLL	t_{CO}	3.250	3.636	4.045	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.060	5.615	6.198	ns
		GCLK PLL	t_{CO}	3.188	3.570	3.974	ns

Table 1–51. EP3C5 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.649	6.313	7.008	ns
		GCLK PLL	t_{CO}	3.777	4.268	4.784	ns
	10 mA	GCLK	t_{CO}	5.661	6.325	7.019	ns
		GCLK PLL	t_{CO}	3.789	4.280	4.795	ns
	12 mA	GCLK	t_{CO}	5.649	6.316	7.014	ns
		GCLK PLL	t_{CO}	3.777	4.271	4.790	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.594	6.259	6.953	ns
		GCLK PLL	t_{CO}	3.722	4.214	4.729	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.886	7.885	8.921	ns
		GCLK PLL	t_{CO}	5.014	5.840	6.697	ns
	10 mA	GCLK	t_{CO}	6.825	7.800	8.812	ns
		GCLK PLL	t_{CO}	4.953	5.755	6.588	ns
3.0-V PCI	—	GCLK	t_{CO}	4.919	5.380	5.866	ns
		GCLK PLL	t_{CO}	3.085	3.372	3.679	ns
3.0-V PCI-X	—	GCLK	t_{CO}	4.919	5.380	5.866	ns
		GCLK PLL	t_{CO}	3.085	3.372	3.679	ns

Table 1–52. EP3C5 Column Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.953	1.036	1.096	ns
			t_{H}	–0.675	–0.720	–0.743	ns
	—	GCLK PLL	t_{SU}	2.798	3.057	3.295	ns
			t_{H}	–2.520	–2.741	–2.942	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.700	5.190	5.711	ns
		GCLK PLL	t_{CO}	2.867	3.183	3.525	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.700	5.190	5.711	ns
		GCLK PLL	t_{CO}	2.867	3.183	3.525	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.081	5.569	6.089	ns
		GCLK PLL	t_{CO}	3.248	3.562	3.903	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.700	5.190	5.711	ns
		GCLK PLL	t_{CO}	2.867	3.183	3.525	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.700	5.190	5.711	ns
		GCLK PLL	t_{CO}	2.867	3.183	3.525	ns

Table 1–53. EP3C5 Row Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	1.035	1.120	1.190	ns
			t_{H}	–0.757	–0.805	–0.836	ns
			t_{CO}	3.879	4.265	4.675	ns
	—	GCLK PLL	t_{SU}	2.819	3.079	3.329	ns
			t_{H}	–2.541	–2.764	–2.975	ns
			t_{CO}	2.021	2.233	2.462	ns
mini-LVDS	—	GCLK	t_{CO}	3.879	4.265	4.675	ns
		GCLK PLL	t_{CO}	2.021	2.233	2.462	ns
PPDS	—	GCLK	t_{CO}	3.879	4.265	4.675	ns
		GCLK PLL	t_{CO}	2.021	2.233	2.462	ns
RSDS	—	GCLK	t_{CO}	3.879	4.265	4.675	ns
		GCLK PLL	t_{CO}	2.021	2.233	2.462	ns

EP3C10 I/O Timing Parameters

Table 1–54 through Table 1–59 show the maximum I/O timing parameters for EP3C10 devices.

Table 1–54. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_{H}	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_{H}	–2.745	–2.914	–3.037	ns
	8 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_{H}	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_{H}	–2.745	–2.914	–3.037	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_{H}	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_{H}	–2.745	–2.914	–3.037	ns

Table 1–54. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVTTL	4 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns
	8 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns
	12 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns
	16 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns
	8 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns
	12 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns
	16 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns

Table 1–54. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
2.5V	4 mA	GCLK	t_{SU}	1.066	1.111	1.135	ns
			t_H	–0.786	–0.794	–0.782	ns
		GCLK PLL	t_{SU}	2.968	3.187	3.359	ns
			t_H	–2.688	–2.870	–3.006	ns
	8 mA	GCLK	t_{SU}	1.066	1.111	1.135	ns
			t_H	–0.786	–0.794	–0.782	ns
		GCLK PLL	t_{SU}	2.968	3.187	3.359	ns
			t_H	–2.688	–2.870	–3.006	ns
	12 mA	GCLK	t_{SU}	1.066	1.111	1.135	ns
			t_H	–0.786	–0.794	–0.782	ns
		GCLK PLL	t_{SU}	2.968	3.187	3.359	ns
			t_H	–2.688	–2.870	–3.006	ns
	16 mA	GCLK	t_{SU}	1.066	1.111	1.135	ns
			t_H	–0.786	–0.794	–0.782	ns
		GCLK PLL	t_{SU}	2.968	3.187	3.359	ns
			t_H	–2.688	–2.870	–3.006	ns
1.8V	2 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.903	3.148	3.346	ns
			t_H	–2.625	–2.832	–2.992	ns
	4 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.903	3.148	3.346	ns
			t_H	–2.625	–2.832	–2.992	ns
	6 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.903	3.148	3.346	ns
			t_H	–2.625	–2.832	–2.992	ns
	8 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.903	3.148	3.346	ns
			t_H	–2.625	–2.832	–2.992	ns
	10 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.903	3.148	3.346	ns
			t_H	–2.625	–2.832	–2.992	ns
	12 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.903	3.148	3.346	ns
			t_H	–2.625	–2.832	–2.992	ns

Table 1–54. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	16 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.903	3.148	3.346	ns
			t_H	–2.625	–2.832	–2.992	ns
1.5V	2 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.972	3.240	3.463	ns
			t_H	–2.692	–2.922	–3.107	ns
	4 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.972	3.240	3.463	ns
			t_H	–2.692	–2.922	–3.107	ns
	6 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.972	3.240	3.463	ns
			t_H	–2.692	–2.922	–3.107	ns
	8 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.972	3.240	3.463	ns
			t_H	–2.692	–2.922	–3.107	ns
	10 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.972	3.240	3.463	ns
			t_H	–2.692	–2.922	–3.107	ns
	12 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.972	3.240	3.463	ns
			t_H	–2.692	–2.922	–3.107	ns
	16 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.972	3.240	3.463	ns
			t_H	–2.692	–2.922	–3.107	ns
1.2V	2 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.124	3.420	3.669	ns
			t_H	–2.842	–3.098	–3.309	ns
	4 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.124	3.420	3.669	ns
			t_H	–2.842	–3.098	–3.309	ns

Table 1–54. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	6 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.124	3.420	3.669	ns
			t_H	–2.842	–3.098	–3.309	ns
	8 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.124	3.420	3.669	ns
			t_H	–2.842	–3.098	–3.309	ns
	10 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.124	3.420	3.669	ns
			t_H	–2.842	–3.098	–3.309	ns
	12 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.124	3.420	3.669	ns
			t_H	–2.842	–3.098	–3.309	ns
SSTL–2 Class I	8 mA	GCLK	t_{SU}	1.055	1.129	1.184	ns
			t_H	–0.775	–0.812	–0.829	ns
		GCLK PLL	t_{SU}	2.954	3.143	3.376	ns
			t_H	–2.674	–2.826	–3.021	ns
	12 mA	GCLK	t_{SU}	1.055	1.129	1.184	ns
			t_H	–0.775	–0.812	–0.829	ns
		GCLK PLL	t_{SU}	2.954	3.143	3.376	ns
			t_H	–2.674	–2.826	–3.021	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	1.055	1.129	1.184	ns
			t_H	–0.775	–0.812	–0.829	ns
		GCLK PLL	t_{SU}	2.954	3.143	3.376	ns
			t_H	–2.674	–2.826	–3.021	ns
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.116	1.218	1.299	ns
			t_H	–0.836	–0.899	–0.942	ns
		GCLK PLL	t_{SU}	3.015	3.232	3.491	ns
			t_H	–2.735	–2.913	–3.134	ns
	10 mA	GCLK	t_{SU}	1.116	1.218	1.299	ns
			t_H	–0.836	–0.899	–0.942	ns
		GCLK PLL	t_{SU}	3.015	3.232	3.491	ns
			t_H	–2.735	–2.913	–3.134	ns
	12 mA	GCLK	t_{SU}	1.116	1.218	1.299	ns
			t_H	–0.836	–0.899	–0.942	ns
		GCLK PLL	t_{SU}	3.015	3.232	3.491	ns
			t_H	–2.735	–2.913	–3.134	ns

Table 1–54. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.116	1.218	1.299	ns
			t_H	–0.836	–0.899	–0.942	ns
		GCLK PLL	t_{SU}	3.015	3.232	3.491	ns
			t_H	–2.735	–2.913	–3.134	ns
	16 mA	GCLK	t_{SU}	1.116	1.218	1.299	ns
			t_H	–0.836	–0.899	–0.942	ns
		GCLK PLL	t_{SU}	3.015	3.232	3.491	ns
			t_H	–2.735	–2.913	–3.134	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.116	1.218	1.299	ns
			t_H	–0.836	–0.899	–0.942	ns
		GCLK PLL	t_{SU}	3.015	3.232	3.491	ns
			t_H	–2.735	–2.913	–3.134	ns
	10 mA	GCLK	t_{SU}	1.116	1.218	1.299	ns
			t_H	–0.836	–0.899	–0.942	ns
		GCLK PLL	t_{SU}	3.015	3.232	3.491	ns
			t_H	–2.735	–2.913	–3.134	ns
	12 mA	GCLK	t_{SU}	1.116	1.218	1.299	ns
			t_H	–0.836	–0.899	–0.942	ns
		GCLK PLL	t_{SU}	3.015	3.232	3.491	ns
			t_H	–2.735	–2.913	–3.134	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.116	1.218	1.299	ns
			t_H	–0.836	–0.899	–0.942	ns
		GCLK PLL	t_{SU}	3.015	3.232	3.491	ns
			t_H	–2.735	–2.913	–3.134	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	1.072	1.178	1.265	ns
			t_H	–0.792	–0.860	–0.909	ns
		GCLK PLL	t_{SU}	2.971	3.192	3.457	ns
			t_H	–2.691	–2.874	–3.101	ns
	10 mA	GCLK	t_{SU}	1.072	1.178	1.265	ns
			t_H	–0.792	–0.860	–0.909	ns
		GCLK PLL	t_{SU}	2.971	3.192	3.457	ns
			t_H	–2.691	–2.874	–3.101	ns
	12 mA	GCLK	t_{SU}	1.072	1.178	1.265	ns
			t_H	–0.792	–0.860	–0.909	ns
		GCLK PLL	t_{SU}	2.971	3.192	3.457	ns
			t_H	–2.691	–2.874	–3.101	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	1.072	1.178	1.265	ns
			t_H	–0.792	–0.860	–0.909	ns
		GCLK PLL	t_{SU}	2.971	3.192	3.457	ns
			t_H	–2.691	–2.874	–3.101	ns

Table 1–54. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.204	1.337	1.449	ns
			t_H	–0.922	–1.015	–1.089	ns
		GCLK PLL	t_{SU}	3.103	3.351	3.641	ns
			t_H	–2.821	–3.029	–3.281	ns
	10 mA	GCLK	t_{SU}	1.204	1.337	1.449	ns
			t_H	–0.922	–1.015	–1.089	ns
		GCLK PLL	t_{SU}	3.103	3.351	3.641	ns
			t_H	–2.821	–3.029	–3.281	ns
	12 mA	GCLK	t_{SU}	1.204	1.337	1.449	ns
			t_H	–0.922	–1.015	–1.089	ns
		GCLK PLL	t_{SU}	3.103	3.351	3.641	ns
			t_H	–2.821	–3.029	–3.281	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	1.204	1.337	1.449	ns
			t_H	–0.922	–1.015	–1.089	ns
		GCLK PLL	t_{SU}	3.103	3.351	3.641	ns
			t_H	–2.821	–3.029	–3.281	ns
3.0-V PCI	—	GCLK	t_{SU}	1.119	1.152	1.162	ns
			t_H	–0.839	–0.834	–0.808	ns
	—	GCLK PLL	t_{SU}	3.021	3.228	3.386	ns
			t_H	–2.741	–2.910	–3.032	ns
3.0-V PCI-X	—	GCLK	t_{SU}	1.119	1.152	1.162	ns
			t_H	–0.839	–0.834	–0.808	ns
	—	GCLK PLL	t_{SU}	3.021	3.228	3.386	ns
			t_H	–2.741	–2.910	–3.032	ns

Table 1–55. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns
	8 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns

Table 1–55. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns
	8 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			th	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns
	12 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns
	16 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns
	8 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns
	12 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns
	16 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns

Table 1–55. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
2.5V	4 mA	GCLK	t_{SU}	1.098	1.149	1.184	ns
			t_H	–0.818	–0.832	–0.830	ns
		GCLK PLL	t_{SU}	2.942	3.169	3.382	ns
			t_H	–2.662	–2.852	–3.028	ns
	8 mA	GCLK	t_{SU}	1.098	1.149	1.184	ns
			t_H	–0.818	–0.832	–0.830	ns
		GCLK PLL	t_{SU}	2.942	3.169	3.382	ns
			t_H	–2.662	–2.852	–3.028	ns
	12 mA	GCLK	t_{SU}	1.098	1.149	1.184	ns
			t_H	–0.818	–0.832	–0.830	ns
		GCLK PLL	t_{SU}	2.942	3.169	3.382	ns
			t_H	–2.662	–2.852	–3.028	ns
	16 mA	GCLK	t_{SU}	1.098	1.149	1.184	ns
			t_H	–0.818	–0.832	–0.830	ns
		GCLK PLL	t_{SU}	2.942	3.169	3.382	ns
			t_H	–2.662	–2.852	–3.028	ns
1.8V	2 mA	GCLK	t_{SU}	1.034	1.110	1.170	ns
			t_H	–0.756	–0.794	–0.815	ns
		GCLK PLL	t_{SU}	2.878	3.130	3.368	ns
			t_H	–2.600	–2.814	–3.013	ns
	4 mA	GCLK	t_{SU}	1.034	1.110	1.170	ns
			t_H	–0.756	–0.794	–0.815	ns
		GCLK PLL	t_{SU}	2.878	3.130	3.368	ns
			t_H	–2.600	–2.814	–3.013	ns
	6 mA	GCLK	t_{SU}	1.034	1.110	1.170	ns
			t_H	–0.756	–0.794	–0.815	ns
		GCLK PLL	t_{SU}	2.878	3.130	3.368	ns
			t_H	–2.600	–2.814	–3.013	ns
	8 mA	GCLK	t_{SU}	1.034	1.110	1.170	ns
			t_H	–0.756	–0.794	–0.815	ns
		GCLK PLL	t_{SU}	2.878	3.130	3.368	ns
			t_H	–2.600	–2.814	–3.013	ns
	10 mA	GCLK	t_{SU}	1.034	1.110	1.170	ns
			t_H	–0.756	–0.794	–0.815	ns
		GCLK PLL	t_{SU}	2.878	3.130	3.368	ns
			t_H	–2.600	–2.814	–3.013	ns
	12 mA	GCLK	t_{SU}	1.034	1.110	1.170	ns
			t_H	–0.756	–0.794	–0.815	ns
		GCLK PLL	t_{SU}	2.878	3.130	3.368	ns
			t_H	–2.600	–2.814	–3.013	ns

Table 1–55. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	16 mA	GCLK	t_{SU}	1.034	1.110	1.170	ns
			t_H	–0.756	–0.794	–0.815	ns
		GCLK PLL	t_{SU}	2.878	3.130	3.368	ns
			t_H	–2.600	–2.814	–3.013	ns
1.5V	2 mA	GCLK	t_{SU}	1.103	1.203	1.288	ns
			t_H	–0.823	–0.885	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.223	3.486	ns
			t_H	–2.667	–2.905	–3.130	ns
	4 mA	GCLK	t_{SU}	1.103	1.203	1.288	ns
			t_H	–0.823	–0.885	–0.932	ns
		GCLK PLL	tsu	2.947	3.223	3.486	ns
			t_H	–2.667	–2.905	–3.130	ns
	6 mA	GCLK	t_{SU}	1.103	1.203	1.288	ns
			t_H	–0.823	–0.885	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.223	3.486	ns
			t_H	–2.667	–2.905	–3.130	ns
	8 mA	GCLK	t_{SU}	1.103	1.203	1.288	ns
			t_H	–0.823	–0.885	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.223	3.486	ns
			t_H	–2.667	–2.905	–3.130	ns
	10 mA	GCLK	t_{SU}	1.103	1.203	1.288	ns
			t_H	–0.823	–0.885	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.223	3.486	ns
			t_H	–2.667	–2.905	–3.130	ns
	12 mA	GCLK	t_{SU}	1.103	1.203	1.288	ns
			t_H	–0.823	–0.885	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.223	3.486	ns
			t_H	–2.667	–2.905	–3.130	ns
	16 mA	GCLK	t_{SU}	1.103	1.203	1.288	ns
			t_H	–0.823	–0.885	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.223	3.486	ns
			t_H	–2.667	–2.905	–3.130	ns

Table 1–55. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	2 mA	GCLK	t_{SU}	1.256	1.383	1.495	ns
			t_H	–0.974	–1.061	–1.134	ns
		GCLK PLL	t_{SU}	3.100	3.403	3.693	ns
			t_H	–2.818	–3.081	–3.332	ns
	4 mA	GCLK	t_{SU}	1.256	1.383	1.495	ns
			t_H	–0.974	–1.061	–1.134	ns
		GCLK PLL	t_{SU}	3.100	3.403	3.693	ns
			t_H	–2.818	–3.081	–3.332	ns
	6 mA	GCLK	t_{SU}	1.256	1.383	1.495	ns
			t_H	–0.974	–1.061	–1.134	ns
		GCLK PLL	t_{SU}	3.100	3.403	3.693	ns
			t_H	–2.818	–3.081	–3.332	ns
	8 mA	GCLK	t_{SU}	1.256	1.383	1.495	ns
			t_H	–0.974	–1.061	–1.134	ns
		GCLK PLL	t_{SU}	3.100	3.403	3.693	ns
			t_H	–2.818	–3.081	–3.332	ns
	10 mA	GCLK	t_{SU}	1.256	1.383	1.495	ns
			t_H	–0.974	–1.061	–1.134	ns
		GCLK PLL	t_{SU}	3.100	3.403	3.693	ns
			t_H	–2.818	–3.081	–3.332	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	1.082	1.162	1.225	ns
			t_H	–0.802	–0.844	–0.869	ns
		GCLK PLL	t_{SU}	2.930	3.184	3.428	ns
			t_H	–2.650	–2.866	–3.072	ns
	12 mA	GCLK	t_{SU}	1.082	1.162	1.225	ns
			t_H	–0.802	–0.844	–0.869	ns
		GCLK PLL	t_{SU}	2.930	3.184	3.428	ns
			t_H	–2.650	–2.866	–3.072	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	1.082	1.162	1.225	ns
			t_H	–0.802	–0.844	–0.869	ns
		GCLK PLL	t_{SU}	2.930	3.184	3.428	ns
			t_H	–2.650	–2.866	–3.072	ns

Table 1–55. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.129	1.236	1.327	ns
			t_H	–0.849	–0.917	–0.969	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.545	ns
			t_H	–2.712	–2.954	–3.187	ns
	10 mA	GCLK	t_{SU}	1.129	1.236	1.327	ns
			t_H	–0.849	–0.917	–0.969	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.545	ns
			t_H	–2.712	–2.954	–3.187	ns
	12 mA	GCLK	t_{SU}	1.129	1.236	1.327	ns
			t_H	–0.849	–0.917	–0.969	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.545	ns
			t_H	–2.712	–2.954	–3.187	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.129	1.236	1.327	ns
			t_H	–0.849	–0.917	–0.969	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.545	ns
			t_H	–2.712	–2.954	–3.187	ns
	16 mA	GCLK	t_{SU}	1.129	1.236	1.327	ns
			t_H	–0.849	–0.917	–0.969	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.545	ns
			t_H	–2.712	–2.954	–3.187	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.129	1.236	1.327	ns
			t_H	–0.849	–0.917	–0.969	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.545	ns
			t_H	–2.712	–2.954	–3.187	ns
	10 mA	GCLK	t_{SU}	1.129	1.236	1.327	ns
			t_H	–0.849	–0.917	–0.969	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.545	ns
			t_H	–2.712	–2.954	–3.187	ns
	12 mA	GCLK	t_{SU}	1.129	1.236	1.327	ns
			t_H	–0.849	–0.917	–0.969	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.545	ns
			t_H	–2.712	–2.954	–3.187	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.129	1.236	1.327	ns
			t_H	–0.849	–0.917	–0.969	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.545	ns
			t_H	–2.712	–2.954	–3.187	ns

Table 1–55. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	1.084	1.195	1.290	ns
			t_H	–0.804	–0.877	–0.933	ns
		GCLK PLL	t_{SU}	2.947	3.232	3.508	ns
			t_H	–2.667	–2.914	–3.151	ns
	10 mA	GCLK	t_{SU}	1.084	1.195	1.290	ns
			t_H	–0.804	–0.877	–0.933	ns
		GCLK PLL	t_{SU}	2.947	3.232	3.508	ns
			t_H	–2.667	–2.914	–3.151	ns
	12 mA	GCLK	t_{SU}	1.084	1.195	1.290	ns
			t_H	–0.804	–0.877	–0.933	ns
		GCLK PLL	t_{SU}	2.947	3.232	3.508	ns
			t_H	–2.667	–2.914	–3.151	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	1.084	1.195	1.290	ns
			t_H	–0.804	–0.877	–0.933	ns
		GCLK PLL	t_{SU}	2.947	3.232	3.508	ns
			t_H	–2.667	–2.914	–3.151	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.215	1.353	1.475	ns
			t_H	–0.933	–1.031	–1.115	ns
		GCLK PLL	t_{SU}	3.078	3.390	3.693	ns
			t_H	–2.796	–3.068	–3.333	ns
	10 mA	GCLK	t_{SU}	1.215	1.353	1.475	ns
			t_H	–0.933	–1.031	–1.115	ns
		GCLK PLL	t_{SU}	3.078	3.390	3.693	ns
			t_H	–2.796	–3.068	–3.333	ns
3.0-V PCI	—	GCLK	t_{SU}	1.151	1.189	1.209	ns
			t_H	–0.871	–0.871	–0.854	ns
	—	GCLK PLL	t_{SU}	2.995	3.209	3.407	ns
			t_H	–2.715	–2.891	–3.052	ns
3.0-V PCI-X	—	GCLK	t_{SU}	1.151	1.189	1.209	ns
			t_H	–0.871	–0.871	–0.854	ns
	—	GCLK PLL	t_{SU}	2.995	3.209	3.407	ns
			t_H	–2.715	–2.891	–3.052	ns

Table 1–56. EP3C10 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.371	5.866	6.382	ns
		GCLK PLL	t_{CO}	3.512	3.831	4.181	ns
	8 mA	GCLK	t_{CO}	5.371	5.866	6.382	ns
		GCLK PLL	t_{CO}	3.512	3.831	4.181	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.330	5.647	5.984	ns
		GCLK PLL	t_{CO}	3.471	3.612	3.783	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.081	5.569	6.080	ns
		GCLK PLL	t_{CO}	3.222	3.534	3.879	ns
	8 mA	GCLK	t_{CO}	4.810	5.285	5.781	ns
		GCLK PLL	t_{CO}	2.951	3.250	3.580	ns
	12 mA	GCLK	t_{CO}	4.713	5.184	5.677	ns
		GCLK PLL	t_{CO}	2.854	3.149	3.476	ns
	16 mA	GCLK	t_{CO}	4.666	5.132	5.619	ns
		GCLK PLL	t_{CO}	2.807	3.097	3.418	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.808	5.282	5.778	ns
		GCLK PLL	t_{CO}	2.949	3.247	3.577	ns
	8 mA	GCLK	t_{CO}	4.667	5.134	5.623	ns
		GCLK PLL	t_{CO}	2.808	3.099	3.422	ns
	12 mA	GCLK	t_{CO}	4.630	5.094	5.580	ns
		GCLK PLL	t_{CO}	2.771	3.059	3.379	ns
	16 mA	GCLK	t_{CO}	4.614	5.079	5.565	ns
		GCLK PLL	t_{CO}	2.755	3.044	3.364	ns
2.5V	4 mA	GCLK	t_{CO}	5.139	5.655	6.194	ns
		GCLK PLL	t_{CO}	3.280	3.620	3.993	ns
	8 mA	GCLK	t_{CO}	4.896	5.402	5.930	ns
		GCLK PLL	t_{CO}	3.037	3.367	3.729	ns
	12 mA	GCLK	t_{CO}	4.798	5.296	5.817	ns
		GCLK PLL	t_{CO}	2.939	3.261	3.616	ns
	16 mA	GCLK	t_{CO}	4.759	5.256	5.776	ns
		GCLK PLL	t_{CO}	2.900	3.221	3.575	ns

Table 1–56. EP3C10 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	2 mA	GCLK	t_{CO}	6.250	6.908	7.592	ns
		GCLK PLL	t_{CO}	4.391	4.873	5.391	ns
	4 mA	GCLK	t_{CO}	5.723	6.363	7.028	ns
		GCLK PLL	t_{CO}	3.864	4.328	4.827	ns
	6 mA	GCLK	t_{CO}	5.498	6.105	6.736	ns
		GCLK PLL	t_{CO}	3.639	4.070	4.535	ns
	8 mA	GCLK	t_{CO}	5.395	5.988	6.607	ns
		GCLK PLL	t_{CO}	3.536	3.953	4.406	ns
	10 mA	GCLK	t_{CO}	5.343	5.940	6.561	ns
		GCLK PLL	t_{CO}	3.484	3.905	4.360	ns
	12 mA	GCLK	t_{CO}	5.286	5.873	6.486	ns
		GCLK PLL	t_{CO}	3.427	3.838	4.285	ns
	16 mA	GCLK	t_{CO}	5.232	5.814	6.421	ns
		GCLK PLL	t_{CO}	3.373	3.779	4.220	ns
1.5V	2 mA	GCLK	t_{CO}	6.638	7.470	8.331	ns
		GCLK PLL	t_{CO}	4.779	5.435	6.130	ns
	4 mA	GCLK	t_{CO}	6.163	6.909	7.683	ns
		GCLK PLL	t_{CO}	4.304	4.874	5.482	ns
	6 mA	GCLK	t_{CO}	5.993	6.726	7.486	ns
		GCLK PLL	t_{CO}	4.134	4.691	5.285	ns
	8 mA	GCLK	t_{CO}	5.905	6.613	7.348	ns
		GCLK PLL	t_{CO}	4.046	4.578	5.147	ns
	10 mA	GCLK	t_{CO}	5.846	6.553	7.287	ns
		GCLK PLL	t_{CO}	3.987	4.518	5.086	ns
	12 mA	GCLK	t_{CO}	5.813	6.512	7.237	ns
		GCLK PLL	t_{CO}	3.954	4.477	5.036	ns
	16 mA	GCLK	t_{CO}	5.699	6.370	7.067	ns
		GCLK PLL	t_{CO}	3.840	4.335	4.866	ns
1.2V	2 mA	GCLK	t_{CO}	7.811	8.998	10.220	ns
		GCLK PLL	t_{CO}	5.952	6.963	8.019	ns
	4 mA	GCLK	t_{CO}	7.366	8.472	9.613	ns
		GCLK PLL	t_{CO}	5.507	6.437	7.412	ns
	6 mA	GCLK	t_{CO}	7.217	8.291	9.399	ns
		GCLK PLL	t_{CO}	5.358	6.256	7.198	ns
	8 mA	GCLK	t_{CO}	7.148	8.211	9.309	ns
		GCLK PLL	t_{CO}	5.289	6.176	7.108	ns
	10 mA	GCLK	t_{CO}	7.012	8.029	9.078	ns
		GCLK PLL	t_{CO}	5.153	5.994	6.877	ns
	12 mA	GCLK	t_{CO}	6.984	8.003	9.056	ns
		GCLK PLL	t_{CO}	5.125	5.968	6.855	ns

Table 1–56. EP3C10 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.754	5.240	5.750	ns
		GCLK PLL	t_{CO}	2.901	3.228	3.570	ns
	12 mA	GCLK	t_{CO}	4.732	5.216	5.727	ns
		GCLK PLL	t_{CO}	2.879	3.204	3.547	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.672	5.154	5.661	ns
		GCLK PLL	t_{CO}	2.819	3.142	3.481	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.188	5.753	6.345	ns
		GCLK PLL	t_{CO}	3.335	3.741	4.165	ns
	10 mA	GCLK	t_{CO}	5.163	5.722	6.308	ns
		GCLK PLL	t_{CO}	3.310	3.710	4.128	ns
	12 mA	GCLK	t_{CO}	5.151	5.708	6.291	ns
		GCLK PLL	t_{CO}	3.298	3.696	4.111	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.122	5.679	6.263	ns
		GCLK PLL	t_{CO}	3.269	3.667	4.083	ns
	16 mA	GCLK	t_{CO}	5.109	5.666	6.249	ns
		GCLK PLL	t_{CO}	3.256	3.654	4.069	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.150	5.705	6.287	ns
		GCLK PLL	t_{CO}	3.297	3.693	4.107	ns
	10 mA	GCLK	t_{CO}	5.139	5.698	6.283	ns
		GCLK PLL	t_{CO}	3.286	3.686	4.103	ns
	12 mA	GCLK	t_{CO}	5.130	5.684	6.263	ns
		GCLK PLL	t_{CO}	3.277	3.672	4.083	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.065	5.618	6.197	ns
		GCLK PLL	t_{CO}	3.212	3.606	4.017	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.664	6.326	7.018	ns
		GCLK PLL	t_{CO}	3.811	4.314	4.838	ns
	10 mA	GCLK	t_{CO}	5.667	6.326	7.013	ns
		GCLK PLL	t_{CO}	3.814	4.314	4.833	ns
	12 mA	GCLK	t_{CO}	5.655	6.318	7.009	ns
		GCLK PLL	t_{CO}	3.802	4.306	4.829	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.593	6.250	6.934	ns
		GCLK PLL	t_{CO}	3.740	4.238	4.754	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.877	7.864	8.885	ns
		GCLK PLL	t_{CO}	5.024	5.852	6.705	ns
	10 mA	GCLK	t_{CO}	6.815	7.775	8.769	ns
		GCLK PLL	t_{CO}	4.962	5.763	6.589	ns
	12 mA	GCLK	t_{CO}	6.817	7.781	8.778	ns
		GCLK PLL	t_{CO}	4.964	5.769	6.598	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.772	7.728	8.718	ns
		GCLK PLL	t_{CO}	4.919	5.716	6.538	ns

Table 1–56. EP3C10 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V PCI	—	GCLK	t_{CO}	4.961	5.426	5.914	ns
		GCLK PLL	t_{CO}	3.102	3.391	3.713	ns
3.0-V PCI-X	—	GCLK	t_{CO}	4.961	5.426	5.914	ns
		GCLK PLL	t_{CO}	3.102	3.391	3.713	ns

Table 1–57. EP3C10 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.308	5.797	6.311	ns
		GCLK PLL	t_{CO}	3.467	3.783	4.118	ns
	8 mA	GCLK	t_{CO}	5.308	5.797	6.311	ns
		GCLK PLL	t_{CO}	3.467	3.783	4.118	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.308	5.623	5.961	ns
		GCLK PLL	t_{CO}	3.467	3.609	3.768	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.022	5.504	6.012	ns
		GCLK PLL	t_{CO}	3.181	3.490	3.819	ns
	8 mA	GCLK	t_{CO}	4.765	5.237	5.735	ns
		GCLK PLL	t_{CO}	2.924	3.223	3.542	ns
	12 mA	GCLK	t_{CO}	4.676	5.142	5.633	ns
		GCLK PLL	t_{CO}	2.835	3.128	3.440	ns
	16 mA	GCLK	t_{CO}	4.630	5.091	5.578	ns
		GCLK PLL	t_{CO}	2.789	3.077	3.385	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.763	5.235	5.733	ns
		GCLK PLL	t_{CO}	2.922	3.221	3.540	ns
	8 mA	GCLK	t_{CO}	4.630	5.092	5.581	ns
		GCLK PLL	t_{CO}	2.789	3.078	3.388	ns
	12 mA	GCLK	t_{CO}	4.595	5.056	5.542	ns
		GCLK PLL	t_{CO}	2.754	3.042	3.349	ns
	16 mA	GCLK	t_{CO}	4.580	5.040	5.525	ns
		GCLK PLL	t_{CO}	2.739	3.026	3.332	ns
2.5V	4 mA	GCLK	t_{CO}	5.120	5.618	6.142	ns
		GCLK PLL	t_{CO}	3.279	3.604	3.949	ns
	8 mA	GCLK	t_{CO}	4.885	5.374	5.888	ns
		GCLK PLL	t_{CO}	3.044	3.360	3.695	ns
	12 mA	GCLK	t_{CO}	4.786	5.269	5.778	ns
		GCLK PLL	t_{CO}	2.945	3.255	3.585	ns
	16 mA	GCLK	t_{CO}	4.745	5.227	5.735	ns
		GCLK PLL	t_{CO}	2.904	3.213	3.542	ns

Table 1–57. EP3C10 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	2 mA	GCLK	t_{CO}	6.214	6.854	7.522	ns
		GCLK PLL	t_{CO}	4.373	4.840	5.329	ns
	4 mA	GCLK	t_{CO}	5.701	6.326	6.978	ns
		GCLK PLL	t_{CO}	3.860	4.312	4.785	ns
	6 mA	GCLK	t_{CO}	5.480	6.072	6.691	ns
		GCLK PLL	t_{CO}	3.639	4.058	4.498	ns
	8 mA	GCLK	t_{CO}	5.379	5.958	6.565	ns
		GCLK PLL	t_{CO}	3.538	3.944	4.372	ns
	10 mA	GCLK	t_{CO}	5.328	5.909	6.519	ns
		GCLK PLL	t_{CO}	3.487	3.895	4.326	ns
	12 mA	GCLK	t_{CO}	5.273	5.846	6.446	ns
		GCLK PLL	t_{CO}	3.432	3.832	4.253	ns
	16 mA	GCLK	t_{CO}	5.230	5.799	6.397	ns
		GCLK PLL	t_{CO}	3.389	3.785	4.204	ns
1.5V	2 mA	GCLK	t_{CO}	6.608	7.421	8.267	ns
		GCLK PLL	t_{CO}	4.767	5.407	6.074	ns
	4 mA	GCLK	t_{CO}	6.152	6.877	7.634	ns
		GCLK PLL	t_{CO}	4.311	4.863	5.441	ns
	6 mA	GCLK	t_{CO}	5.985	6.699	7.443	ns
		GCLK PLL	t_{CO}	4.144	4.685	5.250	ns
	8 mA	GCLK	t_{CO}	5.909	6.606	7.333	ns
		GCLK PLL	t_{CO}	4.068	4.592	5.140	ns
	10 mA	GCLK	t_{CO}	5.849	6.543	7.267	ns
		GCLK PLL	t_{CO}	4.008	4.529	5.074	ns
	12 mA	GCLK	t_{CO}	5.815	6.500	7.216	ns
		GCLK PLL	t_{CO}	3.974	4.486	5.023	ns
	16 mA	GCLK	t_{CO}	5.718	6.392	7.097	ns
		GCLK PLL	t_{CO}	3.877	4.378	4.904	ns
1.2V	2 mA	GCLK	t_{CO}	7.796	8.961	10.163	ns
		GCLK PLL	t_{CO}	5.955	6.947	7.970	ns
	4 mA	GCLK	t_{CO}	7.361	8.447	9.571	ns
		GCLK PLL	t_{CO}	5.520	6.433	7.378	ns
	6 mA	GCLK	t_{CO}	7.233	8.293	9.392	ns
		GCLK PLL	t_{CO}	5.392	6.279	7.199	ns
	8 mA	GCLK	t_{CO}	7.161	8.211	9.297	ns
		GCLK PLL	t_{CO}	5.320	6.197	7.104	ns
	10 mA	GCLK	t_{CO}	7.030	8.048	9.102	ns
		GCLK PLL	t_{CO}	5.189	6.034	6.909	ns

Table 1–57. EP3C10 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.720	5.207	5.723	ns
		GCLK PLL	t_{CO}	2.865	3.176	3.513	ns
	12 mA	GCLK	t_{CO}	4.701	5.188	5.702	ns
		GCLK PLL	t_{CO}	2.846	3.157	3.492	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.646	5.131	5.642	ns
		GCLK PLL	t_{CO}	2.791	3.100	3.432	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.169	5.737	6.333	ns
		GCLK PLL	t_{CO}	3.299	3.691	4.108	ns
	10 mA	GCLK	t_{CO}	5.156	5.719	6.312	ns
		GCLK PLL	t_{CO}	3.286	3.673	4.087	ns
	12 mA	GCLK	t_{CO}	5.143	5.704	6.294	ns
		GCLK PLL	t_{CO}	3.273	3.658	4.069	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.113	5.675	6.266	ns
		GCLK PLL	t_{CO}	3.243	3.629	4.041	ns
	16 mA	GCLK	t_{CO}	5.105	5.669	6.261	ns
		GCLK PLL	t_{CO}	3.235	3.623	4.036	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.133	5.691	6.278	ns
		GCLK PLL	t_{CO}	3.263	3.645	4.053	ns
	10 mA	GCLK	t_{CO}	5.128	5.687	6.275	ns
		GCLK PLL	t_{CO}	3.258	3.641	4.050	ns
	12 mA	GCLK	t_{CO}	5.121	5.680	6.268	ns
		GCLK PLL	t_{CO}	3.251	3.634	4.043	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.059	5.614	6.197	ns
		GCLK PLL	t_{CO}	3.189	3.568	3.972	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.648	6.312	7.007	ns
		GCLK PLL	t_{CO}	3.778	4.266	4.782	ns
	10 mA	GCLK	t_{CO}	5.660	6.324	7.018	ns
		GCLK PLL	t_{CO}	3.790	4.278	4.793	ns
	12 mA	GCLK	t_{CO}	5.648	6.315	7.013	ns
		GCLK PLL	t_{CO}	3.778	4.269	4.788	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.593	6.258	6.952	ns
		GCLK PLL	t_{CO}	3.723	4.212	4.727	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.885	7.884	8.920	ns
		GCLK PLL	t_{CO}	5.015	5.838	6.695	ns
	10 mA	GCLK	t_{CO}	6.824	7.799	8.811	ns
		GCLK PLL	t_{CO}	4.954	5.753	6.586	ns
3.0-V PCI	—	GCLK	t_{CO}	4.922	5.383	5.868	ns
		GCLK PLL	t_{CO}	3.081	3.369	3.675	ns
3.0-V PCI-X	—	GCLK	t_{CO}	4.922	5.383	5.868	ns
		GCLK PLL	t_{CO}	3.081	3.369	3.675	ns

Table 1–58. EP3C10 Column Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.953	1.036	1.096	ns
			t_{H}	–0.675	–0.720	–0.743	ns
	—	GCLK PLL	t_{SU}	2.798	3.057	3.295	ns
			t_{H}	–2.520	–2.741	–2.942	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.700	5.190	5.711	ns
		GCLK PLL	t_{CO}	2.867	3.183	3.525	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.700	5.190	5.711	ns
		GCLK PLL	t_{CO}	2.867	3.183	3.525	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.081	5.569	6.089	ns
		GCLK PLL	t_{CO}	3.248	3.562	3.903	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.700	5.190	5.711	ns
		GCLK PLL	t_{CO}	2.867	3.183	3.525	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.700	5.190	5.711	ns
		GCLK PLL	t_{CO}	2.867	3.183	3.525	ns

Table 1–59. EP3C10 Row Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	1.035	1.120	1.190	ns
			t_{H}	–0.757	–0.805	–0.836	ns
			t_{CO}	3.879	4.265	4.675	ns
	—	GCLK PLL	t_{SU}	2.819	3.079	3.329	ns
			t_{H}	–2.541	–2.764	–2.975	ns
			t_{CO}	2.021	2.233	2.462	ns
mini-LVDS	—	GCLK	t_{CO}	3.879	4.265	4.675	ns
		GCLK PLL	t_{CO}	2.021	2.233	2.462	ns
PPDS	—	GCLK	t_{CO}	3.879	4.265	4.675	ns
		GCLK PLL	t_{CO}	2.021	2.233	2.462	ns
RSDS	—	GCLK	t_{CO}	3.879	4.265	4.675	ns
		GCLK PLL	t_{CO}	2.021	2.233	2.462	ns

EP3C16 I/O Timing Parameters

Table 1–60 through Table 1–71 show the maximum I/O timing parameters for EP3C16 devices.

Table 1–60. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
	8 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
	8 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
	12 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
	16 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns

Table 1–60. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
	8 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
	12 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
	16 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
2.5V	4 mA	GCLK	t_{SU}	1.043	1.081	1.103	ns
			t_H	–0.763	–0.764	–0.750	ns
		GCLK PLL	t_{SU}	2.696	2.892	3.074	ns
			t_H	–2.416	–2.575	–2.721	ns
	8 mA	GCLK	t_{SU}	1.043	1.081	1.103	ns
			t_H	–0.763	–0.764	–0.750	ns
		GCLK PLL	t_{SU}	2.696	2.892	3.074	ns
			t_H	–2.416	–2.575	–2.721	ns
	12 mA	GCLK	t_{SU}	1.043	1.081	1.103	ns
			t_H	–0.763	–0.764	–0.750	ns
		GCLK PLL	t_{SU}	2.696	2.892	3.074	ns
			t_H	–2.416	–2.575	–2.721	ns
	16 mA	GCLK	t_{SU}	1.043	1.081	1.103	ns
			t_H	–0.763	–0.764	–0.750	ns
		GCLK PLL	t_{SU}	2.696	2.892	3.074	ns
			t_H	–2.416	–2.575	–2.721	ns

Table 1–60. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	2 mA	GCLK	t_{SU}	0.978	1.042	1.090	ns
			t_H	–0.700	–0.726	–0.736	ns
		GCLK PLL	t_{SU}	2.630	2.852	3.061	ns
			t_H	–2.352	–2.536	–2.707	ns
	4 mA	GCLK	t_{SU}	0.978	1.042	1.090	ns
			t_H	–0.700	–0.726	–0.736	ns
		GCLK PLL	t_{SU}	2.630	2.852	3.061	ns
			t_H	–2.352	–2.536	–2.707	ns
	6 mA	GCLK	t_{SU}	0.978	1.042	1.090	ns
			t_H	–0.700	–0.726	–0.736	ns
		GCLK PLL	t_{SU}	2.630	2.852	3.061	ns
			t_H	–2.352	–2.536	–2.707	ns
	8 mA	GCLK	t_{SU}	0.978	1.042	1.090	ns
			t_H	–0.700	–0.726	–0.736	ns
		GCLK PLL	t_{SU}	2.630	2.852	3.061	ns
			t_H	–2.352	–2.536	–2.707	ns
	10 mA	GCLK	t_{SU}	0.978	1.042	1.090	ns
			t_H	–0.700	–0.726	–0.736	ns
		GCLK PLL	t_{SU}	2.630	2.852	3.061	ns
			t_H	–2.352	–2.536	–2.707	ns
	12 mA	GCLK	t_{SU}	0.978	1.042	1.090	ns
			t_H	–0.700	–0.726	–0.736	ns
		GCLK PLL	t_{SU}	2.630	2.852	3.061	ns
			t_H	–2.352	–2.536	–2.707	ns
	16 mA	GCLK	t_{SU}	0.978	1.042	1.090	ns
			t_H	–0.700	–0.726	–0.736	ns
		GCLK PLL	t_{SU}	2.630	2.852	3.061	ns
			t_H	–2.352	–2.536	–2.707	ns
1.5V	2 mA	GCLK	t_{SU}	1.047	1.134	1.207	ns
			t_H	–0.767	–0.816	–0.851	ns
		GCLK PLL	t_{SU}	2.699	2.944	3.178	ns
			t_H	–2.419	–2.626	–2.822	ns
	4 mA	GCLK	t_{SU}	1.047	1.134	1.207	ns
			t_H	–0.767	–0.816	–0.851	ns
		GCLK PLL	t_{SU}	2.699	2.944	3.178	ns
			t_H	–2.419	–2.626	–2.822	ns
	6 mA	GCLK	t_{SU}	1.047	1.134	1.207	ns
			t_H	–0.767	–0.816	–0.851	ns
		GCLK PLL	t_{SU}	2.699	2.944	3.178	ns
			t_H	–2.419	–2.626	–2.822	ns

Table 1–60. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	8 mA	GCLK	t_{SU}	1.047	1.134	1.207	ns
			t_H	–0.767	–0.816	–0.851	ns
		GCLK PLL	t_{SU}	2.699	2.944	3.178	ns
			t_H	–2.419	–2.626	–2.822	ns
	10 mA	GCLK	t_{SU}	1.047	1.134	1.207	ns
			t_H	–0.767	–0.816	–0.851	ns
		GCLK PLL	t_{SU}	2.699	2.944	3.178	ns
			t_H	–2.419	–2.626	–2.822	ns
	12 mA	GCLK	t_{SU}	1.047	1.134	1.207	ns
			t_H	–0.767	–0.816	–0.851	ns
		GCLK PLL	t_{SU}	2.699	2.944	3.178	ns
			t_H	–2.419	–2.626	–2.822	ns
	16 mA	GCLK	t_{SU}	1.047	1.134	1.207	ns
			t_H	–0.767	–0.816	–0.851	ns
		GCLK PLL	t_{SU}	2.699	2.944	3.178	ns
			t_H	–2.419	–2.626	–2.822	ns
1.2V	2 mA	GCLK	t_{SU}	1.199	1.314	1.413	ns
			t_H	–0.917	–0.992	–1.053	ns
		GCLK PLL	t_{SU}	2.851	3.124	3.384	ns
			t_H	–2.569	–2.802	–3.024	ns
	4 mA	GCLK	t_{SU}	1.199	1.314	1.413	ns
			t_H	–0.917	–0.992	–1.053	ns
		GCLK PLL	t_{SU}	2.851	3.124	3.384	ns
			t_H	–2.569	–2.802	–3.024	ns
	6 mA	GCLK	t_{SU}	1.199	1.314	1.413	ns
			t_H	–0.917	–0.992	–1.053	ns
		GCLK PLL	t_{SU}	2.851	3.124	3.384	ns
			t_H	–2.569	–2.802	–3.024	ns
	8 mA	GCLK	t_{SU}	1.199	1.314	1.413	ns
			t_H	–0.917	–0.992	–1.053	ns
		GCLK PLL	t_{SU}	2.851	3.124	3.384	ns
			t_H	–2.569	–2.802	–3.024	ns
	10 mA	GCLK	t_{SU}	1.199	1.314	1.413	ns
			t_H	–0.917	–0.992	–1.053	ns
		GCLK PLL	t_{SU}	2.851	3.124	3.384	ns
			t_H	–2.569	–2.802	–3.024	ns
	12 mA	GCLK	t_{SU}	1.199	1.314	1.413	ns
			t_H	–0.917	–0.992	–1.053	ns
		GCLK PLL	t_{SU}	2.851	3.124	3.384	ns
			t_H	–2.569	–2.802	–3.024	ns

Table 1–60. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-2 Class I	8 mA	GCLK	t_{SU}	1.032	1.100	1.152	ns
			t_H	–0.752	–0.783	–0.797	ns
		GCLK PLL	t_{SU}	2.685	2.909	3.123	ns
			t_H	–2.405	–2.592	–2.768	ns
	12 mA	GCLK	t_{SU}	1.032	1.100	1.152	ns
			t_H	–0.752	–0.783	–0.797	ns
		GCLK PLL	t_{SU}	2.685	2.909	3.123	ns
			t_H	–2.405	–2.592	–2.768	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	1.032	1.100	1.152	ns
			t_H	–0.752	–0.783	–0.797	ns
		GCLK PLL	t_{SU}	2.685	2.909	3.123	ns
			t_H	–2.405	–2.592	–2.768	ns
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.093	1.189	1.267	ns
			t_H	–0.813	–0.870	–0.910	ns
		GCLK PLL	t_{SU}	2.745	2.998	3.238	ns
			t_H	–2.465	–2.679	–2.881	ns
	10 mA	GCLK	t_{SU}	1.093	1.189	1.267	ns
			t_H	–0.813	–0.870	–0.910	ns
		GCLK PLL	t_{SU}	2.745	2.998	3.238	ns
			t_H	–2.465	–2.679	–2.881	ns
	12 mA	GCLK	t_{SU}	1.093	1.189	1.267	ns
			t_H	–0.813	–0.870	–0.910	ns
		GCLK PLL	t_{SU}	2.745	2.998	3.238	ns
			t_H	–2.465	–2.679	–2.881	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.093	1.189	1.267	ns
			t_H	–0.813	–0.870	–0.910	ns
		GCLK PLL	t_{SU}	2.745	2.998	3.238	ns
			t_H	–2.465	–2.679	–2.881	ns
	16 mA	GCLK	t_{SU}	1.093	1.189	1.267	ns
			t_H	–0.813	–0.870	–0.910	ns
		GCLK PLL	t_{SU}	2.745	2.998	3.238	ns
			t_H	–2.465	–2.679	–2.881	ns

Table 1–60. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.093	1.189	1.267	ns
			t_H	–0.813	–0.870	–0.910	ns
		GCLK PLL	t_{SU}	2.745	2.998	3.238	ns
			t_H	–2.465	–2.679	–2.881	ns
	10 mA	GCLK	t_{SU}	1.093	1.189	1.267	ns
			t_H	–0.813	–0.870	–0.910	ns
		GCLK PLL	t_{SU}	2.745	2.998	3.238	ns
			t_H	–2.465	–2.679	–2.881	ns
	12 mA	GCLK	t_{SU}	1.093	1.189	1.267	ns
			t_H	–0.813	–0.870	–0.910	ns
		GCLK PLL	t_{SU}	2.745	2.998	3.238	ns
			t_H	–2.465	–2.679	–2.881	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.093	1.189	1.267	ns
			t_H	–0.813	–0.870	–0.910	ns
		GCLK PLL	t_{SU}	2.745	2.998	3.238	ns
			t_H	–2.465	–2.679	–2.881	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	1.049	1.149	1.233	ns
			t_H	–0.769	–0.831	–0.877	ns
		GCLK PLL	t_{SU}	2.701	2.958	3.204	ns
			t_H	–2.421	–2.640	–2.848	ns
	10 mA	GCLK	t_{SU}	1.049	1.149	1.233	ns
			t_H	–0.769	–0.831	–0.877	ns
		GCLK PLL	t_{SU}	2.701	2.958	3.204	ns
			t_H	–2.421	–2.640	–2.848	ns
	12 mA	GCLK	t_{SU}	1.049	1.149	1.233	ns
			t_H	–0.769	–0.831	–0.877	ns
		GCLK PLL	t_{SU}	2.701	2.958	3.204	ns
			t_H	–2.421	–2.640	–2.848	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	1.049	1.149	1.233	ns
			t_H	–0.769	–0.831	–0.877	ns
		GCLK PLL	t_{SU}	2.701	2.958	3.204	ns
			t_H	–2.421	–2.640	–2.848	ns

Table 1–60. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.181	1.308	1.417	ns
			t_H	–0.899	–0.986	–1.057	ns
		GCLK PLL	t_{SU}	2.833	3.117	3.388	ns
			t_H	–2.551	–2.795	–3.028	ns
	10 mA	GCLK	t_{SU}	1.181	1.308	1.417	ns
			t_H	–0.899	–0.986	–1.057	ns
		GCLK PLL	t_{SU}	2.833	3.117	3.388	ns
			t_H	–2.551	–2.795	–3.028	ns
	12 mA	GCLK	t_{SU}	1.181	1.308	1.417	ns
			t_H	–0.899	–0.986	–1.057	ns
		GCLK PLL	t_{SU}	2.833	3.117	3.388	ns
			t_H	–2.551	–2.795	–3.028	ns
1.2–V HSTL Class II	14 mA	GCLK	t_{SU}	1.181	1.308	1.417	ns
			t_H	–0.899	–0.986	–1.057	ns
		GCLK PLL	t_{SU}	2.833	3.117	3.388	ns
			t_H	–2.551	–2.795	–3.028	ns
3.0-V PCI	—	GCLK	t_{SU}	1.096	1.122	1.130	ns
			t_H	–0.816	–0.804	–0.776	ns
	—	GCLK PLL	t_{SU}	2.749	2.933	3.101	ns
			t_H	–2.469	–2.615	–2.747	ns
3.0-V PCI-X	—	GCLK	t_{SU}	1.096	1.122	1.130	ns
			t_H	–0.816	–0.804	–0.776	ns
	—	GCLK PLL	t_{SU}	2.749	2.933	3.101	ns
			t_H	–2.469	–2.615	–2.747	ns

Table 1–61. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns
	8 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns

Table 1–61. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns
	8 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns
	12 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns
	16 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns
	8 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns
	12 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns
	16 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns

Table 1–61. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
2.5V	4 mA	GCLK	t_{SU}	1.084	1.129	1.158	ns
			t_H	–0.804	–0.812	–0.804	ns
		GCLK PLL	t_{SU}	2.739	2.942	3.135	ns
			t_H	–2.459	–2.625	–2.781	ns
	8 mA	GCLK	t_{SU}	1.084	1.129	1.158	ns
			t_H	–0.804	–0.812	–0.804	ns
		GCLK PLL	t_{SU}	2.739	2.942	3.135	ns
			t_H	–2.459	–2.625	–2.781	ns
	12 mA	GCLK	t_{SU}	1.084	1.129	1.158	ns
			t_H	–0.804	–0.812	–0.804	ns
		GCLK PLL	t_{SU}	2.739	2.942	3.135	ns
			t_H	–2.459	–2.625	–2.781	ns
	16 mA	GCLK	t_{SU}	1.084	1.129	1.158	ns
			t_H	–0.804	–0.812	–0.804	ns
		GCLK PLL	t_{SU}	2.739	2.942	3.135	ns
			t_H	–2.459	–2.625	–2.781	ns
1.8V	2 mA	GCLK	t_{SU}	1.020	1.090	1.144	ns
			t_H	–0.742	–0.774	–0.789	ns
		GCLK PLL	t_{SU}	2.675	2.903	3.121	ns
			t_H	–2.397	–2.587	–2.766	ns
	4 mA	GCLK	t_{SU}	1.020	1.090	1.144	ns
			t_H	–0.742	–0.774	–0.789	ns
		GCLK PLL	t_{SU}	2.675	2.903	3.121	ns
			t_H	–2.397	–2.587	–2.766	ns
	6 mA	GCLK	t_{SU}	1.020	1.090	1.144	ns
			t_H	–0.742	–0.774	–0.789	ns
		GCLK PLL	t_{SU}	2.675	2.903	3.121	ns
			t_H	–2.397	–2.587	–2.766	ns
	8 mA	GCLK	t_{SU}	1.020	1.090	1.144	ns
			t_H	–0.742	–0.774	–0.789	ns
		GCLK PLL	t_{SU}	2.675	2.903	3.121	ns
			t_H	–2.397	–2.587	–2.766	ns
	10 mA	GCLK	t_{SU}	1.020	1.090	1.144	ns
			t_H	–0.742	–0.774	–0.789	ns
		GCLK PLL	t_{SU}	2.675	2.903	3.121	ns
			t_H	–2.397	–2.587	–2.766	ns
	12 mA	GCLK	t_{SU}	1.020	1.090	1.144	ns
			t_H	–0.742	–0.774	–0.789	ns
		GCLK PLL	t_{SU}	2.675	2.903	3.121	ns
			t_H	–2.397	–2.587	–2.766	ns

Table 1–61. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	16 mA	GCLK	t_{SU}	1.020	1.090	1.144	ns
			t_H	–0.742	–0.774	–0.789	ns
		GCLK PLL	t_{SU}	2.675	2.903	3.121	ns
			t_H	–2.397	–2.587	–2.766	ns
1.5V	2 mA	GCLK	t_{SU}	1.089	1.183	1.262	ns
			t_H	–0.809	–0.865	–0.906	ns
		GCLK PLL	t_{SU}	2.744	2.996	3.239	ns
			t_H	–2.464	–2.678	–2.883	ns
	4 mA	GCLK	t_{SU}	1.089	1.183	1.262	ns
			t_H	–0.809	–0.865	–0.906	ns
		GCLK PLL	t_{SU}	2.744	2.996	3.239	ns
			t_H	–2.464	–2.678	–2.883	ns
	6 mA	GCLK	t_{SU}	1.089	1.183	1.262	ns
			t_H	–0.809	–0.865	–0.906	ns
		GCLK PLL	t_{SU}	2.744	2.996	3.239	ns
			t_H	–2.464	–2.678	–2.883	ns
	8 mA	GCLK	t_{SU}	1.089	1.183	1.262	ns
			t_H	–0.809	–0.865	–0.906	ns
		GCLK PLL	t_{SU}	2.744	2.996	3.239	ns
			t_H	–2.464	–2.678	–2.883	ns
	10 mA	GCLK	t_{SU}	1.089	1.183	1.262	ns
			t_H	–0.809	–0.865	–0.906	ns
		GCLK PLL	t_{SU}	2.744	2.996	3.239	ns
			t_H	–2.464	–2.678	–2.883	ns
	12 mA	GCLK	t_{SU}	1.089	1.183	1.262	ns
			t_H	–0.809	–0.865	–0.906	ns
		GCLK PLL	t_{SU}	2.744	2.996	3.239	ns
			t_H	–2.464	–2.678	–2.883	ns
	16 mA	GCLK	t_{SU}	1.089	1.183	1.262	ns
			t_H	–0.809	–0.865	–0.906	ns
		GCLK PLL	t_{SU}	2.744	2.996	3.239	ns
			t_H	–2.464	–2.678	–2.883	ns
1.2V	2 mA	GCLK	t_{SU}	1.242	1.363	1.469	ns
			t_H	–0.960	–1.041	–1.108	ns
		GCLK PLL	t_{SU}	2.897	3.176	3.446	ns
			t_H	–2.615	–2.854	–3.085	ns
	4 mA	GCLK	t_{SU}	1.242	1.363	1.469	ns
			t_H	–0.960	–1.041	–1.108	ns
		GCLK PLL	t_{SU}	2.897	3.176	3.446	ns
			t_H	–2.615	–2.854	–3.085	ns

Table 1–61. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	6 mA	GCLK	t_{SU}	1.242	1.363	1.469	ns
			t_H	–0.960	–1.041	–1.108	ns
		GCLK PLL	t_{SU}	2.897	3.176	3.446	ns
			t_H	–2.615	–2.854	–3.085	ns
	8 mA	GCLK	t_{SU}	1.242	1.363	1.469	ns
			t_H	–0.960	–1.041	–1.108	ns
		GCLK PLL	t_{SU}	2.897	3.176	3.446	ns
			t_H	–2.615	–2.854	–3.085	ns
	10 mA	GCLK	t_{SU}	1.242	1.363	1.469	ns
			t_H	–0.960	–1.041	–1.108	ns
		GCLK PLL	t_{SU}	2.897	3.176	3.446	ns
			t_H	–2.615	–2.854	–3.085	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	1.074	1.148	1.209	ns
			t_H	–0.794	–0.830	–0.853	ns
		GCLK PLL	t_{SU}	2.729	2.952	3.174	ns
			t_H	–2.449	–2.634	–2.818	ns
	12 mA	GCLK	t_{SU}	1.074	1.148	1.209	ns
			t_H	–0.794	–0.830	–0.853	ns
		GCLK PLL	t_{SU}	2.729	2.952	3.174	ns
			t_H	–2.449	–2.634	–2.818	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	1.074	1.148	1.209	ns
			t_H	–0.794	–0.830	–0.853	ns
		GCLK PLL	t_{SU}	2.729	2.952	3.174	ns
			t_H	–2.449	–2.634	–2.818	ns
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.136	1.237	1.326	ns
			t_H	–0.856	–0.918	–0.968	ns
		GCLK PLL	t_{SU}	2.791	3.041	3.291	ns
			t_H	–2.511	–2.722	–2.933	ns
	10 mA	GCLK	t_{SU}	1.136	1.237	1.326	ns
			t_H	–0.856	–0.918	–0.968	ns
		GCLK PLL	t_{SU}	2.791	3.041	3.291	ns
			t_H	–2.511	–2.722	–2.933	ns
	12 mA	GCLK	t_{SU}	1.136	1.237	1.326	ns
			t_H	–0.856	–0.918	–0.968	ns
		GCLK PLL	t_{SU}	2.791	3.041	3.291	ns
			t_H	–2.511	–2.722	–2.933	ns

Table 1–61. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.136	1.237	1.326	ns
			t_H	–0.856	–0.918	–0.968	ns
		GCLK PLL	t_{SU}	2.791	3.041	3.291	ns
			t_H	–2.511	–2.722	–2.933	ns
	16 mA	GCLK	t_{SU}	1.136	1.237	1.326	ns
			t_H	–0.856	–0.918	–0.968	ns
		GCLK PLL	t_{SU}	2.791	3.041	3.291	ns
			t_H	–2.511	–2.722	–2.933	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.136	1.237	1.326	ns
			t_H	–0.856	–0.918	–0.968	ns
		GCLK PLL	t_{SU}	2.791	3.041	3.291	ns
			t_H	–2.511	–2.722	–2.933	ns
	10 mA	GCLK	t_{SU}	1.136	1.237	1.326	ns
			t_H	–0.856	–0.918	–0.968	ns
		GCLK PLL	t_{SU}	2.791	3.041	3.291	ns
			t_H	–2.511	–2.722	–2.933	ns
	12 mA	GCLK	t_{SU}	1.136	1.237	1.326	ns
			t_H	–0.856	–0.918	–0.968	ns
		GCLK PLL	t_{SU}	2.791	3.041	3.291	ns
			t_H	–2.511	–2.722	–2.933	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.136	1.237	1.326	ns
			t_H	–0.856	–0.918	–0.968	ns
		GCLK PLL	t_{SU}	2.791	3.041	3.291	ns
			t_H	–2.511	–2.722	–2.933	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	1.091	1.196	1.289	ns
			t_H	–0.811	–0.878	–0.932	ns
		GCLK PLL	t_{SU}	2.746	3.000	3.254	ns
			t_H	–2.466	–2.682	–2.897	ns
	10 mA	GCLK	t_{SU}	1.091	1.196	1.289	ns
			t_H	–0.811	–0.878	–0.932	ns
		GCLK PLL	t_{SU}	2.746	3.000	3.254	ns
			t_H	–2.466	–2.682	–2.897	ns
	12 mA	GCLK	t_{SU}	1.091	1.196	1.289	ns
			t_H	–0.811	–0.878	–0.932	ns
		GCLK PLL	t_{SU}	2.746	3.000	3.254	ns
			t_H	–2.466	–2.682	–2.897	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	1.091	1.196	1.289	ns
			t_H	–0.811	–0.878	–0.932	ns
		GCLK PLL	t_{SU}	2.746	3.000	3.254	ns
			t_H	–2.466	–2.682	–2.897	ns

Table 1–61. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.222	1.354	1.474	ns
			t_H	–0.940	–1.032	–1.114	ns
		GCLK PLL	t_{SU}	2.877	3.158	3.439	ns
			t_H	–2.595	–2.836	–3.079	ns
1.2-V HSTL Class I	10 mA	GCLK	t_{SU}	1.222	1.354	1.474	ns
			t_H	–0.940	–1.032	–1.114	ns
		GCLK PLL	t_{SU}	2.877	3.158	3.439	ns
			t_H	–2.595	–2.836	–3.079	ns
3.0-V PCI	—	GCLK	t_{SU}	1.137	1.169	1.183	ns
			t_H	–0.857	–0.851	–0.828	ns
	—	GCLK PLL	t_{SU}	2.792	2.982	3.160	ns
			t_H	–2.512	–2.664	–2.805	ns
3.0-V PCI-X	—	GCLK	t_{SU}	1.137	1.169	1.183	ns
			t_H	–0.857	–0.851	–0.828	ns
	—	GCLK PLL	t_{SU}	2.792	2.982	3.160	ns
			t_H	–2.512	–2.664	–2.805	ns

Table 1–62. EP3C16 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.480	5.983	6.509	ns
		GCLK PLL	t_{CO}	3.827	4.173	4.537	ns
	8 mA	GCLK	t_{CO}	5.480	5.983	6.509	ns
		GCLK PLL	t_{CO}	3.827	4.173	4.537	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.439	5.764	6.111	ns
		GCLK PLL	t_{CO}	3.786	3.954	4.139	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.190	5.686	6.207	ns
		GCLK PLL	t_{CO}	3.537	3.876	4.235	ns
	8 mA	GCLK	t_{CO}	4.919	5.402	5.908	ns
		GCLK PLL	t_{CO}	3.266	3.592	3.936	ns
	12 mA	GCLK	t_{CO}	4.822	5.301	5.804	ns
		GCLK PLL	t_{CO}	3.169	3.491	3.832	ns
	16 mA	GCLK	t_{CO}	4.775	5.249	5.746	ns
		GCLK PLL	t_{CO}	3.122	3.439	3.774	ns

Table 1–62. EP3C16 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.917	5.399	5.905	ns
		GCLK PLL	t_{CO}	3.264	3.589	3.933	ns
	8 mA	GCLK	t_{CO}	4.776	5.251	5.750	ns
		GCLK PLL	t_{CO}	3.123	3.441	3.778	ns
	12 mA	GCLK	t_{CO}	4.739	5.211	5.707	ns
		GCLK PLL	t_{CO}	3.086	3.401	3.735	ns
	16 mA	GCLK	t_{CO}	4.723	5.196	5.692	ns
		GCLK PLL	t_{CO}	3.070	3.386	3.720	ns
2.5V	4 mA	GCLK	t_{CO}	5.248	5.772	6.321	ns
		GCLK PLL	t_{CO}	3.595	3.962	4.349	ns
	8 mA	GCLK	t_{CO}	5.005	5.519	6.057	ns
		GCLK PLL	t_{CO}	3.352	3.709	4.085	ns
	12 mA	GCLK	t_{CO}	4.907	5.413	5.944	ns
		GCLK PLL	t_{CO}	3.254	3.603	3.972	ns
	16 mA	GCLK	t_{CO}	4.868	5.373	5.903	ns
		GCLK PLL	t_{CO}	3.215	3.563	3.931	ns
1.8V	2 mA	GCLK	t_{CO}	6.359	7.025	7.719	ns
		GCLK PLL	t_{CO}	4.707	5.215	5.747	ns
	4 mA	GCLK	t_{CO}	5.832	6.480	7.155	ns
		GCLK PLL	t_{CO}	4.180	4.670	5.183	ns
	6 mA	GCLK	t_{CO}	5.607	6.222	6.863	ns
		GCLK PLL	t_{CO}	3.955	4.412	4.891	ns
	8 mA	GCLK	t_{CO}	5.504	6.105	6.734	ns
		GCLK PLL	t_{CO}	3.852	4.295	4.762	ns
	10 mA	GCLK	t_{CO}	5.452	6.057	6.688	ns
		GCLK PLL	t_{CO}	3.800	4.247	4.716	ns
	12 mA	GCLK	t_{CO}	5.395	5.990	6.613	ns
		GCLK PLL	t_{CO}	3.743	4.180	4.641	ns
	16 mA	GCLK	t_{CO}	5.341	5.931	6.548	ns
		GCLK PLL	t_{CO}	3.689	4.121	4.576	ns
1.5V	2 mA	GCLK	t_{CO}	6.747	7.587	8.458	ns
		GCLK PLL	t_{CO}	5.095	5.777	6.486	ns
	4 mA	GCLK	t_{CO}	6.272	7.026	7.810	ns
		GCLK PLL	t_{CO}	4.620	5.216	5.838	ns
	6 mA	GCLK	t_{CO}	6.102	6.843	7.613	ns
		GCLK PLL	t_{CO}	4.450	5.033	5.641	ns
	8 mA	GCLK	t_{CO}	6.014	6.730	7.475	ns
		GCLK PLL	t_{CO}	4.362	4.920	5.503	ns

Table 1–62. EP3C16 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	10 mA	GCLK	t_{CO}	5.955	6.670	7.414	ns
		GCLK PLL	t_{CO}	4.303	4.860	5.442	ns
	12 mA	GCLK	t_{CO}	5.922	6.629	7.364	ns
		GCLK PLL	t_{CO}	4.270	4.819	5.392	ns
	16 mA	GCLK	t_{CO}	5.808	6.487	7.194	ns
		GCLK PLL	t_{CO}	4.156	4.677	5.222	ns
1.2V	2 mA	GCLK	t_{CO}	7.920	9.115	10.347	ns
		GCLK PLL	t_{CO}	6.268	7.305	8.375	ns
	4 mA	GCLK	t_{CO}	7.475	8.589	9.740	ns
		GCLK PLL	t_{CO}	5.823	6.779	7.768	ns
	6 mA	GCLK	t_{CO}	7.326	8.408	9.526	ns
		GCLK PLL	t_{CO}	5.674	6.598	7.554	ns
	8 mA	GCLK	t_{CO}	7.257	8.328	9.436	ns
		GCLK PLL	t_{CO}	5.605	6.518	7.464	ns
	10 mA	GCLK	t_{CO}	7.121	8.146	9.205	ns
		GCLK PLL	t_{CO}	5.469	6.336	7.233	ns
	12 mA	GCLK	t_{CO}	7.093	8.120	9.183	ns
		GCLK PLL	t_{CO}	5.441	6.310	7.211	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.863	5.361	5.885	ns
		GCLK PLL	t_{CO}	3.210	3.552	3.913	ns
	12 mA	GCLK	t_{CO}	4.841	5.337	5.862	ns
		GCLK PLL	t_{CO}	3.188	3.528	3.890	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.781	5.275	5.796	ns
		GCLK PLL	t_{CO}	3.128	3.466	3.824	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.297	5.874	6.480	ns
		GCLK PLL	t_{CO}	3.645	4.065	4.508	ns
	10 mA	GCLK	t_{CO}	5.272	5.843	6.443	ns
		GCLK PLL	t_{CO}	3.620	4.034	4.471	ns
	12 mA	GCLK	t_{CO}	5.260	5.829	6.426	ns
		GCLK PLL	t_{CO}	3.608	4.020	4.454	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.231	5.800	6.398	ns
		GCLK PLL	t_{CO}	3.579	3.991	4.426	ns
	16 mA	GCLK	t_{CO}	5.218	5.787	6.384	ns
		GCLK PLL	t_{CO}	3.566	3.978	4.412	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.259	5.826	6.422	ns
		GCLK PLL	t_{CO}	3.607	4.017	4.450	ns
	10 mA	GCLK	t_{CO}	5.248	5.819	6.418	ns
		GCLK PLL	t_{CO}	3.596	4.010	4.446	ns
	12 mA	GCLK	t_{CO}	5.239	5.805	6.398	ns
		GCLK PLL	t_{CO}	3.587	3.996	4.426	ns

Table 1–62. EP3C16 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.174	5.739	6.332	ns
		GCLK PLL	t_{CO}	3.522	3.930	4.360	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.773	6.447	7.153	ns
		GCLK PLL	t_{CO}	4.121	4.638	5.181	ns
	10 mA	GCLK	t_{CO}	5.776	6.447	7.148	ns
		GCLK PLL	t_{CO}	4.124	4.638	5.176	ns
	12 mA	GCLK	t_{CO}	5.764	6.439	7.144	ns
		GCLK PLL	t_{CO}	4.112	4.630	5.172	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.702	6.371	7.069	ns
		GCLK PLL	t_{CO}	4.050	4.562	5.097	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.986	7.985	9.020	ns
		GCLK PLL	t_{CO}	5.334	6.176	7.048	ns
	10 mA	GCLK	t_{CO}	6.924	7.896	8.904	ns
		GCLK PLL	t_{CO}	5.272	6.087	6.932	ns
	12 mA	GCLK	t_{CO}	6.926	7.902	8.913	ns
		GCLK PLL	t_{CO}	5.274	6.093	6.941	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.881	7.849	8.853	ns
		GCLK PLL	t_{CO}	5.229	6.040	6.881	ns
3.0-V PCI	—	GCLK	t_{CO}	5.070	5.543	6.041	ns
		GCLK PLL	t_{CO}	3.417	3.733	4.069	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.070	5.543	6.041	ns
		GCLK PLL	t_{CO}	3.417	3.733	4.069	ns

Table 1–63. EP3C16 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.412	5.907	6.427	ns
		GCLK PLL	t_{CO}	3.757	4.094	4.450	ns
	8 mA	GCLK	t_{CO}	5.412	5.907	6.427	ns
		GCLK PLL	t_{CO}	3.757	4.094	4.450	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.412	5.733	6.077	ns
		GCLK PLL	t_{CO}	3.757	3.920	4.100	ns

Table 1–63. EP3C16 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.126	5.614	6.128	ns
		GCLK PLL	t_{CO}	3.471	3.801	4.151	ns
	8 mA	GCLK	t_{CO}	4.869	5.347	5.851	ns
		GCLK PLL	t_{CO}	3.214	3.534	3.874	ns
	12 mA	GCLK	t_{CO}	4.780	5.252	5.749	ns
		GCLK PLL	t_{CO}	3.125	3.439	3.772	ns
	16 mA	GCLK	t_{CO}	4.734	5.201	5.694	ns
		GCLK PLL	t_{CO}	3.079	3.388	3.717	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.867	5.345	5.849	ns
		GCLK PLL	t_{CO}	3.212	3.532	3.872	ns
	8 mA	GCLK	t_{CO}	4.734	5.202	5.697	ns
		GCLK PLL	t_{CO}	3.079	3.389	3.720	ns
	12 mA	GCLK	t_{CO}	4.699	5.166	5.658	ns
		GCLK PLL	t_{CO}	3.044	3.353	3.681	ns
	16 mA	GCLK	t_{CO}	4.684	5.150	5.641	ns
		GCLK PLL	t_{CO}	3.029	3.337	3.664	ns
2.5V	4 mA	GCLK	t_{CO}	5.224	5.728	6.258	ns
		GCLK PLL	t_{CO}	3.569	3.915	4.281	ns
	8 mA	GCLK	t_{CO}	4.989	5.484	6.004	ns
		GCLK PLL	t_{CO}	3.334	3.671	4.027	ns
	12 mA	GCLK	t_{CO}	4.890	5.379	5.894	ns
		GCLK PLL	t_{CO}	3.235	3.566	3.917	ns
	16 mA	GCLK	t_{CO}	4.849	5.337	5.851	ns
		GCLK PLL	t_{CO}	3.194	3.524	3.874	ns
1.8V	2 mA	GCLK	t_{CO}	6.318	6.964	7.638	ns
		GCLK PLL	t_{CO}	4.663	5.151	5.661	ns
	4 mA	GCLK	t_{CO}	5.805	6.436	7.094	ns
		GCLK PLL	t_{CO}	4.150	4.623	5.117	ns
	6 mA	GCLK	t_{CO}	5.584	6.182	6.807	ns
		GCLK PLL	t_{CO}	3.929	4.369	4.830	ns
	8 mA	GCLK	t_{CO}	5.483	6.068	6.681	ns
		GCLK PLL	t_{CO}	3.828	4.255	4.704	ns
	10 mA	GCLK	t_{CO}	5.432	6.019	6.635	ns
		GCLK PLL	t_{CO}	3.777	4.206	4.658	ns
	12 mA	GCLK	t_{CO}	5.377	5.956	6.562	ns
		GCLK PLL	t_{CO}	3.722	4.143	4.585	ns
	16 mA	GCLK	t_{CO}	5.334	5.909	6.513	ns
		GCLK PLL	t_{CO}	3.679	4.096	4.536	ns

Table 1–63. EP3C16 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	2 mA	GCLK	t_{CO}	6.712	7.531	8.383	ns
		GCLK PLL	t_{CO}	5.057	5.718	6.406	ns
	4 mA	GCLK	t_{CO}	6.256	6.987	7.750	ns
		GCLK PLL	t_{CO}	4.601	5.174	5.773	ns
	6 mA	GCLK	t_{CO}	6.089	6.809	7.559	ns
		GCLK PLL	t_{CO}	4.434	4.996	5.582	ns
	8 mA	GCLK	t_{CO}	6.013	6.716	7.449	ns
		GCLK PLL	t_{CO}	4.358	4.903	5.472	ns
	10 mA	GCLK	t_{CO}	5.953	6.653	7.383	ns
		GCLK PLL	t_{CO}	4.298	4.840	5.406	ns
	12 mA	GCLK	t_{CO}	5.919	6.610	7.332	ns
		GCLK PLL	t_{CO}	4.264	4.797	5.355	ns
	16 mA	GCLK	t_{CO}	5.822	6.502	7.213	ns
		GCLK PLL	t_{CO}	4.167	4.689	5.236	ns
1.2V	2 mA	GCLK	t_{CO}	7.900	9.071	10.279	ns
		GCLK PLL	t_{CO}	6.245	7.258	8.302	ns
	4 mA	GCLK	t_{CO}	7.465	8.557	9.687	ns
		GCLK PLL	t_{CO}	5.810	6.744	7.710	ns
	6 mA	GCLK	t_{CO}	7.337	8.403	9.508	ns
		GCLK PLL	t_{CO}	5.682	6.590	7.531	ns
	8 mA	GCLK	t_{CO}	7.265	8.321	9.413	ns
		GCLK PLL	t_{CO}	5.610	6.508	7.436	ns
	10 mA	GCLK	t_{CO}	7.134	8.158	9.218	ns
		GCLK PLL	t_{CO}	5.479	6.345	7.241	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.818	5.311	5.829	ns
		GCLK PLL	t_{CO}	3.163	3.507	3.864	ns
	12 mA	GCLK	t_{CO}	4.799	5.292	5.808	ns
		GCLK PLL	t_{CO}	3.144	3.488	3.843	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.744	5.235	5.748	ns
		GCLK PLL	t_{CO}	3.089	3.431	3.783	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.252	5.826	6.424	ns
		GCLK PLL	t_{CO}	3.597	4.022	4.459	ns
	10 mA	GCLK	t_{CO}	5.239	5.808	6.403	ns
		GCLK PLL	t_{CO}	3.584	4.004	4.438	ns
	12 mA	GCLK	t_{CO}	5.226	5.793	6.385	ns
		GCLK PLL	t_{CO}	3.571	3.989	4.420	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.196	5.764	6.357	ns
		GCLK PLL	t_{CO}	3.541	3.960	4.392	ns
	16 mA	GCLK	t_{CO}	5.188	5.758	6.352	ns
		GCLK PLL	t_{CO}	3.533	3.954	4.387	ns

Table 1–63. EP3C16 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.216	5.780	6.369	ns
		GCLK PLL	t_{CO}	3.561	3.976	4.404	ns
	10 mA	GCLK	t_{CO}	5.211	5.776	6.366	ns
		GCLK PLL	t_{CO}	3.556	3.972	4.401	ns
	12 mA	GCLK	t_{CO}	5.204	5.769	6.359	ns
		GCLK PLL	t_{CO}	3.549	3.965	4.394	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.142	5.703	6.288	ns
		GCLK PLL	t_{CO}	3.487	3.899	4.323	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.731	6.401	7.098	ns
		GCLK PLL	t_{CO}	4.076	4.597	5.133	ns
	10 mA	GCLK	t_{CO}	5.743	6.413	7.109	ns
		GCLK PLL	t_{CO}	4.088	4.609	5.144	ns
	12 mA	GCLK	t_{CO}	5.731	6.404	7.104	ns
		GCLK PLL	t_{CO}	4.076	4.600	5.139	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.676	6.347	7.043	ns
		GCLK PLL	t_{CO}	4.021	4.543	5.078	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.968	7.973	9.011	ns
		GCLK PLL	t_{CO}	5.313	6.169	7.046	ns
	10 mA	GCLK	t_{CO}	6.907	7.888	8.902	ns
		GCLK PLL	t_{CO}	5.252	6.084	6.937	ns
3.0-V PCI	—	GCLK	t_{CO}	5.026	5.493	5.984	ns
		GCLK PLL	t_{CO}	3.371	3.680	4.007	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.026	5.493	5.984	ns
		GCLK PLL	t_{CO}	3.371	3.680	4.007	ns

Table 1–64. EP3C16 Column Pin Differential I/O Timing Parameters (Part 1 of 2)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.928	1.003	1.060	ns
			t_{H}	–0.650	–0.687	–0.707	ns
		GCLK PLL	t_{SU}	2.581	2.813	3.032	ns
			t_{H}	–2.303	–2.497	–2.679	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.810	5.307	5.829	ns
		GCLK PLL	t_{CO}	3.157	3.497	3.857	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.810	5.307	5.829	ns
		GCLK PLL	t_{CO}	3.157	3.497	3.857	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.191	5.686	6.207	ns
		GCLK PLL	t_{CO}	3.538	3.876	4.235	ns

Table 1–64. EP3C16 Column Pin Differential I/O Timing Parameters (Part 2 of 2)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
RSDS_E_1R	—	GCLK	t_{CO}	4.810	5.307	5.829	ns
		GCLK PLL	t_{CO}	3.157	3.497	3.857	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.810	5.307	5.829	ns
		GCLK PLL	t_{CO}	3.157	3.497	3.857	ns

Table 1–65. EP3C16 Row Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.959	1.038	1.105	ns
			t_{H}	–0.681	–0.723	–0.751	ns
			t_{CO}	3.983	4.375	4.789	ns
	—	GCLK PLL	t_{SU}	2.612	2.848	3.077	ns
			t_{H}	–2.334	–2.533	–2.723	ns
			t_{CO}	2.330	2.565	2.817	ns
mini-LVDS	—	GCLK	t_{CO}	3.983	4.375	4.789	ns
		GCLK PLL	t_{CO}	2.330	2.565	2.817	ns
PPDS	—	GCLK	t_{CO}	3.983	4.375	4.789	ns
		GCLK PLL	t_{CO}	2.330	2.565	2.817	ns
RSDS	—	GCLK	t_{CO}	3.983	4.375	4.789	ns
		GCLK PLL	t_{CO}	2.330	2.565	2.817	ns

EP3C25 I/O Timing Parameters

Table 1–66 through Table 1–71 show the maximum I/O timing parameters for EP3C25 devices.

Table 1–66. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_{H}	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_{H}	–2.513	–2.665	–2.801	ns
	8 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_{H}	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_{H}	–2.513	–2.665	–2.801	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_{H}	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_{H}	–2.513	–2.665	–2.801	ns

Table 1–66. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVTTL	4 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns
	8 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns
	12 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns
	16 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns
	8 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns
	12 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns
	16 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns

Table 1–66. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
2.5V	4 mA	GCLK	t_{SU}	0.992	1.025	1.040	ns
			t_H	–0.712	–0.708	–0.687	ns
		GCLK PLL	t_{SU}	2.736	2.938	3.123	ns
			t_H	–2.456	–2.621	–2.770	ns
	8 mA	GCLK	t_{SU}	0.992	1.025	1.040	ns
			t_H	–0.712	–0.708	–0.687	ns
		GCLK PLL	t_{SU}	2.736	2.938	3.123	ns
			t_H	–2.456	–2.621	–2.770	ns
	12 mA	GCLK	t_{SU}	0.992	1.025	1.040	ns
			t_H	–0.712	–0.708	–0.687	ns
		GCLK PLL	t_{SU}	2.736	2.938	3.123	ns
			t_H	–2.456	–2.621	–2.770	ns
	16 mA	GCLK	t_{SU}	0.992	1.025	1.040	ns
			t_H	–0.712	–0.708	–0.687	ns
		GCLK PLL	t_{SU}	2.736	2.938	3.123	ns
			t_H	–2.456	–2.621	–2.770	ns
1.8V	2 mA	GCLK	t_{SU}	0.927	0.986	1.027	ns
			t_H	–0.649	–0.670	–0.673	ns
		GCLK PLL	t_{SU}	2.671	2.899	3.110	ns
			t_H	–2.393	–2.583	–2.756	ns
	4 mA	GCLK	t_{SU}	0.927	0.986	1.027	ns
			t_H	–0.649	–0.670	–0.673	ns
		GCLK PLL	t_{SU}	2.671	2.899	3.110	ns
			t_H	–2.393	–2.583	–2.756	ns
	6 mA	GCLK	t_{SU}	0.927	0.986	1.027	ns
			t_H	–0.649	–0.670	–0.673	ns
		GCLK PLL	t_{SU}	2.671	2.899	3.110	ns
			t_H	–2.393	–2.583	–2.756	ns
	8 mA	GCLK	t_{SU}	0.927	0.986	1.027	ns
			t_H	–0.649	–0.670	–0.673	ns
		GCLK PLL	t_{SU}	2.671	2.899	3.110	ns
			t_H	–2.393	–2.583	–2.756	ns
	10 mA	GCLK	t_{SU}	0.927	0.986	1.027	ns
			t_H	–0.649	–0.670	–0.673	ns
		GCLK PLL	t_{SU}	2.671	2.899	3.110	ns
			t_H	–2.393	–2.583	–2.756	ns
	12 mA	GCLK	t_{SU}	0.927	0.986	1.027	ns
			t_H	–0.649	–0.670	–0.673	ns
		GCLK PLL	t_{SU}	2.671	2.899	3.110	ns
			t_H	–2.393	–2.583	–2.756	ns

Table 1–66. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	16 mA	GCLK	t_{SU}	0.927	0.986	1.027	ns
			t_H	–0.649	–0.670	–0.673	ns
		GCLK PLL	t_{SU}	2.671	2.899	3.110	ns
			t_H	–2.393	–2.583	–2.756	ns
1.5V	2 mA	GCLK	t_{SU}	0.996	1.078	1.144	ns
			t_H	–0.716	–0.760	–0.788	ns
		GCLK PLL	t_{SU}	2.740	2.991	3.227	ns
			t_H	–2.460	–2.673	–2.871	ns
	4 mA	GCLK	t_{SU}	0.996	1.078	1.144	ns
			t_H	–0.716	–0.760	–0.788	ns
		GCLK PLL	t_{SU}	2.740	2.991	3.227	ns
			t_H	–2.460	–2.673	–2.871	ns
	6 mA	GCLK	t_{SU}	0.996	1.078	1.144	ns
			t_H	–0.716	–0.760	–0.788	ns
		GCLK PLL	t_{SU}	2.740	2.991	3.227	ns
			t_H	–2.460	–2.673	–2.871	ns
	8 mA	GCLK	t_{SU}	0.996	1.078	1.144	ns
			t_H	–0.716	–0.760	–0.788	ns
		GCLK PLL	t_{SU}	2.740	2.991	3.227	ns
			t_H	–2.460	–2.673	–2.871	ns
	10 mA	GCLK	t_{SU}	0.996	1.078	1.144	ns
			t_H	–0.716	–0.760	–0.788	ns
		GCLK PLL	t_{SU}	2.740	2.991	3.227	ns
			t_H	–2.460	–2.673	–2.871	ns
	12 mA	GCLK	t_{SU}	0.996	1.078	1.144	ns
			t_H	–0.716	–0.760	–0.788	ns
		GCLK PLL	t_{SU}	2.740	2.991	3.227	ns
			t_H	–2.460	–2.673	–2.871	ns

Table 1–66. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	16 mA	GCLK	t_{SU}	0.996	1.078	1.144	ns
			t_H	–0.716	–0.760	–0.788	ns
		GCLK PLL	t_{SU}	2.740	2.991	3.227	ns
			t_H	–2.460	–2.673	–2.871	ns
1.2V	2 mA	GCLK	t_{SU}	1.148	1.258	1.350	ns
			t_H	–0.866	–0.936	–0.990	ns
		GCLK PLL	t_{SU}	2.892	3.171	3.433	ns
			t_H	–2.610	–2.849	–3.073	ns
	4 mA	GCLK	t_{SU}	1.148	1.258	1.350	ns
			t_H	–0.866	–0.936	–0.990	ns
		GCLK PLL	t_{SU}	2.892	3.171	3.433	ns
			t_H	–2.610	–2.849	–3.073	ns
	6 mA	GCLK	t_{SU}	1.148	1.258	1.350	ns
			t_H	–0.866	–0.936	–0.990	ns
		GCLK PLL	t_{SU}	2.892	3.171	3.433	ns
			t_H	–2.610	–2.849	–3.073	ns
	8 mA	GCLK	t_{SU}	1.148	1.258	1.350	ns
			t_H	–0.866	–0.936	–0.990	ns
		GCLK PLL	t_{SU}	2.892	3.171	3.433	ns
			t_H	–2.610	–2.849	–3.073	ns
	10 mA	GCLK	t_{SU}	1.148	1.258	1.350	ns
			t_H	–0.866	–0.936	–0.990	ns
		GCLK PLL	t_{SU}	2.892	3.171	3.433	ns
			t_H	–2.610	–2.849	–3.073	ns
	12 mA	GCLK	t_{SU}	1.148	1.258	1.350	ns
			t_H	–0.866	–0.936	–0.990	ns
		GCLK PLL	t_{SU}	2.892	3.171	3.433	ns
			t_H	–2.610	–2.849	–3.073	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.981	1.043	1.089	ns
			t_H	–0.701	–0.726	–0.734	ns
		GCLK PLL	t_{SU}	2.722	2.953	3.171	ns
			t_H	–2.442	–2.636	–2.816	ns
	12 mA	GCLK	t_{SU}	0.981	1.043	1.089	ns
			t_H	–0.701	–0.726	–0.734	ns
		GCLK PLL	t_{SU}	2.722	2.953	3.171	ns
			t_H	–2.442	–2.636	–2.816	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.981	1.043	1.089	ns
			t_H	–0.701	–0.726	–0.734	ns
		GCLK PLL	t_{SU}	2.722	2.953	3.171	ns
			t_H	–2.442	–2.636	–2.816	ns

Table 1–66. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.042	1.132	1.204	ns
			t_H	–0.762	–0.813	–0.847	ns
		GCLK PLL	t_{SU}	2.783	3.042	3.286	ns
			t_H	–2.503	–2.723	–2.929	ns
	10 mA	GCLK	t_{SU}	1.042	1.132	1.204	ns
			t_H	–0.762	–0.813	–0.847	ns
		GCLK PLL	t_{SU}	2.783	3.042	3.286	ns
			t_H	–2.503	–2.723	–2.929	ns
	12 mA	GCLK	t_{SU}	1.042	1.132	1.204	ns
			t_H	–0.762	–0.813	–0.847	ns
		GCLK PLL	t_{SU}	2.783	3.042	3.286	ns
			t_H	–2.503	–2.723	–2.929	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.042	1.132	1.204	ns
			t_H	–0.762	–0.813	–0.847	ns
		GCLK PLL	t_{SU}	2.783	3.042	3.286	ns
			t_H	–2.503	–2.723	–2.929	ns
	16 mA	GCLK	t_{SU}	1.042	1.132	1.204	ns
			t_H	–0.762	–0.813	–0.847	ns
		GCLK PLL	t_{SU}	2.783	3.042	3.286	ns
			t_H	–2.503	–2.723	–2.929	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.042	1.132	1.204	ns
			t_H	–0.762	–0.813	–0.847	ns
		GCLK PLL	t_{SU}	2.783	3.042	3.286	ns
			t_H	–2.503	–2.723	–2.929	ns
	10 mA	GCLK	t_{SU}	1.042	1.132	1.204	ns
			t_H	–0.762	–0.813	–0.847	ns
		GCLK PLL	t_{SU}	2.783	3.042	3.286	ns
			t_H	–2.503	–2.723	–2.929	ns
	12 mA	GCLK	t_{SU}	1.042	1.132	1.204	ns
			t_H	–0.762	–0.813	–0.847	ns
		GCLK PLL	t_{SU}	2.783	3.042	3.286	ns
			t_H	–2.503	–2.723	–2.929	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.042	1.132	1.204	ns
			t_H	–0.762	–0.813	–0.847	ns
		GCLK PLL	t_{SU}	2.783	3.042	3.286	ns
			t_H	–2.503	–2.723	–2.929	ns

Table 1–66. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.998	1.092	1.170	ns
			t_H	–0.718	–0.774	–0.814	ns
		GCLK PLL	t_{SU}	2.739	3.002	3.252	ns
			t_H	–2.459	–2.684	–2.896	ns
	10 mA	GCLK	t_{SU}	0.998	1.092	1.170	ns
			t_H	–0.718	–0.774	–0.814	ns
		GCLK PLL	t_{SU}	2.739	3.002	3.252	ns
			t_H	–2.459	–2.684	–2.896	ns
	12 mA	GCLK	t_{SU}	0.998	1.092	1.170	ns
			t_H	–0.718	–0.774	–0.814	ns
		GCLK PLL	t_{SU}	2.739	3.002	3.252	ns
			t_H	–2.459	–2.684	–2.896	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.998	1.092	1.170	ns
			t_H	–0.718	–0.774	–0.814	ns
		GCLK PLL	t_{SU}	2.739	3.002	3.252	ns
			t_H	–2.459	–2.684	–2.896	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.130	1.251	1.354	ns
			t_H	–0.848	–0.929	–0.994	ns
		GCLK PLL	t_{SU}	2.871	3.161	3.436	ns
			t_H	–2.589	–2.839	–3.076	ns
	10 mA	GCLK	t_{SU}	1.130	1.251	1.354	ns
			t_H	–0.848	–0.929	–0.994	ns
		GCLK PLL	t_{SU}	2.871	3.161	3.436	ns
			t_H	–2.589	–2.839	–3.076	ns
	12 mA	GCLK	t_{SU}	1.130	1.251	1.354	ns
			t_H	–0.848	–0.929	–0.994	ns
		GCLK PLL	t_{SU}	2.871	3.161	3.436	ns
			t_H	–2.589	–2.839	–3.076	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	1.130	1.251	1.354	ns
			t_H	–0.848	–0.929	–0.994	ns
		GCLK PLL	t_{SU}	2.871	3.161	3.436	ns
			t_H	–2.589	–2.839	–3.076	ns
3.0-V PCI	—	GCLK	t_{SU}	1.045	1.066	1.067	ns
			t_H	–0.765	–0.748	–0.713	ns
	—	GCLK PLL	t_{SU}	2.789	2.979	3.150	ns
			t_H	–2.509	–2.661	–2.796	ns
3.0-V PCI-X	—	GCLK	t_{SU}	1.045	1.066	1.067	ns
			t_H	–0.765	–0.748	–0.713	ns
	—	GCLK PLL	t_{SU}	2.789	2.979	3.150	ns
			t_H	–2.509	–2.661	–2.796	ns

Table 1–67. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns
	8 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns
	8 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns
	12 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns
	16 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns

Table 1–67. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns
	8 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns
	12 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns
	16 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns

Table 1–67. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
2.5V	4 mA	GCLK	t_{SU}	1.025	1.068	1.092	ns
			t_H	–0.745	–0.751	–0.738	ns
		GCLK PLL	t_{SU}	2.766	2.976	3.176	ns
			t_H	–2.486	–2.659	–2.822	ns
	8 mA	GCLK	t_{SU}	1.025	1.068	1.092	ns
			t_H	–0.745	–0.751	–0.738	ns
		GCLK PLL	t_{SU}	2.766	2.976	3.176	ns
			t_H	–2.486	–2.659	–2.822	ns
	12 mA	GCLK	t_{SU}	1.025	1.068	1.092	ns
			t_H	–0.745	–0.751	–0.738	ns
		GCLK PLL	t_{SU}	2.766	2.976	3.176	ns
			t_H	–2.486	–2.659	–2.822	ns
	16 mA	GCLK	t_{SU}	1.025	1.068	1.092	ns
			t_H	–0.745	–0.751	–0.738	ns
		GCLK PLL	t_{SU}	2.766	2.976	3.176	ns
			t_H	–2.486	–2.659	–2.822	ns
1.8V	2 mA	GCLK	t_{SU}	0.961	1.029	1.078	ns
			t_H	–0.683	–0.713	–0.723	ns
		GCLK PLL	t_{SU}	2.702	2.937	3.162	ns
			t_H	–2.424	–2.621	–2.807	ns
	4 mA	GCLK	t_{SU}	0.961	1.029	1.078	ns
			t_H	–0.683	–0.713	–0.723	ns
		GCLK PLL	t_{SU}	2.702	2.937	3.162	ns
			t_H	–2.424	–2.621	–2.807	ns
	6 mA	GCLK	t_{SU}	0.961	1.029	1.078	ns
			t_H	–0.683	–0.713	–0.723	ns
		GCLK PLL	t_{SU}	2.702	2.937	3.162	ns
			t_H	–2.424	–2.621	–2.807	ns
	8 mA	GCLK	t_{SU}	0.961	1.029	1.078	ns
			t_H	–0.683	–0.713	–0.723	ns
		GCLK PLL	t_{SU}	2.702	2.937	3.162	ns
			t_H	–2.424	–2.621	–2.807	ns
	10 mA	GCLK	t_{SU}	0.961	1.029	1.078	ns
			t_H	–0.683	–0.713	–0.723	ns
		GCLK PLL	t_{SU}	2.702	2.937	3.162	ns
			t_H	–2.424	–2.621	–2.807	ns
	12 mA	GCLK	t_{SU}	0.961	1.029	1.078	ns
			t_H	–0.683	–0.713	–0.723	ns
		GCLK PLL	t_{SU}	2.702	2.937	3.162	ns
			t_H	–2.424	–2.621	–2.807	ns

Table 1–67. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	16 mA	GCLK	t_{SU}	0.961	1.029	1.078	ns
			t_H	–0.683	–0.713	–0.723	ns
		GCLK PLL	t_{SU}	2.702	2.937	3.162	ns
			t_H	–2.424	–2.621	–2.807	ns
1.5V	2 mA	GCLK	t_{SU}	1.030	1.122	1.196	ns
			t_H	–0.750	–0.804	–0.840	ns
		GCLK PLL	t_{SU}	2.771	3.030	3.280	ns
			t_H	–2.491	–2.712	–2.924	ns
	4 mA	GCLK	t_{SU}	1.030	1.122	1.196	ns
			t_H	–0.750	–0.804	–0.840	ns
		GCLK PLL	t_{SU}	2.771	3.030	3.280	ns
			t_H	–2.491	–2.712	–2.924	ns
	6 mA	GCLK	t_{SU}	1.030	1.122	1.196	ns
			t_H	–0.750	–0.804	–0.840	ns
		GCLK PLL	t_{SU}	2.771	3.030	3.280	ns
			t_H	–2.491	–2.712	–2.924	ns
	8 mA	GCLK	t_{SU}	1.030	1.122	1.196	ns
			t_H	–0.750	–0.804	–0.840	ns
		GCLK PLL	t_{SU}	2.771	3.030	3.280	ns
			t_H	–2.491	–2.712	–2.924	ns
	10 mA	GCLK	t_{SU}	1.030	1.122	1.196	ns
			t_H	–0.750	–0.804	–0.840	ns
		GCLK PLL	t_{SU}	2.771	3.030	3.280	ns
			t_H	–2.491	–2.712	–2.924	ns
	12 mA	GCLK	t_{SU}	1.030	1.122	1.196	ns
			t_H	–0.750	–0.804	–0.840	ns
		GCLK PLL	t_{SU}	2.771	3.030	3.280	ns
			t_H	–2.491	–2.712	–2.924	ns
	16 mA	GCLK	t_{SU}	1.030	1.122	1.196	ns
			t_H	–0.750	–0.804	–0.840	ns
		GCLK PLL	t_{SU}	2.771	3.030	3.280	ns
			t_H	–2.491	–2.712	–2.924	ns
1.2V	2 mA	GCLK	t_{SU}	1.183	1.302	1.403	ns
			t_H	–0.901	–0.980	–1.042	ns
		GCLK PLL	t_{SU}	2.924	3.210	3.487	ns
			t_H	–2.642	–2.888	–3.126	ns
	4 mA	GCLK	t_{SU}	1.183	1.302	1.403	ns
			t_H	–0.901	–0.980	–1.042	ns
		GCLK PLL	t_{SU}	2.924	3.210	3.487	ns
			t_H	–2.642	–2.888	–3.126	ns

Table 1–67. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	6 mA	GCLK	t_{SU}	1.183	1.302	1.403	ns
			t_H	–0.901	–0.980	–1.042	ns
		GCLK PLL	t_{SU}	2.924	3.210	3.487	ns
			t_H	–2.642	–2.888	–3.126	ns
	8 mA	GCLK	t_{SU}	1.183	1.302	1.403	ns
			t_H	–0.901	–0.980	–1.042	ns
		GCLK PLL	t_{SU}	2.924	3.210	3.487	ns
			t_H	–2.642	–2.888	–3.126	ns
	10 mA	GCLK	t_{SU}	1.183	1.302	1.403	ns
			t_H	–0.901	–0.980	–1.042	ns
		GCLK PLL	t_{SU}	2.924	3.210	3.487	ns
			t_H	–2.642	–2.888	–3.126	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	1.016	1.086	1.140	ns
			t_H	–0.736	–0.768	–0.784	ns
		GCLK PLL	t_{SU}	2.756	2.995	3.229	ns
			t_H	–2.476	–2.677	–2.873	ns
	12 mA	GCLK	t_{SU}	1.016	1.086	1.140	ns
			t_H	–0.736	–0.768	–0.784	ns
		GCLK PLL	t_{SU}	2.756	2.995	3.229	ns
			t_H	–2.476	–2.677	–2.873	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	1.016	1.086	1.140	ns
			t_H	–0.736	–0.768	–0.784	ns
		GCLK PLL	t_{SU}	2.756	2.995	3.229	ns
			t_H	–2.476	–2.677	–2.873	ns
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.078	1.175	1.257	ns
			t_H	–0.798	–0.856	–0.899	ns
		GCLK PLL	t_{SU}	2.818	3.084	3.346	ns
			t_H	–2.538	–2.765	–2.988	ns
	10 mA	GCLK	t_{SU}	1.078	1.175	1.257	ns
			t_H	–0.798	–0.856	–0.899	ns
		GCLK PLL	t_{SU}	2.818	3.084	3.346	ns
			t_H	–2.538	–2.765	–2.988	ns
	12 mA	GCLK	t_{SU}	1.078	1.175	1.257	ns
			t_H	–0.798	–0.856	–0.899	ns
		GCLK PLL	t_{SU}	2.818	3.084	3.346	ns
			t_H	–2.538	–2.765	–2.988	ns

Table 1–67. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.078	1.175	1.257	ns
			t_H	–0.798	–0.856	–0.899	ns
		GCLK PLL	t_{SU}	2.818	3.084	3.346	ns
			t_H	–2.538	–2.765	–2.988	ns
	16 mA	GCLK	t_{SU}	1.078	1.175	1.257	ns
			t_H	–0.798	–0.856	–0.899	ns
		GCLK PLL	t_{SU}	2.818	3.084	3.346	ns
			t_H	–2.538	–2.765	–2.988	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.078	1.175	1.257	ns
			t_H	–0.798	–0.856	–0.899	ns
		GCLK PLL	t_{SU}	2.818	3.084	3.346	ns
			t_H	–2.538	–2.765	–2.988	ns
	10 mA	GCLK	t_{SU}	1.078	1.175	1.257	ns
			t_H	–0.798	–0.856	–0.899	ns
		GCLK PLL	t_{SU}	2.818	3.084	3.346	ns
			t_H	–2.538	–2.765	–2.988	ns
	12 mA	GCLK	t_{SU}	1.078	1.175	1.257	ns
			t_H	–0.798	–0.856	–0.899	ns
		GCLK PLL	t_{SU}	2.818	3.084	3.346	ns
			t_H	–2.538	–2.765	–2.988	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.078	1.175	1.257	ns
			t_H	–0.798	–0.856	–0.899	ns
		GCLK PLL	t_{SU}	2.818	3.084	3.346	ns
			t_H	–2.538	–2.765	–2.988	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	1.033	1.134	1.220	ns
			t_H	–0.753	–0.816	–0.863	ns
		GCLK PLL	t_{SU}	2.773	3.043	3.309	ns
			t_H	–2.493	–2.725	–2.952	ns
	10 mA	GCLK	t_{SU}	1.033	1.134	1.220	ns
			t_H	–0.753	–0.816	–0.863	ns
		GCLK PLL	t_{SU}	2.773	3.043	3.309	ns
			t_H	–2.493	–2.725	–2.952	ns
	12 mA	GCLK	t_{SU}	1.033	1.134	1.220	ns
			t_H	–0.753	–0.816	–0.863	ns
		GCLK PLL	t_{SU}	2.773	3.043	3.309	ns
			t_H	–2.493	–2.725	–2.952	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	1.033	1.134	1.220	ns
			t_H	–0.753	–0.816	–0.863	ns
		GCLK PLL	t_{SU}	2.773	3.043	3.309	ns
			t_H	–2.493	–2.725	–2.952	ns

Table 1–67. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.164	1.292	1.405	ns
			t_H	–0.882	–0.970	–1.045	ns
		GCLK PLL	t_{SU}	2.904	3.201	3.494	ns
			t_H	–2.622	–2.879	–3.134	ns
	10 mA	GCLK	t_{SU}	1.164	1.292	1.405	ns
			t_H	–0.882	–0.970	–1.045	ns
		GCLK PLL	t_{SU}	2.904	3.201	3.494	ns
			t_H	–2.622	–2.879	–3.134	ns
3.0-V PCI	—	GCLK	t_{SU}	1.078	1.108	1.117	ns
			t_H	–0.798	–0.790	–0.762	ns
	—	GCLK PLL	t_{SU}	2.819	3.016	3.201	ns
			t_H	–2.539	–2.698	–2.846	ns
3.0-V PCI-X	—	GCLK	t_{SU}	1.078	1.108	1.117	ns
			t_H	–0.798	–0.790	–0.762	ns
	—	GCLK PLL	t_{SU}	2.819	3.016	3.201	ns
			t_H	–2.539	–2.698	–2.846	ns

Table 1–68. EP3C25 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.531	6.039	6.571	ns
		GCLK PLL	t_{CO}	3.787	4.126	4.488	ns
	8 mA	GCLK	t_{CO}	5.531	6.039	6.571	ns
		GCLK PLL	t_{CO}	3.787	4.126	4.488	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.490	5.820	6.173	ns
		GCLK PLL	t_{CO}	3.746	3.907	4.090	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.241	5.742	6.269	ns
		GCLK PLL	t_{CO}	3.497	3.829	4.186	ns
	8 mA	GCLK	t_{CO}	4.970	5.458	5.970	ns
		GCLK PLL	t_{CO}	3.226	3.545	3.887	ns
	12 mA	GCLK	t_{CO}	4.873	5.357	5.866	ns
		GCLK PLL	t_{CO}	3.129	3.444	3.783	ns
	16 mA	GCLK	t_{CO}	4.826	5.305	5.808	ns
		GCLK PLL	t_{CO}	3.082	3.392	3.725	ns

Table 1–68. EP3C25 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.968	5.455	5.967	ns
		GCLK PLL	t_{CO}	3.224	3.542	3.884	ns
	8 mA	GCLK	t_{CO}	4.827	5.307	5.812	ns
		GCLK PLL	t_{CO}	3.083	3.394	3.729	ns
	12 mA	GCLK	t_{CO}	4.790	5.267	5.769	ns
		GCLK PLL	t_{CO}	3.046	3.354	3.686	ns
	16 mA	GCLK	t_{CO}	4.774	5.252	5.754	ns
		GCLK PLL	t_{CO}	3.030	3.339	3.671	ns
2.5V	4 mA	GCLK	t_{CO}	5.299	5.828	6.383	ns
		GCLK PLL	t_{CO}	3.555	3.915	4.300	ns
	8 mA	GCLK	t_{CO}	5.056	5.575	6.119	ns
		GCLK PLL	t_{CO}	3.312	3.662	4.036	ns
	12 mA	GCLK	t_{CO}	4.958	5.469	6.006	ns
		GCLK PLL	t_{CO}	3.214	3.556	3.923	ns
	16 mA	GCLK	t_{CO}	4.919	5.429	5.965	ns
		GCLK PLL	t_{CO}	3.175	3.516	3.882	ns
1.8V	2 mA	GCLK	t_{CO}	6.410	7.081	7.781	ns
		GCLK PLL	t_{CO}	4.666	5.168	5.698	ns
	4 mA	GCLK	t_{CO}	5.883	6.536	7.217	ns
		GCLK PLL	t_{CO}	4.139	4.623	5.134	ns
	6 mA	GCLK	t_{CO}	5.658	6.278	6.925	ns
		GCLK PLL	t_{CO}	3.914	4.365	4.842	ns
	8 mA	GCLK	t_{CO}	5.555	6.161	6.796	ns
		GCLK PLL	t_{CO}	3.811	4.248	4.713	ns
	10 mA	GCLK	t_{CO}	5.503	6.113	6.750	ns
		GCLK PLL	t_{CO}	3.759	4.200	4.667	ns
	12 mA	GCLK	t_{CO}	5.446	6.046	6.675	ns
		GCLK PLL	t_{CO}	3.702	4.133	4.592	ns
	16 mA	GCLK	t_{CO}	5.392	5.987	6.610	ns
		GCLK PLL	t_{CO}	3.648	4.074	4.527	ns

Table 1–68. EP3C25 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	2 mA	GCLK	t_{CO}	6.798	7.643	8.520	ns
		GCLK PLL	t_{CO}	5.054	5.730	6.437	ns
	4 mA	GCLK	t_{CO}	6.323	7.082	7.872	ns
		GCLK PLL	t_{CO}	4.579	5.169	5.789	ns
	6 mA	GCLK	t_{CO}	6.153	6.899	7.675	ns
		GCLK PLL	t_{CO}	4.409	4.986	5.592	ns
	8 mA	GCLK	t_{CO}	6.065	6.786	7.537	ns
		GCLK PLL	t_{CO}	4.321	4.873	5.454	ns
	10 mA	GCLK	t_{CO}	6.006	6.726	7.476	ns
		GCLK PLL	t_{CO}	4.262	4.813	5.393	ns
	12 mA	GCLK	t_{CO}	5.973	6.685	7.426	ns
		GCLK PLL	t_{CO}	4.229	4.772	5.343	ns
	16 mA	GCLK	t_{CO}	5.859	6.543	7.256	ns
		GCLK PLL	t_{CO}	4.115	4.630	5.173	ns
1.2V	2 mA	GCLK	t_{CO}	7.971	9.171	10.409	ns
		GCLK PLL	t_{CO}	6.227	7.258	8.326	ns
	4 mA	GCLK	t_{CO}	7.526	8.645	9.802	ns
		GCLK PLL	t_{CO}	5.782	6.732	7.719	ns
	6 mA	GCLK	t_{CO}	7.377	8.464	9.588	ns
		GCLK PLL	t_{CO}	5.633	6.551	7.505	ns
	8 mA	GCLK	t_{CO}	7.308	8.384	9.498	ns
		GCLK PLL	t_{CO}	5.564	6.471	7.415	ns
	10 mA	GCLK	t_{CO}	7.172	8.202	9.267	ns
		GCLK PLL	t_{CO}	5.428	6.289	7.184	ns
	12 mA	GCLK	t_{CO}	7.144	8.176	9.245	ns
		GCLK PLL	t_{CO}	5.400	6.263	7.162	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.914	5.418	5.947	ns
		GCLK PLL	t_{CO}	3.173	3.508	3.864	ns
	12 mA	GCLK	t_{CO}	4.892	5.394	5.924	ns
		GCLK PLL	t_{CO}	3.151	3.484	3.841	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.832	5.332	5.858	ns
		GCLK PLL	t_{CO}	3.091	3.422	3.775	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.348	5.931	6.542	ns
		GCLK PLL	t_{CO}	3.607	4.021	4.459	ns
	10 mA	GCLK	t_{CO}	5.323	5.900	6.505	ns
		GCLK PLL	t_{CO}	3.582	3.990	4.422	ns
	12 mA	GCLK	t_{CO}	5.311	5.886	6.488	ns
		GCLK PLL	t_{CO}	3.570	3.976	4.405	ns

Table 1–68. EP3C25 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.282	5.857	6.460	ns
		GCLK PLL	t_{CO}	3.541	3.947	4.377	ns
	16 mA	GCLK	t_{CO}	5.269	5.844	6.446	ns
		GCLK PLL	t_{CO}	3.528	3.934	4.363	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.310	5.883	6.484	ns
		GCLK PLL	t_{CO}	3.569	3.973	4.401	ns
	10 mA	GCLK	t_{CO}	5.299	5.876	6.480	ns
		GCLK PLL	t_{CO}	3.558	3.966	4.397	ns
	12 mA	GCLK	t_{CO}	5.290	5.862	6.460	ns
		GCLK PLL	t_{CO}	3.549	3.952	4.377	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.225	5.796	6.394	ns
		GCLK PLL	t_{CO}	3.484	3.886	4.311	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.824	6.504	7.215	ns
		GCLK PLL	t_{CO}	4.083	4.594	5.132	ns
	10 mA	GCLK	t_{CO}	5.827	6.504	7.210	ns
		GCLK PLL	t_{CO}	4.086	4.594	5.127	ns
	12 mA	GCLK	t_{CO}	5.815	6.496	7.206	ns
		GCLK PLL	t_{CO}	4.074	4.586	5.123	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.753	6.428	7.131	ns
		GCLK PLL	t_{CO}	4.012	4.518	5.048	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.037	8.042	9.082	ns
		GCLK PLL	t_{CO}	5.296	6.132	6.999	ns
	10 mA	GCLK	t_{CO}	6.975	7.953	8.966	ns
		GCLK PLL	t_{CO}	5.234	6.043	6.883	ns
	12 mA	GCLK	t_{CO}	6.977	7.959	8.975	ns
		GCLK PLL	t_{CO}	5.236	6.049	6.892	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.932	7.906	8.915	ns
		GCLK PLL	t_{CO}	5.191	5.996	6.832	ns
3.0-V PCI	—	GCLK	t_{CO}	5.121	5.599	6.103	ns
		GCLK PLL	t_{CO}	3.377	3.686	4.020	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.121	5.599	6.103	ns
		GCLK PLL	t_{CO}	3.377	3.686	4.020	ns

Table 1–69. EP3C25 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.471	5.968	6.493	ns
		GCLK PLL	t_{CO}	3.730	4.060	4.409	ns
	8 mA	GCLK	t_{CO}	5.471	5.968	6.493	ns
		GCLK PLL	t_{CO}	3.730	4.060	4.409	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.471	5.794	6.143	ns
		GCLK PLL	t_{CO}	3.730	3.886	4.059	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.185	5.675	6.194	ns
		GCLK PLL	t_{CO}	3.444	3.767	4.110	ns
	8 mA	GCLK	t_{CO}	4.928	5.408	5.917	ns
		GCLK PLL	t_{CO}	3.187	3.500	3.833	ns
	12 mA	GCLK	t_{CO}	4.839	5.313	5.815	ns
		GCLK PLL	t_{CO}	3.098	3.405	3.731	ns
	16 mA	GCLK	t_{CO}	4.793	5.262	5.760	ns
		GCLK PLL	t_{CO}	3.052	3.354	3.676	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.926	5.406	5.915	ns
		GCLK PLL	t_{CO}	3.185	3.498	3.831	ns
	8 mA	GCLK	t_{CO}	4.793	5.263	5.763	ns
		GCLK PLL	t_{CO}	3.052	3.355	3.679	ns
	12 mA	GCLK	t_{CO}	4.758	5.227	5.724	ns
		GCLK PLL	t_{CO}	3.017	3.319	3.640	ns
	16 mA	GCLK	t_{CO}	4.743	5.211	5.707	ns
		GCLK PLL	t_{CO}	3.002	3.303	3.623	ns
2.5V	4 mA	GCLK	t_{CO}	5.283	5.789	6.324	ns
		GCLK PLL	t_{CO}	3.542	3.881	4.240	ns
	8 mA	GCLK	t_{CO}	5.048	5.545	6.070	ns
		GCLK PLL	t_{CO}	3.307	3.637	3.986	ns
	12 mA	GCLK	t_{CO}	4.949	5.440	5.960	ns
		GCLK PLL	t_{CO}	3.208	3.532	3.876	ns
	16 mA	GCLK	t_{CO}	4.908	5.398	5.917	ns
		GCLK PLL	t_{CO}	3.167	3.490	3.833	ns

Table 1–69. EP3C25 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	2 mA	GCLK	t_{CO}	6.377	7.025	7.704	ns
		GCLK PLL	t_{CO}	4.636	5.117	5.620	ns
	4 mA	GCLK	t_{CO}	5.864	6.497	7.160	ns
		GCLK PLL	t_{CO}	4.123	4.589	5.076	ns
	6 mA	GCLK	t_{CO}	5.643	6.243	6.873	ns
		GCLK PLL	t_{CO}	3.902	4.335	4.789	ns
	8 mA	GCLK	t_{CO}	5.542	6.129	6.747	ns
		GCLK PLL	t_{CO}	3.801	4.221	4.663	ns
	10 mA	GCLK	t_{CO}	5.491	6.080	6.701	ns
		GCLK PLL	t_{CO}	3.750	4.172	4.617	ns
	12 mA	GCLK	t_{CO}	5.436	6.017	6.628	ns
		GCLK PLL	t_{CO}	3.695	4.109	4.544	ns
	16 mA	GCLK	t_{CO}	5.393	5.970	6.579	ns
		GCLK PLL	t_{CO}	3.652	4.062	4.495	ns
1.5V	2 mA	GCLK	t_{CO}	6.771	7.592	8.449	ns
		GCLK PLL	t_{CO}	5.030	5.684	6.365	ns
	4 mA	GCLK	t_{CO}	6.315	7.048	7.816	ns
		GCLK PLL	t_{CO}	4.574	5.140	5.732	ns
	6 mA	GCLK	t_{CO}	6.148	6.870	7.625	ns
		GCLK PLL	t_{CO}	4.407	4.962	5.541	ns
	8 mA	GCLK	t_{CO}	6.072	6.777	7.515	ns
		GCLK PLL	t_{CO}	4.331	4.869	5.431	ns
	10 mA	GCLK	t_{CO}	6.012	6.714	7.449	ns
		GCLK PLL	t_{CO}	4.271	4.806	5.365	ns
	12 mA	GCLK	t_{CO}	5.978	6.671	7.398	ns
		GCLK PLL	t_{CO}	4.237	4.763	5.314	ns
	16 mA	GCLK	t_{CO}	5.881	6.563	7.279	ns
		GCLK PLL	t_{CO}	4.140	4.655	5.195	ns
1.2V	2 mA	GCLK	t_{CO}	7.959	9.132	10.345	ns
		GCLK PLL	t_{CO}	6.218	7.224	8.261	ns
	4 mA	GCLK	t_{CO}	7.524	8.618	9.753	ns
		GCLK PLL	t_{CO}	5.783	6.710	7.669	ns
	6 mA	GCLK	t_{CO}	7.396	8.464	9.574	ns
		GCLK PLL	t_{CO}	5.655	6.556	7.490	ns
	8 mA	GCLK	t_{CO}	7.324	8.382	9.479	ns
		GCLK PLL	t_{CO}	5.583	6.474	7.395	ns
	10 mA	GCLK	t_{CO}	7.193	8.219	9.284	ns
		GCLK PLL	t_{CO}	5.452	6.311	7.200	ns

Table 1–69. EP3C25 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.876	5.373	5.898	ns
		GCLK PLL	t_{CO}	3.136	3.464	3.809	ns
	12 mA	GCLK	t_{CO}	4.857	5.354	5.877	ns
		GCLK PLL	t_{CO}	3.117	3.445	3.788	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.802	5.297	5.817	ns
		GCLK PLL	t_{CO}	3.062	3.388	3.728	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.310	5.888	6.493	ns
		GCLK PLL	t_{CO}	3.570	3.979	4.404	ns
	10 mA	GCLK	t_{CO}	5.297	5.870	6.472	ns
		GCLK PLL	t_{CO}	3.557	3.961	4.383	ns
	12 mA	GCLK	t_{CO}	5.284	5.855	6.454	ns
		GCLK PLL	t_{CO}	3.544	3.946	4.365	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.254	5.826	6.426	ns
		GCLK PLL	t_{CO}	3.514	3.917	4.337	ns
	16 mA	GCLK	t_{CO}	5.246	5.820	6.421	ns
		GCLK PLL	t_{CO}	3.506	3.911	4.332	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.274	5.842	6.438	ns
		GCLK PLL	t_{CO}	3.534	3.933	4.349	ns
	10 mA	GCLK	t_{CO}	5.269	5.838	6.435	ns
		GCLK PLL	t_{CO}	3.529	3.929	4.346	ns
	12 mA	GCLK	t_{CO}	5.262	5.831	6.428	ns
		GCLK PLL	t_{CO}	3.522	3.922	4.339	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.200	5.765	6.357	ns
		GCLK PLL	t_{CO}	3.460	3.856	4.268	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.789	6.463	7.167	ns
		GCLK PLL	t_{CO}	4.049	4.554	5.078	ns
	10 mA	GCLK	t_{CO}	5.801	6.475	7.178	ns
		GCLK PLL	t_{CO}	4.061	4.566	5.089	ns
	12 mA	GCLK	t_{CO}	5.789	6.466	7.173	ns
		GCLK PLL	t_{CO}	4.049	4.557	5.084	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.734	6.409	7.112	ns
		GCLK PLL	t_{CO}	3.994	4.500	5.023	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.026	8.035	9.080	ns
		GCLK PLL	t_{CO}	5.286	6.126	6.991	ns
	10 mA	GCLK	t_{CO}	6.965	7.950	8.971	ns
		GCLK PLL	t_{CO}	5.225	6.041	6.882	ns
3.0-V PCI	—	GCLK	t_{CO}	5.085	5.554	6.050	ns
		GCLK PLL	t_{CO}	3.344	3.646	3.966	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.085	5.554	6.050	ns
		GCLK PLL	t_{CO}	3.344	3.646	3.966	ns

Table 1–70. EP3C25 Column Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.876	0.946	0.996	ns
			t_{H}	–0.598	–0.630	–0.643	ns
	—	GCLK PLL	t_{SU}	2.618	2.857	3.080	ns
			t_{H}	–2.340	–2.541	–2.727	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.861	5.364	5.893	ns
		GCLK PLL	t_{CO}	3.119	3.453	3.809	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.861	5.364	5.893	ns
		GCLK PLL	t_{CO}	3.119	3.453	3.809	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.242	5.743	6.271	ns
		GCLK PLL	t_{CO}	3.500	3.832	4.187	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.861	5.364	5.893	ns
		GCLK PLL	t_{CO}	3.119	3.453	3.809	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.861	5.364	5.893	ns
		GCLK PLL	t_{CO}	3.119	3.453	3.809	ns

Table 1–71. EP3C25 Row Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.906	0.982	1.042	ns
			t_{H}	–0.628	–0.667	–0.688	ns
			t_{CO}	4.038	4.433	4.853	ns
	—	GCLK PLL	t_{SU}	2.648	2.893	3.127	ns
			t_{H}	–2.370	–2.578	–2.773	ns
			t_{CO}	2.295	2.522	2.769	ns
mini-LVDS	—	GCLK	t_{CO}	4.038	4.433	4.853	ns
		GCLK PLL	t_{CO}	2.295	2.522	2.769	ns
PPDS	—	GCLK	t_{CO}	4.038	4.433	4.853	ns
		GCLK PLL	t_{CO}	2.295	2.522	2.769	ns
RSDS	—	GCLK	t_{CO}	4.038	4.433	4.853	ns
		GCLK PLL	t_{CO}	2.295	2.522	2.769	ns

EP3C40 I/O Timing Parameters

Table 1–72 through Table 1–77 show the maximum I/O timing parameters for EP3C40 devices.

Table 1–72. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
	8 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
	8 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
	12 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
	16 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
	8 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns

Table 1–72. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	12 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
	16 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
2.5V	4 mA	GCLK	t_{SU}	0.863	0.884	0.886	ns
			t_H	–0.583	–0.567	–0.533	ns
		GCLK PLL	t_{SU}	2.743	2.952	3.144	ns
			t_H	–2.463	–2.635	–2.791	ns
	8 mA	GCLK	t_{SU}	0.863	0.884	0.886	ns
			t_H	–0.583	–0.567	–0.533	ns
		GCLK PLL	t_{SU}	2.743	2.952	3.144	ns
			t_H	–2.463	–2.635	–2.791	ns
	12 mA	GCLK	t_{SU}	0.863	0.884	0.886	ns
			t_H	–0.583	–0.567	–0.533	ns
		GCLK PLL	t_{SU}	2.743	2.952	3.144	ns
			t_H	–2.463	–2.635	–2.791	ns
	16 mA	GCLK	t_{SU}	0.863	0.884	0.886	ns
			t_H	–0.583	–0.567	–0.533	ns
		GCLK PLL	t_{SU}	2.743	2.952	3.144	ns
			t_H	–2.463	–2.635	–2.791	ns
1.8V	2 mA	GCLK	t_{SU}	0.799	0.845	0.873	ns
			t_H	–0.521	–0.529	–0.519	ns
		GCLK PLL	t_{SU}	2.678	2.913	3.131	ns
			t_H	–2.400	–2.597	–2.777	ns
	4 mA	GCLK	t_{SU}	0.799	0.845	0.873	ns
			t_H	–0.521	–0.529	–0.519	ns
		GCLK PLL	t_{SU}	2.678	2.913	3.131	ns
			t_H	–2.400	–2.597	–2.777	ns
	6 mA	GCLK	t_{SU}	0.799	0.845	0.873	ns
			t_H	–0.521	–0.529	–0.519	ns
		GCLK PLL	t_{SU}	2.678	2.913	3.131	ns
			t_H	–2.400	–2.597	–2.777	ns
	8 mA	GCLK	t_{SU}	0.799	0.845	0.873	ns
			t_H	–0.521	–0.529	–0.519	ns
		GCLK PLL	t_{SU}	2.678	2.913	3.131	ns
			t_H	–2.400	–2.597	–2.777	ns

Table 1–72. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	10 mA	GCLK	t_{SU}	0.799	0.845	0.873	ns
			t_H	–0.521	–0.529	–0.519	ns
		GCLK PLL	t_{SU}	2.678	2.913	3.131	ns
			t_H	–2.400	–2.597	–2.777	ns
	12 mA	GCLK	t_{SU}	0.799	0.845	0.873	ns
			t_H	–0.521	–0.529	–0.519	ns
		GCLK PLL	t_{SU}	2.678	2.913	3.131	ns
			t_H	–2.400	–2.597	–2.777	ns
	16 mA	GCLK	t_{SU}	0.799	0.845	0.873	ns
			t_H	–0.521	–0.529	–0.519	ns
		GCLK PLL	t_{SU}	2.678	2.913	3.131	ns
			t_H	–2.400	–2.597	–2.777	ns
1.5V	2 mA	GCLK	t_{SU}	0.868	0.937	0.990	ns
			t_H	–0.588	–0.619	–0.634	ns
		GCLK PLL	t_{SU}	2.747	3.005	3.248	ns
			t_H	–2.467	–2.687	–2.892	ns
	4 mA	GCLK	t_{SU}	0.868	0.937	0.990	ns
			t_H	–0.588	–0.619	–0.634	ns
		GCLK PLL	t_{SU}	2.747	3.005	3.248	ns
			t_H	–2.467	–2.687	–2.892	ns
	6 mA	GCLK	t_{SU}	0.868	0.937	0.990	ns
			t_H	–0.588	–0.619	–0.634	ns
		GCLK PLL	t_{SU}	2.747	3.005	3.248	ns
			t_H	–2.467	–2.687	–2.892	ns
	8 mA	GCLK	t_{SU}	0.868	0.937	0.990	ns
			t_H	–0.588	–0.619	–0.634	ns
		GCLK PLL	t_{SU}	2.747	3.005	3.248	ns
			t_H	–2.467	–2.687	–2.892	ns
	10 mA	GCLK	t_{SU}	0.868	0.937	0.990	ns
			t_H	–0.588	–0.619	–0.634	ns
		GCLK PLL	t_{SU}	2.747	3.005	3.248	ns
			t_H	–2.467	–2.687	–2.892	ns
	12 mA	GCLK	t_{SU}	0.868	0.937	0.990	ns
			t_H	–0.588	–0.619	–0.634	ns
		GCLK PLL	t_{SU}	2.747	3.005	3.248	ns
			t_H	–2.467	–2.687	–2.892	ns
	16 mA	GCLK	t_{SU}	0.868	0.937	0.990	ns
			t_H	–0.588	–0.619	–0.634	ns
		GCLK PLL	t_{SU}	2.747	3.005	3.248	ns
			t_H	–2.467	–2.687	–2.892	ns

Table 1–72. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	2 mA	GCLK	t_{SU}	1.020	1.117	1.196	ns
			t_H	–0.738	–0.795	–0.836	ns
		GCLK PLL	t_{SU}	2.899	3.185	3.454	ns
			t_H	–2.617	–2.863	–3.094	ns
	4 mA	GCLK	t_{SU}	1.020	1.117	1.196	ns
			t_H	–0.738	–0.795	–0.836	ns
		GCLK PLL	t_{SU}	2.899	3.185	3.454	ns
			t_H	–2.617	–2.863	–3.094	ns
	6 mA	GCLK	t_{SU}	1.020	1.117	1.196	ns
			t_H	–0.738	–0.795	–0.836	ns
		GCLK PLL	t_{SU}	2.899	3.185	3.454	ns
			t_H	–2.617	–2.863	–3.094	ns
	8 mA	GCLK	t_{SU}	1.020	1.117	1.196	ns
			t_H	–0.738	–0.795	–0.836	ns
		GCLK PLL	t_{SU}	2.899	3.185	3.454	ns
			t_H	–2.617	–2.863	–3.094	ns
	10 mA	GCLK	t_{SU}	1.020	1.117	1.196	ns
			t_H	–0.738	–0.795	–0.836	ns
		GCLK PLL	t_{SU}	2.899	3.185	3.454	ns
			t_H	–2.617	–2.863	–3.094	ns
	12 mA	GCLK	t_{SU}	1.020	1.117	1.196	ns
			t_H	–0.738	–0.795	–0.836	ns
		GCLK PLL	t_{SU}	2.899	3.185	3.454	ns
			t_H	–2.617	–2.863	–3.094	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.852	0.902	0.935	ns
			t_H	–0.572	–0.585	–0.580	ns
		GCLK PLL	t_{SU}	2.733	2.969	3.193	ns
			t_H	–2.453	–2.652	–2.838	ns
	12 mA	GCLK	t_{SU}	0.852	0.902	0.935	ns
			t_H	–0.572	–0.585	–0.580	ns
		GCLK PLL	t_{SU}	2.733	2.969	3.193	ns
			t_H	–2.453	–2.652	–2.838	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.852	0.902	0.935	ns
			t_H	–0.572	–0.585	–0.580	ns
		GCLK PLL	t_{SU}	2.733	2.969	3.193	ns
			t_H	–2.453	–2.652	–2.838	ns

Table 1–72. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.913	0.991	1.050	ns
			t_H	–0.633	–0.672	–0.693	ns
		GCLK PLL	t_{SU}	2.794	3.058	3.308	ns
			t_H	–2.514	–2.739	–2.951	ns
	10 mA	GCLK	t_{SU}	0.913	0.991	1.050	ns
			t_H	–0.633	–0.672	–0.693	ns
		GCLK PLL	t_{SU}	2.794	3.058	3.308	ns
			t_H	–2.514	–2.739	–2.951	ns
	12 mA	GCLK	t_{SU}	0.913	0.991	1.050	ns
			t_H	–0.633	–0.672	–0.693	ns
		GCLK PLL	t_{SU}	2.794	3.058	3.308	ns
			t_H	–2.514	–2.739	–2.951	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.913	0.991	1.050	ns
			t_H	–0.633	–0.672	–0.693	ns
		GCLK PLL	t_{SU}	2.794	3.058	3.308	ns
			t_H	–2.514	–2.739	–2.951	ns
	16 mA	GCLK	t_{SU}	0.913	0.991	1.050	ns
			t_H	–0.633	–0.672	–0.693	ns
		GCLK PLL	t_{SU}	2.794	3.058	3.308	ns
			t_H	–2.514	–2.739	–2.951	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.913	0.991	1.050	ns
			t_H	–0.633	–0.672	–0.693	ns
		GCLK PLL	t_{SU}	2.794	3.058	3.308	ns
			t_H	–2.514	–2.739	–2.951	ns
	10 mA	GCLK	t_{SU}	0.913	0.991	1.050	ns
			t_H	–0.633	–0.672	–0.693	ns
		GCLK PLL	t_{SU}	2.794	3.058	3.308	ns
			t_H	–2.514	–2.739	–2.951	ns
	12 mA	GCLK	t_{SU}	0.913	0.991	1.050	ns
			t_H	–0.633	–0.672	–0.693	ns
		GCLK PLL	t_{SU}	2.794	3.058	3.308	ns
			t_H	–2.514	–2.739	–2.951	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.913	0.991	1.050	ns
			t_H	–0.633	–0.672	–0.693	ns
		GCLK PLL	t_{SU}	2.794	3.058	3.308	ns
			t_H	–2.514	–2.739	–2.951	ns

Table 1–72. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.869	0.951	1.016	ns
			t_H	–0.589	–0.633	–0.660	ns
		GCLK PLL	t_{SU}	2.750	3.018	3.274	ns
			t_H	–2.470	–2.700	–2.918	ns
	10 mA	GCLK	t_{SU}	0.869	0.951	1.016	ns
			t_H	–0.589	–0.633	–0.660	ns
		GCLK PLL	t_{SU}	2.750	3.018	3.274	ns
			t_H	–2.470	–2.700	–2.918	ns
	12 mA	GCLK	t_{SU}	0.869	0.951	1.016	ns
			t_H	–0.589	–0.633	–0.660	ns
		GCLK PLL	t_{SU}	2.750	3.018	3.274	ns
			t_H	–2.470	–2.700	–2.918	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.869	0.951	1.016	ns
			t_H	–0.589	–0.633	–0.660	ns
		GCLK PLL	t_{SU}	2.750	3.018	3.274	ns
			t_H	–2.470	–2.700	–2.918	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.001	1.110	1.200	ns
			t_H	–0.719	–0.788	–0.840	ns
		GCLK PLL	t_{SU}	2.882	3.177	3.458	ns
			t_H	–2.600	–2.855	–3.098	ns
	10 mA	GCLK	t_{SU}	1.001	1.110	1.200	ns
			t_H	–0.719	–0.788	–0.840	ns
		GCLK PLL	t_{SU}	2.882	3.177	3.458	ns
			t_H	–2.600	–2.855	–3.098	ns
	12 mA	GCLK	t_{SU}	1.001	1.110	1.200	ns
			t_H	–0.719	–0.788	–0.840	ns
		GCLK PLL	t_{SU}	2.882	3.177	3.458	ns
			t_H	–2.600	–2.855	–3.098	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	1.001	1.110	1.200	ns
			t_H	–0.719	–0.788	–0.840	ns
		GCLK PLL	t_{SU}	2.882	3.177	3.458	ns
			t_H	–2.600	–2.855	–3.098	ns
3.0-V PCI	—	GCLK	t_{SU}	0.916	0.925	0.913	ns
			t_H	–0.636	–0.607	–0.559	ns
		GCLK PLL	t_{SU}	2.796	2.993	3.171	ns
			t_H	–2.516	–2.675	–2.817	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.916	0.925	0.913	ns
			t_H	–0.636	–0.607	–0.559	ns
		GCLK PLL	t_{SU}	2.796	2.993	3.171	ns
			t_H	–2.516	–2.675	–2.817	ns

Table 1–73. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
	8 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
	8 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
	12 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
	16 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
	8 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns

Table 1–73. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	12 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
	16 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
2.5V	4 mA	GCLK	t_{SU}	0.896	0.922	0.933	ns
			t_H	–0.616	–0.605	–0.579	ns
		GCLK PLL	t_{SU}	2.786	3.002	3.185	ns
			t_H	–2.506	–2.685	–2.831	ns
	8 mA	GCLK	t_{SU}	0.896	0.922	0.933	ns
			t_H	–0.616	–0.605	–0.579	ns
		GCLK PLL	t_{SU}	2.786	3.002	3.185	ns
			t_H	–2.506	–2.685	–2.831	ns
	12 mA	GCLK	t_{SU}	0.896	0.922	0.933	ns
			t_H	–0.616	–0.605	–0.579	ns
		GCLK PLL	t_{SU}	2.786	3.002	3.185	ns
			t_H	–2.506	–2.685	–2.831	ns
	16 mA	GCLK	t_{SU}	0.896	0.922	0.933	ns
			t_H	–0.616	–0.605	–0.579	ns
		GCLK PLL	t_{SU}	2.786	3.002	3.185	ns
			t_H	–2.506	–2.685	–2.831	ns
1.8V	2 mA	GCLK	t_{SU}	0.832	0.883	0.919	ns
			t_H	–0.554	–0.567	–0.564	ns
		GCLK PLL	t_{SU}	2.722	2.963	3.171	ns
			t_H	–2.444	–2.647	–2.816	ns
	4 mA	GCLK	t_{SU}	0.832	0.883	0.919	ns
			t_H	–0.554	–0.567	–0.564	ns
		GCLK PLL	t_{SU}	2.722	2.963	3.171	ns
			t_H	–2.444	–2.647	–2.816	ns
	6 mA	GCLK	t_{SU}	0.832	0.883	0.919	ns
			t_H	–0.554	–0.567	–0.564	ns
		GCLK PLL	t_{SU}	2.722	2.963	3.171	ns
			t_H	–2.444	–2.647	–2.816	ns
	8 mA	GCLK	t_{SU}	0.832	0.883	0.919	ns
			t_H	–0.554	–0.567	–0.564	ns
		GCLK PLL	t_{SU}	2.722	2.963	3.171	ns
			t_H	–2.444	–2.647	–2.816	ns

Table 1–73. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	10 mA	GCLK	t_{SU}	0.832	0.883	0.919	ns
			t_H	–0.554	–0.567	–0.564	ns
		GCLK PLL	t_{SU}	2.722	2.963	3.171	ns
			t_H	–2.444	–2.647	–2.816	ns
	12 mA	GCLK	t_{SU}	0.832	0.883	0.919	ns
			t_H	–0.554	–0.567	–0.564	ns
		GCLK PLL	t_{SU}	2.722	2.963	3.171	ns
			t_H	–2.444	–2.647	–2.816	ns
	16 mA	GCLK	t_{SU}	0.832	0.883	0.919	ns
			t_H	–0.554	–0.567	–0.564	ns
		GCLK PLL	t_{SU}	2.722	2.963	3.171	ns
			t_H	–2.444	–2.647	–2.816	ns
1.5V	2 mA	GCLK	t_{SU}	0.901	0.976	1.037	ns
			t_H	–0.621	–0.658	–0.681	ns
		GCLK PLL	t_{SU}	2.791	3.056	3.289	ns
			t_H	–2.511	–2.738	–2.933	ns
	4 mA	GCLK	t_{SU}	0.901	0.976	1.037	ns
			t_H	–0.621	–0.658	–0.681	ns
		GCLK PLL	t_{SU}	2.791	3.056	3.289	ns
			t_H	–2.511	–2.738	–2.933	ns
	6 mA	GCLK	t_{SU}	0.901	0.976	1.037	ns
			t_H	–0.621	–0.658	–0.681	ns
		GCLK PLL	t_{SU}	2.791	3.056	3.289	ns
			t_H	–2.511	–2.738	–2.933	ns
	8 mA	GCLK	t_{SU}	0.901	0.976	1.037	ns
			t_H	–0.621	–0.658	–0.681	ns
		GCLK PLL	t_{SU}	2.791	3.056	3.289	ns
			t_H	–2.511	–2.738	–2.933	ns
	10 mA	GCLK	t_{SU}	0.901	0.976	1.037	ns
			t_H	–0.621	–0.658	–0.681	ns
		GCLK PLL	t_{SU}	2.791	3.056	3.289	ns
			t_H	–2.511	–2.738	–2.933	ns
	12 mA	GCLK	t_{SU}	0.901	0.976	1.037	ns
			t_H	–0.621	–0.658	–0.681	ns
		GCLK PLL	t_{SU}	2.791	3.056	3.289	ns
			t_H	–2.511	–2.738	–2.933	ns
	16 mA	GCLK	t_{SU}	0.901	0.976	1.037	ns
			t_H	–0.621	–0.658	–0.681	ns
		GCLK PLL	t_{SU}	2.791	3.056	3.289	ns
			t_H	–2.511	–2.738	–2.933	ns

Table 1–73. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	2 mA	GCLK	t_{SU}	1.054	1.156	1.244	ns
			t_H	–0.772	–0.834	–0.883	ns
		GCLK PLL	t_{SU}	2.944	3.236	3.496	ns
			t_H	–2.662	–2.914	–3.135	ns
	4 mA	GCLK	t_{SU}	1.054	1.156	1.244	ns
			t_H	–0.772	–0.834	–0.883	ns
		GCLK PLL	t_{SU}	2.944	3.236	3.496	ns
			t_H	–2.662	–2.914	–3.135	ns
	6 mA	GCLK	t_{SU}	1.054	1.156	1.244	ns
			t_H	–0.772	–0.834	–0.883	ns
		GCLK PLL	t_{SU}	2.944	3.236	3.496	ns
			t_H	–2.662	–2.914	–3.135	ns
	8 mA	GCLK	t_{SU}	1.054	1.156	1.244	ns
			t_H	–0.772	–0.834	–0.883	ns
		GCLK PLL	t_{SU}	2.944	3.236	3.496	ns
			t_H	–2.662	–2.914	–3.135	ns
	10 mA	GCLK	t_{SU}	1.054	1.156	1.244	ns
			t_H	–0.772	–0.834	–0.883	ns
		GCLK PLL	t_{SU}	2.944	3.236	3.496	ns
			t_H	–2.662	–2.914	–3.135	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.882	0.940	0.976	ns
			t_H	–0.602	–0.622	–0.620	ns
		GCLK PLL	t_{SU}	2.776	3.020	3.247	ns
			t_H	–2.496	–2.702	–2.891	ns
	12 mA	GCLK	t_{SU}	0.882	0.940	0.976	ns
			t_H	–0.602	–0.622	–0.620	ns
		GCLK PLL	t_{SU}	2.776	3.020	3.247	ns
			t_H	–2.496	–2.702	–2.891	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.882	0.940	0.976	ns
			t_H	–0.602	–0.622	–0.620	ns
		GCLK PLL	t_{SU}	2.776	3.020	3.247	ns
			t_H	–2.496	–2.702	–2.891	ns

Table 1–73. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.944	1.029	1.093	ns
			t_H	–0.664	–0.710	–0.735	ns
		GCLK PLL	t_{SU}	2.838	3.109	3.364	ns
			t_H	–2.558	–2.790	–3.006	ns
	10 mA	GCLK	t_{SU}	0.944	1.029	1.093	ns
			t_H	–0.664	–0.710	–0.735	ns
		GCLK PLL	t_{SU}	2.838	3.109	3.364	ns
			t_H	–2.558	–2.790	–3.006	ns
	12 mA	GCLK	t_{SU}	0.944	1.029	1.093	ns
			t_H	–0.664	–0.710	–0.735	ns
		GCLK PLL	t_{SU}	2.838	3.109	3.364	ns
			t_H	–2.558	–2.790	–3.006	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.944	1.029	1.093	ns
			t_H	–0.664	–0.710	–0.735	ns
		GCLK PLL	t_{SU}	2.838	3.109	3.364	ns
			t_H	–2.558	–2.790	–3.006	ns
	16 mA	GCLK	t_{SU}	0.944	1.029	1.093	ns
			t_H	–0.664	–0.710	–0.735	ns
		GCLK PLL	t_{SU}	2.838	3.109	3.364	ns
			t_H	–2.558	–2.790	–3.006	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.944	1.029	1.093	ns
			t_H	–0.664	–0.710	–0.735	ns
		GCLK PLL	t_{SU}	2.838	3.109	3.364	ns
			t_H	–2.558	–2.790	–3.006	ns
	10 mA	GCLK	t_{SU}	0.944	1.029	1.093	ns
			t_H	–0.664	–0.710	–0.735	ns
		GCLK PLL	t_{SU}	2.838	3.109	3.364	ns
			t_H	–2.558	–2.790	–3.006	ns
1.8-V HSTL Class I	12 mA	GCLK	t_{SU}	0.944	1.029	1.093	ns
			t_H	–0.664	–0.710	–0.735	ns
		GCLK PLL	t_{SU}	2.838	3.109	3.364	ns
			t_H	–2.558	–2.790	–3.006	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.944	1.029	1.093	ns
			t_H	–0.664	–0.710	–0.735	ns
		GCLK PLL	t_{SU}	2.838	3.109	3.364	ns
			t_H	–2.558	–2.790	–3.006	ns

Table 1–73. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.899	0.988	1.056	ns
			t_H	–0.619	–0.670	–0.699	ns
		GCLK PLL	t_{SU}	2.793	3.068	3.327	ns
			t_H	–2.513	–2.750	–2.970	ns
	10 mA	GCLK	t_{SU}	0.899	0.988	1.056	ns
			t_H	–0.619	–0.670	–0.699	ns
		GCLK PLL	t_{SU}	2.793	3.068	3.327	ns
			t_H	–2.513	–2.750	–2.970	ns
	12 mA	GCLK	t_{SU}	0.899	0.988	1.056	ns
			t_H	–0.619	–0.670	–0.699	ns
		GCLK PLL	t_{SU}	2.793	3.068	3.327	ns
			t_H	–2.513	–2.750	–2.970	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.899	0.988	1.056	ns
			t_H	–0.619	–0.670	–0.699	ns
		GCLK PLL	t_{SU}	2.793	3.068	3.327	ns
			t_H	–2.513	–2.750	–2.970	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.030	1.146	1.241	ns
			t_H	–0.748	–0.824	–0.881	ns
		GCLK PLL	t_{SU}	2.924	3.226	3.512	ns
			t_H	–2.642	–2.904	–3.152	ns
	10 mA	GCLK	t_{SU}	1.030	1.146	1.241	ns
			t_H	–0.748	–0.824	–0.881	ns
		GCLK PLL	t_{SU}	2.924	3.226	3.512	ns
			t_H	–2.642	–2.904	–3.152	ns
3.0-V PCI	—	GCLK	t_{SU}	0.949	0.962	0.958	ns
			t_H	–0.669	–0.644	–0.603	ns
	—	GCLK PLL	t_{SU}	2.839	3.042	3.210	ns
			t_H	–2.559	–2.724	–2.855	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.949	0.962	0.958	ns
			t_H	–0.669	–0.644	–0.603	ns
	—	GCLK PLL	t_{SU}	2.839	3.042	3.210	ns
			t_H	–2.559	–2.724	–2.855	ns

Table 1–74. EP3C40 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.660	6.180	6.725	ns
		GCLK PLL	t_{CO}	3.780	4.112	4.467	ns
	8 mA	GCLK	t_{CO}	5.660	6.180	6.725	ns
		GCLK PLL	t_{CO}	3.780	4.112	4.467	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.619	5.961	6.327	ns
		GCLK PLL	t_{CO}	3.739	3.893	4.069	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.370	5.883	6.423	ns
		GCLK PLL	t_{CO}	3.490	3.815	4.165	ns
	8 mA	GCLK	t_{CO}	5.099	5.599	6.124	ns
		GCLK PLL	t_{CO}	3.219	3.531	3.866	ns
	12 mA	GCLK	t_{CO}	5.002	5.498	6.020	ns
		GCLK PLL	t_{CO}	3.122	3.430	3.762	ns
	16 mA	GCLK	t_{CO}	4.955	5.446	5.962	ns
		GCLK PLL	t_{CO}	3.075	3.378	3.704	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.097	5.596	6.121	ns
		GCLK PLL	t_{CO}	3.217	3.528	3.863	ns
	8 mA	GCLK	t_{CO}	4.956	5.448	5.966	ns
		GCLK PLL	t_{CO}	3.076	3.380	3.708	ns
	12 mA	GCLK	t_{CO}	4.919	5.408	5.923	ns
		GCLK PLL	t_{CO}	3.039	3.340	3.665	ns
	16 mA	GCLK	t_{CO}	4.903	5.393	5.908	ns
		GCLK PLL	t_{CO}	3.023	3.325	3.650	ns
2.5V	4 mA	GCLK	t_{CO}	5.428	5.969	6.537	ns
		GCLK PLL	t_{CO}	3.548	3.901	4.279	ns
	8 mA	GCLK	t_{CO}	5.185	5.716	6.273	ns
		GCLK PLL	t_{CO}	3.305	3.648	4.015	ns
	12 mA	GCLK	t_{CO}	5.087	5.610	6.160	ns
		GCLK PLL	t_{CO}	3.207	3.542	3.902	ns
	16 mA	GCLK	t_{CO}	5.048	5.570	6.119	ns
		GCLK PLL	t_{CO}	3.168	3.502	3.861	ns

Table 1–74. EP3C40 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	2 mA	GCLK	t_{CO}	6.538	7.222	7.935	ns
		GCLK PLL	t_{CO}	4.659	5.154	5.677	ns
	4 mA	GCLK	t_{CO}	6.011	6.677	7.371	ns
		GCLK PLL	t_{CO}	4.132	4.609	5.113	ns
	6 mA	GCLK	t_{CO}	5.786	6.419	7.079	ns
		GCLK PLL	t_{CO}	3.907	4.351	4.821	ns
	8 mA	GCLK	t_{CO}	5.683	6.302	6.950	ns
		GCLK PLL	t_{CO}	3.804	4.234	4.692	ns
	10 mA	GCLK	t_{CO}	5.631	6.254	6.904	ns
		GCLK PLL	t_{CO}	3.752	4.186	4.646	ns
	12 mA	GCLK	t_{CO}	5.574	6.187	6.829	ns
		GCLK PLL	t_{CO}	3.695	4.119	4.571	ns
	16 mA	GCLK	t_{CO}	5.520	6.128	6.764	ns
		GCLK PLL	t_{CO}	3.641	4.060	4.506	ns
1.5V	2 mA	GCLK	t_{CO}	6.926	7.784	8.674	ns
		GCLK PLL	t_{CO}	5.047	5.716	6.416	ns
	4 mA	GCLK	t_{CO}	6.451	7.223	8.026	ns
		GCLK PLL	t_{CO}	4.572	5.155	5.768	ns
	6 mA	GCLK	t_{CO}	6.281	7.040	7.829	ns
		GCLK PLL	t_{CO}	4.402	4.972	5.571	ns
	8 mA	GCLK	t_{CO}	6.193	6.927	7.691	ns
		GCLK PLL	t_{CO}	4.314	4.859	5.433	ns
	10 mA	GCLK	t_{CO}	6.134	6.867	7.630	ns
		GCLK PLL	t_{CO}	4.255	4.799	5.372	ns
	12 mA	GCLK	t_{CO}	6.101	6.826	7.580	ns
		GCLK PLL	t_{CO}	4.222	4.758	5.322	ns
	16 mA	GCLK	t_{CO}	5.987	6.684	7.410	ns
		GCLK PLL	t_{CO}	4.108	4.616	5.152	ns
1.2V	2 mA	GCLK	t_{CO}	8.099	9.312	10.563	ns
		GCLK PLL	t_{CO}	6.220	7.244	8.305	ns
	4 mA	GCLK	t_{CO}	7.654	8.786	9.956	ns
		GCLK PLL	t_{CO}	5.775	6.718	7.698	ns
	6 mA	GCLK	t_{CO}	7.505	8.605	9.742	ns
		GCLK PLL	t_{CO}	5.626	6.537	7.484	ns
	8 mA	GCLK	t_{CO}	7.436	8.525	9.652	ns
		GCLK PLL	t_{CO}	5.557	6.457	7.394	ns
	10 mA	GCLK	t_{CO}	7.300	8.343	9.421	ns
		GCLK PLL	t_{CO}	5.421	6.275	7.163	ns
	12 mA	GCLK	t_{CO}	7.272	8.317	9.399	ns
		GCLK PLL	t_{CO}	5.393	6.249	7.141	ns

Table 1–74. EP3C40 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.043	5.559	6.101	ns
		GCLK PLL	t_{CO}	3.162	3.492	3.843	ns
	12 mA	GCLK	t_{CO}	5.021	5.535	6.078	ns
		GCLK PLL	t_{CO}	3.140	3.468	3.820	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.961	5.473	6.012	ns
		GCLK PLL	t_{CO}	3.080	3.406	3.754	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.477	6.072	6.696	ns
		GCLK PLL	t_{CO}	3.596	4.005	4.438	ns
	10 mA	GCLK	t_{CO}	5.452	6.041	6.659	ns
		GCLK PLL	t_{CO}	3.571	3.974	4.401	ns
	12 mA	GCLK	t_{CO}	5.440	6.027	6.642	ns
		GCLK PLL	t_{CO}	3.559	3.960	4.384	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.411	5.998	6.614	ns
		GCLK PLL	t_{CO}	3.530	3.931	4.356	ns
	16 mA	GCLK	t_{CO}	5.398	5.985	6.600	ns
		GCLK PLL	t_{CO}	3.517	3.918	4.342	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.439	6.024	6.638	ns
		GCLK PLL	t_{CO}	3.558	3.957	4.380	ns
	10 mA	GCLK	t_{CO}	5.428	6.017	6.634	ns
		GCLK PLL	t_{CO}	3.547	3.950	4.376	ns
	12 mA	GCLK	t_{CO}	5.419	6.003	6.614	ns
		GCLK PLL	t_{CO}	3.538	3.936	4.356	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.354	5.937	6.548	ns
		GCLK PLL	t_{CO}	3.473	3.870	4.290	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.953	6.645	7.369	ns
		GCLK PLL	t_{CO}	4.072	4.578	5.111	ns
	10 mA	GCLK	t_{CO}	5.956	6.645	7.364	ns
		GCLK PLL	t_{CO}	4.075	4.578	5.106	ns
	12 mA	GCLK	t_{CO}	5.944	6.637	7.360	ns
		GCLK PLL	t_{CO}	4.063	4.570	5.102	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.882	6.569	7.285	ns
		GCLK PLL	t_{CO}	4.001	4.502	5.027	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.166	8.183	9.236	ns
		GCLK PLL	t_{CO}	5.285	6.116	6.978	ns
	10 mA	GCLK	t_{CO}	7.104	8.094	9.120	ns
		GCLK PLL	t_{CO}	5.223	6.027	6.862	ns
	12 mA	GCLK	t_{CO}	7.106	8.100	9.129	ns
		GCLK PLL	t_{CO}	5.225	6.033	6.871	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	7.061	8.047	9.069	ns
		GCLK PLL	t_{CO}	5.180	5.980	6.811	ns

Table 1–74. EP3C40 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V PCI	—	GCLK	t_{CO}	5.250	5.740	6.257	ns
		GCLK PLL	t_{CO}	3.370	3.672	3.999	ns
3.0-V PCI–X	—	GCLK	t_{CO}	5.250	5.740	6.257	ns
		GCLK PLL	t_{CO}	3.370	3.672	3.999	ns

Table 1–75. EP3C40 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.600	6.114	6.652	ns
		GCLK PLL	t_{CO}	3.710	4.034	4.400	ns
	8 mA	GCLK	t_{CO}	5.600	6.114	6.652	ns
		GCLK PLL	t_{CO}	3.710	4.034	4.400	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.600	5.940	6.302	ns
		GCLK PLL	t_{CO}	3.710	3.860	4.050	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.314	5.821	6.353	ns
		GCLK PLL	t_{CO}	3.424	3.741	4.101	ns
	8 mA	GCLK	t_{CO}	5.057	5.554	6.076	ns
		GCLK PLL	t_{CO}	3.167	3.474	3.824	ns
	12 mA	GCLK	t_{CO}	4.968	5.459	5.974	ns
		GCLK PLL	t_{CO}	3.078	3.379	3.722	ns
	16 mA	GCLK	t_{CO}	4.922	5.408	5.919	ns
		GCLK PLL	t_{CO}	3.032	3.328	3.667	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.055	5.552	6.074	ns
		GCLK PLL	t_{CO}	3.165	3.472	3.822	ns
	8 mA	GCLK	t_{CO}	4.922	5.409	5.922	ns
		GCLK PLL	t_{CO}	3.032	3.329	3.670	ns
	12 mA	GCLK	t_{CO}	4.887	5.373	5.883	ns
		GCLK PLL	t_{CO}	2.997	3.293	3.631	ns
	16 mA	GCLK	t_{CO}	4.872	5.357	5.866	ns
		GCLK PLL	t_{CO}	2.982	3.277	3.614	ns
2.5V	4 mA	GCLK	t_{CO}	5.412	5.935	6.483	ns
		GCLK PLL	t_{CO}	3.522	3.855	4.231	ns
	8 mA	GCLK	t_{CO}	5.177	5.691	6.229	ns
		GCLK PLL	t_{CO}	3.287	3.611	3.977	ns
	12 mA	GCLK	t_{CO}	5.078	5.586	6.119	ns
		GCLK PLL	t_{CO}	3.188	3.506	3.867	ns
	16 mA	GCLK	t_{CO}	5.037	5.544	6.076	ns
		GCLK PLL	t_{CO}	3.147	3.464	3.824	ns

Table 1–75. EP3C40 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	2 mA	GCLK	t_{CO}	6.506	7.171	7.863	ns
		GCLK PLL	t_{CO}	4.616	5.091	5.611	ns
	4 mA	GCLK	t_{CO}	5.993	6.643	7.319	ns
		GCLK PLL	t_{CO}	4.103	4.563	5.067	ns
	6 mA	GCLK	t_{CO}	5.772	6.389	7.032	ns
		GCLK PLL	t_{CO}	3.882	4.309	4.780	ns
	8 mA	GCLK	t_{CO}	5.671	6.275	6.906	ns
		GCLK PLL	t_{CO}	3.781	4.195	4.654	ns
	10 mA	GCLK	t_{CO}	5.620	6.226	6.860	ns
		GCLK PLL	t_{CO}	3.730	4.146	4.608	ns
	12 mA	GCLK	t_{CO}	5.565	6.163	6.787	ns
		GCLK PLL	t_{CO}	3.675	4.083	4.535	ns
	16 mA	GCLK	t_{CO}	5.522	6.116	6.738	ns
		GCLK PLL	t_{CO}	3.632	4.036	4.486	ns
1.5V	2 mA	GCLK	t_{CO}	6.900	7.738	8.608	ns
		GCLK PLL	t_{CO}	5.010	5.658	6.356	ns
	4 mA	GCLK	t_{CO}	6.444	7.194	7.975	ns
		GCLK PLL	t_{CO}	4.554	5.114	5.723	ns
	6 mA	GCLK	t_{CO}	6.277	7.016	7.784	ns
		GCLK PLL	t_{CO}	4.387	4.936	5.532	ns
	8 mA	GCLK	t_{CO}	6.201	6.923	7.674	ns
		GCLK PLL	t_{CO}	4.311	4.843	5.422	ns
	10 mA	GCLK	t_{CO}	6.141	6.860	7.608	ns
		GCLK PLL	t_{CO}	4.251	4.780	5.356	ns
	12 mA	GCLK	t_{CO}	6.107	6.817	7.557	ns
		GCLK PLL	t_{CO}	4.217	4.737	5.305	ns
	16 mA	GCLK	t_{CO}	6.010	6.709	7.438	ns
		GCLK PLL	t_{CO}	4.120	4.629	5.186	ns
1.2V	2 mA	GCLK	t_{CO}	8.088	9.278	10.504	ns
		GCLK PLL	t_{CO}	6.198	7.198	8.252	ns
	4 mA	GCLK	t_{CO}	7.653	8.764	9.912	ns
		GCLK PLL	t_{CO}	5.763	6.684	7.660	ns
	6 mA	GCLK	t_{CO}	7.525	8.610	9.733	ns
		GCLK PLL	t_{CO}	5.635	6.530	7.481	ns
	8 mA	GCLK	t_{CO}	7.453	8.528	9.638	ns
		GCLK PLL	t_{CO}	5.563	6.448	7.386	ns
	10 mA	GCLK	t_{CO}	7.322	8.365	9.443	ns
		GCLK PLL	t_{CO}	5.432	6.285	7.191	ns

Table 1–75. EP3C40 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.010	5.519	6.062	ns
		GCLK PLL	t_{CO}	3.116	3.439	3.791	ns
	12 mA	GCLK	t_{CO}	4.991	5.500	6.041	ns
		GCLK PLL	t_{CO}	3.097	3.420	3.770	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.936	5.443	5.981	ns
		GCLK PLL	t_{CO}	3.042	3.363	3.710	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.444	6.034	6.657	ns
		GCLK PLL	t_{CO}	3.550	3.954	4.386	ns
	10 mA	GCLK	t_{CO}	5.431	6.016	6.636	ns
		GCLK PLL	t_{CO}	3.537	3.936	4.365	ns
	12 mA	GCLK	t_{CO}	5.418	6.001	6.618	ns
		GCLK PLL	t_{CO}	3.524	3.921	4.347	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.388	5.972	6.590	ns
		GCLK PLL	t_{CO}	3.494	3.892	4.319	ns
	16 mA	GCLK	t_{CO}	5.380	5.966	6.585	ns
		GCLK PLL	t_{CO}	3.486	3.886	4.314	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.408	5.988	6.602	ns
		GCLK PLL	t_{CO}	3.514	3.908	4.331	ns
	10 mA	GCLK	t_{CO}	5.403	5.984	6.599	ns
		GCLK PLL	t_{CO}	3.509	3.904	4.328	ns
	12 mA	GCLK	t_{CO}	5.396	5.977	6.592	ns
		GCLK PLL	t_{CO}	3.502	3.897	4.321	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.334	5.911	6.521	ns
		GCLK PLL	t_{CO}	3.440	3.831	4.250	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.923	6.609	7.331	ns
		GCLK PLL	t_{CO}	4.029	4.529	5.060	ns
	10 mA	GCLK	t_{CO}	5.935	6.621	7.342	ns
		GCLK PLL	t_{CO}	4.041	4.541	5.071	ns
	12 mA	GCLK	t_{CO}	5.923	6.612	7.337	ns
		GCLK PLL	t_{CO}	4.029	4.532	5.066	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.868	6.555	7.276	ns
		GCLK PLL	t_{CO}	3.974	4.475	5.005	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.160	8.181	9.244	ns
		GCLK PLL	t_{CO}	5.266	6.101	6.973	ns
	10 mA	GCLK	t_{CO}	7.099	8.096	9.135	ns
		GCLK PLL	t_{CO}	5.205	6.016	6.864	ns
3.0-V PCI	—	GCLK	t_{CO}	5.214	5.700	6.209	ns
		GCLK PLL	t_{CO}	3.324	3.620	3.957	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.214	5.700	6.209	ns
		GCLK PLL	t_{CO}	3.324	3.620	3.957	ns

Table 1–76. EP3C40 Column Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.748	0.806	0.844	ns
			t_{H}	-0.470	-0.490	-0.491	ns
	—	GCLK PLL	t_{SU}	2.628	2.872	3.101	ns
			t_{H}	-2.350	-2.556	-2.748	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.989	5.504	6.045	ns
		GCLK PLL	t_{CO}	3.109	3.438	3.788	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.989	5.504	6.045	ns
		GCLK PLL	t_{CO}	3.109	3.438	3.788	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.370	5.883	6.423	ns
		GCLK PLL	t_{CO}	3.490	3.817	4.166	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.989	5.504	6.045	ns
		GCLK PLL	t_{CO}	3.109	3.438	3.788	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.989	5.504	6.045	ns
		GCLK PLL	t_{CO}	3.109	3.438	3.788	ns

Table 1–77. EP3C40 Row Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	-6	-7	-8	Units
LVDS	—	GCLK	t_{SU}	0.772	0.836	0.879	ns
			t_{H}	-0.494	-0.521	-0.525	ns
			t_{CO}	4.170	4.579	5.015	ns
	—	GCLK PLL	t_{SU}	2.652	2.902	3.136	ns
			t_{H}	-2.374	-2.587	-2.782	ns
			t_{CO}	2.290	2.513	2.758	ns
mini-LVDS	—	GCLK	t_{CO}	4.170	4.579	5.015	ns
		GCLK PLL	t_{CO}	2.290	2.513	2.758	ns
PPDS	—	GCLK	t_{CO}	4.170	4.579	5.015	ns
		GCLK PLL	t_{CO}	2.290	2.513	2.758	ns
RSDS	—	GCLK	t_{CO}	4.170	4.579	5.015	ns
		GCLK PLL	t_{CO}	2.290	2.513	2.758	ns

EP3C55 I/O Timing Parameters

Table 1–78 through Table 1–83 show the maximum I/O timing parameters for EP3C55 devices.

Table 1–78. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	tsu	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
	8 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
	8 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
	12 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
	16 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns

Table 1–78. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
	8 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
	12 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
	16 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
2.5V	4 mA	GCLK	t_{SU}	0.759	0.771	0.765	ns
			t_H	–0.479	–0.454	–0.412	ns
		GCLK PLL	t_{SU}	2.693	2.901	3.082	ns
			t_H	–2.413	–2.584	–2.729	ns
	8 mA	GCLK	t_{SU}	0.759	0.771	0.765	ns
			t_H	–0.479	–0.454	–0.412	ns
		GCLK PLL	t_{SU}	2.693	2.901	3.082	ns
			t_H	–2.413	–2.584	–2.729	ns
	12 mA	GCLK	t_{SU}	0.759	0.771	0.765	ns
			t_H	–0.479	–0.454	–0.412	ns
		GCLK PLL	t_{SU}	2.693	2.901	3.082	ns
			t_H	–2.413	–2.584	–2.729	ns
	16 mA	GCLK	t_{SU}	0.759	0.771	0.765	ns
			t_H	–0.479	–0.454	–0.412	ns
		GCLK PLL	t_{SU}	2.693	2.901	3.082	ns
			t_H	–2.413	–2.584	–2.729	ns

Table 1–78. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	2 mA	GCLK	t_{SU}	0.694	0.732	0.752	ns
			t_H	–0.416	–0.416	–0.398	ns
		GCLK PLL	t_{SU}	2.628	2.863	3.069	ns
			t_H	–2.350	–2.547	–2.715	ns
	4 mA	GCLK	t_{SU}	0.694	0.732	0.752	ns
			t_H	–0.416	–0.416	–0.398	ns
		GCLK PLL	t_{SU}	2.628	2.863	3.069	ns
			t_H	–2.350	–2.547	–2.715	ns
	6 mA	GCLK	t_{SU}	0.694	0.732	0.752	ns
			t_H	–0.416	–0.416	–0.398	ns
		GCLK PLL	t_{SU}	2.628	2.863	3.069	ns
			t_H	–2.350	–2.547	–2.715	ns
	8 mA	GCLK	t_{SU}	0.694	0.732	0.752	ns
			t_H	–0.416	–0.416	–0.398	ns
		GCLK PLL	t_{SU}	2.628	2.863	3.069	ns
			t_H	–2.350	–2.547	–2.715	ns
	10 mA	GCLK	t_{SU}	0.694	0.732	0.752	ns
			t_H	–0.416	–0.416	–0.398	ns
		GCLK PLL	t_{SU}	2.628	2.863	3.069	ns
			t_H	–2.350	–2.547	–2.715	ns
	12 mA	GCLK	t_{SU}	0.694	0.732	0.752	ns
			t_H	–0.416	–0.416	–0.398	ns
		GCLK PLL	t_{SU}	2.628	2.863	3.069	ns
			t_H	–2.350	–2.547	–2.715	ns
	16 mA	GCLK	t_{SU}	0.694	0.732	0.752	ns
			t_H	–0.416	–0.416	–0.398	ns
		GCLK PLL	t_{SU}	2.628	2.863	3.069	ns
			t_H	–2.350	–2.547	–2.715	ns

Table 1–78. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	2 mA	GCLK	t_{SU}	0.763	0.824	0.869	ns
			t_H	–0.483	–0.506	–0.513	ns
		GCLK PLL	t_{SU}	2.697	2.955	3.186	ns
			t_H	–2.417	–2.637	–2.830	ns
	4 mA	GCLK	t_{SU}	0.763	0.824	0.869	ns
			t_H	–0.483	–0.506	–0.513	ns
		GCLK PLL	t_{SU}	2.697	2.955	3.186	ns
			t_H	–2.417	–2.637	–2.830	ns
	6 mA	GCLK	t_{SU}	0.763	0.824	0.869	ns
			t_H	–0.483	–0.506	–0.513	ns
		GCLK PLL	t_{SU}	2.697	2.955	3.186	ns
			t_H	–2.417	–2.637	–2.830	ns
	8 mA	GCLK	t_{SU}	0.763	0.824	0.869	ns
			t_H	–0.483	–0.506	–0.513	ns
		GCLK PLL	t_{SU}	2.697	2.955	3.186	ns
			t_H	–2.417	–2.637	–2.830	ns
	10 mA	GCLK	t_{SU}	0.763	0.824	0.869	ns
			t_H	–0.483	–0.506	–0.513	ns
		GCLK PLL	t_{SU}	2.697	2.955	3.186	ns
			t_H	–2.417	–2.637	–2.830	ns
	12 mA	GCLK	t_{SU}	0.763	0.824	0.869	ns
			t_H	–0.483	–0.506	–0.513	ns
		GCLK PLL	t_{SU}	2.697	2.955	3.186	ns
			t_H	–2.417	–2.637	–2.830	ns
	16 mA	GCLK	t_{SU}	0.763	0.824	0.869	ns
			t_H	–0.483	–0.506	–0.513	ns
		GCLK PLL	t_{SU}	2.697	2.955	3.186	ns
			t_H	–2.417	–2.637	–2.830	ns

Table 1–78. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	2 mA	GCLK	t_{SU}	0.915	1.004	1.075	ns
			t_H	–0.633	–0.682	–0.715	ns
		GCLK PLL	t_{SU}	2.849	3.135	3.392	ns
			t_H	–2.567	–2.813	–3.032	ns
	4 mA	GCLK	t_{SU}	0.915	1.004	1.075	ns
			t_H	–0.633	–0.682	–0.715	ns
		GCLK PLL	t_{SU}	2.849	3.135	3.392	ns
			t_H	–2.567	–2.813	–3.032	ns
	6 mA	GCLK	t_{SU}	0.915	1.004	1.075	ns
			t_H	–0.633	–0.682	–0.715	ns
		GCLK PLL	t_{SU}	2.849	3.135	3.392	ns
			t_H	–2.567	–2.813	–3.032	ns
	8 mA	GCLK	t_{SU}	0.915	1.004	1.075	ns
			t_H	–0.633	–0.682	–0.715	ns
		GCLK PLL	t_{SU}	2.849	3.135	3.392	ns
			t_H	–2.567	–2.813	–3.032	ns
	10 mA	GCLK	t_{SU}	0.915	1.004	1.075	ns
			t_H	–0.633	–0.682	–0.715	ns
		GCLK PLL	t_{SU}	2.849	3.135	3.392	ns
			t_H	–2.567	–2.813	–3.032	ns
	12 mA	GCLK	t_{SU}	0.915	1.004	1.075	ns
			t_H	–0.633	–0.682	–0.715	ns
		GCLK PLL	t_{SU}	2.849	3.135	3.392	ns
			t_H	–2.567	–2.813	–3.032	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.747	0.789	0.812	ns
			t_H	–0.467	–0.472	–0.457	ns
		GCLK PLL	t_{SU}	2.683	2.917	3.137	ns
			t_H	–2.403	–2.600	–2.782	ns
	12 mA	GCLK	t_{SU}	0.747	0.789	0.812	ns
			t_H	–0.467	–0.472	–0.457	ns
		GCLK PLL	t_{SU}	2.683	2.917	3.137	ns
			t_H	–2.403	–2.600	–2.782	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.747	0.789	0.812	ns
			t_H	–0.467	–0.472	–0.457	ns
		GCLK PLL	t_{SU}	2.683	2.917	3.137	ns
			t_H	–2.403	–2.600	–2.782	ns

Table 1–78. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.808	0.878	0.930	ns
			t_H	–0.528	–0.559	–0.573	ns
		GCLK PLL	t_{SU}	2.744	3.009	3.248	ns
			t_H	–2.464	–2.690	–2.891	ns
	10 mA	GCLK	t_{SU}	0.808	0.878	0.930	ns
			t_H	–0.528	–0.559	–0.573	ns
		GCLK PLL	t_{SU}	2.744	3.009	3.248	ns
			t_H	–2.464	–2.690	–2.891	ns
	12 mA	GCLK	t_{SU}	0.808	0.878	0.930	ns
			t_H	–0.528	–0.559	–0.573	ns
		GCLK PLL	t_{SU}	2.744	3.009	3.248	ns
			t_H	–2.464	–2.690	–2.891	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.808	0.878	0.930	ns
			t_H	–0.528	–0.559	–0.573	ns
		GCLK PLL	t_{SU}	2.744	3.009	3.248	ns
			t_H	–2.464	–2.690	–2.891	ns
	16 mA	GCLK	t_{SU}	0.808	0.878	0.930	ns
			t_H	–0.528	–0.559	–0.573	ns
		GCLK PLL	t_{SU}	2.744	3.009	3.248	ns
			t_H	–2.464	–2.690	–2.891	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.808	0.878	0.930	ns
			t_H	–0.528	–0.559	–0.573	ns
		GCLK PLL	t_{SU}	2.744	3.009	3.248	ns
			t_H	–2.464	–2.690	–2.891	ns
	10 mA	GCLK	t_{SU}	0.808	0.878	0.930	ns
			t_H	–0.528	–0.559	–0.573	ns
		GCLK PLL	t_{SU}	2.744	3.009	3.248	ns
			t_H	–2.464	–2.690	–2.891	ns
	12 mA	GCLK	t_{SU}	0.808	0.878	0.930	ns
			t_H	–0.528	–0.559	–0.573	ns
		GCLK PLL	t_{SU}	2.744	3.009	3.248	ns
			t_H	–2.464	–2.690	–2.891	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.808	0.878	0.930	ns
			t_H	–0.528	–0.559	–0.573	ns
		GCLK PLL	t_{SU}	2.744	3.009	3.248	ns
			t_H	–2.464	–2.690	–2.891	ns

Table 1–78. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.764	0.838	0.896	ns
			t_H	–0.484	–0.520	–0.540	ns
		GCLK PLL	t_{SU}	2.700	2.969	3.214	ns
			t_H	–2.420	–2.651	–2.858	ns
	10 mA	GCLK	t_{SU}	0.764	0.838	0.896	ns
			t_H	–0.484	–0.520	–0.540	ns
		GCLK PLL	t_{SU}	2.700	2.969	3.214	ns
			t_H	–2.420	–2.651	–2.858	ns
	12 mA	GCLK	t_{SU}	0.764	0.838	0.896	ns
			t_H	–0.484	–0.520	–0.540	ns
		GCLK PLL	t_{SU}	2.700	2.969	3.214	ns
			t_H	–2.420	–2.651	–2.858	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.764	0.838	0.896	ns
			t_H	–0.484	–0.520	–0.540	ns
		GCLK PLL	t_{SU}	2.700	2.969	3.214	ns
			t_H	–2.420	–2.651	–2.858	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.896	0.997	1.080	ns
			t_H	–0.614	–0.675	–0.720	ns
		GCLK PLL	t_{SU}	2.832	3.128	3.398	ns
			t_H	–2.550	–2.806	–3.038	ns
	10 mA	GCLK	t_{SU}	0.896	0.997	1.080	ns
			t_H	–0.614	–0.675	–0.720	ns
		GCLK PLL	t_{SU}	2.832	3.128	3.398	ns
			t_H	–2.550	–2.806	–3.038	ns
	12 mA	GCLK	t_{SU}	0.896	0.997	1.080	ns
			t_H	–0.614	–0.675	–0.720	ns
		GCLK PLL	t_{SU}	2.832	3.128	3.398	ns
			t_H	–2.550	–2.806	–3.038	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	0.896	0.997	1.080	ns
			t_H	–0.614	–0.675	–0.720	ns
		GCLK PLL	t_{SU}	2.832	3.128	3.398	ns
			t_H	–2.550	–2.806	–3.038	ns
3.0-V PCI	—	GCLK	t_{SU}	0.812	0.812	0.792	ns
			t_H	–0.532	–0.494	–0.438	ns
	—	GCLK PLL	t_{SU}	2.746	2.942	3.109	ns
			t_H	–2.466	–2.624	–2.755	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.812	0.812	0.792	ns
			t_H	–0.532	–0.494	–0.438	ns
	—	GCLK PLL	t_{SU}	2.746	2.942	3.109	ns
			t_H	–2.466	–2.624	–2.755	ns

Table 1–79. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
	8 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
	8 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
	12 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
	16 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns

Table 1–79. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
	8 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
	12 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
	16 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
2.5V	4 mA	GCLK	t_{SU}	0.783	0.805	0.803	ns
			t_H	–0.503	–0.488	–0.449	ns
		GCLK PLL	t_{SU}	2.737	2.949	3.132	ns
			t_H	–2.457	–2.632	–2.778	ns
	8 mA	GCLK	t_{SU}	0.783	0.805	0.803	ns
			t_H	–0.503	–0.488	–0.449	ns
		GCLK PLL	t_{SU}	2.737	2.949	3.132	ns
			t_H	–2.457	–2.632	–2.778	ns
	12 mA	GCLK	t_{SU}	0.783	0.805	0.803	ns
			t_H	–0.503	–0.488	–0.449	ns
		GCLK PLL	t_{SU}	2.737	2.949	3.132	ns
			t_H	–2.457	–2.632	–2.778	ns
	16 mA	GCLK	t_{SU}	0.783	0.805	0.803	ns
			t_H	–0.503	–0.488	–0.449	ns
		GCLK PLL	t_{SU}	2.737	2.949	3.132	ns
			t_H	–2.457	–2.632	–2.778	ns

Table 1–79. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	2 mA	GCLK	t_{SU}	0.719	0.766	0.789	ns
			t_H	–0.441	–0.450	–0.434	ns
		GCLK PLL	t_{SU}	2.673	2.910	3.118	ns
			t_H	–2.395	–2.594	–2.763	ns
	4 mA	GCLK	t_{SU}	0.719	0.766	0.789	ns
			t_H	–0.441	–0.450	–0.434	ns
		GCLK PLL	t_{SU}	2.673	2.910	3.118	ns
			t_H	–2.395	–2.594	–2.763	ns
	6 mA	GCLK	t_{SU}	0.719	0.766	0.789	ns
			t_H	–0.441	–0.450	–0.434	ns
		GCLK PLL	t_{SU}	2.673	2.910	3.118	ns
			t_H	–2.395	–2.594	–2.763	ns
	8 mA	GCLK	t_{SU}	0.719	0.766	0.789	ns
			t_H	–0.441	–0.450	–0.434	ns
		GCLK PLL	t_{SU}	2.673	2.910	3.118	ns
			t_H	–2.395	–2.594	–2.763	ns
	10 mA	GCLK	t_{SU}	0.719	0.766	0.789	ns
			t_H	–0.441	–0.450	–0.434	ns
		GCLK PLL	t_{SU}	2.673	2.910	3.118	ns
			t_H	–2.395	–2.594	–2.763	ns
	12 mA	GCLK	t_{SU}	0.719	0.766	0.789	ns
			t_H	–0.441	–0.450	–0.434	ns
		GCLK PLL	t_{SU}	2.673	2.910	3.118	ns
			t_H	–2.395	–2.594	–2.763	ns
	16 mA	GCLK	t_{SU}	0.719	0.766	0.789	ns
			t_H	–0.441	–0.450	–0.434	ns
		GCLK PLL	t_{SU}	2.673	2.910	3.118	ns
			t_H	–2.395	–2.594	–2.763	ns
1.5V	2 mA	GCLK	t_{SU}	0.788	0.859	0.907	ns
			t_H	–0.508	–0.541	–0.551	ns
		GCLK PLL	t_{SU}	2.742	3.003	3.236	ns
			t_H	–2.462	–2.685	–2.880	ns
	4 mA	GCLK	t_{SU}	0.788	0.859	0.907	ns
			t_H	–0.508	–0.541	–0.551	ns
		GCLK PLL	t_{SU}	2.742	3.003	3.236	ns
			t_H	–2.462	–2.685	–2.880	ns
	6 mA	GCLK	t_{SU}	0.788	0.859	0.907	ns
			t_H	–0.508	–0.541	–0.551	ns
		GCLK PLL	t_{SU}	2.742	3.003	3.236	ns
			t_H	–2.462	–2.685	–2.880	ns

Table 1–79. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	8 mA	GCLK	t_{SU}	0.788	0.859	0.907	ns
			t_H	–0.508	–0.541	–0.551	ns
		GCLK PLL	t_{SU}	2.742	3.003	3.236	ns
			t_H	–2.462	–2.685	–2.880	ns
	10 mA	GCLK	t_{SU}	0.788	0.859	0.907	ns
			t_H	–0.508	–0.541	–0.551	ns
		GCLK PLL	t_{SU}	2.742	3.003	3.236	ns
			t_H	–2.462	–2.685	–2.880	ns
	12 mA	GCLK	t_{SU}	0.788	0.859	0.907	ns
			t_H	–0.508	–0.541	–0.551	ns
		GCLK PLL	t_{SU}	2.742	3.003	3.236	ns
			t_H	–2.462	–2.685	–2.880	ns
	16 mA	GCLK	t_{SU}	0.788	0.859	0.907	ns
			t_H	–0.508	–0.541	–0.551	ns
		GCLK PLL	t_{SU}	2.742	3.003	3.236	ns
			t_H	–2.462	–2.685	–2.880	ns
1.2V	2 mA	GCLK	t_{SU}	0.941	1.039	1.114	ns
			t_H	–0.659	–0.717	–0.753	ns
		GCLK PLL	t_{SU}	2.895	3.183	3.443	ns
			t_H	–2.613	–2.861	–3.082	ns
	4 mA	GCLK	t_{SU}	0.941	1.039	1.114	ns
			t_H	–0.659	–0.717	–0.753	ns
		GCLK PLL	t_{SU}	2.895	3.183	3.443	ns
			t_H	–2.613	–2.861	–3.082	ns
	6 mA	GCLK	t_{SU}	0.941	1.039	1.114	ns
			t_H	–0.659	–0.717	–0.753	ns
		GCLK PLL	t_{SU}	2.895	3.183	3.443	ns
			t_H	–2.613	–2.861	–3.082	ns
	8 mA	GCLK	t_{SU}	0.941	1.039	1.114	ns
			t_H	–0.659	–0.717	–0.753	ns
		GCLK PLL	t_{SU}	2.895	3.183	3.443	ns
			t_H	–2.613	–2.861	–3.082	ns
	10 mA	GCLK	t_{SU}	0.941	1.039	1.114	ns
			t_H	–0.659	–0.717	–0.753	ns
		GCLK PLL	t_{SU}	2.895	3.183	3.443	ns
			t_H	–2.613	–2.861	–3.082	ns

Table 1–79. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.773	0.824	0.851	ns
			t_H	–0.493	–0.506	–0.495	ns
		GCLK PLL	t_{SU}	2.722	2.960	3.177	ns
			t_H	–2.442	–2.642	–2.821	ns
	12 mA	GCLK	t_{SU}	0.773	0.824	0.851	ns
			t_H	–0.493	–0.506	–0.495	ns
		GCLK PLL	t_{SU}	2.722	2.960	3.177	ns
			t_H	–2.442	–2.642	–2.821	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.773	0.824	0.851	ns
			t_H	–0.493	–0.506	–0.495	ns
		GCLK PLL	t_{SU}	2.722	2.960	3.177	ns
			t_H	–2.442	–2.642	–2.821	ns
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.835	0.913	0.968	ns
			t_H	–0.555	–0.594	–0.610	ns
		GCLK PLL	t_{SU}	2.784	3.049	3.294	ns
			t_H	–2.504	–2.730	–2.936	ns
	10 mA	GCLK	t_{SU}	0.835	0.913	0.968	ns
			t_H	–0.555	–0.594	–0.610	ns
		GCLK PLL	t_{SU}	2.784	3.049	3.294	ns
			t_H	–2.504	–2.730	–2.936	ns
	12 mA	GCLK	t_{SU}	0.835	0.913	0.968	ns
			t_H	–0.555	–0.594	–0.610	ns
		GCLK PLL	t_{SU}	2.784	3.049	3.294	ns
			t_H	–2.504	–2.730	–2.936	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.835	0.913	0.968	ns
			t_H	–0.555	–0.594	–0.610	ns
		GCLK PLL	t_{SU}	2.784	3.049	3.294	ns
			t_H	–2.504	–2.730	–2.936	ns
	16 mA	GCLK	t_{SU}	0.835	0.913	0.968	ns
			t_H	–0.555	–0.594	–0.610	ns
		GCLK PLL	t_{SU}	2.784	3.049	3.294	ns
			t_H	–2.504	–2.730	–2.936	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.835	0.913	0.968	ns
			t_H	–0.555	–0.594	–0.610	ns
		GCLK PLL	t_{SU}	2.784	3.049	3.294	ns
			t_H	–2.504	–2.730	–2.936	ns
	10 mA	GCLK	t_{SU}	0.835	0.913	0.968	ns
			t_H	–0.555	–0.594	–0.610	ns
		GCLK PLL	t_{SU}	2.784	3.049	3.294	ns
			t_H	–2.504	–2.730	–2.936	ns

Table 1–79. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8-V HSTL Class I	12 mA	GCLK	t_{SU}	0.835	0.913	0.968	ns
			t_H	–0.555	–0.594	–0.610	ns
		GCLK PLL	t_{SU}	2.784	3.049	3.294	ns
			t_H	–2.504	–2.730	–2.936	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.835	0.913	0.968	ns
			t_H	–0.555	–0.594	–0.610	ns
		GCLK PLL	t_{SU}	2.784	3.049	3.294	ns
			t_H	–2.504	–2.730	–2.936	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.790	0.872	0.931	ns
			t_H	–0.510	–0.554	–0.574	ns
		GCLK PLL	t_{SU}	2.739	3.008	3.257	ns
			t_H	–2.459	–2.690	–2.900	ns
	10 mA	GCLK	t_{SU}	0.790	0.872	0.931	ns
			t_H	–0.510	–0.554	–0.574	ns
		GCLK PLL	t_{SU}	2.739	3.008	3.257	ns
			t_H	–2.459	–2.690	–2.900	ns
	12 mA	GCLK	t_{SU}	0.790	0.872	0.931	ns
			t_H	–0.510	–0.554	–0.574	ns
		GCLK PLL	t_{SU}	2.739	3.008	3.257	ns
			t_H	–2.459	–2.690	–2.900	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.790	0.872	0.931	ns
			t_H	–0.510	–0.554	–0.574	ns
		GCLK PLL	t_{SU}	2.739	3.008	3.257	ns
			t_H	–2.459	–2.690	–2.900	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.921	1.030	1.116	ns
			t_H	–0.639	–0.708	–0.756	ns
		GCLK PLL	t_{SU}	2.870	3.166	3.442	ns
			t_H	–2.588	–2.844	–3.082	ns
	10 mA	GCLK	t_{SU}	0.921	1.030	1.116	ns
			t_H	–0.639	–0.708	–0.756	ns
		GCLK PLL	t_{SU}	2.870	3.166	3.442	ns
			t_H	–2.588	–2.844	–3.082	ns
3.0-V PCI	—	GCLK	t_{SU}	0.836	0.845	0.828	ns
			t_H	–0.556	–0.527	–0.473	ns
	—	GCLK PLL	t_{SU}	2.790	2.989	3.157	ns
			t_H	–2.510	–2.671	–2.802	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.836	0.845	0.828	ns
			t_H	–0.556	–0.527	–0.473	ns
	—	GCLK PLL	t_{SU}	2.790	2.989	3.157	ns
			t_H	–2.510	–2.671	–2.802	ns

Table 1–80. EP3C55 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.764	6.293	6.845	ns
		GCLK PLL	t_{CO}	3.830	4.163	4.528	ns
	8 mA	GCLK	t_{CO}	5.764	6.293	6.845	ns
		GCLK PLL	t_{CO}	3.830	4.163	4.528	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.723	6.074	6.447	ns
		GCLK PLL	t_{CO}	3.789	3.944	4.130	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.474	5.996	6.543	ns
		GCLK PLL	t_{CO}	3.540	3.866	4.226	ns
	8 mA	GCLK	t_{CO}	5.203	5.712	6.244	ns
		GCLK PLL	t_{CO}	3.269	3.582	3.927	ns
	12 mA	GCLK	t_{CO}	5.106	5.611	6.140	ns
		GCLK PLL	t_{CO}	3.172	3.481	3.823	ns
	16 mA	GCLK	t_{CO}	5.059	5.559	6.082	ns
		GCLK PLL	t_{CO}	3.125	3.429	3.765	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.201	5.709	6.241	ns
		GCLK PLL	t_{CO}	3.267	3.579	3.924	ns
	8 mA	GCLK	t_{CO}	5.060	5.561	6.086	ns
		GCLK PLL	t_{CO}	3.126	3.431	3.769	ns
	12 mA	GCLK	t_{CO}	5.023	5.521	6.043	ns
		GCLK PLL	t_{CO}	3.089	3.391	3.726	ns
	16 mA	GCLK	t_{CO}	5.007	5.506	6.028	ns
		GCLK PLL	t_{CO}	3.073	3.376	3.711	ns
2.5V	4 mA	GCLK	t_{CO}	5.532	6.082	6.657	ns
		GCLK PLL	t_{CO}	3.598	3.952	4.340	ns
	8 mA	GCLK	t_{CO}	5.289	5.829	6.393	ns
		GCLK PLL	t_{CO}	3.355	3.699	4.076	ns
	12 mA	GCLK	t_{CO}	5.191	5.723	6.280	ns
		GCLK PLL	t_{CO}	3.257	3.593	3.963	ns
	16 mA	GCLK	t_{CO}	5.152	5.683	6.239	ns
		GCLK PLL	t_{CO}	3.218	3.553	3.922	ns
1.8V	2 mA	GCLK	t_{CO}	6.643	7.335	8.056	ns
		GCLK PLL	t_{CO}	4.709	5.204	5.738	ns
	4 mA	GCLK	t_{CO}	6.116	6.790	7.492	ns
		GCLK PLL	t_{CO}	4.182	4.659	5.174	ns
	6 mA	GCLK	t_{CO}	5.891	6.532	7.200	ns
		GCLK PLL	t_{CO}	3.957	4.401	4.882	ns
	8 mA	GCLK	t_{CO}	5.788	6.415	7.071	ns
		GCLK PLL	t_{CO}	3.854	4.284	4.753	ns

Table 1–80. EP3C55 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	10 mA	GCLK	t_{CO}	5.736	6.367	7.025	ns
		GCLK PLL	t_{CO}	3.802	4.236	4.707	ns
	12 mA	GCLK	t_{CO}	5.679	6.300	6.950	ns
		GCLK PLL	t_{CO}	3.745	4.169	4.632	ns
	16 mA	GCLK	t_{CO}	5.625	6.241	6.885	ns
		GCLK PLL	t_{CO}	3.691	4.110	4.567	ns
1.5V	2 mA	GCLK	t_{CO}	7.031	7.897	8.795	ns
		GCLK PLL	t_{CO}	5.097	5.766	6.477	ns
	4 mA	GCLK	t_{CO}	6.556	7.336	8.147	ns
		GCLK PLL	t_{CO}	4.622	5.205	5.829	ns
	6 mA	GCLK	t_{CO}	6.386	7.153	7.950	ns
		GCLK PLL	t_{CO}	4.452	5.022	5.632	ns
	8 mA	GCLK	t_{CO}	6.298	7.040	7.812	ns
		GCLK PLL	t_{CO}	4.364	4.909	5.494	ns
	10 mA	GCLK	t_{CO}	6.239	6.980	7.751	ns
		GCLK PLL	t_{CO}	4.305	4.849	5.433	ns
	12 mA	GCLK	t_{CO}	6.206	6.939	7.701	ns
		GCLK PLL	t_{CO}	4.272	4.808	5.383	ns
	16 mA	GCLK	t_{CO}	6.092	6.797	7.531	ns
		GCLK PLL	t_{CO}	4.158	4.666	5.213	ns
1.2V	2 mA	GCLK	t_{CO}	8.204	9.425	10.684	ns
		GCLK PLL	t_{CO}	6.270	7.294	8.366	ns
	4 mA	GCLK	t_{CO}	7.759	8.899	10.077	ns
		GCLK PLL	t_{CO}	5.825	6.768	7.759	ns
	6 mA	GCLK	t_{CO}	7.610	8.718	9.863	ns
		GCLK PLL	t_{CO}	5.676	6.587	7.545	ns
	8 mA	GCLK	t_{CO}	7.541	8.638	9.773	ns
		GCLK PLL	t_{CO}	5.607	6.507	7.455	ns
	10 mA	GCLK	t_{CO}	7.405	8.456	9.542	ns
		GCLK PLL	t_{CO}	5.471	6.325	7.224	ns
	12 mA	GCLK	t_{CO}	7.377	8.430	9.520	ns
		GCLK PLL	t_{CO}	5.443	6.299	7.202	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.148	5.672	6.224	ns
		GCLK PLL	t_{CO}	3.212	3.544	3.899	ns
	12 mA	GCLK	t_{CO}	5.126	5.648	6.201	ns
		GCLK PLL	t_{CO}	3.190	3.520	3.876	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	5.066	5.586	6.135	ns
		GCLK PLL	t_{CO}	3.130	3.458	3.810	ns

Table 1–80. EP3C55 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.582	6.185	6.816	ns
		GCLK PLL	t_{CO}	3.646	4.054	4.498	ns
	10 mA	GCLK	t_{CO}	5.557	6.154	6.779	ns
		GCLK PLL	t_{CO}	3.621	4.023	4.461	ns
	12 mA	GCLK	t_{CO}	5.545	6.140	6.762	ns
		GCLK PLL	t_{CO}	3.609	4.009	4.444	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.516	6.111	6.734	ns
		GCLK PLL	t_{CO}	3.580	3.980	4.416	ns
	16 mA	GCLK	t_{CO}	5.503	6.098	6.720	ns
		GCLK PLL	t_{CO}	3.567	3.967	4.402	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.544	6.137	6.758	ns
		GCLK PLL	t_{CO}	3.608	4.006	4.440	ns
	10 mA	GCLK	t_{CO}	5.533	6.130	6.754	ns
		GCLK PLL	t_{CO}	3.597	3.999	4.436	ns
	12 mA	GCLK	t_{CO}	5.524	6.116	6.734	ns
		GCLK PLL	t_{CO}	3.588	3.985	4.416	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.459	6.050	6.668	ns
		GCLK PLL	t_{CO}	3.523	3.919	4.350	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	6.058	6.758	7.489	ns
		GCLK PLL	t_{CO}	4.122	4.627	5.171	ns
	10 mA	GCLK	t_{CO}	6.061	6.758	7.484	ns
		GCLK PLL	t_{CO}	4.125	4.627	5.166	ns
	12 mA	GCLK	t_{CO}	6.049	6.750	7.480	ns
		GCLK PLL	t_{CO}	4.113	4.619	5.162	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.987	6.682	7.405	ns
		GCLK PLL	t_{CO}	4.051	4.551	5.087	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.271	8.296	9.356	ns
		GCLK PLL	t_{CO}	5.335	6.165	7.038	ns
	10 mA	GCLK	t_{CO}	7.209	8.207	9.240	ns
		GCLK PLL	t_{CO}	5.273	6.076	6.922	ns
	12 mA	GCLK	t_{CO}	7.211	8.213	9.249	ns
		GCLK PLL	t_{CO}	5.275	6.082	6.931	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	7.166	8.160	9.189	ns
		GCLK PLL	t_{CO}	5.230	6.029	6.871	ns
3.0-V PCI	—	GCLK	t_{CO}	5.354	5.853	6.377	ns
		GCLK PLL	t_{CO}	3.420	3.723	4.060	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.354	5.853	6.377	ns
		GCLK PLL	t_{CO}	3.420	3.723	4.060	ns

Table 1–81. EP3C55 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.713	6.231	6.782	ns
		GCLK PLL	t_{CO}	3.759	4.087	4.453	ns
	8 mA	GCLK	t_{CO}	5.713	6.231	6.782	ns
		GCLK PLL	t_{CO}	3.759	4.087	4.453	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.713	6.057	6.432	ns
		GCLK PLL	t_{CO}	3.759	3.913	4.103	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.427	5.938	6.483	ns
		GCLK PLL	t_{CO}	3.473	3.794	4.154	ns
	8 mA	GCLK	t_{CO}	5.170	5.671	6.206	ns
		GCLK PLL	t_{CO}	3.216	3.527	3.877	ns
	12 mA	GCLK	t_{CO}	5.081	5.576	6.104	ns
		GCLK PLL	t_{CO}	3.127	3.432	3.775	ns
	16 mA	GCLK	t_{CO}	5.035	5.525	6.049	ns
		GCLK PLL	t_{CO}	3.081	3.381	3.720	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.168	5.669	6.204	ns
		GCLK PLL	t_{CO}	3.214	3.525	3.875	ns
	8 mA	GCLK	t_{CO}	5.035	5.526	6.052	ns
		GCLK PLL	t_{CO}	3.081	3.382	3.723	ns
	12 mA	GCLK	t_{CO}	5.000	5.490	6.013	ns
		GCLK PLL	t_{CO}	3.046	3.346	3.684	ns
	16 mA	GCLK	t_{CO}	4.985	5.474	5.996	ns
		GCLK PLL	t_{CO}	3.031	3.330	3.667	ns
2.5V	4 mA	GCLK	t_{CO}	5.525	6.052	6.613	ns
		GCLK PLL	t_{CO}	3.571	3.908	4.284	ns
	8 mA	GCLK	t_{CO}	5.290	5.808	6.359	ns
		GCLK PLL	t_{CO}	3.336	3.664	4.030	ns
	12 mA	GCLK	t_{CO}	5.191	5.703	6.249	ns
		GCLK PLL	t_{CO}	3.237	3.559	3.920	ns
	16 mA	GCLK	t_{CO}	5.150	5.661	6.206	ns
		GCLK PLL	t_{CO}	3.196	3.517	3.877	ns
1.8V	2 mA	GCLK	t_{CO}	6.619	7.288	7.993	ns
		GCLK PLL	t_{CO}	4.665	5.144	5.664	ns
	4 mA	GCLK	t_{CO}	6.106	6.760	7.449	ns
		GCLK PLL	t_{CO}	4.152	4.616	5.120	ns
	6 mA	GCLK	t_{CO}	5.885	6.506	7.162	ns
		GCLK PLL	t_{CO}	3.931	4.362	4.833	ns
	8 mA	GCLK	t_{CO}	5.784	6.392	7.036	ns
		GCLK PLL	t_{CO}	3.830	4.248	4.707	ns

Table 1–81. EP3C55 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	10 mA	GCLK	t_{CO}	5.733	6.343	6.990	ns
		GCLK PLL	t_{CO}	3.779	4.199	4.661	ns
	12 mA	GCLK	t_{CO}	5.678	6.280	6.917	ns
		GCLK PLL	t_{CO}	3.724	4.136	4.588	ns
	16 mA	GCLK	t_{CO}	5.635	6.233	6.868	ns
		GCLK PLL	t_{CO}	3.681	4.089	4.539	ns
1.5V	2 mA	GCLK	t_{CO}	7.013	7.855	8.738	ns
		GCLK PLL	t_{CO}	5.059	5.711	6.409	ns
	4 mA	GCLK	t_{CO}	6.557	7.311	8.105	ns
		GCLK PLL	t_{CO}	4.603	5.167	5.776	ns
	6 mA	GCLK	t_{CO}	6.390	7.133	7.914	ns
		GCLK PLL	t_{CO}	4.436	4.989	5.585	ns
	8 mA	GCLK	t_{CO}	6.314	7.040	7.804	ns
		GCLK PLL	t_{CO}	4.360	4.896	5.475	ns
	10mA	GCLK	t_{CO}	6.254	6.977	7.738	ns
		GCLK PLL	t_{CO}	4.300	4.833	5.409	ns
	12 mA	GCLK	t_{CO}	6.220	6.934	7.687	ns
		GCLK PLL	t_{CO}	4.266	4.790	5.358	ns
	16 mA	GCLK	t_{CO}	6.123	6.826	7.568	ns
		GCLK PLL	t_{CO}	4.169	4.682	5.239	ns
1.2V	2 mA	GCLK	t_{CO}	8.201	9.395	10.634	ns
		GCLK PLL	t_{CO}	6.247	7.251	8.305	ns
	4 mA	GCLK	t_{CO}	7.766	8.881	10.042	ns
		GCLK PLL	t_{CO}	5.812	6.737	7.713	ns
	6 mA	GCLK	t_{CO}	7.638	8.727	9.863	ns
		GCLK PLL	t_{CO}	5.684	6.583	7.534	ns
	8 mA	GCLK	t_{CO}	7.566	8.645	9.768	ns
		GCLK PLL	t_{CO}	5.612	6.501	7.439	ns
	10 mA	GCLK	t_{CO}	7.435	8.482	9.573	ns
		GCLK PLL	t_{CO}	5.481	6.338	7.244	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.119	5.635	6.187	ns
		GCLK PLL	t_{CO}	3.170	3.499	3.861	ns
	12 mA	GCLK	t_{CO}	5.100	5.616	6.166	ns
		GCLK PLL	t_{CO}	3.151	3.480	3.840	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	5.045	5.559	6.106	ns
		GCLK PLL	t_{CO}	3.096	3.423	3.780	ns

Table 1–81. EP3C55 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.553	6.150	6.782	ns
		GCLK PLL	t_{CO}	3.604	4.014	4.456	ns
	10 mA	GCLK	t_{CO}	5.540	6.132	6.761	ns
		GCLK PLL	t_{CO}	3.591	3.996	4.435	ns
	12 mA	GCLK	t_{CO}	5.527	6.117	6.743	ns
		GCLK PLL	t_{CO}	3.578	3.981	4.417	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.497	6.088	6.715	ns
		GCLK PLL	t_{CO}	3.548	3.952	4.389	ns
	16 mA	GCLK	t_{CO}	5.489	6.082	6.710	ns
		GCLK PLL	t_{CO}	3.540	3.946	4.384	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.517	6.104	6.727	ns
		GCLK PLL	t_{CO}	3.568	3.968	4.401	ns
	10 mA	GCLK	t_{CO}	5.512	6.100	6.724	ns
		GCLK PLL	t_{CO}	3.563	3.964	4.398	ns
	12 mA	GCLK	t_{CO}	5.505	6.093	6.717	ns
		GCLK PLL	t_{CO}	3.556	3.957	4.391	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.443	6.027	6.646	ns
		GCLK PLL	t_{CO}	3.494	3.891	4.320	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	6.032	6.725	7.456	ns
		GCLK PLL	t_{CO}	4.083	4.589	5.130	ns
	10 mA	GCLK	t_{CO}	6.044	6.737	7.467	ns
		GCLK PLL	t_{CO}	4.095	4.601	5.141	ns
	12 mA	GCLK	t_{CO}	6.032	6.728	7.462	ns
		GCLK PLL	t_{CO}	4.083	4.592	5.136	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.977	6.671	7.401	ns
		GCLK PLL	t_{CO}	4.028	4.535	5.075	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.269	8.297	9.369	ns
		GCLK PLL	t_{CO}	5.320	6.161	7.043	ns
	10 mA	GCLK	t_{CO}	7.208	8.212	9.260	ns
		GCLK PLL	t_{CO}	5.259	6.076	6.934	ns
3.0-V PCI	—	GCLK	t_{CO}	5.327	5.817	6.339	ns
		GCLK PLL	t_{CO}	3.373	3.673	4.010	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.327	5.817	6.339	ns
		GCLK PLL	t_{CO}	3.373	3.673	4.010	ns

Table 1–82. EP3C55 Column Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.644	0.695	0.720	ns
			t_{H}	–0.366	–0.379	–0.367	ns
	—	GCLK PLL	t_{SU}	2.579	2.821	3.042	ns
			t_{H}	–2.301	–2.505	–2.689	ns
LVDS_E_3R	—	GCLK	t_{CO}	5.093	5.615	6.169	ns
		GCLK PLL	t_{CO}	3.158	3.489	3.847	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	5.093	5.615	6.169	ns
		GCLK PLL	t_{CO}	3.158	3.489	3.847	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.474	5.994	6.547	ns
		GCLK PLL	t_{CO}	3.539	3.868	4.225	ns
RSDS_E_1R	—	GCLK	t_{CO}	5.093	5.615	6.169	ns
		GCLK PLL	t_{CO}	3.158	3.489	3.847	ns
RSDS_E_3R	—	GCLK	t_{CO}	5.093	5.615	6.169	ns
		GCLK PLL	t_{CO}	3.158	3.489	3.847	ns

Table 1–83. EP3C55 Row Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.670	0.725	0.758	ns
			t_{H}	–0.392	–0.410	–0.404	ns
			t_{CO}	4.278	4.693	5.139	ns
	—	GCLK PLL	t_{SU}	2.607	2.852	3.081	ns
			t_{H}	–2.329	–2.537	–2.727	ns
			t_{CO}	2.336	2.562	2.813	ns
mini-LVDS	—	GCLK	t_{CO}	4.278	4.693	5.139	ns
		GCLK PLL	t_{CO}	2.336	2.562	2.813	ns
PPDS	—	GCLK	t_{CO}	4.278	4.693	5.139	ns
		GCLK PLL	t_{CO}	2.336	2.562	2.813	ns
RSDS	—	GCLK	t_{CO}	4.278	4.693	5.139	ns
		GCLK PLL	t_{CO}	2.336	2.562	2.813	ns

EP3C80 I/O Timing Parameters

Table 1–84 through Table 1–89 show the maximum I/O timing parameters for EP3C80 devices.

Table 1–84. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_{H}	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_{H}	–2.494	–2.650	–2.784	ns
	8 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_{H}	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_{H}	–2.494	–2.650	–2.784	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_{H}	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_{H}	–2.494	–2.650	–2.784	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_{H}	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_{H}	–2.494	–2.650	–2.784	ns
	8 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_{H}	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_{H}	–2.494	–2.650	–2.784	ns
	12 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_{H}	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_{H}	–2.494	–2.650	–2.784	ns
	16 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_{H}	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_{H}	–2.494	–2.650	–2.784	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_{H}	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_{H}	–2.494	–2.650	–2.784	ns
	8 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_{H}	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_{H}	–2.494	–2.650	–2.784	ns

Table 1–84. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	12 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_H	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_H	–2.494	–2.650	–2.784	ns
	16 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_H	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_H	–2.494	–2.650	–2.784	ns
2.5V	4 mA	GCLK	t_{SU}	0.664	0.668	0.647	ns
			t_H	–0.384	–0.351	–0.294	ns
		GCLK PLL	t_{SU}	2.717	2.923	3.106	ns
			t_H	–2.437	–2.606	–2.753	ns
	8 mA	GCLK	t_{SU}	0.664	0.668	0.647	ns
			t_H	–0.384	–0.351	–0.294	ns
		GCLK PLL	t_{SU}	2.717	2.923	3.106	ns
			t_H	–2.437	–2.606	–2.753	ns
	12 mA	GCLK	t_{SU}	0.664	0.668	0.647	ns
			t_H	–0.384	–0.351	–0.294	ns
		GCLK PLL	t_{SU}	2.717	2.923	3.106	ns
			t_H	–2.437	–2.606	–2.753	ns
	16 mA	GCLK	t_{SU}	0.664	0.668	0.647	ns
			t_H	–0.384	–0.351	–0.294	ns
		GCLK PLL	t_{SU}	2.717	2.923	3.106	ns
			t_H	–2.437	–2.606	–2.753	ns
1.8V	2 mA	GCLK	t_{SU}	0.599	0.629	0.634	ns
			t_H	–0.321	–0.313	–0.280	ns
		GCLK PLL	t_{SU}	2.652	2.885	3.093	ns
			t_H	–2.374	–2.569	–2.739	ns
	4 mA	GCLK	t_{SU}	0.599	0.629	0.634	ns
			t_H	–0.321	–0.313	–0.280	ns
		GCLK PLL	t_{SU}	2.652	2.885	3.093	ns
			t_H	–2.374	–2.569	–2.739	ns
	6 mA	GCLK	t_{SU}	0.599	0.629	0.634	ns
			t_H	–0.321	–0.313	–0.280	ns
		GCLK PLL	t_{SU}	2.652	2.885	3.093	ns
			t_H	–2.374	–2.569	–2.739	ns
	8 mA	GCLK	t_{SU}	0.599	0.629	0.634	ns
			t_H	–0.321	–0.313	–0.280	ns
		GCLK PLL	t_{SU}	2.652	2.885	3.093	ns
			t_H	–2.374	–2.569	–2.739	ns

Table 1–84. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	10 mA	GCLK	t_{SU}	0.599	0.629	0.634	ns
			t_H	–0.321	–0.313	–0.280	ns
		GCLK PLL	t_{SU}	2.652	2.885	3.093	ns
			t_H	–2.374	–2.569	–2.739	ns
	12 mA	GCLK	t_{SU}	0.599	0.629	0.634	ns
			t_H	–0.321	–0.313	–0.280	ns
		GCLK PLL	t_{SU}	2.652	2.885	3.093	ns
			t_H	–2.374	–2.569	–2.739	ns
	16 mA	GCLK	t_{SU}	0.599	0.629	0.634	ns
			t_H	–0.321	–0.313	–0.280	ns
		GCLK PLL	t_{SU}	2.652	2.885	3.093	ns
			t_H	–2.374	–2.569	–2.739	ns
1.5V	2 mA	GCLK	t_{SU}	0.668	0.721	0.751	ns
			t_H	–0.388	–0.403	–0.395	ns
		GCLK PLL	t_{SU}	2.721	2.977	3.210	ns
			t_H	–2.441	–2.659	–2.854	ns
	4 mA	GCLK	t_{SU}	0.668	0.721	0.751	ns
			t_H	–0.388	–0.403	–0.395	ns
		GCLK PLL	t_{SU}	2.721	2.977	3.210	ns
			t_H	–2.441	–2.659	–2.854	ns
	6 mA	GCLK	t_{SU}	0.668	0.721	0.751	ns
			t_H	–0.388	–0.403	–0.395	ns
		GCLK PLL	t_{SU}	2.721	2.977	3.210	ns
			t_H	–2.441	–2.659	–2.854	ns
	8 mA	GCLK	t_{SU}	0.668	0.721	0.751	ns
			t_H	–0.388	–0.403	–0.395	ns
		GCLK PLL	t_{SU}	2.721	2.977	3.210	ns
			t_H	–2.441	–2.659	–2.854	ns
	10 mA	GCLK	t_{SU}	0.668	0.721	0.751	ns
			t_H	–0.388	–0.403	–0.395	ns
		GCLK PLL	t_{SU}	2.721	2.977	3.210	ns
			t_H	–2.441	–2.659	–2.854	ns
	12 mA	GCLK	t_{SU}	0.668	0.721	0.751	ns
			t_H	–0.388	–0.403	–0.395	ns
		GCLK PLL	t_{SU}	2.721	2.977	3.210	ns
			t_H	–2.441	–2.659	–2.854	ns
	16 mA	GCLK	t_{SU}	0.668	0.721	0.751	ns
			t_H	–0.388	–0.403	–0.395	ns
		GCLK PLL	t_{SU}	2.721	2.977	3.210	ns
			t_H	–2.441	–2.659	–2.854	ns

Table 1–84. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	2 mA	GCLK	t_{SU}	0.820	0.901	0.957	ns
			t_H	–0.538	–0.579	–0.597	ns
		GCLK PLL	t_{SU}	2.873	3.157	3.416	ns
			t_H	–2.591	–2.835	–3.056	ns
	4 mA	GCLK	t_{SU}	0.820	0.901	0.957	ns
			t_H	–0.538	–0.579	–0.597	ns
		GCLK PLL	t_{SU}	2.873	3.157	3.416	ns
			t_H	–2.591	–2.835	–3.056	ns
	6 mA	GCLK	t_{SU}	0.820	0.901	0.957	ns
			t_H	–0.538	–0.579	–0.597	ns
		GCLK PLL	t_{SU}	2.873	3.157	3.416	ns
			t_H	–2.591	–2.835	–3.056	ns
	8 mA	GCLK	t_{SU}	0.820	0.901	0.957	ns
			t_H	–0.538	–0.579	–0.597	ns
		GCLK PLL	t_{SU}	2.873	3.157	3.416	ns
			t_H	–2.591	–2.835	–3.056	ns
	10 mA	GCLK	t_{SU}	0.820	0.901	0.957	ns
			t_H	–0.538	–0.579	–0.597	ns
		GCLK PLL	t_{SU}	2.873	3.157	3.416	ns
			t_H	–2.591	–2.835	–3.056	ns
	12 mA	GCLK	t_{SU}	0.820	0.901	0.957	ns
			t_H	–0.538	–0.579	–0.597	ns
		GCLK PLL	t_{SU}	2.873	3.157	3.416	ns
			t_H	–2.591	–2.835	–3.056	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.654	0.686	0.694	ns
			t_H	–0.374	–0.369	–0.339	ns
		GCLK PLL	t_{SU}	2.705	2.940	3.154	ns
			t_H	–2.425	–2.623	–2.799	ns
	12 mA	GCLK	t_{SU}	0.654	0.686	0.694	ns
			t_H	–0.374	–0.369	–0.339	ns
		GCLK PLL	t_{SU}	2.705	2.940	3.154	ns
			t_H	–2.425	–2.623	–2.799	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.654	0.686	0.694	ns
			t_H	–0.374	–0.369	–0.339	ns
		GCLK PLL	t_{SU}	2.705	2.940	3.154	ns
			t_H	–2.425	–2.623	–2.799	ns

Table 1–84. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.715	0.775	0.809	ns
			t_H	–0.435	–0.456	–0.452	ns
		GCLK PLL	t_{SU}	2.766	3.029	3.269	ns
			t_H	–2.486	–2.710	–2.912	ns
	10 mA	GCLK	t_{SU}	0.715	0.775	0.809	ns
			t_H	–0.435	–0.456	–0.452	ns
		GCLK PLL	t_{SU}	2.766	3.029	3.269	ns
			t_H	–2.486	–2.710	–2.912	ns
	12 mA	GCLK	t_{SU}	0.715	0.775	0.809	ns
			t_H	–0.435	–0.456	–0.452	ns
		GCLK PLL	t_{SU}	2.766	3.029	3.269	ns
			t_H	–2.486	–2.710	–2.912	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.715	0.775	0.809	ns
			t_H	–0.435	–0.456	–0.452	ns
		GCLK PLL	t_{SU}	2.766	3.029	3.269	ns
			t_H	–2.486	–2.710	–2.912	ns
	16 mA	GCLK	t_{SU}	0.715	0.775	0.809	ns
			t_H	–0.435	–0.456	–0.452	ns
		GCLK PLL	t_{SU}	2.766	3.029	3.269	ns
			t_H	–2.486	–2.710	–2.912	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.715	0.775	0.809	ns
			t_H	–0.435	–0.456	–0.452	ns
		GCLK PLL	t_{SU}	2.766	3.029	3.269	ns
			t_H	–2.486	–2.710	–2.912	ns
	10 mA	GCLK	t_{SU}	0.715	0.775	0.809	ns
			t_H	–0.435	–0.456	–0.452	ns
		GCLK PLL	t_{SU}	2.766	3.029	3.269	ns
			t_H	–2.486	–2.710	–2.912	ns
	12 mA	GCLK	t_{SU}	0.715	0.775	0.809	ns
			t_H	–0.435	–0.456	–0.452	ns
		GCLK PLL	t_{SU}	2.766	3.029	3.269	ns
			t_H	–2.486	–2.710	–2.912	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.715	0.775	0.809	ns
			t_H	–0.435	–0.456	–0.452	ns
		GCLK PLL	t_{SU}	2.766	3.029	3.269	ns
			t_H	–2.486	–2.710	–2.912	ns

Table 1–84. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.671	0.735	0.775	ns
			t_H	–0.391	–0.417	–0.419	ns
		GCLK PLL	t_{SU}	2.722	2.989	3.235	ns
			t_H	–2.442	–2.671	–2.879	ns
	10 mA	GCLK	t_{SU}	0.671	0.735	0.775	ns
			t_H	–0.391	–0.417	–0.419	ns
		GCLK PLL	t_{SU}	2.722	2.989	3.235	ns
			t_H	–2.442	–2.671	–2.879	ns
	12 mA	GCLK	t_{SU}	0.671	0.735	0.775	ns
			t_H	–0.391	–0.417	–0.419	ns
		GCLK PLL	t_{SU}	2.722	2.989	3.235	ns
			t_H	–2.442	–2.671	–2.879	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.671	0.735	0.775	ns
			t_H	–0.391	–0.417	–0.419	ns
		GCLK PLL	t_{SU}	2.722	2.989	3.235	ns
			t_H	–2.442	–2.671	–2.879	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.803	0.894	0.959	ns
			t_H	–0.521	–0.572	–0.599	ns
		GCLK PLL	t_{SU}	2.854	3.148	3.419	ns
			t_H	–2.572	–2.826	–3.059	ns
	10 mA	GCLK	t_{SU}	0.803	0.894	0.959	ns
			t_H	–0.521	–0.572	–0.599	ns
		GCLK PLL	t_{SU}	2.854	3.148	3.419	ns
			t_H	–2.572	–2.826	–3.059	ns
	12 mA	GCLK	t_{SU}	0.803	0.894	0.959	ns
			t_H	–0.521	–0.572	–0.599	ns
		GCLK PLL	t_{SU}	2.854	3.148	3.419	ns
			t_H	–2.572	–2.826	–3.059	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	0.803	0.894	0.959	ns
			t_H	–0.521	–0.572	–0.599	ns
		GCLK PLL	t_{SU}	2.854	3.148	3.419	ns
			t_H	–2.572	–2.826	–3.059	ns
3.0-V PCI	—	GCLK	t_{SU}	0.717	0.709	0.674	ns
			t_H	–0.437	–0.391	–0.320	ns
	—	GCLK PLL	t_{SU}	2.770	2.964	3.133	ns
			t_H	–2.490	–2.646	–2.779	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.717	0.709	0.674	ns
			t_H	–0.437	–0.391	–0.320	ns
	—	GCLK PLL	t_{SU}	2.770	2.964	3.133	ns
			t_H	–2.490	–2.646	–2.779	ns

Table 1–85. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
	8 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
	8 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
	12 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
	16 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
	8 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns

Table 1–85. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	12 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
	16 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
2.5V	4 mA	GCLK	t_{SU}	0.676	0.687	0.671	ns
			t_H	–0.396	–0.370	–0.317	ns
		GCLK PLL	t_{SU}	2.747	2.962	3.135	ns
			t_H	–2.467	–2.645	–2.781	ns
	8 mA	GCLK	t_{SU}	0.676	0.687	0.671	ns
			t_H	–0.396	–0.370	–0.317	ns
		GCLK PLL	t_{SU}	2.747	2.962	3.135	ns
			t_H	–2.467	–2.645	–2.781	ns
	12 mA	GCLK	t_{SU}	0.676	0.687	0.671	ns
			t_H	–0.396	–0.370	–0.317	ns
		GCLK PLL	t_{SU}	2.747	2.962	3.135	ns
			t_H	–2.467	–2.645	–2.781	ns
	16 mA	GCLK	t_{SU}	0.676	0.687	0.671	ns
			t_H	–0.396	–0.370	–0.317	ns
		GCLK PLL	t_{SU}	2.747	2.962	3.135	ns
			t_H	–2.467	–2.645	–2.781	ns
1.8V	2 mA	GCLK	t_{SU}	0.612	0.648	0.657	ns
			t_H	–0.334	–0.332	–0.302	ns
		GCLK PLL	t_{SU}	2.683	2.923	3.121	ns
			t_H	–2.405	–2.607	–2.766	ns
	4 mA	GCLK	t_{SU}	0.612	0.648	0.657	ns
			t_H	–0.334	–0.332	–0.302	ns
		GCLK PLL	t_{SU}	2.683	2.923	3.121	ns
			t_H	–2.405	–2.607	–2.766	ns
	6 mA	GCLK	t_{SU}	0.612	0.648	0.657	ns
			t_H	–0.334	–0.332	–0.302	ns
		GCLK PLL	t_{SU}	2.683	2.923	3.121	ns
			t_H	–2.405	–2.607	–2.766	ns
	8 mA	GCLK	t_{SU}	0.612	0.648	0.657	ns
			t_H	–0.334	–0.332	–0.302	ns
		GCLK PLL	t_{SU}	2.683	2.923	3.121	ns
			t_H	–2.405	–2.607	–2.766	ns

Table 1–85. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	10 mA	GCLK	t_{SU}	0.612	0.648	0.657	ns
			t_H	–0.334	–0.332	–0.302	ns
		GCLK PLL	t_{SU}	2.683	2.923	3.121	ns
			t_H	–2.405	–2.607	–2.766	ns
	12 mA	GCLK	t_{SU}	0.612	0.648	0.657	ns
			t_H	–0.334	–0.332	–0.302	ns
		GCLK PLL	t_{SU}	2.683	2.923	3.121	ns
			t_H	–2.405	–2.607	–2.766	ns
	16 mA	GCLK	t_{SU}	0.612	0.648	0.657	ns
			t_H	–0.334	–0.332	–0.302	ns
		GCLK PLL	t_{SU}	2.683	2.923	3.121	ns
			t_H	–2.405	–2.607	–2.766	ns
1.5V	2 mA	GCLK	t_{SU}	0.681	0.741	0.775	ns
			t_H	–0.401	–0.423	–0.419	ns
		GCLK PLL	t_{SU}	2.752	3.016	3.239	ns
			t_H	–2.–472	–2.698	–2.883	ns
	4 mA	GCLK	t_{SU}	0.681	0.741	0.775	ns
			t_H	–0.401	–0.423	–0.419	ns
		GCLK PLL	t_{SU}	2.752	3.016	3.239	ns
			t_H	–2.472	–2.698	–2.883	ns
	6 mA	GCLK	t_{SU}	0.681	0.741	0.775	ns
			t_H	–0.401	–0.423	–0.419	ns
		GCLK PLL	t_{SU}	2.752	3.016	3.239	ns
			t_H	–2.472	–2.698	–2.883	ns
	8 mA	GCLK	t_{SU}	0.681	0.741	0.775	ns
			t_H	–0.401	–0.423	–0.419	ns
		GCLK PLL	t_{SU}	2.752	3.016	3.239	ns
			t_H	–2.472	–2.698	–2.883	ns
	10 mA	GCLK	t_{SU}	0.681	0.741	0.775	ns
			t_H	–0.401	–0.423	–0.419	ns
		GCLK PLL	t_{SU}	2.752	3.016	3.239	ns
			t_H	–2.472	–2.698	–2.883	ns
	12 mA	GCLK	t_{SU}	0.681	0.741	0.775	ns
			t_H	–0.401	–0.423	–0.419	ns
		GCLK PLL	t_{SU}	2.752	3.016	3.239	ns
			t_H	–2.472	–2.698	–2.883	ns
	16 mA	GCLK	t_{SU}	0.681	0.741	0.775	ns
			t_H	–0.401	–0.423	–0.419	ns
		GCLK PLL	t_{SU}	2.752	3.016	3.239	ns
			t_H	–2.472	–2.698	–2.883	ns

Table 1–85. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	2 mA	GCLK	t_{SU}	0.834	0.921	0.982	ns
			t_H	–0.552	–0.599	–0.621	ns
		GCLK PLL	t_{SU}	2.905	3.196	3.446	ns
			t_H	–2.623	–2.874	–3.085	ns
	4 mA	GCLK	t_{SU}	0.834	0.921	0.982	ns
			t_H	–0.552	–0.599	–0.621	ns
		GCLK PLL	t_{SU}	2.905	3.196	3.446	ns
			t_H	–2.623	–2.874	–3.085	ns
	6 mA	GCLK	t_{SU}	0.834	0.921	0.982	ns
			t_H	–0.552	–0.599	–0.621	ns
		GCLK PLL	t_{SU}	2.905	3.196	3.446	ns
			t_H	–2.623	–2.874	–3.085	ns
	8 mA	GCLK	t_{SU}	0.834	0.921	0.982	ns
			t_H	–0.552	–0.599	–0.621	ns
		GCLK PLL	t_{SU}	2.905	3.196	3.446	ns
			t_H	–2.623	–2.874	–3.085	ns
	10 mA	GCLK	t_{SU}	0.834	0.921	0.982	ns
			t_H	–0.552	–0.599	–0.621	ns
		GCLK PLL	t_{SU}	2.905	3.196	3.446	ns
			t_H	–2.623	–2.874	–3.085	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.666	0.706	0.719	ns
			t_H	–0.386	–0.388	–0.363	ns
		GCLK PLL	t_{SU}	2.730	2.982	3.199	ns
			t_H	–2.450	–2.664	–2.843	ns
	12 mA	GCLK	t_{SU}	0.666	0.706	0.719	ns
			t_H	–0.386	–0.388	–0.363	ns
		GCLK PLL	t_{SU}	2.730	2.982	3.199	ns
			t_H	–2.450	–2.664	–2.843	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.666	0.706	0.719	ns
			t_H	–0.386	–0.388	–0.363	ns
		GCLK PLL	t_{SU}	2.730	2.982	3.199	ns
			t_H	–2.450	–2.664	–2.843	ns
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.728	0.795	0.836	ns
			t_H	–0.448	–0.476	–0.478	ns
		GCLK PLL	t_{SU}	2.792	3.071	3.316	ns
			t_H	–2.512	–2.752	–2.958	ns
	10 mA	GCLK	t_{SU}	0.728	0.795	0.836	ns
			t_H	–0.448	–0.476	–0.478	ns
		GCLK PLL	t_{SU}	2.792	3.071	3.316	ns
			t_H	–2.512	–2.752	–2.958	ns

Table 1–85. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	12 mA	GCLK	t_{SU}	0.728	0.795	0.836	ns
			t_H	–0.448	–0.476	–0.478	ns
		GCLK PLL	t_{SU}	2.792	3.071	3.316	ns
			t_H	–2.512	–2.752	–2.958	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.728	0.795	0.836	ns
			t_H	–0.448	–0.476	–0.478	ns
		GCLK PLL	t_{SU}	2.792	3.071	3.316	ns
			t_H	–2.512	–2.752	–2.958	ns
	16 mA	GCLK	t_{SU}	0.728	0.795	0.836	ns
			t_H	–0.448	–0.476	–0.478	ns
		GCLK PLL	t_{SU}	2.792	3.071	3.316	ns
			t_H	–2.512	–2.752	–2.958	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.728	0.795	0.836	ns
			t_H	–0.448	–0.476	–0.478	ns
		GCLK PLL	t_{SU}	2.792	3.071	3.316	ns
			t_H	–2.512	–2.752	–2.958	ns
	10 mA	GCLK	t_{SU}	0.728	0.795	0.836	ns
			t_H	–0.448	–0.476	–0.478	ns
		GCLK PLL	t_{SU}	2.792	3.071	3.316	ns
			t_H	–2.512	–2.752	–2.958	ns
	12 mA	GCLK	t_{SU}	0.728	0.795	0.836	ns
			t_H	–0.448	–0.476	–0.478	ns
		GCLK PLL	t_{SU}	2.792	3.071	3.316	ns
			t_H	–2.512	–2.752	–2.958	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.728	0.795	0.836	ns
			t_H	–0.448	–0.476	–0.478	ns
		GCLK PLL	t_{SU}	2.792	3.071	3.316	ns
			t_H	–2.512	–2.752	–2.958	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.683	0.754	0.799	ns
			t_H	–0.403	–0.436	–0.442	ns
		GCLK PLL	t_{SU}	2.747	3.030	3.279	ns
			t_H	–2.467	–2.712	–2.922	ns
	10 mA	GCLK	t_{SU}	0.683	0.754	0.799	ns
			t_H	–0.403	–0.436	–0.442	ns
		GCLK PLL	t_{SU}	2.747	3.030	3.279	ns
			t_H	–2.467	–2.712	–2.922	ns
	12 mA	GCLK	t_{SU}	0.683	0.754	0.799	ns
			t_H	–0.403	–0.436	–0.442	ns
		GCLK PLL	t_{SU}	2.747	3.030	3.279	ns
			t_H	–2.467	–2.712	–2.922	ns

Table 1–85. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.683	0.754	0.799	ns
			t_H	–0.403	–0.436	–0.442	ns
		GCLK PLL	t_{SU}	2.747	3.030	3.279	ns
			t_H	–2.467	–2.712	–2.922	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.814	0.912	0.984	ns
			t_H	–0.532	–0.590	–0.624	ns
		GCLK PLL	t_{SU}	2.878	3.188	3.464	ns
			t_H	–2.596	–2.866	–3.104	ns
	10 mA	GCLK	t_{SU}	0.814	0.912	0.984	ns
			t_H	–0.532	–0.590	–0.624	ns
		GCLK PLL	t_{SU}	2.878	3.188	3.464	ns
			t_H	–2.596	–2.866	–3.104	ns
3.0-V PCI	—	GCLK	t_{SU}	0.729	0.727	0.696	ns
			t_H	–0.449	–0.409	–0.341	ns
	—	GCLK PLL	t_{SU}	2.800	3.002	3.160	ns
			t_H	–2.520	–2.684	–2.805	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.729	0.727	0.696	ns
			t_H	–0.449	–0.409	–0.341	ns
	—	GCLK PLL	t_{SU}	2.800	3.002	3.160	ns
			t_H	–2.520	–2.684	–2.805	ns

Table 1–86. EP3C80 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.858	6.396	6.964	ns
		GCLK PLL	t_{CO}	3.805	4.141	4.505	ns
	8 mA	GCLK	t_{CO}	5.858	6.396	6.964	ns
		GCLK PLL	t_{CO}	3.805	4.141	4.505	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.817	6.177	6.566	ns
		GCLK PLL	t_{CO}	3.764	3.922	4.107	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.568	6.099	6.662	ns
		GCLK PLL	t_{CO}	3.515	3.844	4.203	ns
	8 mA	GCLK	t_{CO}	5.297	5.815	6.363	ns
		GCLK PLL	t_{CO}	3.244	3.560	3.904	ns
	12 mA	GCLK	t_{CO}	5.200	5.714	6.259	ns
		GCLK PLL	t_{CO}	3.147	3.459	3.800	ns
	16 mA	GCLK	t_{CO}	5.153	5.662	6.201	ns
		GCLK PLL	t_{CO}	3.100	3.407	3.742	ns

Table 1–86. EP3C80 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.295	5.812	6.360	ns
		GCLK PLL	t_{CO}	3.242	3.557	3.901	ns
	8 mA	GCLK	t_{CO}	5.154	5.664	6.205	ns
		GCLK PLL	t_{CO}	3.101	3.409	3.746	ns
	12 mA	GCLK	t_{CO}	5.117	5.624	6.162	ns
		GCLK PLL	t_{CO}	3.064	3.369	3.703	ns
	16 mA	GCLK	t_{CO}	5.101	5.609	6.147	ns
		GCLK PLL	t_{CO}	3.048	3.354	3.688	ns
2.5V	4 mA	GCLK	t_{CO}	5.626	6.185	6.776	ns
		GCLK PLL	t_{CO}	3.573	3.930	4.317	ns
	8 mA	GCLK	t_{CO}	5.383	5.932	6.512	ns
		GCLK PLL	t_{CO}	3.330	3.677	4.053	ns
	12 mA	GCLK	t_{CO}	5.285	5.826	6.399	ns
		GCLK PLL	t_{CO}	3.232	3.571	3.940	ns
	16 mA	GCLK	t_{CO}	5.246	5.786	6.358	ns
		GCLK PLL	t_{CO}	3.193	3.531	3.899	ns
1.8V	2 mA	GCLK	t_{CO}	6.737	7.438	8.174	ns
		GCLK PLL	t_{CO}	4.684	5.181	5.715	ns
	4 mA	GCLK	t_{CO}	6.210	6.893	7.610	ns
		GCLK PLL	t_{CO}	4.157	4.636	5.151	ns
	6 mA	GCLK	t_{CO}	5.985	6.635	7.318	ns
		GCLK PLL	t_{CO}	3.932	4.378	4.859	ns
	8 mA	GCLK	t_{CO}	5.882	6.518	7.189	ns
		GCLK PLL	t_{CO}	3.829	4.261	4.730	ns
	10 mA	GCLK	t_{CO}	5.830	6.470	7.143	ns
		GCLK PLL	t_{CO}	3.777	4.213	4.684	ns
	12 mA	GCLK	t_{CO}	5.773	6.403	7.068	ns
		GCLK PLL	t_{CO}	3.720	4.146	4.609	ns
	16 mA	GCLK	t_{CO}	5.719	6.344	7.003	ns
		GCLK PLL	t_{CO}	3.666	4.087	4.544	ns
1.5V	2 mA	GCLK	t_{CO}	7.125	8.000	8.913	ns
		GCLK PLL	t_{CO}	5.072	5.743	6.454	ns
	4 mA	GCLK	t_{CO}	6.650	7.439	8.265	ns
		GCLK PLL	t_{CO}	4.597	5.182	5.806	ns
	6 mA	GCLK	t_{CO}	6.480	7.256	8.068	ns
		GCLK PLL	t_{CO}	4.427	4.999	5.609	ns
	8 mA	GCLK	t_{CO}	6.392	7.143	7.930	ns
		GCLK PLL	t_{CO}	4.339	4.886	5.471	ns
	10 mA	GCLK	t_{CO}	6.333	7.083	7.869	ns
		GCLK PLL	t_{CO}	4.280	4.826	5.410	ns

Table 1–86. EP3C80 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	12 mA	GCLK	t_{CO}	6.300	7.042	7.819	ns
		GCLK PLL	t_{CO}	4.247	4.785	5.360	ns
	16 mA	GCLK	t_{CO}	6.186	6.900	7.649	ns
		GCLK PLL	t_{CO}	4.133	4.643	5.190	ns
1.2V	2 mA	GCLK	t_{CO}	8.298	9.528	10.802	ns
		GCLK PLL	t_{CO}	6.245	7.271	8.343	ns
	4 mA	GCLK	t_{CO}	7.853	9.002	10.195	ns
		GCLK PLL	t_{CO}	5.800	6.745	7.736	ns
	6 mA	GCLK	t_{CO}	7.704	8.821	9.981	ns
		GCLK PLL	t_{CO}	5.651	6.564	7.522	ns
	8 mA	GCLK	t_{CO}	7.635	8.741	9.891	ns
		GCLK PLL	t_{CO}	5.582	6.484	7.432	ns
	10 mA	GCLK	t_{CO}	7.499	8.559	9.660	ns
		GCLK PLL	t_{CO}	5.446	6.302	7.201	ns
	12 mA	GCLK	t_{CO}	7.471	8.533	9.638	ns
		GCLK PLL	t_{CO}	5.418	6.276	7.179	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.240	5.774	6.341	ns
		GCLK PLL	t_{CO}	3.190	3.521	3.882	ns
	12 mA	GCLK	t_{CO}	5.218	5.750	6.318	ns
		GCLK PLL	t_{CO}	3.168	3.497	3.859	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	5.158	5.688	6.252	ns
		GCLK PLL	t_{CO}	3.108	3.435	3.793	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.674	6.287	6.937	ns
		GCLK PLL	t_{CO}	3.624	4.034	4.477	ns
	10 mA	GCLK	t_{CO}	5.649	6.256	6.900	ns
		GCLK PLL	t_{CO}	3.599	4.003	4.440	ns
	12 mA	GCLK	t_{CO}	5.637	6.242	6.883	ns
		GCLK PLL	t_{CO}	3.587	3.989	4.423	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.608	6.213	6.855	ns
		GCLK PLL	t_{CO}	3.558	3.960	4.395	ns
	16 mA	GCLK	t_{CO}	5.595	6.200	6.841	ns
		GCLK PLL	t_{CO}	3.545	3.947	4.381	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.636	6.239	6.879	ns
		GCLK PLL	t_{CO}	3.586	3.986	4.419	ns
	10 mA	GCLK	t_{CO}	5.625	6.232	6.875	ns
		GCLK PLL	t_{CO}	3.575	3.979	4.415	ns
	12 mA	GCLK	t_{CO}	5.616	6.218	6.855	ns
		GCLK PLL	t_{CO}	3.566	3.965	4.395	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.551	6.152	6.789	ns
		GCLK PLL	t_{CO}	3.501	3.899	4.329	ns

Table 1–86. EP3C80 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	6.150	6.860	7.610	ns
		GCLK PLL	t_{CO}	4.100	4.607	5.150	ns
	10 mA	GCLK	t_{CO}	6.153	6.860	7.605	ns
		GCLK PLL	t_{CO}	4.103	4.607	5.145	ns
	12 mA	GCLK	t_{CO}	6.141	6.852	7.601	ns
		GCLK PLL	t_{CO}	4.091	4.599	5.141	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	6.079	6.784	7.526	ns
		GCLK PLL	t_{CO}	4.029	4.531	5.066	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.363	8.398	9.477	ns
		GCLK PLL	t_{CO}	5.313	6.145	7.017	ns
	10 mA	GCLK	t_{CO}	7.301	8.309	9.361	ns
		GCLK PLL	t_{CO}	5.251	6.056	6.901	ns
	12 mA	GCLK	t_{CO}	7.303	8.315	9.370	ns
		GCLK PLL	t_{CO}	5.253	6.062	6.910	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	7.258	8.262	9.310	ns
		GCLK PLL	t_{CO}	5.208	6.009	6.850	ns
3.0-V PCI	—	GCLK	t_{CO}	5.448	5.956	6.496	ns
		GCLK PLL	t_{CO}	3.395	3.701	4.037	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.448	5.956	6.496	ns
		GCLK PLL	t_{CO}	3.395	3.701	4.037	ns

Table 1–87. EP3C80 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.820	6.349	6.914	ns
		GCLK PLL	t_{CO}	3.749	4.074	4.450	ns
	8 mA	GCLK	t_{CO}	5.820	6.349	6.914	ns
		GCLK PLL	t_{CO}	3.749	4.074	4.450	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.820	6.175	6.564	ns
		GCLK PLL	t_{CO}	3.749	3.900	4.100	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.534	6.056	6.615	ns
		GCLK PLL	t_{CO}	3.463	3.781	4.151	ns
	8 mA	GCLK	t_{CO}	5.277	5.789	6.338	ns
		GCLK PLL	t_{CO}	3.206	3.514	3.874	ns
	12 mA	GCLK	t_{CO}	5.188	5.694	6.236	ns
		GCLK PLL	t_{CO}	3.117	3.419	3.772	ns
	16 mA	GCLK	t_{CO}	5.142	5.643	6.181	ns
		GCLK PLL	t_{CO}	3.071	3.368	3.717	ns

Table 1–87. EP3C80 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.275	5.787	6.336	ns
		GCLK PLL	t_{CO}	3.204	3.512	3.872	ns
	8 mA	GCLK	t_{CO}	5.142	5.644	6.184	ns
		GCLK PLL	t_{CO}	3.071	3.369	3.720	ns
	12 mA	GCLK	t_{CO}	5.107	5.608	6.145	ns
		GCLK PLL	t_{CO}	3.036	3.333	3.681	ns
	16 mA	GCLK	t_{CO}	5.092	5.592	6.128	ns
		GCLK PLL	t_{CO}	3.021	3.317	3.664	ns
2.5V	4 mA	GCLK	t_{CO}	5.632	6.170	6.745	ns
		GCLK PLL	t_{CO}	3.561	3.895	4.281	ns
	8 mA	GCLK	t_{CO}	5.397	5.926	6.491	ns
		GCLK PLL	t_{CO}	3.326	3.651	4.027	ns
	12 mA	GCLK	t_{CO}	5.298	5.821	6.381	ns
		GCLK PLL	t_{CO}	3.227	3.546	3.917	ns
	16 mA	GCLK	t_{CO}	5.257	5.779	6.338	ns
		GCLK PLL	t_{CO}	3.186	3.504	3.874	ns
1.8V	2 mA	GCLK	t_{CO}	6.726	7.406	8.125	ns
		GCLK PLL	t_{CO}	4.655	5.131	5.661	ns
	4 mA	GCLK	t_{CO}	6.213	6.878	7.581	ns
		GCLK PLL	t_{CO}	4.142	4.603	5.117	ns
	6 mA	GCLK	t_{CO}	5.992	6.624	7.294	ns
		GCLK PLL	t_{CO}	3.921	4.349	4.830	ns
	8 mA	GCLK	t_{CO}	5.891	6.510	7.168	ns
		GCLK PLL	t_{CO}	3.820	4.235	4.704	ns
	10 mA	GCLK	t_{CO}	5.840	6.461	7.122	ns
		GCLK PLL	t_{CO}	3.769	4.186	4.658	ns
	12 mA	GCLK	t_{CO}	5.785	6.398	7.049	ns
		GCLK PLL	t_{CO}	3.714	4.123	4.585	ns
	16 mA	GCLK	t_{CO}	5.742	6.351	7.000	ns
		GCLK PLL	t_{CO}	3.671	4.076	4.536	ns
1.5V	2 mA	GCLK	t_{CO}	7.120	7.973	8.870	ns
		GCLK PLL	t_{CO}	5.049	5.698	6.406	ns
	4 mA	GCLK	t_{CO}	6.664	7.429	8.237	ns
		GCLK PLL	t_{CO}	4.593	5.154	5.773	ns
	6 mA	GCLK	t_{CO}	6.497	7.251	8.046	ns
		GCLK PLL	t_{CO}	4.426	4.976	5.582	ns
	8 mA	GCLK	t_{CO}	6.421	7.158	7.936	ns
		GCLK PLL	t_{CO}	4.350	4.883	5.472	ns
	10 mA	GCLK	t_{CO}	6.361	7.095	7.870	ns
		GCLK PLL	t_{CO}	4.290	4.820	5.406	ns

Table 1–87. EP3C80 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	12 mA	GCLK	t_{CO}	6.327	7.052	7.819	ns
		GCLK PLL	t_{CO}	4.256	4.777	5.355	ns
	16 mA	GCLK	t_{CO}	6.230	6.944	7.700	ns
		GCLK PLL	t_{CO}	4.159	4.669	5.236	ns
1.2V	2 mA	GCLK	t_{CO}	8.308	9.513	10.766	ns
		GCLK PLL	t_{CO}	6.237	7.238	8.302	ns
	4 mA	GCLK	t_{CO}	7.873	8.999	10.174	ns
		GCLK PLL	t_{CO}	5.802	6.724	7.710	ns
	6 mA	GCLK	t_{CO}	7.745	8.845	9.995	ns
		GCLK PLL	t_{CO}	5.674	6.570	7.531	ns
	8 mA	GCLK	t_{CO}	7.673	8.763	9.900	ns
		GCLK PLL	t_{CO}	5.602	6.488	7.436	ns
	10 mA	GCLK	t_{CO}	7.542	8.600	9.705	ns
		GCLK PLL	t_{CO}	5.471	6.325	7.241	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.226	5.753	6.319	ns
		GCLK PLL	t_{CO}	3.162	3.477	3.839	ns
	12 mA	GCLK	t_{CO}	5.207	5.734	6.298	ns
		GCLK PLL	t_{CO}	3.143	3.458	3.818	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	5.152	5.677	6.238	ns
		GCLK PLL	t_{CO}	3.088	3.401	3.758	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.660	6.268	6.914	ns
		GCLK PLL	t_{CO}	3.596	3.992	4.434	ns
	10 mA	GCLK	t_{CO}	5.647	6.250	6.893	ns
		GCLK PLL	t_{CO}	3.583	3.974	4.413	ns
	12 mA	GCLK	t_{CO}	5.634	6.235	6.875	ns
		GCLK PLL	t_{CO}	3.570	3.959	4.395	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.604	6.206	6.847	ns
		GCLK PLL	t_{CO}	3.540	3.930	4.367	ns
	16 mA	GCLK	t_{CO}	5.596	6.200	6.842	ns
		GCLK PLL	t_{CO}	3.532	3.924	4.362	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.624	6.222	6.859	ns
		GCLK PLL	t_{CO}	3.560	3.946	4.379	ns
	10 mA	GCLK	t_{CO}	5.619	6.218	6.856	ns
		GCLK PLL	t_{CO}	3.555	3.942	4.376	ns
	12 mA	GCLK	t_{CO}	5.612	6.211	6.849	ns
		GCLK PLL	t_{CO}	3.548	3.935	4.369	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.550	6.145	6.778	ns
		GCLK PLL	t_{CO}	3.486	3.869	4.298	ns

Table 1–87. EP3C80 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	6.139	6.843	7.588	ns
		GCLK PLL	t_{CO}	4.075	4.567	5.108	ns
	10 mA	GCLK	t_{CO}	6.151	6.855	7.599	ns
		GCLK PLL	t_{CO}	4.087	4.579	5.119	ns
	12 mA	GCLK	t_{CO}	6.139	6.846	7.594	ns
		GCLK PLL	t_{CO}	4.075	4.570	5.114	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	6.084	6.789	7.533	ns
		GCLK PLL	t_{CO}	4.020	4.513	5.053	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.376	8.415	9.501	ns
		GCLK PLL	t_{CO}	5.312	6.139	7.021	ns
	10 mA	GCLK	t_{CO}	7.315	8.330	9.392	ns
		GCLK PLL	t_{CO}	5.251	6.054	6.912	ns
3.0-V PCI	—	GCLK	t_{CO}	5.434	5.935	6.471	ns
		GCLK PLL	t_{CO}	3.363	3.660	4.007	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.434	5.935	6.471	ns
		GCLK PLL	t_{CO}	3.363	3.660	4.007	ns

Table 1–88. EP3C80 Column Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.548	0.588	0.601	ns
			t_{H}	–0.270	–0.272	–0.248	ns
	—	GCLK PLL	t_{SU}	2.599	2.842	3.061	ns
			t_{H}	–2.321	–2.526	–2.708	ns
LVDS_E_3R	—	GCLK	t_{CO}	5.189	5.722	6.288	ns
		GCLK PLL	t_{CO}	3.138	3.468	3.828	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	5.189	5.722	6.288	ns
		GCLK PLL	t_{CO}	3.138	3.468	3.828	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.570	6.101	6.666	ns
	—	GCLK PLL	t_{CO}	3.519	3.847	4.206	ns
RSDS_E_1R	—	GCLK	t_{CO}	5.189	5.722	6.288	ns
	—	GCLK PLL	t_{CO}	3.138	3.468	3.828	ns
RSDS_E_3R	—	GCLK	t_{CO}	5.189	5.722	6.288	ns
	—	GCLK PLL	t_{CO}	3.138	3.468	3.828	ns

Table 1–89. EP3C80 Row Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.572	0.616	0.638	ns
			t_{H}	–0.294	–0.301	–0.284	ns
			t_{CO}	4.385	4.811	5.271	ns
	—	GCLK PLL	t_{SU}	2.628	2.874	3.102	ns
			t_{H}	–2.350	–2.559	–2.748	ns
			t_{CO}	2.321	2.546	2.799	ns
mini-LVDS	—	GCLK	t_{CO}	4.385	4.811	5.271	ns
		GCLK PLL	t_{CO}	2.321	2.546	2.799	ns
PPDS	—	GCLK	t_{CO}	4.385	4.811	5.271	ns
		GCLK PLL	t_{CO}	2.321	2.546	2.799	ns
RSDS	—	GCLK	t_{CO}	4.385	4.811	5.271	ns
		GCLK PLL	t_{CO}	2.321	2.546	2.799	ns

EP3C120 I/O Timing Parameters

Table 1–90 through Table 1–95 show the maximum I/O timing parameters for EP3C120 devices. EP3C120 devices are offered in –7 and –8 speed grades only.

Table 1–90. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	0.501	0.449	ns
			t_{H}	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_{H}	–2.771	–2.904	ns
	8 mA	GCLK	t_{SU}	0.501	0.449	ns
			t_{H}	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_{H}	–2.771	–2.904	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.501	0.449	ns
			t_{H}	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_{H}	–2.771	–2.904	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	0.501	0.449	ns
			t_{H}	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_{H}	–2.771	–2.904	ns

Table 1–90. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
3.0-V LVTTL	8 mA	GCLK	t_{SU}	0.501	0.449	ns
			t_H	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_H	–2.771	–2.904	ns
	12mA	GCLK	t_{SU}	0.501	0.449	ns
			t_H	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_H	–2.771	–2.904	ns
	16mA	GCLK	t_{SU}	0.501	0.449	ns
			t_H	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_H	–2.771	–2.904	ns
3.0-V LVCMOS	4mA	GCLK	t_{SU}	0.501	0.449	ns
			t_H	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_H	–2.771	–2.904	ns
	8mA	GCLK	t_{SU}	0.501	0.449	ns
			t_H	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_H	–2.771	–2.904	ns
	12mA	GCLK	t_{SU}	0.501	0.449	ns
			t_H	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_H	–2.771	–2.904	ns
	16mA	GCLK	t_{SU}	0.501	0.449	ns
			t_H	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_H	–2.771	–2.904	ns
2.5V	4mA	GCLK	t_{SU}	0.456	0.417	ns
			t_H	–0.139	–0.064	ns
		GCLK PLL	t_{SU}	3.044	3.226	ns
			t_H	–2.727	–2.873	ns
	8mA	GCLK	t_{SU}	0.456	0.417	ns
			t_H	–0.139	–0.064	ns
		GCLK PLL	t_{SU}	3.044	3.226	ns
			t_H	–2.727	–2.873	ns
	12mA	GCLK	t_{SU}	0.456	0.417	ns
			t_H	–0.139	–0.064	ns
		GCLK PLL	t_{SU}	3.044	3.226	ns
			t_H	–2.727	–2.873	ns

Table 1–90. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
2.5V	16 mA	GCLK	t_{SU}	0.456	0.417	ns
			t_H	–0.139	–0.064	ns
		GCLK PLL	t_{SU}	3.044	3.226	ns
			t_H	–2.727	–2.873	ns
1.8V	2 mA	GCLK	t_{SU}	0.417	0.404	ns
			t_H	–0.101	–0.050	ns
		GCLK PLL	t_{SU}	3.005	3.217	ns
			t_H	–2.689	–2.863	ns
	4 mA	GCLK	t_{SU}	0.417	0.404	ns
			t_H	–0.101	–0.050	ns
		GCLK PLL	t_{SU}	3.005	3.217	ns
			t_H	–2.689	–2.863	ns
	6 mA	GCLK	t_{SU}	0.417	0.404	ns
			t_H	–0.101	–0.050	ns
		GCLK PLL	t_{SU}	3.005	3.217	ns
			t_H	–2.689	–2.863	ns
	8 mA	GCLK	t_{SU}	0.417	0.404	ns
			t_H	–0.101	–0.050	ns
		GCLK PLL	t_{SU}	3.005	3.217	ns
			t_H	–2.689	–2.863	ns
	10 mA	GCLK	t_{SU}	0.417	0.404	ns
			t_H	–0.101	–0.050	ns
		GCLK PLL	t_{SU}	3.005	3.217	ns
			t_H	–2.689	–2.863	ns
	12 mA	GCLK	t_{SU}	0.417	0.404	ns
			t_H	–0.101	–0.050	ns
		GCLK PLL	t_{SU}	3.005	3.217	ns
			t_H	–2.689	–2.863	ns
	16 mA	GCLK	t_{SU}	0.417	0.404	ns
			t_H	–0.101	–0.050	ns
		GCLK PLL	t_{SU}	3.005	3.217	ns
			t_H	–2.689	–2.863	ns
1.5V	2 mA	GCLK	t_{SU}	0.509	0.521	ns
			t_H	–0.191	–0.165	ns
		GCLK PLL	t_{SU}	3.097	3.334	ns
			t_H	–2.779	–2.978	ns
	4 mA	GCLK	t_{SU}	0.509	0.521	ns
			t_H	–0.191	–0.165	ns
		GCLK PLL	t_{SU}	3.097	3.334	ns
			t_H	–2.779	–2.978	ns

Table 1–90. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.5V	6 mA	GCLK	t_{SU}	0.509	0.521	ns
			t_H	–0.191	–0.165	ns
		GCLK PLL	t_{SU}	3.097	3.334	ns
			t_H	–2.779	–2.978	ns
	8 mA	GCLK	t_{SU}	0.509	0.521	ns
			t_H	–0.191	–0.165	ns
		GCLK PLL	t_{SU}	3.097	3.334	ns
			t_H	–2.779	–2.978	ns
	10 mA	GCLK	t_{SU}	0.509	0.521	ns
			t_H	–0.191	–0.165	ns
		GCLK PLL	t_{SU}	3.097	3.334	ns
			t_H	–2.779	–2.978	ns
	12 mA	GCLK	t_{SU}	0.509	0.521	ns
			t_H	–0.191	–0.165	ns
		GCLK PLL	t_{SU}	3.097	3.334	ns
			t_H	–2.779	–2.978	ns
	16 mA	GCLK	t_{SU}	0.509	0.521	ns
			t_H	–0.191	–0.165	ns
		GCLK PLL	t_{SU}	3.097	3.334	ns
			t_H	–2.779	–2.978	ns
1.2V	2 mA	GCLK	t_{SU}	0.689	0.727	ns
			t_H	–0.367	–0.367	ns
		GCLK PLL	t_{SU}	3.277	3.540	ns
			t_H	–2.955	–3.180	ns
	4 mA	GCLK	t_{SU}	0.689	0.727	ns
			t_H	–0.367	–0.367	ns
		GCLK PLL	t_{SU}	3.277	3.540	ns
			t_H	–2.955	–3.180	ns
	6 mA	GCLK	t_{SU}	0.689	0.727	ns
			t_H	–0.367	–0.367	ns
		GCLK PLL	t_{SU}	3.277	3.540	ns
			t_H	–2.955	–3.180	ns
	8 mA	GCLK	t_{SU}	0.689	0.727	ns
			t_H	–0.367	–0.367	ns
		GCLK PLL	t_{SU}	3.277	3.540	ns
			t_H	–2.955	–3.180	ns
	10 mA	GCLK	t_{SU}	0.689	0.727	ns
			t_H	–0.367	–0.367	ns
		GCLK PLL	t_{SU}	3.277	3.540	ns
			t_H	–2.955	–3.180	ns

Table 1–90. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.2V	12 mA	GCLK	t_{SU}	0.689	0.727	ns
			t_H	–0.367	–0.367	ns
		GCLK PLL	t_{SU}	3.277	3.540	ns
			t_H	–2.955	–3.180	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.478	0.463	ns
			t_H	–0.161	–0.108	ns
		GCLK PLL	t_{SU}	3.059	3.278	ns
			t_H	–2.742	–2.923	ns
	12 mA	GCLK	t_{SU}	0.478	0.463	ns
			t_H	–0.161	–0.108	ns
		GCLK PLL	t_{SU}	3.059	3.278	ns
			t_H	–2.742	–2.923	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.478	0.463	ns
			t_H	–0.161	–0.108	ns
		GCLK PLL	t_{SU}	3.059	3.278	ns
			t_H	–2.742	–2.923	ns
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.564	0.578	ns
			t_H	–0.245	–0.221	ns
		GCLK PLL	t_{SU}	3.161	3.403	ns
			t_H	–2.842	–3.046	ns
	10 mA	GCLK	t_{SU}	0.564	0.578	ns
			t_H	–0.245	–0.221	ns
		GCLK PLL	t_{SU}	3.161	3.403	ns
			t_H	–2.842	–3.046	ns
	12 mA	GCLK	t_{SU}	0.564	0.578	ns
			t_H	–0.245	–0.221	ns
		GCLK PLL	t_{SU}	3.161	3.403	ns
			t_H	–2.842	–3.046	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.564	0.578	ns
			t_H	–0.245	–0.221	ns
		GCLK PLL	t_{SU}	3.161	3.403	ns
			t_H	–2.842	–3.046	ns
	16 mA	GCLK	t_{SU}	0.564	0.578	ns
			t_H	–0.245	–0.221	ns
		GCLK PLL	t_{SU}	3.161	3.403	ns
			t_H	–2.842	–3.046	ns

Table 1–90. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.564	0.578	ns
			t_H	–0.245	–0.221	ns
		GCLK PLL	t_{SU}	3.161	3.403	ns
			t_H	–2.842	–3.046	ns
	10 mA	GCLK	t_{SU}	0.564	0.578	ns
			t_H	–0.245	–0.221	ns
		GCLK PLL	t_{SU}	3.161	3.403	ns
			t_H	–2.842	–3.046	ns
	12 mA	GCLK	t_{SU}	0.564	0.578	ns
			t_H	–0.245	–0.221	ns
		GCLK PLL	t_{SU}	3.161	3.403	ns
			t_H	–2.842	–3.046	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.564	0.578	ns
			t_H	–0.245	–0.221	ns
		GCLK PLL	t_{SU}	3.161	3.403	ns
			t_H	–2.842	–3.046	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.524	0.544	ns
			t_H	–0.206	–0.188	ns
		GCLK PLL	t_{SU}	3.121	3.369	ns
			t_H	–2.803	–3.013	ns
	10 mA	GCLK	t_{SU}	0.524	0.544	ns
			t_H	–0.206	–0.188	ns
		GCLK PLL	t_{SU}	3.121	3.369	ns
			t_H	–2.803	–3.013	ns
	12 mA	GCLK	t_{SU}	0.524	0.544	ns
			t_H	–0.206	–0.188	ns
		GCLK PLL	t_{SU}	3.121	3.369	ns
			t_H	–2.803	–3.013	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.524	0.544	ns
			t_H	–0.206	–0.188	ns
		GCLK PLL	t_{SU}	3.121	3.369	ns
			t_H	–2.803	–3.013	ns

Table 1–90. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.683	0.728	ns
			t_H	–0.361	–0.368	ns
		GCLK PLL	t_{SU}	3.280	3.553	ns
			t_H	–2.958	–3.193	ns
	10 mA	GCLK	t_{SU}	0.683	0.728	ns
			t_H	–0.361	–0.368	ns
		GCLK PLL	t_{SU}	3.280	3.553	ns
			t_H	–2.958	–3.193	ns
	12 mA	GCLK	t_{SU}	0.683	0.728	ns
			t_H	–0.361	–0.368	ns
		GCLK PLL	t_{SU}	3.280	3.553	ns
			t_H	–2.958	–3.193	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	0.683	0.728	ns
			t_H	–0.361	–0.368	ns
		GCLK PLL	t_{SU}	3.280	3.553	ns
			t_H	–2.958	–3.193	ns
3.0-V PCI	—	GCLK	t_{SU}	0.497	0.444	ns
			t_H	–0.179	–0.090	ns
	—	GCLK PLL	t_{SU}	3.085	3.253	ns
			t_H	–2.767	–2.899	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.497	0.444	ns
			t_H	–0.179	–0.090	ns
	—	GCLK PLL	t_{SU}	3.085	3.253	ns
			t_H	–2.767	–2.899	ns

Table 1–91. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns
	8 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns

Table 1–91. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns
	8 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns
	12 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns
	16 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns
	8 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns
	12 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns
	16 mA	GCLK	t_{SU}	0.640	0.608	ns
			th	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns

Table 1–91. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
2.5V	4 mA	GCLK	t_{SU}	0.596	0.579	ns
			t_H	–0.279	–0.225	ns
		GCLK PLL	t_{SU}	3.189	3.400	ns
			t_H	–2.872	–3.046	ns
	8 mA	GCLK	t_{SU}	0.596	0.579	ns
			t_H	–0.279	–0.225	ns
		GCLK PLL	t_{SU}	3.189	3.400	ns
			t_H	–2.872	–3.046	ns
	12 mA	GCLK	t_{SU}	0.596	0.579	ns
			t_H	–0.279	–0.225	ns
		GCLK PLL	t_{SU}	3.189	3.400	ns
			t_H	–2.872	–3.046	ns
	16 mA	GCLK	t_{SU}	0.596	0.579	ns
			t_H	–0.279	–0.225	ns
		GCLK PLL	t_{SU}	3.189	3.400	ns
			t_H	–2.872	–3.046	ns
1.8V	2 mA	GCLK	t_{SU}	0.557	0.565	ns
			t_H	–0.241	–0.210	ns
		GCLK PLL	t_{SU}	3.150	3.386	ns
			t_H	–2.834	–3.031	ns
	4 mA	GCLK	t_{SU}	0.557	0.565	ns
			t_H	–0.241	–0.210	ns
		GCLK PLL	t_{SU}	3.150	3.386	ns
			t_H	–2.834	–3.031	ns
	6 mA	GCLK	t_{SU}	0.557	0.565	ns
			t_H	–0.241	–0.210	ns
		GCLK PLL	t_{SU}	3.150	3.386	ns
			t_H	–2.834	–3.031	ns
	8 mA	GCLK	t_{SU}	0.557	0.565	ns
			t_H	–0.241	–0.210	ns
		GCLK PLL	t_{SU}	3.150	3.386	ns
			t_H	–2.834	–3.031	ns
	10 mA	GCLK	t_{SU}	0.557	0.565	ns
			t_H	–0.241	–0.210	ns
		GCLK PLL	t_{SU}	3.150	3.386	ns
			t_H	–2.834	–3.031	ns
	12 mA	GCLK	t_{SU}	0.557	0.565	ns
			t_H	–0.241	–0.210	ns
		GCLK PLL	t_{SU}	3.150	3.386	ns
			t_H	–2.834	–3.031	ns

Table 1–91. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.8V	16 mA	GCLK	t_{SU}	0.557	0.565	ns
			t_H	–0.241	–0.210	ns
		GCLK PLL	t_{SU}	3.150	3.386	ns
			t_H	–2.834	–3.031	ns
1.5V	2 mA	GCLK	t_{SU}	0.650	0.683	ns
			t_H	–0.332	–0.327	ns
		GCLK PLL	t_{SU}	3.243	3.504	ns
			t_H	–2.925	–3.148	ns
	4 mA	GCLK	t_{SU}	0.650	0.683	ns
			t_H	–0.332	–0.327	ns
		GCLK PLL	t_{SU}	3.243	3.504	ns
			t_H	–2.925	–3.148	ns
	6 mA	GCLK	t_{SU}	0.650	0.683	ns
			t_H	–0.332	–0.327	ns
		GCLK PLL	t_{SU}	3.243	3.504	ns
			t_H	–2.925	–3.148	ns
	8 mA	GCLK	t_{SU}	0.650	0.683	ns
			t_H	–0.332	–0.327	ns
		GCLK PLL	t_{SU}	3.243	3.504	ns
			t_H	–2.925	–3.148	ns
	10 mA	GCLK	t_{SU}	0.650	0.683	ns
			t_H	–0.332	–0.327	ns
		GCLK PLL	t_{SU}	3.243	3.504	ns
			t_H	–2.925	–3.148	ns
	12 mA	GCLK	t_{SU}	0.650	0.683	ns
			t_H	–0.332	–0.327	ns
		GCLK PLL	t_{SU}	3.243	3.504	ns
			t_H	–2.925	–3.148	ns
	16 mA	GCLK	t_{SU}	0.650	0.683	ns
			t_H	–0.332	–0.327	ns
		GCLK PLL	t_{SU}	3.243	3.504	ns
			t_H	–2.925	–3.148	ns
1.2V	2 mA	GCLK	t_{SU}	0.830	0.890	ns
			t_H	–0.508	–0.529	ns
		GCLK PLL	t_{SU}	3.423	3.711	ns
			t_H	–3.101	–3.350	ns
	4 mA	GCLK	t_{SU}	0.830	0.890	ns
			t_H	–0.508	–0.529	ns
		GCLK PLL	t_{SU}	3.423	3.711	ns
			t_H	–3.101	–3.350	ns

Table 1–91. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.2V	6 mA	GCLK	t_{SU}	0.830	0.890	ns
			t_H	–0.508	–0.529	ns
		GCLK PLL	t_{SU}	3.423	3.711	ns
			t_H	–3.101	–3.350	ns
	8 mA	GCLK	t_{SU}	0.830	0.890	ns
			t_H	–0.508	–0.529	ns
		GCLK PLL	t_{SU}	3.423	3.711	ns
			t_H	–3.101	–3.350	ns
	10 mA	GCLK	t_{SU}	0.830	0.890	ns
			t_H	–0.508	–0.529	ns
		GCLK PLL	t_{SU}	3.423	3.711	ns
			th	–3.101	–3.350	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.615	0.627	ns
			t_H	–0.297	–0.271	ns
		GCLK PLL	t_{SU}	3.208	3.448	ns
			t_H	–2.890	–3.092	ns
	12 mA	GCLK	t_{SU}	0.615	0.627	ns
			t_H	–0.297	–0.271	ns
		GCLK PLL	t_{SU}	3.208	3.448	ns
			t_H	–2.890	–3.092	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.615	0.627	ns
			t_H	–0.297	–0.271	ns
		GCLK PLL	t_{SU}	3.208	3.448	ns
			t_H	–2.890	–3.092	ns
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.704	0.744	ns
			t_H	–0.385	–0.386	ns
		GCLK PLL	t_{SU}	3.297	3.565	ns
			t_H	–2.978	–3.207	ns
	10 mA	GCLK	t_{SU}	0.704	0.744	ns
			t_H	–0.385	–0.386	ns
		GCLK PLL	t_{SU}	3.297	3.565	ns
			t_H	–2.978	–3.207	ns
	12 mA	GCLK	t_{SU}	0.704	0.744	ns
			t_H	–0.385	–0.386	ns
		GCLK PLL	t_{SU}	3.297	3.565	ns
			t_H	–2.978	–3.207	ns

Table 1–91. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.704	0.744	ns
			t_H	–0.385	–0.386	ns
		GCLK PLL	t_{SU}	3.297	3.565	ns
			t_H	–2.978	–3.207	ns
	16 mA	GCLK	t_{SU}	0.704	0.744	ns
			t_H	–0.385	–0.386	ns
		GCLK PLL	t_{SU}	3.297	3.565	ns
			t_H	–2.978	–3.207	ns
1.8–V HSTL Class I	8 mA	GCLK	t_{SU}	0.704	0.744	ns
			t_H	–0.385	–0.386	ns
		GCLK PLL	t_{SU}	3.297	3.565	ns
			t_H	–2.978	–3.207	ns
	10 mA	GCLK	t_{SU}	0.704	0.744	ns
			t_H	–0.385	–0.386	ns
		GCLK PLL	t_{SU}	3.297	3.565	ns
			t_H	–2.978	–3.207	ns
	12 mA	GCLK	t_{SU}	0.704	0.744	ns
			t_H	–0.385	–0.386	ns
		GCLK PLL	t_{SU}	3.297	3.565	ns
			t_H	–2.978	–3.207	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.704	0.744	ns
			t_H	–0.385	–0.386	ns
		GCLK PLL	t_{SU}	3.297	3.565	ns
			t_H	–2.978	–3.207	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.663	0.707	ns
			t_H	–0.345	–0.350	ns
		GCLK PLL	t_{SU}	3.256	3.528	ns
			t_H	–2.938	–3.171	ns
	10 mA	GCLK	t_{SU}	0.663	0.707	ns
			t_H	–0.345	–0.350	ns
		GCLK PLL	t_{SU}	3.256	3.528	ns
			t_H	–2.938	–3.171	ns
	12 mA	GCLK	t_{SU}	0.663	0.707	ns
			t_H	–0.345	–0.350	ns
		GCLK PLL	t_{SU}	3.256	3.528	ns
			t_H	–2.938	–3.171	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.663	0.707	ns
			t_H	–0.345	–0.350	ns
		GCLK PLL	t_{SU}	3.256	3.528	ns
			t_H	–2.938	–3.171	ns

Table 1–91. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.821	0.892	ns
			t_H	–0.499	–0.532	ns
		GCLK PLL	t_{SU}	3.414	3.713	ns
			t_H	–3.092	–3.353	ns
	10 mA	GCLK	t_{SU}	0.821	0.892	ns
			t_H	–0.499	–0.532	ns
		GCLK PLL	t_{SU}	3.414	3.713	ns
			t_H	–3.092	–3.353	ns
3.0-V PCI	—	GCLK	t_{SU}	0.636	0.604	ns
			t_H	–0.318	–0.249	ns
	—	GCLK PLL	t_{SU}	3.229	3.425	ns
			t_H	–2.911	–3.070	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.636	0.604	ns
			t_H	–0.318	–0.249	ns
	—	GCLK PLL	t_{SU}	3.229	3.425	ns
			t_H	–2.911	–3.070	ns

Table 1–92. EP3C120 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	6.607	7.194	ns
		GCLK PLL	t_{CO}	4.020	4.385	ns
	8 mA	GCLK	t_{CO}	6.607	7.194	ns
		GCLK PLL	t_{CO}	4.020	4.385	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	6.388	6.796	ns
		GCLK PLL	t_{CO}	3.801	3.987	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	6.310	6.892	ns
		GCLK PLL	t_{CO}	3.723	4.083	ns
	8 mA	GCLK	t_{CO}	6.026	6.593	ns
		GCLK PLL	t_{CO}	3.439	3.784	ns
	12 mA	GCLK	t_{CO}	5.925	6.489	ns
		GCLK PLL	t_{CO}	3.338	3.680	ns
	16 mA	GCLK	t_{CO}	5.873	6.431	ns
		GCLK PLL	t_{CO}	3.286	3.622	ns

Table 1–92. EP3C120 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	6.023	6.590	ns
		GCLK PLL	t_{CO}	3.436	3.781	ns
	8 mA	GCLK	t_{CO}	5.875	6.435	ns
		GCLK PLL	t_{CO}	3.288	3.626	ns
	12 mA	GCLK	t_{CO}	5.835	6.392	ns
		GCLK PLL	t_{CO}	3.248	3.583	ns
	16 mA	GCLK	t_{CO}	5.820	6.377	ns
		GCLK PLL	t_{CO}	3.233	3.568	ns
2.5V	4 mA	GCLK	t_{CO}	6.396	7.006	ns
		GCLK PLL	t_{CO}	3.809	4.197	ns
	8 mA	GCLK	t_{CO}	6.143	6.742	ns
		GCLK PLL	t_{CO}	3.556	3.933	ns
	12 mA	GCLK	t_{CO}	6.037	6.629	ns
		GCLK PLL	t_{CO}	3.450	3.820	ns
	16 mA	GCLK	t_{CO}	5.997	6.588	ns
		GCLK PLL	t_{CO}	3.410	3.779	ns
1.8V	2 mA	GCLK	t_{CO}	7.649	8.404	ns
		GCLK PLL	t_{CO}	5.062	5.592	ns
	4 mA	GCLK	t_{CO}	7.104	7.840	ns
		GCLK PLL	t_{CO}	4.517	5.028	ns
	6 mA	GCLK	t_{CO}	6.846	7.548	ns
		GCLK PLL	t_{CO}	4.259	4.736	ns
	8 mA	GCLK	t_{CO}	6.729	7.419	ns
		GCLK PLL	t_{CO}	4.142	4.607	ns
	10 mA	GCLK	t_{CO}	6.681	7.373	ns
		GCLK PLL	t_{CO}	4.094	4.561	ns
	12 mA	GCLK	t_{CO}	6.614	7.298	ns
		GCLK PLL	t_{CO}	4.027	4.486	ns
	16 mA	GCLK	t_{CO}	6.555	7.233	ns
		GCLK PLL	t_{CO}	3.968	4.421	ns
1.5V	2 mA	GCLK	t_{CO}	8.211	9.143	ns
		GCLK PLL	t_{CO}	5.624	6.331	ns
	4 mA	GCLK	t_{CO}	7.650	8.495	ns
		GCLK PLL	t_{CO}	5.063	5.683	ns
	6 mA	GCLK	t_{CO}	7.467	8.298	ns
		GCLK PLL	t_{CO}	4.880	5.486	ns
	8 mA	GCLK	t_{CO}	7.354	8.160	ns
		GCLK PLL	t_{CO}	4.767	5.348	ns
	10 mA	GCLK	t_{CO}	7.294	8.099	ns
		GCLK PLL	t_{CO}	4.707	5.287	ns

Table 1–92. EP3C120 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.5V	12 mA	GCLK	t_{CO}	7.253	8.049	ns
		GCLK PLL	t_{CO}	4.666	5.237	ns
	16 mA	GCLK	t_{CO}	7.111	7.879	ns
		GCLK PLL	t_{CO}	4.524	5.067	ns
1.2V	2 mA	GCLK	t_{CO}	9.739	11.032	ns
		GCLK PLL	t_{CO}	7.152	8.220	ns
	4 mA	GCLK	t_{CO}	9.213	10.425	ns
		GCLK PLL	t_{CO}	6.626	7.613	ns
	6 mA	GCLK	t_{CO}	9.032	10.211	ns
		GCLK PLL	t_{CO}	6.445	7.399	ns
	8 mA	GCLK	t_{CO}	8.952	10.121	ns
		GCLK PLL	t_{CO}	6.365	7.309	ns
	10 mA	GCLK	t_{CO}	8.770	9.890	ns
		GCLK PLL	t_{CO}	6.183	7.078	ns
	12 mA	GCLK	t_{CO}	8.744	9.868	ns
		GCLK PLL	t_{CO}	6.157	7.056	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.983	6.573	ns
		GCLK PLL	t_{CO}	3.402	3.758	ns
	12 mA	GCLK	t_{CO}	5.959	6.550	ns
		GCLK PLL	t_{CO}	3.378	3.735	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	5.897	6.484	ns
		GCLK PLL	t_{CO}	3.316	3.669	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	6.499	7.168	ns
		GCLK PLL	t_{CO}	3.903	4.345	ns
	10 mA	GCLK	t_{CO}	6.468	7.131	ns
		GCLK PLL	t_{CO}	3.872	4.308	ns
	12 mA	GCLK	t_{CO}	6.454	7.114	ns
		GCLK PLL	t_{CO}	3.858	4.291	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	6.425	7.086	ns
		GCLK PLL	t_{CO}	3.829	4.263	ns
	16 mA	GCLK	t_{CO}	6.412	7.072	ns
		GCLK PLL	t_{CO}	3.816	4.249	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	6.451	7.110	ns
		GCLK PLL	t_{CO}	3.855	4.287	ns
	10 mA	GCLK	t_{CO}	6.444	7.106	ns
		GCLK PLL	t_{CO}	3.848	4.283	ns
	12 mA	GCLK	t_{CO}	6.430	7.086	ns
		GCLK PLL	t_{CO}	3.834	4.263	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	6.364	7.020	ns
		GCLK PLL	t_{CO}	3.768	4.197	ns

Table 1–92. EP3C120 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	7.072	7.841	ns
		GCLK PLL	t_{CO}	4.476	5.018	ns
	10 mA	GCLK	t_{CO}	7.072	7.836	ns
		GCLK PLL	t_{CO}	4.476	5.013	ns
	12 mA	GCLK	t_{CO}	7.064	7.832	ns
		GCLK PLL	t_{CO}	4.468	5.009	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	6.996	7.757	ns
		GCLK PLL	t_{CO}	4.400	4.934	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	8.610	9.708	ns
		GCLK PLL	t_{CO}	6.014	6.885	ns
	10 mA	GCLK	t_{CO}	8.521	9.592	ns
		GCLK PLL	t_{CO}	5.925	6.769	ns
	12 mA	GCLK	t_{CO}	8.527	9.601	ns
		GCLK PLL	t_{CO}	5.931	6.778	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	8.474	9.541	ns
		GCLK PLL	t_{CO}	5.878	6.718	ns
3.0-V PCI	—	GCLK	t_{CO}	6.167	6.726	ns
		GCLK PLL	t_{CO}	3.580	3.917	ns
3.0-V PCI-X	—	GCLK	t_{CO}	6.167	6.726	ns
		GCLK PLL	t_{CO}	3.580	3.917	ns

Table 1–93. EP3C120 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	6.440	7.006	ns
		GCLK PLL	t_{CO}	3.847	4.185	ns
	8 mA	GCLK	t_{CO}	6.440	7.006	ns
		GCLK PLL	t_{CO}	3.847	4.185	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	6.266	6.656	ns
		GCLK PLL	t_{CO}	3.673	3.835	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	6.147	6.707	ns
		GCLK PLL	t_{CO}	3.554	3.886	ns
	8 mA	GCLK	t_{CO}	5.880	6.430	ns
		GCLK PLL	t_{CO}	3.287	3.609	ns
	12 mA	GCLK	t_{CO}	5.785	6.328	ns
		GCLK PLL	t_{CO}	3.192	3.507	ns
	16 mA	GCLK	t_{CO}	5.734	6.273	ns
		GCLK PLL	t_{CO}	3.141	3.452	ns

Table 1–93. EP3C120 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.878	6.428	ns
		GCLK PLL	t_{CO}	3.285	3.607	ns
	8 mA	GCLK	t_{CO}	5.735	6.276	ns
		GCLK PLL	t_{CO}	3.142	3.455	ns
	12 mA	GCLK	t_{CO}	5.699	6.237	ns
		GCLK PLL	t_{CO}	3.106	3.416	ns
	16 mA	GCLK	t_{CO}	5.683	6.220	ns
		GCLK PLL	t_{CO}	3.090	3.399	ns
2.5V	4 mA	GCLK	t_{CO}	6.261	6.837	ns
		GCLK PLL	t_{CO}	3.668	4.016	ns
	8 mA	GCLK	t_{CO}	6.017	6.583	ns
		GCLK PLL	t_{CO}	3.424	3.762	ns
	12 mA	GCLK	t_{CO}	5.912	6.473	ns
		GCLK PLL	t_{CO}	3.319	3.652	ns
	16 mA	GCLK	t_{CO}	5.870	6.430	ns
		GCLK PLL	t_{CO}	3.277	3.609	ns
1.8V	2 mA	GCLK	t_{CO}	7.497	8.217	ns
		GCLK PLL	t_{CO}	4.904	5.396	ns
	4 mA	GCLK	t_{CO}	6.969	7.673	ns
		GCLK PLL	t_{CO}	4.376	4.852	ns
	6 mA	GCLK	t_{CO}	6.715	7.386	ns
		GCLK PLL	t_{CO}	4.122	4.565	ns
	8 mA	GCLK	t_{CO}	6.601	7.260	ns
		GCLK PLL	t_{CO}	4.008	4.439	ns
	10 mA	GCLK	t_{CO}	6.552	7.214	ns
		GCLK PLL	t_{CO}	3.959	4.393	ns
	12 mA	GCLK	t_{CO}	6.489	7.141	ns
		GCLK PLL	t_{CO}	3.896	4.320	ns
	16 mA	GCLK	t_{CO}	6.442	7.092	ns
		GCLK PLL	t_{CO}	3.849	4.271	ns
1.5V	2 mA	GCLK	t_{CO}	8.064	8.962	ns
		GCLK PLL	t_{CO}	5.471	6.141	ns
	4 mA	GCLK	t_{CO}	7.520	8.329	ns
		GCLK PLL	t_{CO}	4.927	5.508	ns
	6 mA	GCLK	t_{CO}	7.342	8.138	ns
		GCLK PLL	t_{CO}	4.749	5.317	ns
	8 mA	GCLK	t_{CO}	7.249	8.028	ns
		GCLK PLL	t_{CO}	4.656	5.207	ns
	10 mA	GCLK	t_{CO}	7.186	7.962	ns
		GCLK PLL	t_{CO}	4.593	5.141	ns

Table 1–93. EP3C120 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.5V	12 mA	GCLK	t_{CO}	7.143	7.911	ns
		GCLK PLL	t_{CO}	4.550	5.090	ns
	16 mA	GCLK	t_{CO}	7.035	7.792	ns
		GCLK PLL	t_{CO}	4.442	4.971	ns
1.2V	2 mA	GCLK	t_{CO}	9.604	10.858	ns
		GCLK PLL	t_{CO}	7.011	8.037	ns
	4 mA	GCLK	t_{CO}	9.090	10.266	ns
		GCLK PLL	t_{CO}	6.497	7.445	ns
	6 mA	GCLK	t_{CO}	8.936	10.087	ns
		GCLK PLL	t_{CO}	6.343	7.266	ns
	8 mA	GCLK	t_{CO}	8.854	9.992	ns
		GCLK PLL	t_{CO}	6.261	7.171	ns
	10 mA	GCLK	t_{CO}	8.691	9.797	ns
		GCLK PLL	t_{CO}	6.098	6.976	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.844	6.411	ns
		GCLK PLL	t_{CO}	3.251	3.590	ns
	12 mA	GCLK	t_{CO}	5.825	6.390	ns
		GCLK PLL	t_{CO}	3.232	3.569	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	5.768	6.330	ns
		GCLK PLL	t_{CO}	3.175	3.509	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	6.359	7.006	ns
		GCLK PLL	t_{CO}	3.766	4.185	ns
	10 mA	GCLK	t_{CO}	6.341	6.985	ns
		GCLK PLL	t_{CO}	3.748	4.164	ns
	12 mA	GCLK	t_{CO}	6.326	6.967	ns
		GCLK PLL	t_{CO}	3.733	4.146	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	6.297	6.939	ns
		GCLK PLL	t_{CO}	3.704	4.118	ns
	16 mA	GCLK	t_{CO}	6.291	6.934	ns
		GCLK PLL	t_{CO}	3.698	4.113	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	6.313	6.951	ns
		GCLK PLL	t_{CO}	3.720	4.130	ns
	10 mA	GCLK	t_{CO}	6.309	6.948	ns
		GCLK PLL	t_{CO}	3.716	4.127	ns
	12 mA	GCLK	t_{CO}	6.302	6.941	ns
		GCLK PLL	t_{CO}	3.709	4.120	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	6.236	6.870	ns
		GCLK PLL	t_{CO}	3.643	4.049	ns

Table 1–93. EP3C120 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	6.934	7.680	ns
		GCLK PLL	t_{CO}	4.341	4.859	ns
	10 mA	GCLK	t_{CO}	6.946	7.691	ns
		GCLK PLL	t_{CO}	4.353	4.870	ns
	12 mA	GCLK	t_{CO}	6.937	7.686	ns
		GCLK PLL	t_{CO}	4.344	4.865	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	6.880	7.625	ns
		GCLK PLL	t_{CO}	4.287	4.804	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	8.506	9.593	ns
		GCLK PLL	t_{CO}	5.913	6.772	ns
	10 mA	GCLK	t_{CO}	8.421	9.484	ns
		GCLK PLL	t_{CO}	5.828	6.663	ns
3.0-V PCI	—	GCLK	t_{CO}	6.026	6.563	ns
		GCLK PLL	t_{CO}	3.433	3.742	ns
3.0-V PCI-X	—	GCLK	t_{CO}	6.026	6.563	ns
		GCLK PLL	t_{CO}	3.433	3.742	ns

Table 1–94. EP3C120 Column Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.379	0.372	ns
			t_{H}	–0.063	–0.019	ns
	—	GCLK PLL	t_{SU}	2.965	3.187	ns
			t_{H}	–2.649	–2.834	ns
LVDS_E_3R	—	GCLK	t_{CO}	5.931	6.517	ns
		GCLK PLL	t_{CO}	3.347	3.705	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	5.931	6.517	ns
		GCLK PLL	t_{CO}	3.347	3.705	ns
PPDS_E_3R	—	GCLK	t_{CO}	6.310	6.895	ns
		GCLK PLL	t_{CO}	3.726	4.083	ns
RSDS_E_1R	—	GCLK	t_{CO}	5.931	6.517	ns
		GCLK PLL	t_{CO}	3.347	3.705	ns
RSDS_E_3R	—	GCLK	t_{CO}	5.931	6.517	ns
		GCLK PLL	t_{CO}	3.347	3.705	ns

Table 1–95. EP3C120 Row Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.519	0.538	ns
			t_{H}	–0.204	–0.184	ns
			t_{CO}	4.902	5.363	ns
	—	GCLK PLL	t_{SU}	3.105	3.351	ns
			t_{H}	–2.790	–2.997	ns
			t_{CO}	2.313	2.547	ns
mini-LVDS	—	GCLK	t_{CO}	4.902	5.363	ns
		GCLK PLL	t_{CO}	2.313	2.547	ns
PPDS	—	GCLK	t_{CO}	4.902	5.363	ns
		GCLK PLL	t_{CO}	2.313	2.547	ns
RSDS	—	GCLK	t_{CO}	4.902	5.363	ns
		GCLK PLL	t_{CO}	2.313	2.547	ns

Dedicated Clock Pin Timing Parameters

Table 1–96 to Table 1–111 show clock pin timing for Cyclone III devices.

EP3C5 Clock Timing Parameters

Table 1–96 through Table 1–97 show the maximum clock timing parameters for EP3C5 devices.

Table 1–96. EP3C5 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.543	2.287	2.519	2.790	ns
tcout	—	1.573	2.340	2.580	2.845	ns
tpllcin	—	0.964	1.349	1.462	1.617	ns
tpllcout	—	0.994	1.402	1.523	1.686	ns

Table 1–97. EP3C5 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.540	2.274	2.502	2.769	ns
tcout	—	1.570	2.327	2.563	2.824	ns
tpllcin	—	0.961	1.336	1.445	1.596	ns
tpllcout	—	0.991	1.389	1.506	1.665	ns

EP3C10 Clock Timing Parameters

Table 1–98 through Table 1–99 show the maximum clock timing parameters for EP3C10 devices.

Table 1–98. EP3C10 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.542	2.286	2.518	2.789	ns
tcout	—	1.572	2.339	2.579	2.845	ns
tpllcin	—	0.963	1.348	1.461	1.617	ns
tpllcout	—	0.993	1.401	1.522	1.686	ns

Table 1–99. EP3C10 Row Pin Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.536	2.274	2.499	2.762	ns
tcout	—	1.566	2.327	2.560	2.819	ns

Table 1–99. EP3C10 Row Pin Global Clock Timing Parameters (Part 2 of 2)						
Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tpllcin	—	0.957	1.336	1.442	1.591	ns
tpllcout	—	0.987	1.389	1.503	1.660	ns

EP3C16 Clock Timing Parameters

Table 1–100 through Table 1–101 show the maximum clock timing parameters for EP3C16 devices.

Table 1–100. EP3C16 Column Pin Global Clock Timing Parameters						
Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.620	2.389	2.627	2.896	ns
tcout	—	1.650	2.442	2.688	2.956	ns
tpllcin	—	0.919	1.239	1.335	1.467	ns
tpllcout	—	0.949	1.292	1.396	1.536	ns

Table 1–101. EP3C16 Row Pin Global Clock Timing Parameters						
Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.605	2.364	2.598	2.858	ns
tcout	—	1.635	2.417	2.659	2.920	ns
tpllcin	—	0.904	1.214	1.306	1.431	ns
tpllcout	—	0.934	1.267	1.367	1.500	ns

EP3C25 Clock Timing Parameters

Table 1–102 through Table 1–103 show the maximum clock timing parameters for EP3C25 devices.

Table 1–102. EP3C25 Column Pin Global Clock Timing Parameters						
Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.652	2.438	2.682	2.959	ns
tcout	—	1.682	2.491	2.743	3.017	ns
tpllcin	—	0.938	1.271	1.370	1.505	ns
tpllcout	—	0.968	1.324	1.431	1.574	ns

Table 1–103. EP3C25 Row Pin Global Clock Timing Parameters						
Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.640	2.419	2.660	2.929	ns
tcout	—	1.670	2.472	2.721	2.991	ns
tpllcin	—	0.926	1.252	1.348	1.479	ns
tpllcout	—	0.956	1.305	1.409	1.548	ns

EP3C40 Clock Timing Parameters

Table 1–104 through Table 1–105 show the maximum clock timing parameters for EP3C40 device.

Table 1–104. EP3C40 Column Pin Global Clock Timing Parameters						
Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.734	2.568	2.824	3.106	ns
tcout	—	1.764	2.621	2.885	3.172	ns
tpllcin	—	0.972	1.318	1.418	1.558	ns
tpllcout	—	1.002	1.371	1.479	1.627	ns

Table 1–105. EP3C40 Row Pin Global Clock Timing Parameters						
Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.721	2.543	2.804	3.078	ns
tcout	—	1.751	2.596	2.865	3.142	ns
tpllcin	—	0.959	1.293	1.398	1.528	ns
tpllcout	—	0.989	1.346	1.459	1.597	ns

EP3C55 Clock Timing Parameters

Table 1–106 through Table 1–107 show the maximum clock timing parameters for EP3C55 devices.

Table 1–106. EP3C55 Column Pin Global Clock Timing Parameters						
Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.801	2.672	2.935	3.229	ns
tcout	—	1.831	2.725	2.996	3.296	ns
tpllcin	—	1.014	1.378	1.481	1.629	ns
tpllcout	—	1.044	1.431	1.542	1.698	ns

Table 1–107. EP3C55 Row Pin Global Clock Timing Parameters						
Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.805	2.666	2.926	3.207	ns
tcout	—	1.835	2.719	2.987	3.276	ns
tpllcin	—	1.018	1.372	1.472	1.609	ns
tpllcout	—	1.048	1.425	1.533	1.678	ns

EP3C80 Clock Timing Parameters

Table 1–108 through Table 1–109 show the maximum clock timing parameters for EP3C80 devices.

Table 1–108. EP3C80 Column Pin Global Clock Timing Parameters						
Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.868	2.765	3.039	3.345	ns
tcout	—	1.898	2.818	3.100	3.412	ns
tpllcin	—	1.052	1.423	1.526	1.685	ns
tpllcout	—	1.082	1.476	1.587	1.754	ns

Table 1–109. EP3C80 Row Pin Global Clock Timing Parameters						
Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.881	2.776	3.038	3.346	ns
tcout	—	1.911	2.829	3.099	3.415	ns
tpllcin	—	1.065	1.434	1.525	1.688	ns
tpllcout	—	1.095	1.487	1.586	1.757	ns

EP3C120 Clock Timing Parameters

Table 1–110 through Table 1–111 show the maximum clock timing parameters for EP3C120 devices. EP3C120 devices are offered in –7 and –8 speed grades only.

Table 1–110. EP3C120 Column Pin Global Clock Timing Parameters					
Parameter	Fast Model		–7	-8	Units
	Industrial	Commercial			
tcin	—	1.990	3.249	3.580	ns
tcout	—	2.020	3.310	3.644	ns
tpllcin	—	0.951	1.345	1.480	ns
tpllcout	—	0.981	1.406	1.549	ns

Table 1–111. EP3C120 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		–7	–8	Units
	Industrial	Commercial			
tcin	—	1.921	3.130	3.433	ns
tcout	—	1.951	3.191	3.490	ns
tpllcin	—	0.882	1.226	1.326	ns
tpllcout	—	0.912	1.287	1.395	ns

Glossary

Table 1–112 shows the glossary for this chapter.

Table 1–112. Glossary (Part 1 of 4)

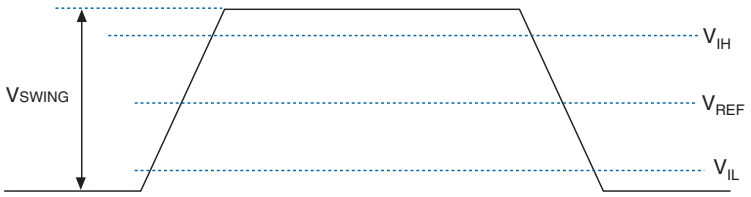
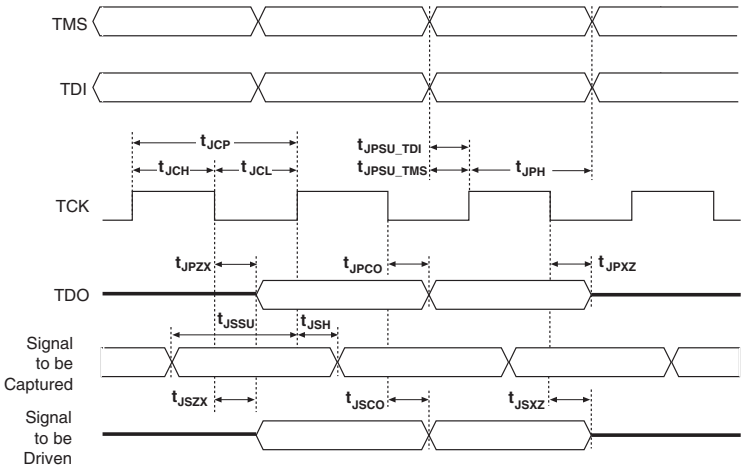
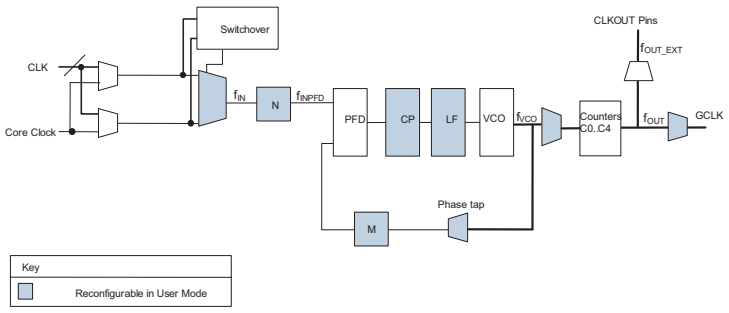
Letter	Term	Definitions
A	—	—
B	—	—
C	—	—
D	—	—
E	—	—
F	f_{HSCLK}	HIGH-SPEED I/O Block: High-speed receiver/transmitter input and output clock frequency.
G	GCLK	Input pin directly to Global Clock network.
	GCLK PLL	Input pin to Global Clock network through PLL.
H	HSIODR	HIGH-SPEED I/O Block: Maximum/minimum LVDS data transfer rate (HSIODR = 1/TUI).
I	Input Waveforms for the SSTL Differential I/O Standard	
J	JTAG Waveform	
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—
P	PLL Block	The following block diagram highlights the PLL Specification parameters. 

Table 1–112. Glossary (Part 2 of 4)

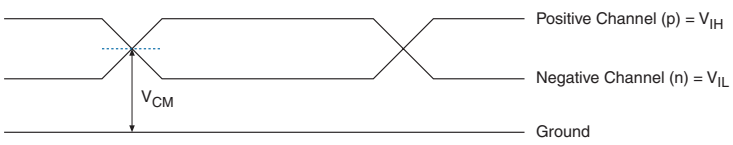
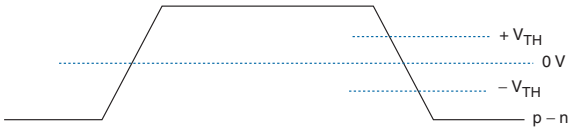
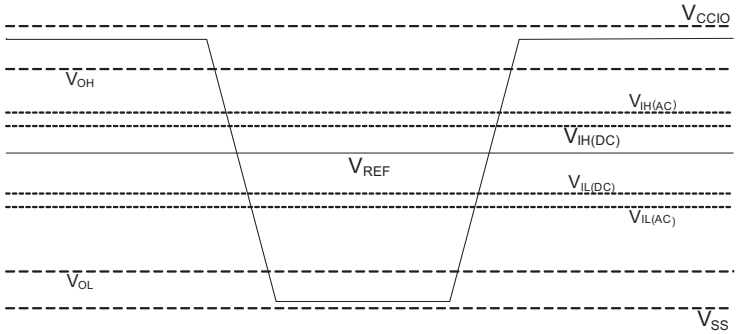
Letter	Term	Definitions
Q	—	—
R	R_L	Receiver differential input discrete resistor (external to Cyclone III device).
	Receiver Input Waveform	Receiver Input Waveform for LVDS and LVPECL Differential Standard. **Single-Ended Waveform**  **Differential Input Waveform** 
	RSKM (Receiver input skew margin)	HIGH-SPEED I/O Block: The total margin left after accounting for the sampling window and TCCS. RSKM = (TUI – SW – TCCS) / 2.
S	Single-ended Voltage referenced I/O Standard	 The JEDEC standard for SSTI and HSTL I/O standards defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. Once the receiver input has crossed the AC value, the receiver will change to the new logic state. The new logic state will then be maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform *ringing*.
	SW (Sampling Window)	HIGH-SPEED I/O Block: The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.

Table 1–112. Glossary (Part 3 of 4)

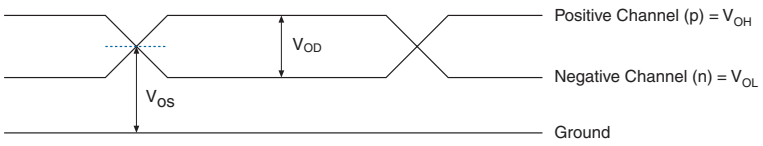
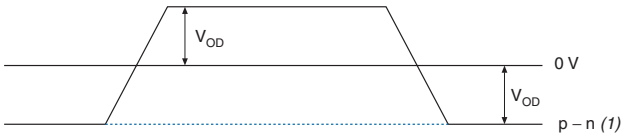
Letter	Term	Definitions
T	t_C	High-speed receiver/transmitter input and output clock period.
	TCCS (Channel-to-channel-skew)	HIGH-SPEED I/O Block: The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
	tcin	Delay from clock pad to I/O input register.
	t_{CO}	Delay from clock pad to I/O output.
	tcout	Delay from clock pad to I/O output register.
	t_{DUTY}	HIGH-SPEED I/O Block: Duty cycle on high-speed transmitter output clock.
	t_{FALL}	Signal High-to-low transition time (80-20%).
	t_H	Input register hold time.
	Timing Unit Interval (TUI)	HIGH-SPEED I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
	$t_{INJITTER}$	Period jitter on PLL clock input.
	$t_{OUTJITTER\_DEDCLK}$	Period jitter on dedicated clock output driven by a PLL.
	$t_{OUTJITTER\_IO}$	Period jitter on general purpose I/O driven by a PLL.
	tpllcin	Delay from PLL inclk pad to I/O input register.
	tpllcout	Delay from PLL inclk pad to I/O output register.
	Transmitter Output Waveform	Transmitter Output Waveforms for the LVDS, mini-LVDS, PPDS and RSDS Differential I/O Standard **Single-Ended Waveform**  **Differential Waveform (Mathematical Function of Positive & Negative Channel)** 
	t_{RISE}	Signal Low-to-high transition time (20-80%).
	t_{SU}	Input register setup time.
U	—	—

Table 1–112. Glossary (Part 4 of 4)

Letter	Term	Definitions
V	$V_{CM(DC)}$	DC Common Mode Input Voltage.
	$V_{DIF(AC)}$	AC differential Input Voltage: The minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential Input Voltage: The minimum DC input differential voltage required for switching.
	V_{ICM}	Input Common Mode Voltage: The common mode of the differential signal at the receiver.
	V_{ID}	Input differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V_{IH}	Voltage Input High: The minimum positive voltage applied to the input which will be accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage.
	$V_{IH(DC)}$	High-level DC input voltage.
	V_{IL}	Voltage Input Low: The maximum positive voltage applied to the input which will be accepted by the device as a logic low.
	$V_{IL\ (AC)}$	Low-level AC input voltage.
	$V_{IL\ (DC)}$	Low-level DC input voltage.
	V_{IN}	DC input voltage.
	V_{OCM}	Output Common Mode Voltage: The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. $V_{OD} = V_{OH} – V_{OL}$.
	V_{OH}	Voltage Output High: The maximum positive voltage from an output which the device considers will be accepted as the minimum positive high level.
	V_{OL}	Voltage Output Low: The maximum positive voltage from an output which the device considers will be accepted as the maximum positive low level.
	V_{OS}	Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$.
	$V_{OX\ (AC)}$	AC differential Output cross point voltage: The voltage at which the differential output signals must cross.
	V_{REF}	Reference voltage for SSTL, HSTL I/O Standards.
	$V_{REF\ (AC)}$	AC input reference voltage for SSTL, HSTL I/O Standards. $V_{REF(AC)} = V_{REF(DC)}$ + noise, The peak-to-peak AC noise on V_{REF} should not exceed 2% of $V_{REF(DC)}$.
	$V_{REF\ (DC)}$	DC input reference voltage for SSTL, HSTL I/O Standards.
	$V_{SWING\ (AC)}$	AC differential Input Voltage: AC Input differential voltage required for switching. Refer to Input Waveforms for the SSTL Differential I/O Standard.
	$V_{SWING\ (DC)}$	DC differential Input Voltage: DC Input differential voltage required for switching. Refer to Input Waveforms for the SSTL Differential I/O Standard.
V	V_{TH}	Differential input threshold.
	V_{TT}	Termination voltage for SSTL, HSTL I/O Standards.
	$V_{X\ (AC)}$	AC differential Input cross point Voltage: The voltage at which the differential input signals must cross.
W	—	—
X	—	—
Y	—	—
Z	—	—

Referenced Documents

This chapter references the following documents:

- *AN 447: Interfacing Cyclone III Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems*
- *High-Speed Differential Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*

Document Revision History

Table 1–113 shows the revision history for this document.

Table 1–113. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.3	• Updated Table 1–1 with V_{ESDHBM} and V_{ESDCDM} information. • Updated R_{CONF_PD} information in Table 1–10. • Added *Note (3)* to Table 1–12. • Updated t_{DLOCK} information in Table 1–19. • Updated Table 1–43 and Table 1–44. • Added "Referenced Documents" section.	—
June 2007 v1.2	Updated Cyclone III graphic in cover page.	Revised Cover
May 2007 v1.1	• Corrected current unit in Table 1–1, Table 1–12, and Table 1–14. • Added *Note (3)* to Table 1–3. • Updated Table 1–4 with I_{CCINT0}, I_{CCA0}, I_{CCD_PLL0}, and I_{CCIO0} information. • Updated Table 1–9 and added *Note (2)*. • Updated Table 1–19. • Updated Table 1–22 and added *Note (1)*. • Changed I/O standard from 1.5-V LVTTL/LVCMOS and 1.2-V LVTTL/LVCMOS to 1.5-V LVCMOS and 1.2-V LVCMOS in Table 1–41, Table 1–42, Table 1–43, Table 1–44, and Table 1–45. • Updated Table 1–43 with changes to LVPEC and LVDS and added Note 5. • Updated Table 1–46, Table 1–47, Tables 1–54 through 1–95, and Tables 1–98 through 1–111. • Removed speed grade –6 from Tables 1–90 through 1–95, and from Tables 1–110 through 1–111. • Added new Tables 1–48 through 1–53, Table 1–96, and Table 1–97. • Added a waveform (Receiver Input Waveform) in glossary under letter "R" (Table 1–112).	• Updated Timing Model information and other parts of the document as well.
March 2007 v1.0	Initial Release.	N/A