











LM237, LM337

SLVS047L-NOVEMBER 1981-REVISED JANUARY 2015

LMx37 3-Terminal Adjustable Regulators

Features

- Output Voltage Range Adjustable From -1.2 V to -37 V
- Output Current Capability of 1.5 A Max
- Input Regulation Typically 0.01% Per Input-Voltage Change
- Output Regulation Typically 0.3%
- Peak Output Current Constant Over Temperature Range of Regulator
- Ripple Rejection Typically 77 dB
- Direct Replacement for Industry-Standard LM237 and LM337

2 Applications

- Applications Requiring Negative Output Voltage or **Precision Current Regulation**
- Consumer Electronics
- **End Equipment**
- Portable Applications

3 Description

The LM237 and LM337 are adjustable 3-terminal negative-voltage regulators capable of supplying in excess of -1.5 A over an output voltage range of -1.2 V to -37 V. They require only two external resistors to set the output voltage and one output capacitor for frequency compensation.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
	TO-220 (4)	10.16 mm x 8.82 mm
LMx37	TO-263 (4)	10.16 mm x 9.02 mm
	TO-252 (4)	6.6 mm x 6.10 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

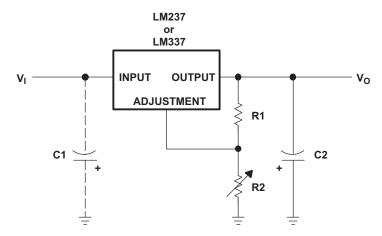




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5 Revision History

Changes from Revision K (November 2007) to Revision L

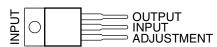
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Added Applications, Device Information table, Pin Functions table, ESD Ratings table, Thermal Information table, Typical Characteristics, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.



6 Pin Configuration and Functions

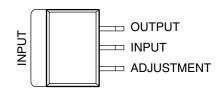




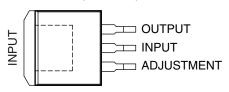
LM337...KCS (TO-220) PACKAGE (TOP VIEW)



LM337...KTE, KTP, OR KVU PACKAGE (TOP VIEW)



LM337...KTT (TO-263) PACKAGE (TOP VIEW)



Pin Functions

PIN		TYPE	DESCRIPTION						
NAME	NO.	ITPE	DESCRIPTION						
ADJUSTMENT	1	I	Adjustment pin for the output voltage. Connect two external resistors to adjust the output voltage.						
INPUT	2	I	Input voltage. The input voltage and current will be designated V _I and I _I respectively.						
OUTPUT	3	0	Output voltage. The output voltage and current will be designated $V_{\rm O}$ and $I_{\rm O}$ respectively.						



7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature ranges (unless otherwise noted) (1)

			MIN	MAX	UNIT
$V_I - V_O$	Input-to-output differential voltage			-40	V
TJ	Operating virtual junction temperature		150	°C	
	Lead temperature	1.6 mm (1/16 in) from case for 10 s		260	°C
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	1500	
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	1500	V

Recommended Operating Conditions 7.3

			MIN	MAX	UNIT	
V_I - V_O	Input-to-output differential voltage		-2.5	-37		
L Output ourrent	Output ourrent	$ V_I - V_O \le 40 \text{ V}, \text{ P} \le 15 \text{ W}$	10	1500	mA	
10	Output current	$ V_I - V_O \le 10 \text{ V, P} \le 15 \text{ W}$	6	1500	IIIA	
_		LM237	-25	150	۰,0	
TJ	Operating virtual junction temperature	LM337	0	125	°C	

7.4 Thermal Information

		LM237	LM	x37		LM337		
	THERMAL METRIC ⁽¹⁾	КС	KCS	KTE	KTP	KTT	KVU	UNIT
		4 PINS						
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.8	24.8	23	28	25.3	30.3	
$R_{\theta JC(top}$	Junction-to-case (top) thermal resistance	3	3	3	19	30.3	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report (SPRA953).

JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



Electrical Characteristics

over recommended ranges of operating virtual junction temperature (unless otherwise noted)

		a.v.a/1)		LM237			LM337			
PARAMETER	TEST CONDITI	MIN	TYP	MAX	MIN	TYP	MAX	UNIT		
I (2)	V V 0V/+- 40V/	T _J = 25°C		0.01	0.02		0.01	0.04	%/V	
Input regulation (2)	$V_1 - V_0 = -3 \text{ V to } -40 \text{ V}$	$T_J = MIN \text{ to } MAX$		0.02	0.05		0.02	0.07	%/V	
Dinale rejection	V _O = -10 V, f = 120 Hz			60			60		dB	
Ripple rejection	$V_{O} = -10 \text{ V}, f = 120 \text{ Hz}, C_{ADJ} = 0$	10 μF	66	77		66	77		uБ	
	I _O = 10 mA to 1.5 A,	V ₀ ≤ 5 V			25			50	mV	
Output regulation	$T_J = 25^{\circ}C$	V _O ≥ 5 V		0.3%	0.5%		0.3%	1%	_	
Output regulation	10 50 40 45 4	$ V_0 \le 5 \text{ V}$			50			70	mV	
	$I_0 = 10 \text{ mA to } 1.5 \text{ A}$	V _O ≥ 5 V			1%			1.5%	_	
Output-voltage change with temperature	T _J = MIN to MAX	T _J = MIN to MAX					0.6%		_	
Output-voltage long-term drift	After 1000 h at T _J = MAX and V _I	− V _O = −40 V		0.3%	1%		0.3%	1%	_	
Output noise voltage	$f = 10 \text{ Hz to } 10 \text{ kHz}, T_J = 25^{\circ}\text{C}$			0.003%			0.003%		_	
Minimum output current to	$ V_I - V_O \le 40 \text{ V}$		2.5	5		2.5	10	mA		
maintain regulation	$ V_I - V_O \le 10 \text{ V}$		1.2	3		1.5	6	ША		
Peak output current	$ V_I - V_O \le 15 \text{ V}$		1.5	2.2		1.5	2.2		Α	
reak output current	$ V_I - V_O \le 40 \text{ V}, T_J = 25^{\circ}\text{C}$	0.24	0.4		0.15	0.4				
ADJUSTMENT current				65	100		65	100	μΑ	
Change in ADJUSTMENT current	$V_I - V_O = -2.5$ V to -40 V, $I_O = 10$ mA to MAX, $T_J = 25$ °C			2	5		2	5	μA	
Reference voltage (OUTPUT	$V_I - V_O = -3 \text{ V to } -40 \text{ V},$	T _J = 25°C	-1.225	-1.25	-1.275	-1.213	-1.25	-1.287		
to ADJUSTMENT)	I _O = 10 mA to 1.5 A, P ≤ rated dissipation	T _J = MIN to MAX	-1.2	-1.25	-1.3	-1.2	-1.25	-1.3	V	
Thermal regulation	Initial T _J = 25°C, 10-ms pulse		0.002	0.02		0.003	0.04	%/W		

⁽¹⁾ Unless otherwise noted, the following test conditions apply: $|V_1 - V_0| = 5$ V and $I_0 = 0.5$ A. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. All characteristics are measured with a 0.1-µF capacitor across the input and a 1-µF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

(2) Input regulation is expressed here as the percentage change in output voltage per 1-V change at the input.

Electrical Characteristics

 $T_{.1} = 25^{\circ}C$

DADAMETER	TEST CONDITIONS ⁽¹⁾	LM	LM237, LM337			
PARAMETER	TEST CONDITIONS.	MIN	TYP	MAX	UNIT	
Input regulation (2)	$V_1 - V_0 = -3 \text{ V to } -40 \text{ V}$			0.01	0.04	%/V
Ripple rejection	$V_O = -10 \text{ V}, f = 120 \text{ Hz}$			60		dB
Rippie rejection	$V_{O} = -10 \text{ V}, f = 120 \text{ Hz}, C_{ADJ} = 10 \mu\text{F}$		66	77		uБ
Output regulation	1 10 m \ to 1 5 \	$ V_0 \le 5 \text{ V}$			50	mV
Output regulation	I _O = 10 mA to 1.5 A	$ V_O \ge 5 \text{ V}$		0.3%	1%	_
Output noise voltage	f = 10 Hz to 10 kHz			0.003%		_
Minimum output current to maintain	$ V_I - V_O \le 40 \text{ V}$		2.5	10	mA	
regulation	$ V_I - V_O \le 10 \text{ V}$		1.5	6	IIIA	
Dook output ourrent	$ V_I - V_O \le 15 \text{ V}$	1.5	2.2		۸	
Peak output current	$ V_I - V_O \le 40 \text{ V}$	0.15	0.4		Α	
ADJUSTMENT current				65	100	μΑ
Change in ADJUSTMENT current	$V_I - V_O = -2.5 \text{ V to } -40 \text{ V}, I_O = 10 \text{ mA to}$		2	5	μΑ	
Reference voltage (OUTPUT to ADJUSTMENT)	$V_I - V_O = -3 \text{ V to } -40 \text{ V}, I_O = 10 \text{ mA to } 0$ P \le \text{ rated dissipation}	-1.213	-1.25	-1.287	V	

Unless otherwise noted, the following test conditions apply: $|V_1 - V_0| = 5 \text{ V}$ and $I_0 = 0.5 \text{ A}$. All characteristics are measured with a 0.1μF capacitor across the input and a 1-μF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.

Input regulation is expressed here as the percentage change in output voltage per 1-V change at the input.



7.7 Typical Characteristics

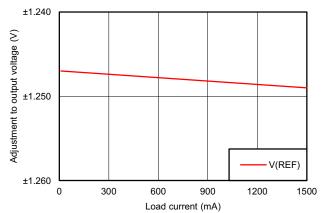


Figure 1. Adjustment Voltage vs Load current ($V_{IN} = -4.3 \text{ V}$)

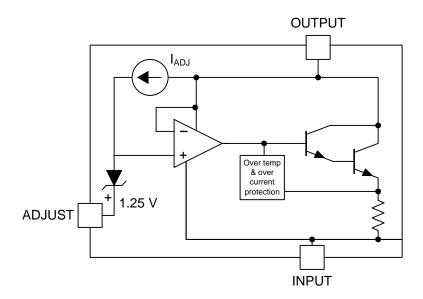


8 Detailed Description

8.1 Overview

The LMx37 devices are adjustable 3-terminal negative-voltage regulators capable of supplying in excess of -1.5 A over an output voltage range of -1.2 V to -37 V. They are exceptionally easy to use, requiring only two external resistors to set the output voltage and one output capacitor for frequency compensation. The current design is optimized for excellent regulation and low thermal transients. In addition, LM237 and LM337 feature internal current limiting, thermal shutdown, and safe-area compensation, making them virtually immune to failure by overloads. The LMx37 devices serve a wide variety of applications, including local on-card regulation, programmable output-voltage regulation, and precision current regulation.

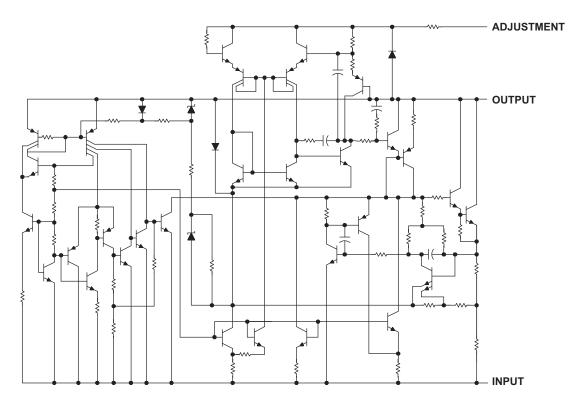
8.2 Functional Block Diagram



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8.3 Design Schematic



8.4 Feature Description

8.4.1 Output Voltage Adjustment

The ADJUSTMENT pin serves as a voltage adjustment reference for the output. The ADJUSTMENT pin can be attached to a resistor divider circuit to adjust its own voltage level. The reference voltage $V_{ADJUSTMENT}$ will typically be 1.25 V higher than V_O .

8.5 Device Functional Modes

8.5.1 Adjustable Output Mode

The device has a single functional mode: Adjustable output voltage mode. A resistor divider circuit on the ADJUSTMENT pin determines the output voltage.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 General Configurations

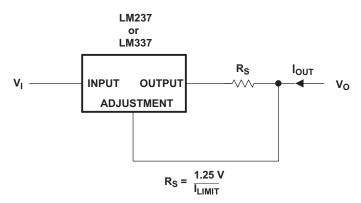


Figure 2. Current-Limiting Circuit

This application uses the LMx37 device's reference voltage, combined with the series resistor R_S , to limit the current to 1.25 V \div R_S

9.2 Typical Application

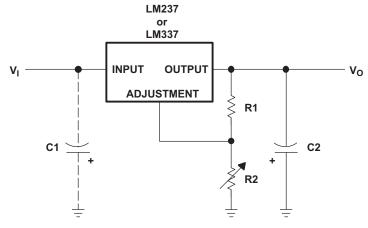


Figure 3. Adjustable Negative-Voltage Regulator

9.2.1 Design Requirements

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- 1-μF solid tantalum on the input pin if the regulator is more than 10 cm from the power supply filter capacitor
- 1-µF solid tantalum or 10-µF aluminum electrolytic capacitor is required on the output pin for stability.
- R1, which is usually 120 Ω as part of the resistor divider.
- R2, which can be varied to change the value of V_O.



Typical Application (continued)

9.2.2 Detailed Design Procedure

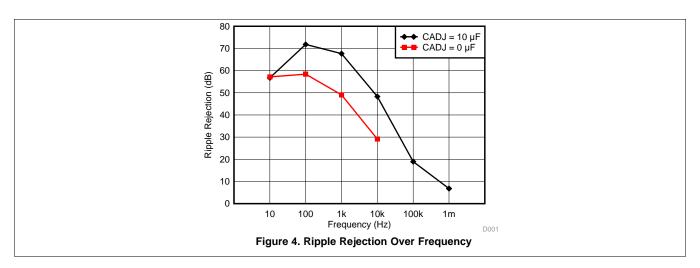
 V_O is determined by the values of R1 and R2. Choosing R1 = 120 Ω means that about 10.42 mA of current will flow through R1. The ~10 mA of current satisfies the minimum operating current and renders I_{REF} negligible. Since the current is coming from ground, the same amount of current will flow through R2. Therefore, the size of R2 will be the dominant factor in adjusting V_O . The relationship between R1, R2, and V_O is as follows:

$$R2=R1\left(\frac{V_{0}}{-1.25}-1\right)$$

where V_O is the output in volts.

(1)

9.2.3 Application Curves



10 Power Supply Recommendations

For best performance, the difference in voltage between the output and input must be between -2.5 V and -37 V. A 1- μ F solid tantalum capacitor is required on the input pin if the regulator is more than 10 cm from the power supply filter capacitor. A 1- μ F solid tantalum or 10- μ F aluminum electrolytic capacitor is required on the output pin for stability.

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11 Layout

11.1 Layout Guidelines

Traces on the input and output pins should be thick enough to carry 1.5 A of current without violating thermal requirements of the device or the system. In addition, a 1-μF solid tantalum capacitor is required on the input pin if the regulator is more than 10 cm from the power supply filter capacitor. A 1-μF solid tantalum or 10-μF aluminum electrolytic capacitor is required on the output pin for stability.

11.2 Layout Example

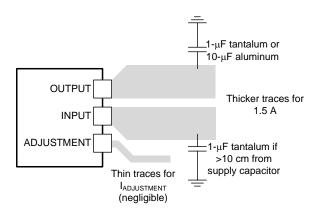


Figure 5. Layout Diagram

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM237	Click here	Click here	Click here	Click here	Click here
LM337	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.





17-Mar-2017

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
LM237KCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-25 to 150	LM237	Samples
LM337KCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	LM337	Samples
LM337KTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	LM337	Samples
LM337KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	LM337	Samples
LM337KVURG3	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	LM337	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



PACKAGE OPTION ADDENDUM

17-Mar-2017

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM337KTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
LM337KVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

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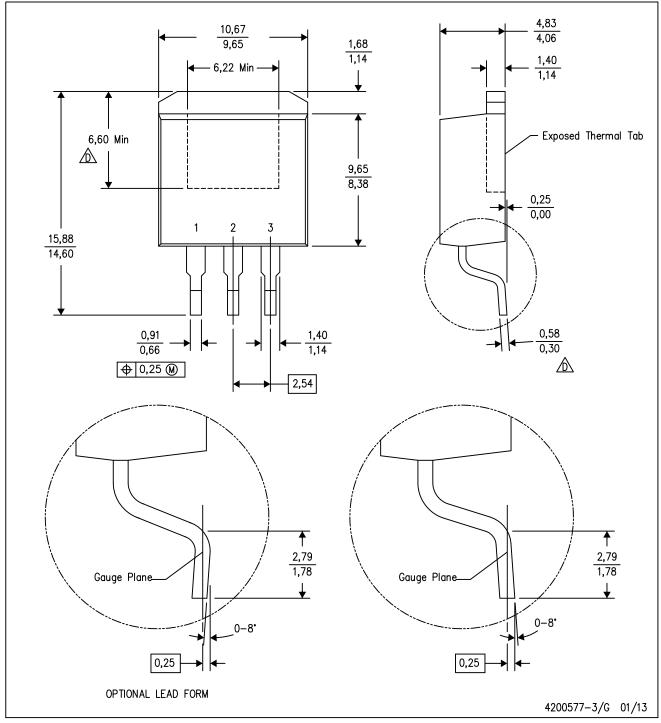


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
LM337KTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0	
LM337KVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0	

KTT (R-PSFM-G3)

PLASTIC FLANGE-MOUNT PACKAGE



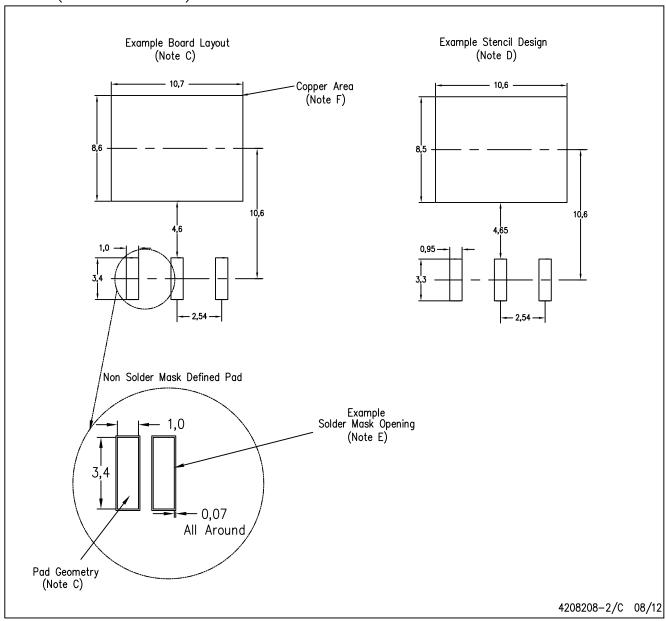
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- ⚠ Falls within JEDEC T0—263 variation AA, except minimum lead thickness and minimum exposed pad length.



KTT (R-PSFM-G3)

PLASTIC FLANGE-MOUNT PACKAGE



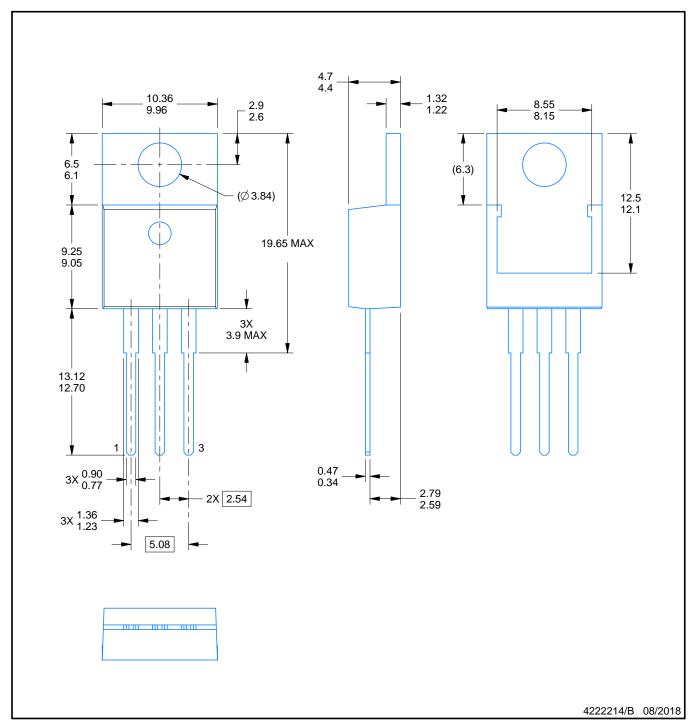
NOTES: A.

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-SM-782 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.

 Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.







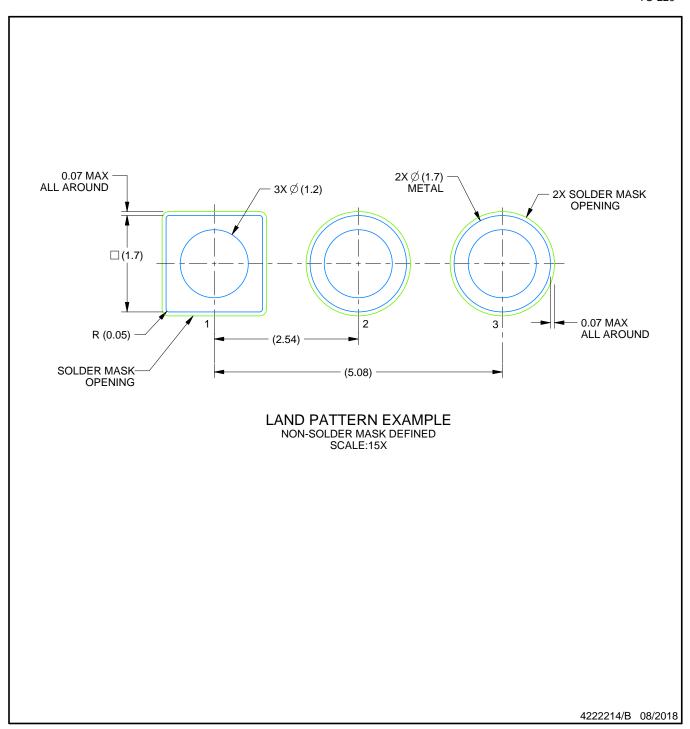
NOTES:

- 1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

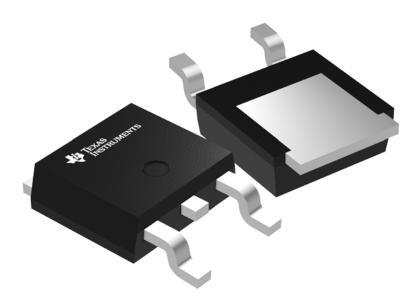
 2. This drawing is subject to change without notice.

 3. Reference JEDEC registration TO-220.





			PFV/IS	SIONS					
REV		DESCRIPTION		7.0.10	ECR	DATE	ENGINEER / DRA	FTSMA	N
Α	RELEASE NEW DRAWING				2151829	10/22/2015	J. NOQUIL / T. LE	QUAN	3
Α	CORRECT NOTE 1				2175971	08/17/2018	E. PREISS / K. SIN	CERBO	ΟX
			SCALE	SIZE		400004	1	B	PAGE
				Α		4222214	+	B	4 of 4

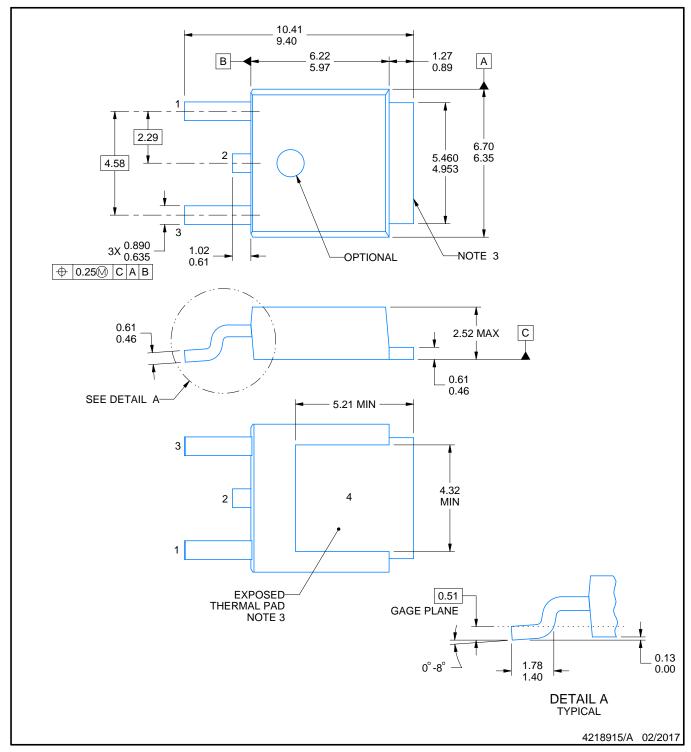


Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4205521-2/E







NOTES:

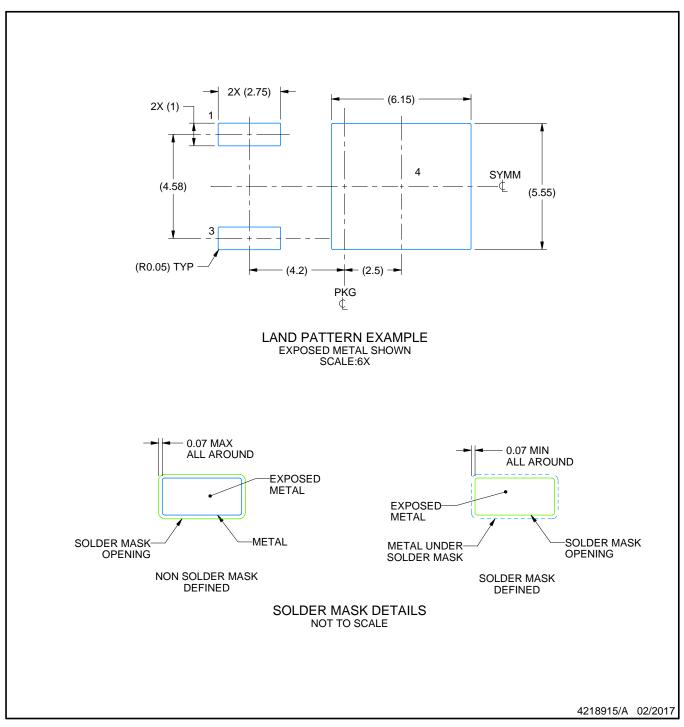
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Shape may vary per different assembly sites.

 4. Reference JEDEC registration TO-252.

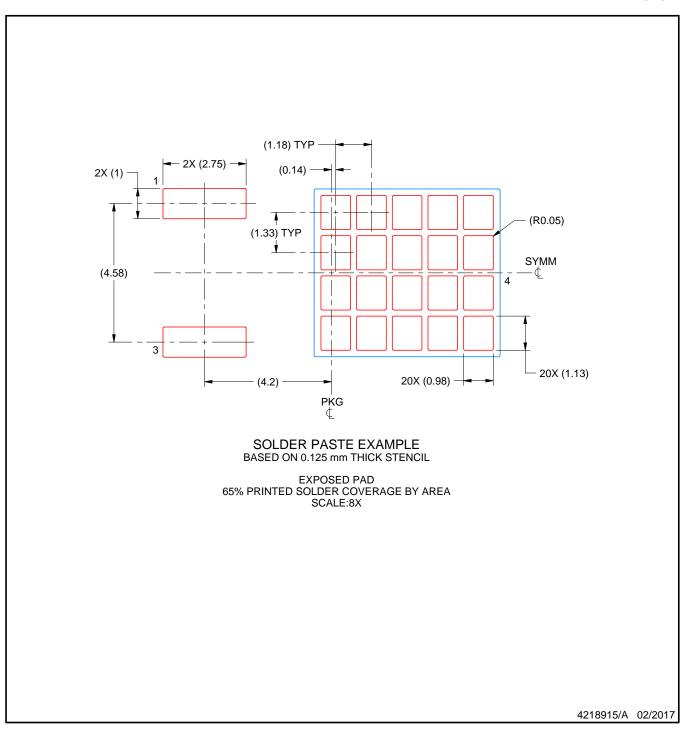




NOTES: (continued)

- 5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
- 6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.





NOTES: (continued)



^{7.} Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

8. Board assembly site may have different recommendations for stencil design.

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