Quad 2:1 Multiplexer/ Demultiplexer Bus Switch

74FST3257

The **onsemi** 74FST3257 is a quad 2:1, high performance multiplexer/demultiplexer bus switch. The device is CMOS TTL compatible when operating between 4 and 5.5 Volts. The device exhibits extremely low R_{ON} and adds nearly zero propagation delay. The device adds no noise or ground bounce to the system.

Features

- $R_{ON} < 4\ \Omega$ Typical
- Less Than 0.25 ns−Max Delay Through Switch
- Nearly Zero Standby Current
- No Circuit Bounce
- Control Inputs are TTL/CMOS Compatible
- Pin−For−Pin Compatible With QS3257, FST3257, CBT3257
- All Popular Packages: SOIC−16, TSSOP−16, QFN16
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant
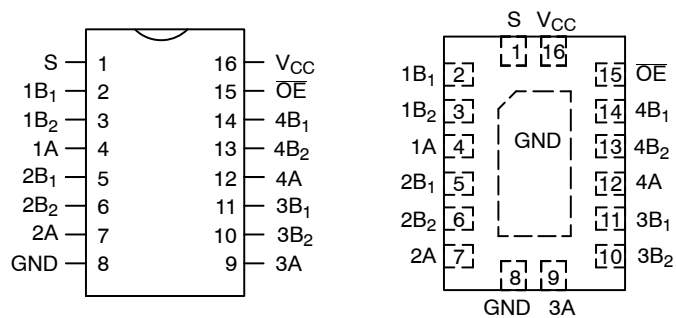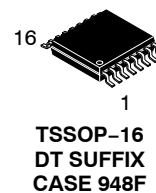

Figure 1. 16−Lead Pinout Diagrams

S	$\overline{OE}$	Function
X	H	Disconnect
L	L	$A = B_1$
H	L	$A = B_2$

Figure 2. Truth Table

MARKING DIAGRAMS

SOIC−16 D SUFFIX CASE 751B

FST3257G AWLYWW

TSSOP−16 DT SUFFIX CASE 948F

FST 3257 ALYW ▪

QFN16 MN SUFFIX CASE 485AW

3257 ALYW▪
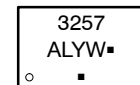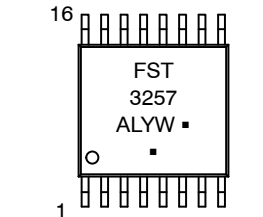
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN NAMES

Pin	Description
$\overline{OE}_1$, $\overline{OE}_2$	Bus Switch Enables
S_0, S_1	Select Inputs
A	Bus A
B_1, B_2, B_3, B_4	Bus B

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.
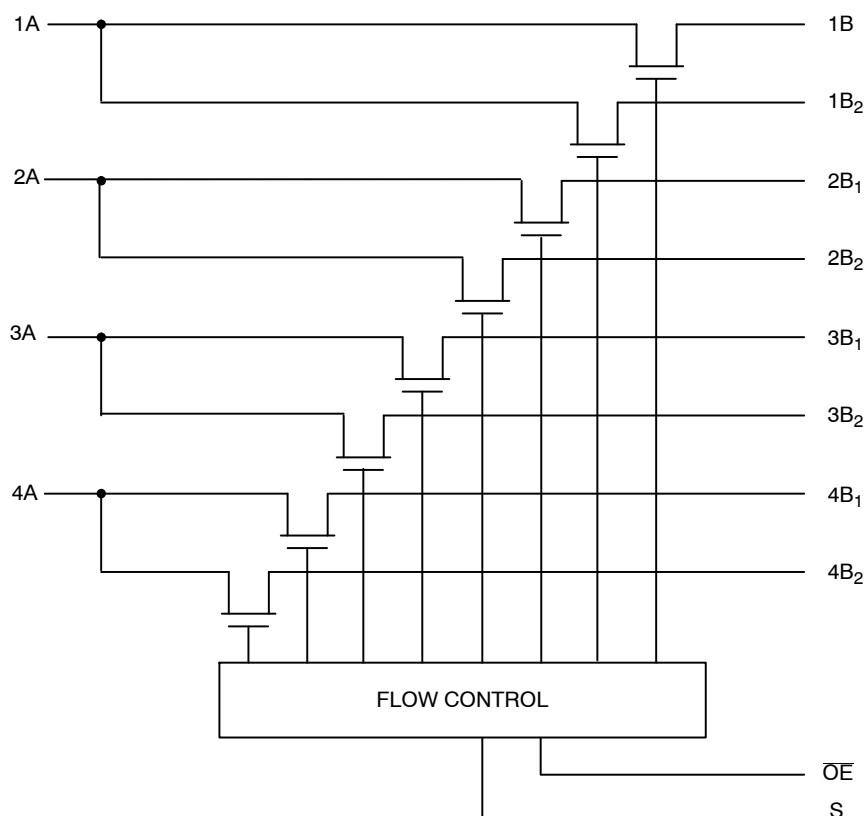
74FST3257

Figure 3. Logic Diagram

ORDERING INFORMATION

Device Order Number	Package	Shipping†
74FST3257DR2G	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
NLV74FST3257DR2G*		
74FST3257DTR2G	TSSOP−16 (Pb−Free)	2500 Units / Tape & Reel
74FST3257MNTWG	QFN16 (Pb−Free)	3000 Units / Tape & Reel
74FST3257MN2TWG	QFN16 (Pb−Free)	3000 Units / Tape & Reel (4mm pitch carrier tape)

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

74FST3257

MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V_{CC}	DC Supply Voltage	−0.5 to +7.0	V
V_I	DC Input Voltage	−0.5 to +7.0	V
V_O	DC Output Voltage	−0.5 to +7.0	V
I_{IK}	DC Input Diode Current $V_I < GND$	−50	mA
I_{OK}	DC Output Diode Current $V_O < GND$	−50	mA
I_O	DC Output Sink Current	128	mA
I_{CC}	DC Supply Current per Supply Pin	±100	mA
I_{GND}	DC Ground Current per Ground Pin	±100	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature Under Bias	+150	°C

θ_{JA}	Thermal Resistance
	    SOIC
	    TSSOP
	    QFN
		125
		170
		N/A
			°C/W

MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	

V_{ESD}	ESD Withstand Voltage
	    Human Body Model (Note 1)
	    Machine Model (Note 2)
	    Charged Device Model (Note 3)
		>2000
		>200
		N/A
			V

$I_{Latchup}$	Latchup Performance Above V_{CC} and Below GND at 85°C (Note 4)	±500	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Tested to EIA/JESD22−A114−A.
2. Tested to EIA/JESD22−A115−A.
3. Tested to JESD22−C101−A.
4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage Operating, Data Retention Only		4.0	5.5	V
V_I	Input Voltage (Note 5)		0	5.5	V
V_O	Output Voltage (HIGH or LOW State)		0	5.5	V
T_A	Operating Free−Air Temperature		−40	+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate Switch I/O	Switch Control Input $V_{CC} = 5.0 V \pm 0.5 V$	0	DC 5	ns/V

5. Unused control inputs may not be left open. All control inputs must be tied to a high or low logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$			Units
				Min	Typ*	Max	
V_{IK}	Clamp Diode Voltage	$I_{IN} = -18$ mA	4.5			−1.2	V
V_{IH}	High−Level Input Voltage		4.0 to 5.5	2.0			V
V_{IL}	Low−Level Input Voltage		4.0 to 5.5			0.8	V
I_I	Input Leakage Current	$0 \leq V_{IN} \leq 5.5$ V	5.5			±1.0	μA
I_{OZ}	Off−State Leakage Current	$0 \leq A, B \leq V_{CC}$	5.5			±1.0	μA
R_{ON}	Switch On Resistance (Note 6)	$V_{IN} = 0$ V, $I_{IN} = 64$ mA	4.5		4	7	Ω
		$V_{IN} = 0$ V, $I_{IN} = 30$ mA	4.5		4	7	
		$V_{IN} = 2.4$ V, $I_{IN} = 15$ mA	4.5		8	15	
		$V_{IN} = 2.4$ V, $I_{IN} = 15$ mA	4.0		11	20	
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$	5.5			3	μA
ΔI_{CC}	Increase In I_{CC} per Input	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5			2.5	mA

*Typical values are at $V_{CC} = 5.0$ V and $T_A = 25°C$.
6. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC ELECTRICAL CHARACTERISTICS

| Symbol	Parameter	Conditions	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF, RU = RD = 500 Ω				Units
			$V_{CC} = 4.5–5.5$ V		$V_{CC} = 4.0$ V		
			Min	Max	Min	Max	
t_{PHL}, t_{PLH}	Prop Delay Bus to Bus (Note 7)	$V_I = $ OPEN		0.25		0.25	ns
	Prop Delay, Select to Bus A		1.0	4.7		5.2	
t_{PZH}, t_{PZL}	Output Enable Time, Select to Bus B	$V_I = 7$ V for t_{PZL}	1.0	5.2		5.7	ns
	Output Enable Time, I_{OE} to Bus A, B	$V_I = $ OPEN for t_{PZH}	1.0	5.1		5.6	
t_{PHZ}, t_{PLZ}	Output Disable Time, Select to Bus B	$V_I = 7$ V for t_{PLZ}	1.0	5.2		5.5	ns
	Output Disable Time, I_{OE} to Bus A, B	$V_I = $ OPEN for t_{PHZ}	1.0	5.5		5.5	

7. This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

CAPACITANCE (Note 8)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Control Pin Input Capacitance	$V_{CC} = 5.0$ V	3		pF
$C_{I/O}$	A Port Input/Output Capacitance	V_{CC}, $\overline{OE} = 5.0$ V	7		pF
$C_{I/O}$	B Port Input/Output Capacitance	V_{CC}, $\overline{OE} = 5.0$ V	5		pF

8. $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

74FST3257

AC Loading and Waveforms

V_I

500 Ω

FROM
OUTPUT
UNDER
TEST

C_L*

500 Ω
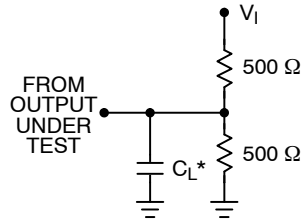
NOTES:
1. Input driven by 50 Ω source terminated in 50 Ω.
2. CL includes load and stray capacitance.
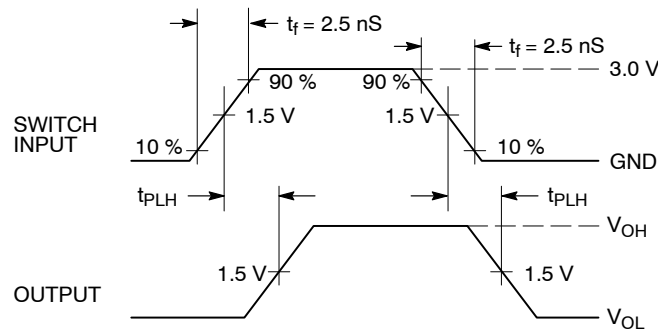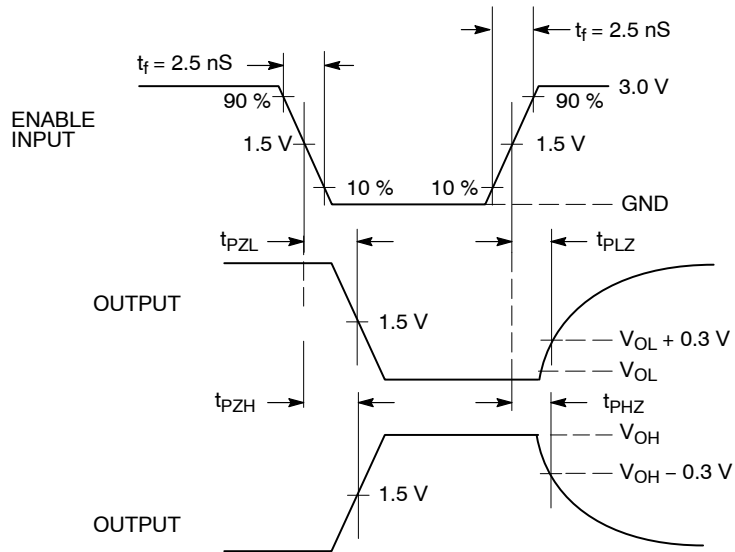   *C_L = 50 pF

Figure 4. AC Test Circuit

$t_f = 2.5$ nS

$t_f = 2.5$ nS

SWITCH
INPUT

90 %   90 %

3.0 V

1.5 V   1.5 V

10 %   10 %

GND

t_{PLH} t_{PLH}

V_{OH}

1.5 V   1.5 V

OUTPUT

V_{OL}

Figure 5. Propagation Delays

$t_f = 2.5$ nS

$t_f = 2.5$ nS

ENABLE
INPUT

90 %   90 %

3.0 V

1.5 V   1.5 V

10 %   10 %

GND

t_{PZL} t_{PLZ}

OUTPUT

1.5 V

V_{OL} + 0.3 V

V_{OL}

t_{PZH} t_{PHZ}

V_{OH}

V_{OH} − 0.3 V

1.5 V

OUTPUT

Figure 6. Enable/Disable Delays

QFN16, 2.5x3.5, 0.5P
CASE 485AW−01
ISSUE O

DATE 11 DEC 2008

1

SCALE 2:1

PIN ONE REFERENCE

2X | △ | 0.15 | C

2X | △ | 0.15 | C

TOP VIEW
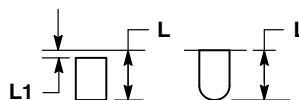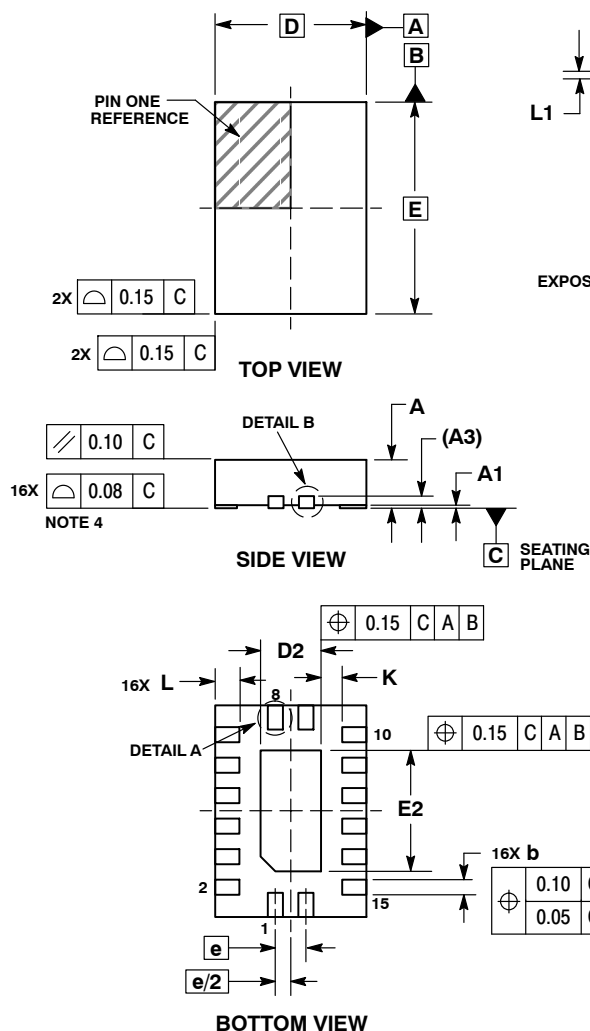
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

EXPOSED Cu   **MOLD CMPD**
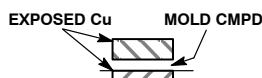
DETAIL B
ALTERNATE CONSTRUCTIONS

| ∥ | 0.10 | C |

16X | △ | 0.08 | C
NOTE 4

DETAIL B

SIDE VIEW

SEATING PLANE

| ⊕ | 0.15 | C | A | B |

16X L

DETAIL A

| ⊕ | 0.15 | C | A | B |

| ⊕ | 0.10 | C | A | B |
| | 0.05 | C | | |
NOTE 3

16X b

BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
E	3.50 BSC	
E2	1.85	2.15
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	---	0.15

GENERIC MARKING DIAGRAM*
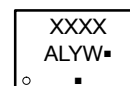
XXXX
ALYW■

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ■", may or may not be present.

SOLDERING FOOTPRINT*

3.80

2.10

2.80 1.10

0.50 PITCH

1

16X 0.60

16X 0.30

PACKAGE OUTLINE

DIMENSIONS: MILLIMETERS
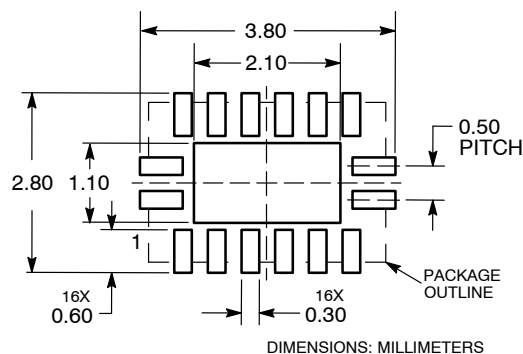
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON36347E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**QFN16, 2.5X3.5, 0.5P**		**PAGE 1 OF 1**

SOIC−16
CASE 751B−05
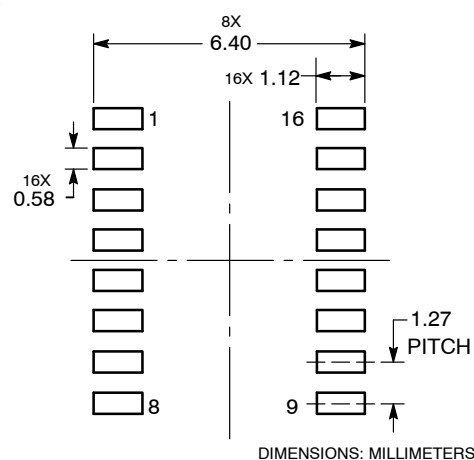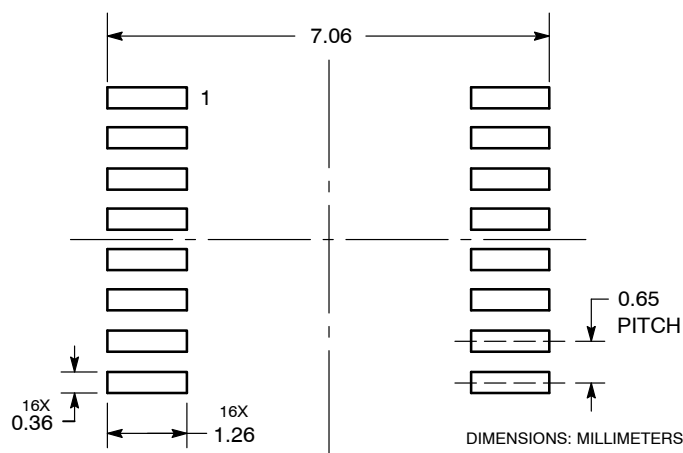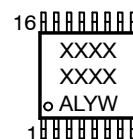ISSUE K
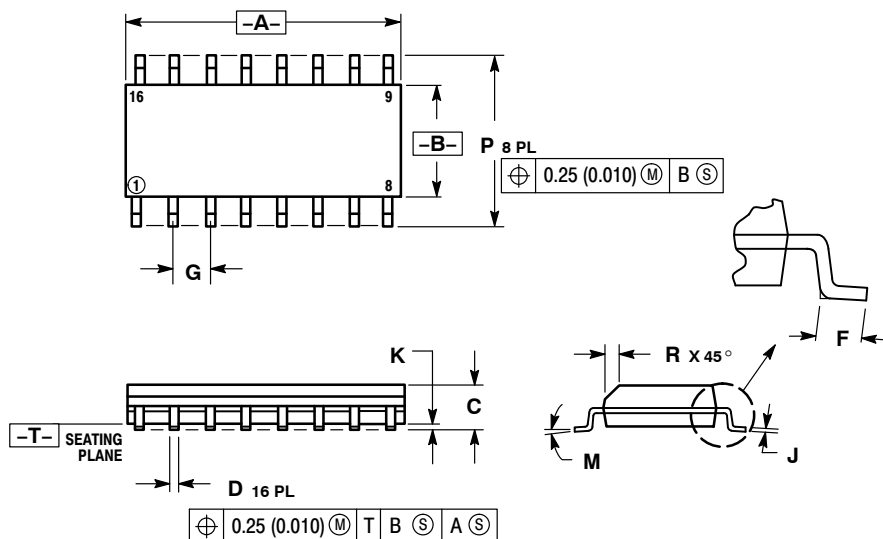
SCALE 1:1

DATE 29 DEC 2006

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

$\bigoplus$ 0.25 (0.010) Ⓜ B Ⓢ

$\bigoplus$ 0.25 (0.010) Ⓜ T B Ⓢ A Ⓢ

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT

8X
6.40

16X 1.12

16X
0.58

1.27
PITCH

DIMENSIONS: MILLIMETERS

DOCUMENT NUMBER:	98ASB42566B		
DESCRIPTION:	SOIC−16		PAGE 1 OF 1

TSSOP−16
CASE 948F−01
ISSUE B

DATE 19 OCT 2006
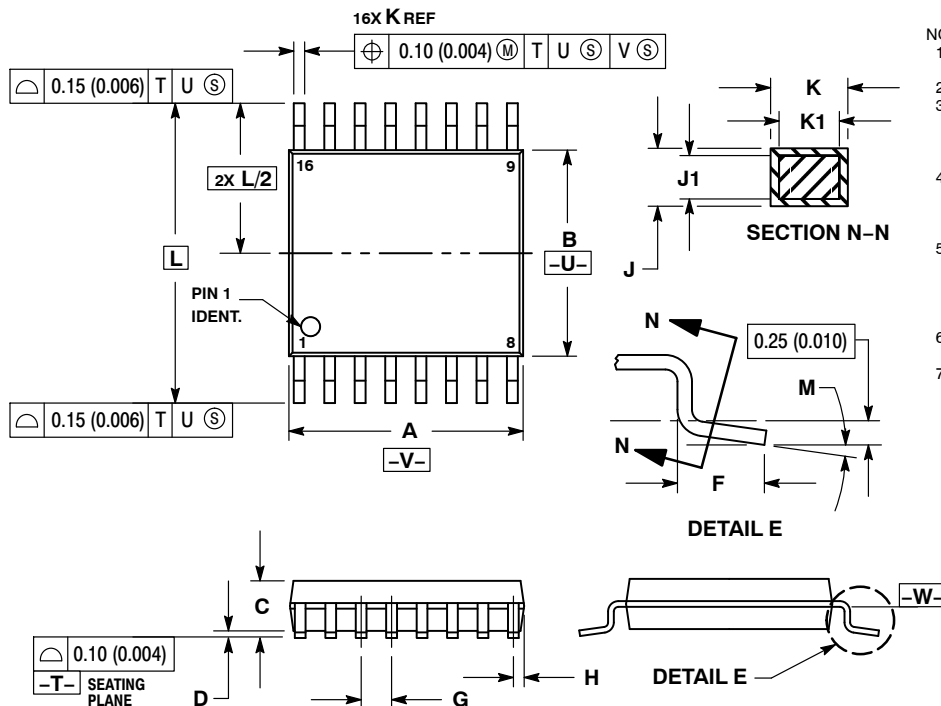
16

1

SCALE 2:1

16X **K** REF

⊕ | 0.10 (0.004) Ⓜ | T | U Ⓢ | V Ⓢ

△ | 0.15 (0.006) | T | U Ⓢ

2X **L/2**

L

PIN 1
IDENT.

△ | 0.15 (0.006) | T | U Ⓢ

16   9

8   1

B
–U–

A
–V–

K
K1

J1

J

SECTION N–N

N

0.25 (0.010)

M

N

F

DETAIL E

C

△ | 0.10 (0.004)

–T– SEATING
PLANE

D

G

H

–W–

DETAIL E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	–––	1.20	–––	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT

7.06

1

0.65
PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS

**GENERIC
MARKING DIAGRAM***

16

XXXX
XXXX
ALYW

1

XXXX = Specific Device Code
A   = Assembly Location
L   = Wafer Lot
Y   = Year
W   = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

DOCUMENT NUMBER:	98ASH70247A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	TSSOP−16		PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

◊