



# SiI9385, SiI9387, and SiI9389 Port Processor

## Data Brief

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## General Description

The SiI9385, SiI9387, and SiI9389 Port Processor is the second generation HDMI® port processor with HDMI Ethernet and Audio-return Channel (HEAC) support on one input port. They provide a simple, low-cost method of retransmitting protected digital audio, video, Mobile HD signals, and Ethernet, giving manufacturers a low-cost method of adding an HEAC-capable port to the latest digital TVs. Backward compatibility allows HEAC systems to connect to any existing HDMI and DVI 1.0 source.

These parts support the Audio return Channel (ARC) described in the HDMI 1.4 Specification, which provides an S/PDIF link from an HDMI sink to an HDMI source in the opposite direction of the TMDS™ data flow.

The SiI9387/SiI9389 device supports the HDMI Ethernet Channel (HEC) described in the HDMI 1.4 Specification. The HEC feature adds a connection to the HDMI link that is capable of carrying the same data as a full duplex, 100 Mbps Ethernet connection. An HDMI with Ethernet cable used with the SiI9387/SiI9389 device eliminates the need for additional Ethernet cables, allowing for convenient integration of Digital Televisions (DTVs) into the end user's home network system.

The SiI9389 device supports Vendor Specific InfoFrame (VSIF) extraction, which allows the host system to receive information about the 3D video mode being passed-through.

## Features

- Audio Return Channel that allows an S/PDIF uplink from HDMI sink device to an HDMI source available in one receiver port
- InstaPort™ viewing technology that reduces port switching time to less than one second
- Adaptive equalizer provides long cable support, even at Deep Color resolutions

- Standby power modes and built-in regulator meets Energy Star and other power saving requirements, lowers system cost, and optimizes board design

## HDMI Inputs and Output

- Five HDMI input ports and single output port
- HDMI, HDCP, and DVI compatibility
- TMDS cores run at 2.25 Gbps
- Supports video resolutions up to 1080p, 60 Hz, 12-bit or 720p/1080i, 120 Hz, 12-bit
- Supports all the mandatory and several optional 3D formats described in the HDMI 1.4 Specification
- Mobile HD support for 1080i @ 60 Hz on two ports
- Pre-programmed with HDCP keys
- HDMI Ethernet Channel support for one receive port (SiI9387/SiI9389 device only)
- Repeater function supports up to 127 devices (SiI9387/SiI9389 device only)
- Vendor Specific InfoFrame (VSIF) extraction to support 3D video (SiI9389 only)

## Control Capability

- Consumer Electronics Control (CEC) interface incorporates an HDMI-compliant CEC I/O and an integrated Silicon Image CEC Programming Interface (CPI); these simplify design and lower costs and software overhead
- Integrated EDID and DDC support for the HDMI ports using a 512-byte NVRAM shared between ports that loads into separate 256-byte SRAM for each of 5 HDMI ports and 128-byte SRAM for VGA EDID
- Individual control of Hot Plug Detect (HPD) for each of the ports
- Controllable by the local I<sup>2</sup>C bus

## Packaging

- 100-pin, 14 mm x 14 mm, 0.5 mm pitch TQFP package with enhanced ePad™

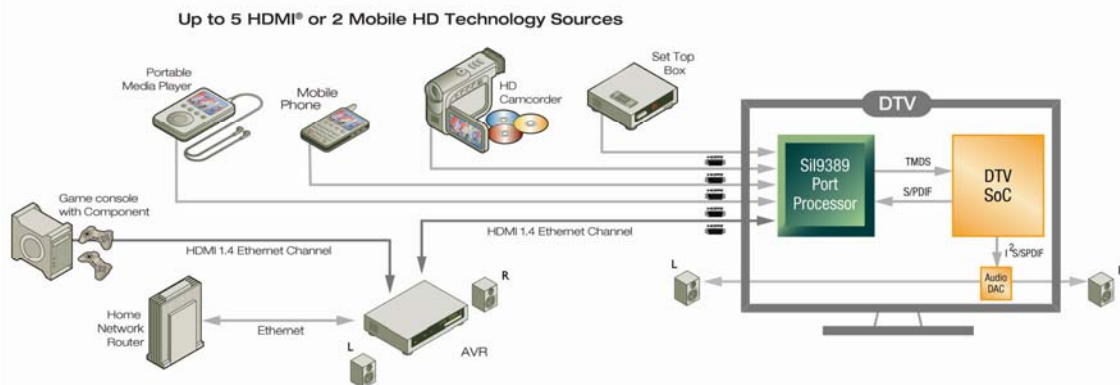


Figure 1. Port Processor Application

## Pin Diagram

Figure 2 shows the pin assignments of the port processor. The package is a 14 mm x 14 mm 100-pin TQFP with an ePad, which *must* be connected to ground. Pin names are generalized by type for this document. The list below the diagram describes the purpose of each type.

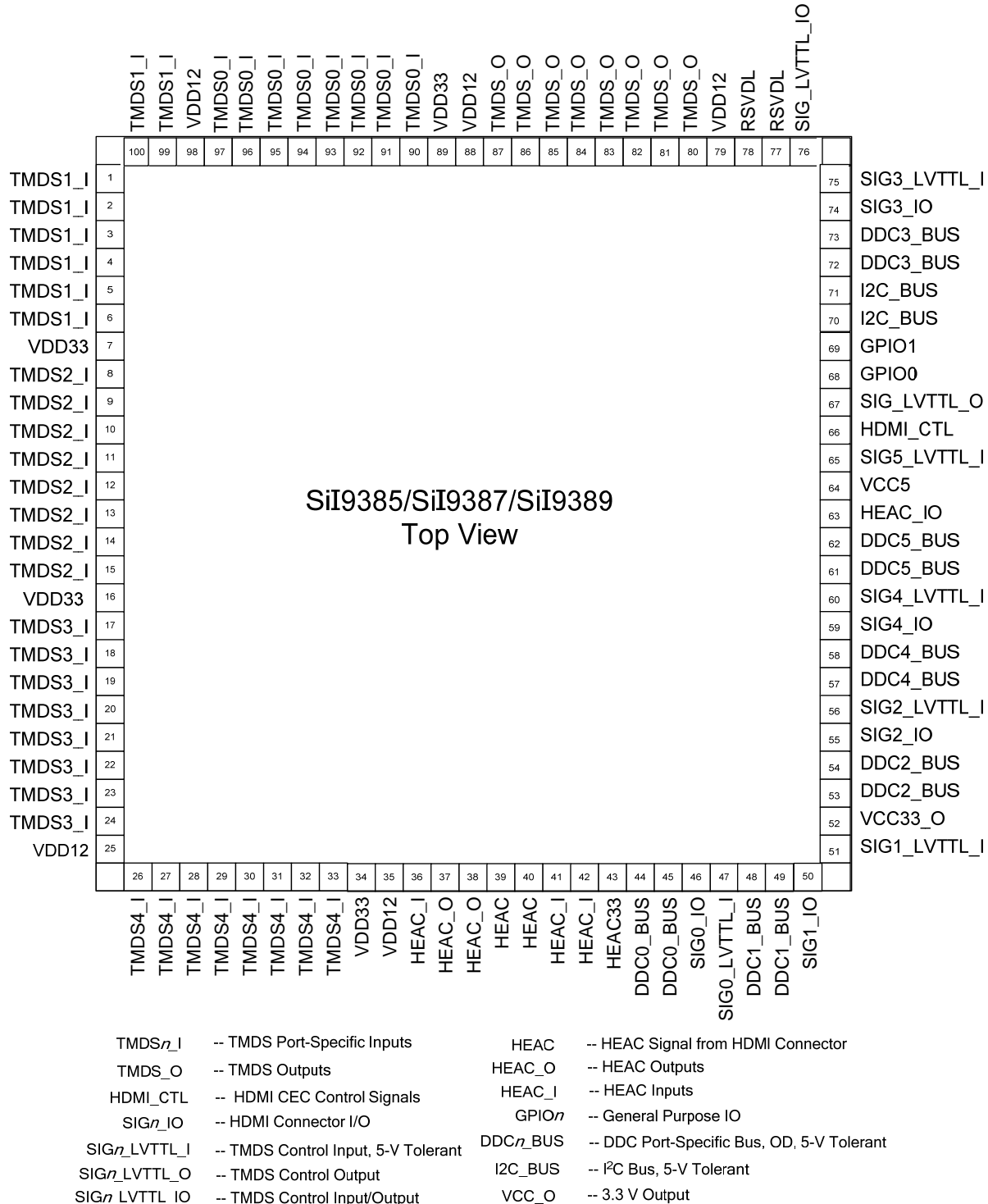


Figure 2. Pin Diagram (Top View)

## Package Information

### ePad Requirements

The SiI9385, SiI9387, and SiI9389 Port Processor chip is packaged in a 100-pin, 14 mm x 14mm TQFP package with an ExposedPad™ (ePad™) that is used both for the electrical connectivity ground of the device and for improved thermal transfer characteristics. The ePad dimensions are 5 mm x 5 mm  $\pm$ 0.15 mm. Soldering of the ePad to the ground plane of the PCB is **required** to meet package power dissipation requirements at full speed operation, and to correctly connect the chip circuitry to electrical ground.

**Note:** The ePad **must** be soldered to an electrically grounded plane on the PCB. A clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical shorts.

The thermal land area on the PCB may use thermal vias to improve heat removal from the package. These thermal vias also double as the ground connections of the chip and must attach internally in the PCB to the ground plane. An array of vias should be designed into the PCB beneath the package. For optimum thermal performance, the via diameter should be 12 mils to 13 mils (0.30 mm to 0.33 mm) and the via barrel should be plated with 1-ounce copper to plug the via. This design helps to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be tented with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

Package stand-off when mounting the device also needs to be considered. For a nominal stand-off of approximately 0.1 mm the stencil thickness of 5 mils to 8 mils should provide a good solder joint between the ePad and the thermal land.

[Figure 3](#) shows the package dimensions of the SiI9385/SiI9387/SiI9389 port processor.

## Package Dimensions

These drawings are not to scale.

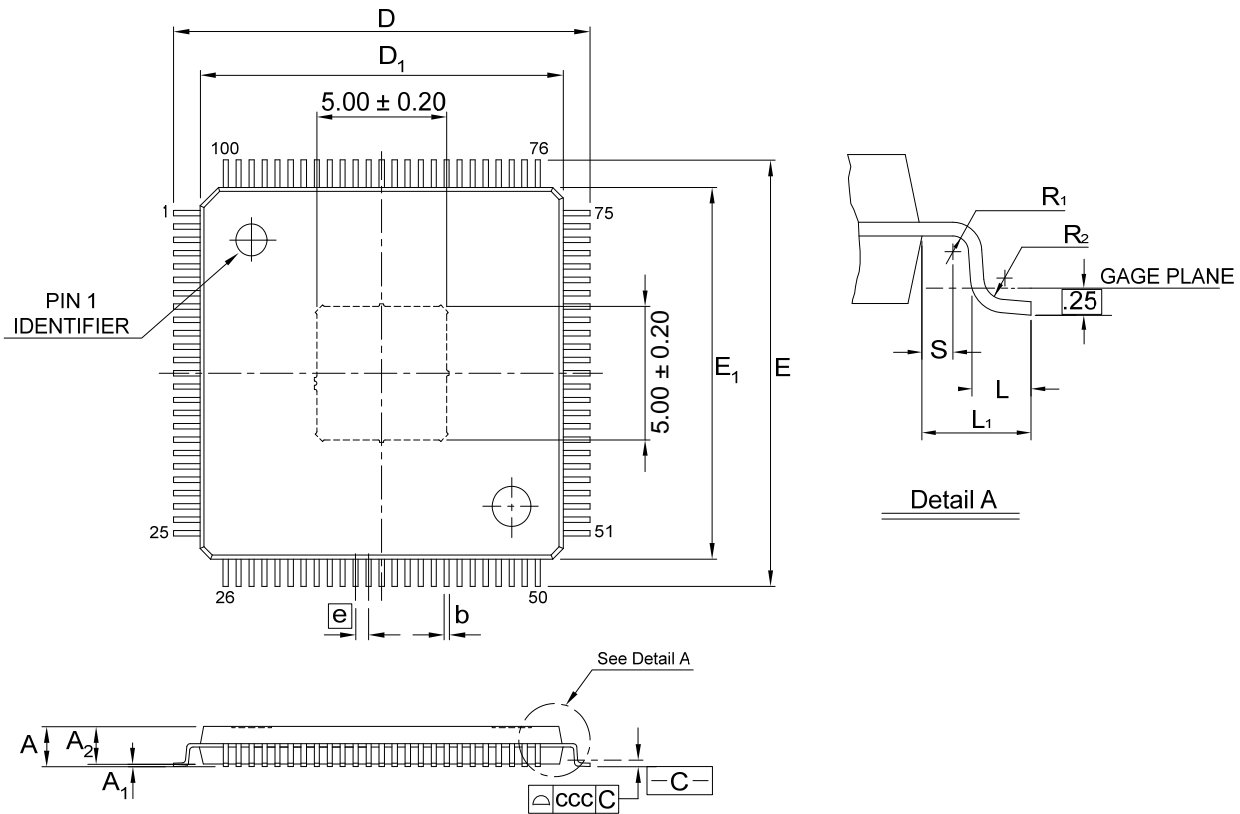


Figure 3. Package Diagram

### JEDEC Package Code MS-026

Item	Description	Min	Typ	Max
A	Thickness	—	—	1.20
A1	Stand-off	0.05	—	0.15
A2	Body thickness	0.95	1.00	1.05
D	Footprint	16.00 BSC		
E	Footprint	16.00 BSC		
D <sub>1</sub>	Body size	14.00 BSC		
E <sub>1</sub>	Body size	14.00 BSC		
b	Lead width	0.17	0.22	0.27

Item	Description	Min	Typ	Max
C	Lead thickness	0.09	—	0.20
e	Lead pitch	0.50 BSC		
L	Lead foot length	0.45	0.60	0.75
L <sub>1</sub>	Total lead length	1.00 REF		
R <sub>1</sub>	Lead radius, inside	0.08	—	—
R <sub>2</sub>	Lead radius, outside	0.08	—	0.20
S	Lead horizontal run	0.20	—	—
ccc	Lead coplanarity	0.08		

## Marking Specification

Figure 4 shows the markings of the SiI9385/SiI9387/SiI9389 package. This drawing is not to scale.

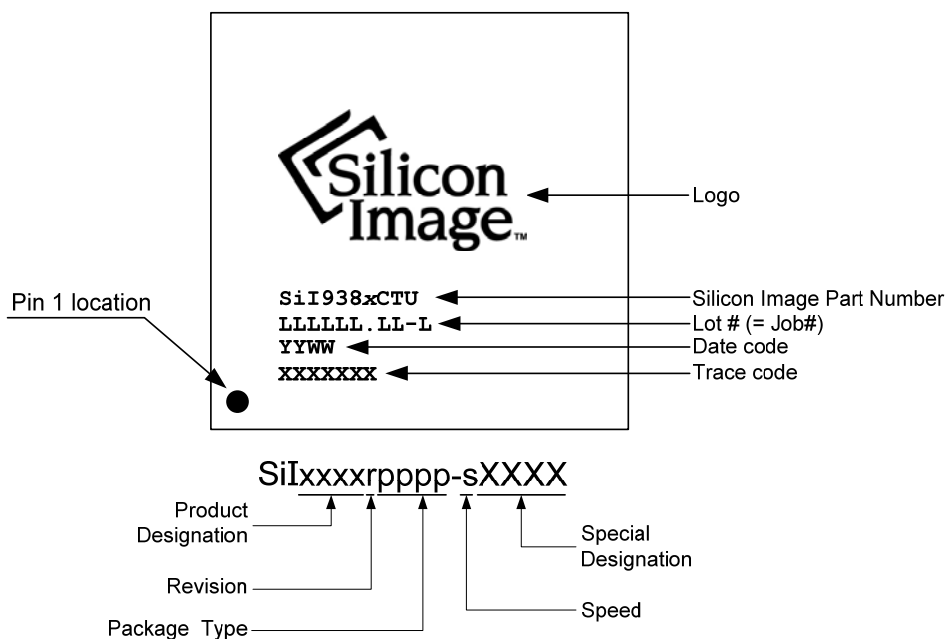


Figure 4. Marking Diagram

## Ordering Information

Production Part Numbers:

Device	Part Number
Standard port processor with ARC	SiI9385CTU
Port processor with HEAC and repeater capability	SiI9387CTU
Port processor with HEAC, repeater capability, and 3D VSIF	SiI9389CTU

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1060 E. Arques Avenue  
Sunnyvale, CA 94085

T 408.616.4000 F 408.830.9530

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