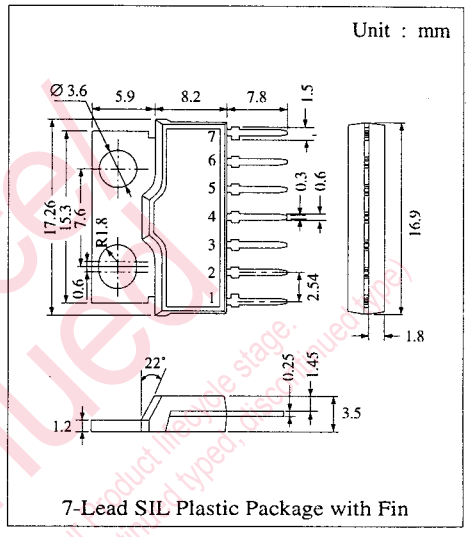
AN5515

TV Vertical Deflection Output Circuit

■ Description

The AN5515 is an integrated circuit designed for TV vertical deflection output circuit. Combining with the deflection signal processing IC can facilitate the vertical output circuit design.



7-Lead SIL Plastic Package with Fin

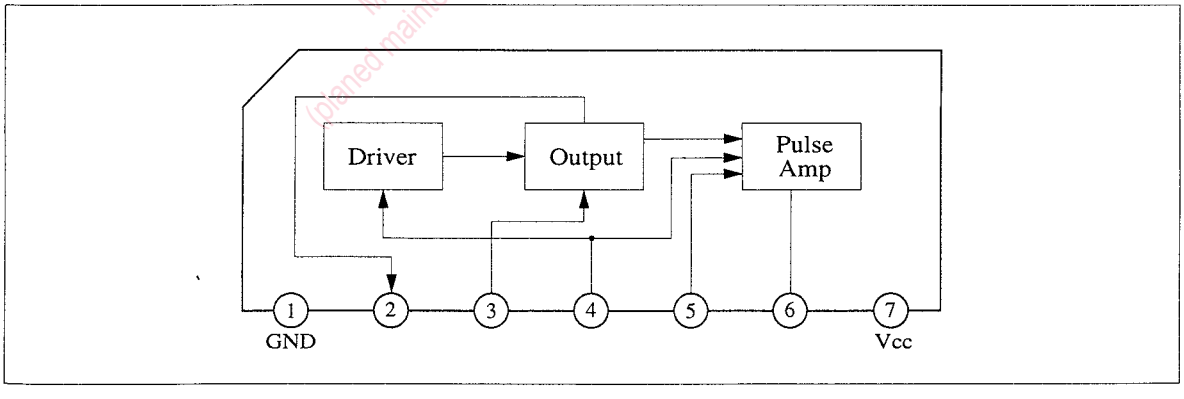
■ Features

- Low power consumption
- Direct deflection coil driving capability (Flyback voltage two times as high as supply voltage is supplied during flyback period only)
- High breakdown voltage: 60V

■ Pin Descriptions

Pin No.	Pin Name
1	GND
2	Output
3	Supply Voltage for Output
4	Input
5	Trigger Pulse Input
6	Pulse Amp. Output
7	Vcc

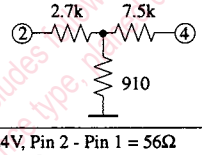
■ Block Diagram



■ Absolute Maximum Ratings (Ta=25°C)

Item		Symbol	Rating		Unit
Voltage	Supply Voltage	V_{CC}	30		V
	Circuit Voltage	V_{2-1}	0	60	V
		V_{3-1}	0	60	V
		V_{4-1}	-1	6	V
		V_{5-1}	-1	3	V
Current	Supply Current	I_{CC}	300		mA
	Circuit Current	I_2	-1300	1300	mA_{O-P}
		I_6	-1300	1300	mA_{O-P}
Power Dissipation		P_D	6		W
Operating Ambient Temperature		Topr	-20 ~ +70		°C
Storage Temperature		Tstg	-55 ~ +150		°C

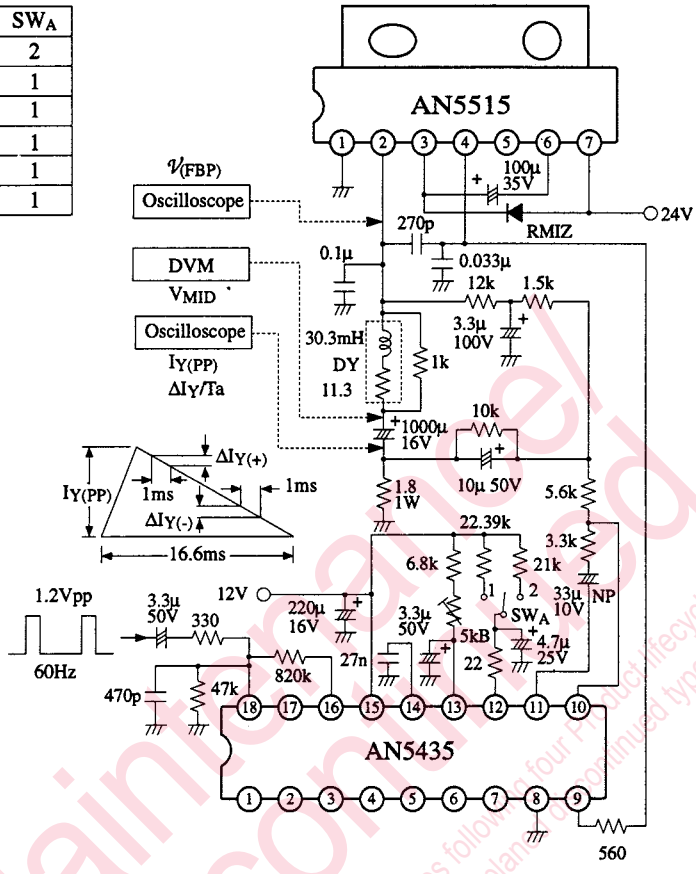
■ Electrical Characteristics (Ta=25°C)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Deflection Current (Peak Value)	$I_{Y(PP)}$	1		1280	1380	1480	mApp
Deflection Current Linearity	$\Delta I_{Y(+)}$	1		46		140	mApp
	$\Delta I_{Y(-)}$	1		42		126	mApp
Deflection Current Change with Ambient Temp.*	$\Delta I_Y/Ta$	1	Ta = -20 ~ +70°C	-1.5		1.5	%
Center Voltage	V_{MID}	1		13.2	13.8	14.4	V
Flyback Pulse Amplitude	$V_{(FBP)}$	1		47			V
Static Circuit Current	I_{CQ}		V_{3-1} = 24V V_{7-1} = 24V V_{5-1} = 0 	8	14	24	mA
Output Tr Saturation Voltage	V_{3-2}		V_{3-1} = V_{7-1} = 24V, Pin 2 - Pin 1 = 56Ω V_{4-1} = 0.3V, V_{5-1} = 0		2.7	3.7	V
Output Tr Saturation Voltage	V_{2-1}		V_{3-1} = V_{7-1} = 24V, Pin 2 - Pin 3 = 56Ω V_{4-1} = 3V, V_{5-1} = 0		0.6	1	V
Q_{21} Saturation Voltage	V_{6-1}		V_{7-1} = 24V, Pin 7 - Pin 6 = 1.2kΩ V_{5-1} = 2V, V_{5-1} = 0			0.5	V
Thermal Resistance	$R_{th(j-c)}$					4	°C/W

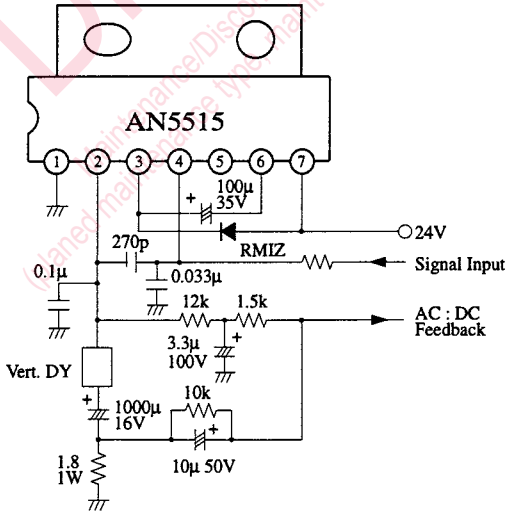
* Design reference value

Test Circuit 1 ($I_{Y(PP)}$, $\Delta I_{Y(+)}$, $\Delta I_{Y(-)}$, $\Delta I_Y/Ta$, V_{MID}, $\mathcal{V}_{(FBP)}$)

Item	SW_A
$I_{Y(PP)}$	2
$\Delta I_{Y(+)}$	1
$\Delta I_{Y(-)}$	1
$\Delta I_Y/Ta$	1
V_{MID}	1
$\mathcal{V}_{(FBP)}$	1



■ Application Circuit



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