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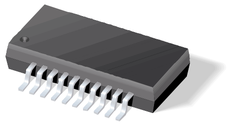

PLL1707
PLL1708

SLES065 – DECEMBER 2002

3.3-V DUAL PLL MULTICLOCK GENERATOR

FEATURES

- **27-MHz Master Clock Input**
- **Generated Audio System Clock (PLL1707):**
  - **SCKO0: 768 f_S (f_S = 44.1 kHz)**
  - **SCKO1: 768 f_S, 512 f_S (f_S = 48 kHz)**
  - **SCKO2: 256 f_S (f_S = 32, 44.1, 48, 64, 88.2, 96 kHz)**
  - **SCKO3: 384 f_S (f_S = 32, 44.1, 48, 64, 88.2, 96 kHz)**
- **Generated Audio System Clock (PLL1708):**
  - **SCKO0: 768 f_S (f_S = 44.1 kHz)**
  - **SCKO1: 768 f_S, 512 f_S, 384 f_S, 256 f_S (f_S = 48 kHz)**
  - **SCKO2: 256 f_S (f_S = 16, 22.05, 24, 32, 44.1, 48, 64, 88.2, 96 kHz)**
  - **SCKO3: 384 f_S (f_S = 16, 22.05, 24, 32, 44.1, 48, 64, 88.2, 96 kHz)**
- **Zero PPM Error Output Clocks**
- **Low Clock Jitter: 50 ps (Typical)**
- **Multiple Sampling Frequencies (PLL1707):**
  - **f_S = 32, 44.1, 48, 64, 88.2, 96 kHz**
- **Multiple Sampling Frequencies (PLL1708):**
  - **f_S = 16, 22.05, 24, 32, 44.1, 48, 64, 88.2, 96 kHz**
- **3.3-V Single Power Supply**
- **PLL1707: Parallel Control**
  PLL1708: Serial Control
- **Package: 20-Pin SSOP (150 mil), Lead-Free Product**

APPLICATIONS

- **HDD + DVD Recorders**
- **DVD Recorders**
- **HDD Recorders**
- **DVD Players**
- **DVD Add-On Cards for Multimedia PCs**
- **Digital HDTV Systems**
- **Set-Top Boxes**

DESCRIPTION

The PLL1707[†] and PLL1708[†] are low cost, phase-locked loop (PLL) multiclock generators. The PLL1707 and PLL1708 can generate four system clocks from a 27-MHz reference input frequency. The clock outputs of the PLL1707 can be controlled by sampling frequency-control pins and those of the PLL1708 can be controlled through serial-mode control pins. The device gives customers both cost and space savings by eliminating external components and enables customers to achieve the very low-jitter performance needed for high performance audio DACs and/or ADCs. The PLL1707 and PLL1708 are ideal for MPEG-2 applications which use a 27-MHz master clock such as DVD recorders, HDD recorders, DVD add-on cards for multimedia PCs, digital HDTV systems, and set-top boxes.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

[†] The PLL1707 and PLL1708 use the same die and they are electrically identical except for mode control.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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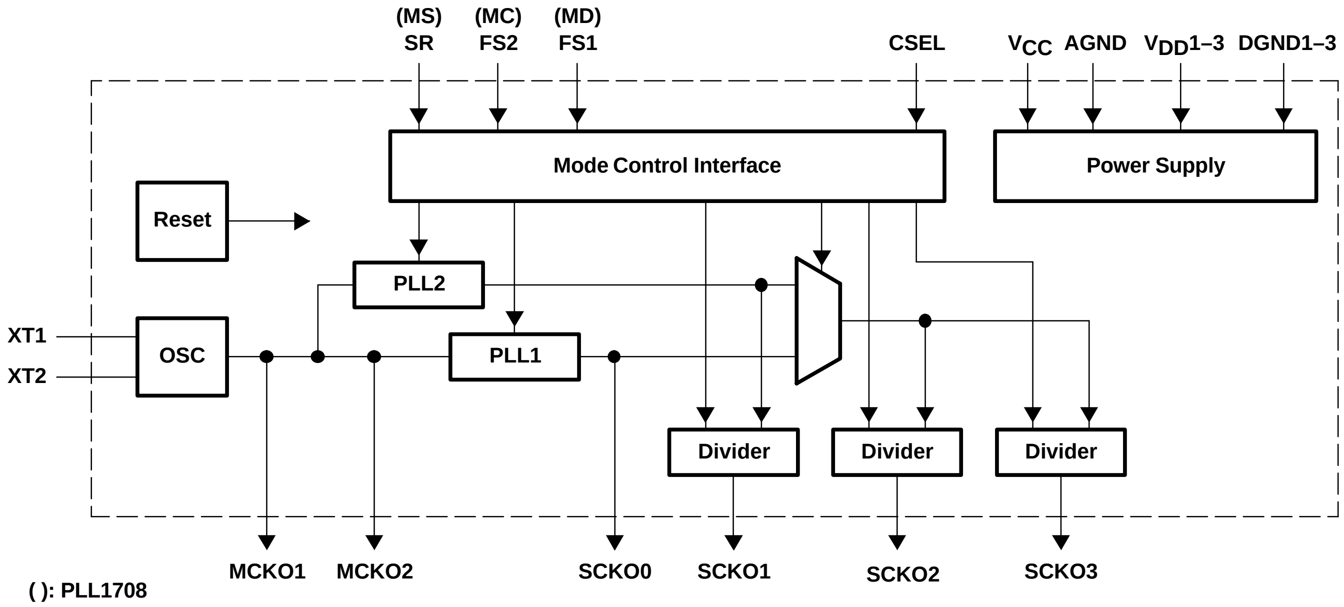
FUNCTIONAL BLOCK DIAGRAM


(MS)
SR
(MC)
FS2
(MD)
FS1
CSEL
V_{CC}
AGND
V_{DD}1–3
DGND1–3
Mode Control Interface
Power Supply
Reset
PLL2
PLL1
OSC
XT1
XT2
Divider
Divider
Divider
MCKO1
MCKO2
SCKO0
SCKO1
SCKO2
SCKO3
( ): PLL1708

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE CODE	OPERATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
PLL1707DBQ	SSOP 20	20DBQ	–25°C to 85°C	PLL1707	PLL1707DBQ	Tube
					PLL1707DBQR	Tape and reel
PLL1708DBQ	SSOP 20	20DBQ	–25°C to 85°C	PLL1708	PLL1708DBQ	Tube
					PLL1708DBQR	Tape and reel

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	PLL1705 AND PLL1706
Supply voltage: V_{CC}, $V_{DD}1–V_{DD}3$	4 V
Supply voltage differences: V_{CC}, $V_{DD}1–V_{DD}3$	±0.1 V
Ground voltage differences: AGND, DGND1–DGND3	±0.1 V
Digital input voltage: FS1 (MD), FS2 (MC), SR (MS), CSEL	– 0.3 V to (V_{DD} + 0.3) V
Analog input voltage, XT1, XT2	– 0.3 V to (V_{CC} + 0.3) V
Input current (any pins except supplies)	±10 mA
Ambient temperature under bias	–40°C to 125°C
Storage temperature	–55°C to 150°C
Junction temperature	150°C
Lead temperature (soldering)	260°C, 5 s
Package temperature (IR reflow, peak)	260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, $V_{DD}1$–$V_{DD}3$ (= V_{DD}) = V_{CC} = 3.3 V, f_M = 27 MHz, crystal oscillation, f_S = 48 kHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT							
	Logic input			CMOS compatible			
V_{IH} (1)	Input logic level			$0.7V_{DD}$		3.6	Vdc
V_{IL} (1)						0.3 V_{DD}	
I_{IH} (1)	Input logic current		V_{IN} = V_{DD}		65	100	μA
I_{IL} (1)			V_{IN} = 0 V			±10	
	Logic output			CMOS			
V_{OH} (2)	Output logic level		I_{OH} = –4 mA	V_{DD} – 0.4 V			Vdc
V_{OL} (2)			I_{OL} = 4 mA			0.4	Vdc
	Sampling frequency	PLL1707	Standard f_S	32	44.1	48	kHz
			Double f_S	64	88.2	96	
		PLL1708	Half f_S	16	22.05	24	
			Standard f_S	32	44.1	48	
			Double f_S	64	88.2	96	
MASTER CLOCK (MCKO1, MCKO2) CHARACTERISTICS (f_M = 27 MHz, C_1 = C_2 = 15 pF, C_L = 20 pF on measurement pin)							
	Master clock frequency			26.73	27	27.27	MHz
V_{IH}	Input level(3)			0.7 V_{CC}			V
V_{IL}						0.3 V_{CC}	
I_{IH}	Input current(3)		V_{IN} = V_{CC}			±10	μA
I_{IL}			V_{IN} = 0 V			±10	
	Output voltage (4)				3.5		Vp-p
	Output rise time		20% to 80% of V_{DD}		2.0		ns
	Output fall time		80% to 20% of V_{DD}		2.0		ns
	Duty cycle		For crystal oscillation	45%	51%	55%	
			For external clock		50%		
	Clock jitter (5)				50		ps
	Power-up time (6)				0.5	1.5	ms
PLL AC CHARACTERISTICS (SCKO0–SCKO3) (f_M = 27 MHz, C_L = 20 pF on measurement pin)							
SCKO0	Output system clock frequency	PLL1707	Fixed		33.8688		MHz
SCKO1			Selectable for 48 kHz	24.576		36.864	
SCKO2			256 f_S	8.192	12.288	24.576	
SCKO3			384 f_S	12.288	18.432	36.864	
SCKO0		PLL1708	Fixed		33.8688		
SCKO1			Selectable for 48 kHz	12.288	24.576	36.864	
SCKO2			256 f_S	4.096	12.288	24.576	
SCKO3			384 f_S	6.144	18.432	36.864	
	Output rise time		20% to 80% of V_{DD}		2.0		ns
	Output fall time		80% to 20% of V_{DD}		2.0		ns
	Output duty cycle			45	50	55	%

(1) Pins 5, 6, 7, 12: FS1/MD, FS2/MC, SR/MS, CSEL (Schmitt-trigger input with internal pulldown, 3.3-V tolerant)

(2) Pins 2, 3, 14, 15, 18, 19: SCKO2, SCKO3, MCKO1, MCKO2, SCKO0, SCKO1

(3) Pin 10: XT1

(4) Pin 11: XT2

(5) Jitter performance is specified as standard deviation of jitter for 27-MHz crystal oscillation and default SCKO frequency setting. Jitter performance varies with master clock mode, SCKO frequency setting and load capacitance on each clock output.

(6) The delay time from power on to oscillation

(7) The settling time when the sampling frequency is changed

(8) The delay time from power on to lockup

(9) f_M = 27-MHz crystal oscillation, no load on MCKO1, MCKO2, SCKO0, SCKO1, SCKO2, SCKO3. Power supply current varies with sampling frequency selection and load condition.

(10) While all bits of CE[6:1] are 0, the PLL1708 goes into power-down mode.

ELECTRICAL CHARACTERISTICS (continued)

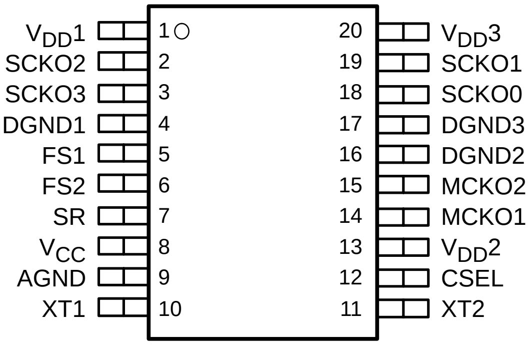
all specifications at T_A = 25°C, $V_{DD}1$–$V_{DD}3$ (= V_{DD}) = V_{CC} = 3.3 V, f_M = 27 MHz, crystal oscillation, f_S = 48 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output clock jitter (5)	SCKO0, SCKO1		58	100	ps
		SCKO2, SCKO3		50	100	ps
	Frequency Settling Time(7)	PLL1707, to stated output frequency		50	150	ns
		PLL1708, to stated output frequency		80	300	
	Power-up time (8)	To stated output frequency		3	6	ms
POWER SUPPLY REQUIREMENTS						
V_{CC}, V_{DD}	Supply voltage range		2.7	3.3	3.6	Vdc
$I_{DD} + I_{CC}$	Supply current (9)	$V_{DD} = V_{CC}$ = 3.3 V, f_S = 48 kHz		19	25	mA
		Power down(10)		350	550	µA
	Power dissipation	$V_{DD} = V_{CC}$ = 3.3 V, f_S = 48 kHz		63	90	mW
TEMPERATURE RANGE						
	Operating temperature		–25		85	°C
θ_{JA}	Thermal resistance	PLL1707/8DBQ: 20-pin SSOP (150 mil)		150		°C/W

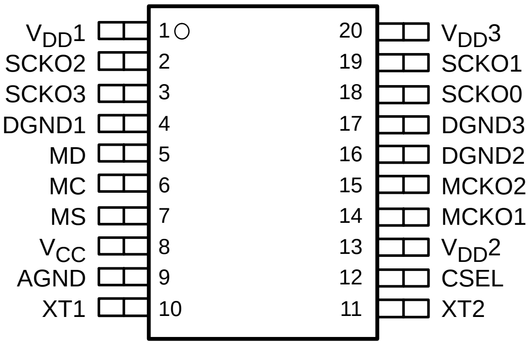
(1) Pins 5, 6, 7, 12: FS1/MD, FS2/MC, SR/MS, CSEL (Schmitt-trigger input with internal pulldown, 3.3-V tolerant)
(2) Pins 2, 3, 14, 15, 18, 19: SCKO2, SCKO3, MCKO1, MCKO2, SCKO0, SCKO1
(3) Pin 10: XT1
(4) Pin 11: XT2
(5) Jitter performance is specified as standard deviation of jitter for 27-MHz crystal oscillation and default SCKO frequency setting. Jitter performance varies with master clock mode, SCKO frequency setting and load capacitance on each clock output.
(6) The delay time from power on to oscillation
(7) The settling time when the sampling frequency is changed
(8) The delay time from power on to lockup
(9) f_M = 27-MHz crystal oscillation, no load on MCKO1, MCKO2, SCKO0, SCKO1, SCKO2, SCKO3. Power supply current varies with sampling frequency selection and load condition.
(10) While all bits of CE[6:1] are 0, the PLL1708 goes into power-down mode.

PIN ASSIGNMENTS

PLL1707
(TOP VIEW)


$V_{DD}1$ 1 ○ 20 $V_{DD}3$
SCKO2 2 19 SCKO1
SCKO3 3 18 SCKO0
DGND1 4 17 DGND3
FS1 5 16 DGND2
FS2 6 15 MCKO2
SR 7 14 MCKO1
V_{CC} 8 13 $V_{DD}2$
AGND 9 12 CSEL
XT1 10 11 XT2

PLL1708
(TOP VIEW)


$V_{DD}1$ 1 ○ 20 $V_{DD}3$
SCKO2 2 19 SCKO1
SCKO3 3 18 SCKO0
DGND1 4 17 DGND3
MD 5 16 DGND2
MC 6 15 MCKO2
MS 7 14 MCKO1
V_{CC} 8 13 $V_{DD}2$
AGND 9 12 CSEL
XT1 10 11 XT2

PLL1707 Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	9	–	Analog ground
CSEL	12	I	SCKO1 frequency selection control(1)
DGND1	4	–	Digital ground 1
DGND2	16	–	Digital ground 2
DGND3	17	–	Digital ground 3
FS1	5	I	Sampling frequency group control 1(1)
FS2	6	I	Sampling frequency group control 2(1)
MCKO1	14	O	27-MHz master clock output 1
MCKO2	15	O	27-MHz master clock output 2
SCKO0	18	O	System clock output 0 (33.8688 MHz fixed)
SCKO1	19	O	System clock output 1 (selectable for 48 kHz)
SCKO2	2	O	System clock output 2 (256 f_S selectable)
SCKO3	3	O	System clock output 3 (384 f_S selectable)
SR	7	I	Sampling rate control(1)
V_{CC}	8	–	Analog power supply, 3.3 V
$V_{DD}1$	1	–	Digital power supply 1, 3.3 V
$V_{DD}2$	13	–	Digital power supply 2, 3.3 V
$V_{DD}3$	20	–	Digital power supply 3, 3.3 V
XT1	10	I	27-MHz crystal oscillator, or external clock input
XT2	11	O	27-MHz crystal oscillator, must be OPEN for external clock input mode

(1) Schmitt-trigger input with internal pulldown.

PLL1708 Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	9	–	Analog ground
CSEL	12	I	SCKO1 frequency selection control(1)
DGND1	4	–	Digital ground 1
DGND2	16	–	Digital ground 2
DGND3	17	–	Digital ground 3
MC	6	I	Bit clock input for serial control(1)
MCKO1	14	O	27-MHz master clock output 1
MCKO2	15	O	27-MHz master clock output 2
MD	5	I	Data input for serial control(1)
MS	7	I	Chip select input for serial control(1)
SCKO0	18	O	System clock output 0 (33.8688 MHz fixed)
SCKO1	19	O	System clock output 1 (selectable for 48 kHz)
SCKO2	2	O	System clock output 2 (256 f_S selectable)
SCKO3	3	O	System clock output 3 (384 f_S selectable)
V_{CC}	8	–	Analog power supply, 3.3 V
$V_{DD}1$	1	–	Digital power supply 1, 3.3 V
$V_{DD}2$	13	–	Digital power supply 2, 3.3 V
$V_{DD}3$	20	–	Digital power supply 3, 3.3 V
XT1	10	I	27-MHz crystal oscillator, or external clock input
XT2	11	O	27-MHz crystal oscillator, must be OPEN for external clock input mode

(1) Schmitt-trigger input with internal pulldown.

TYPICAL PERFORMANCE CURVES

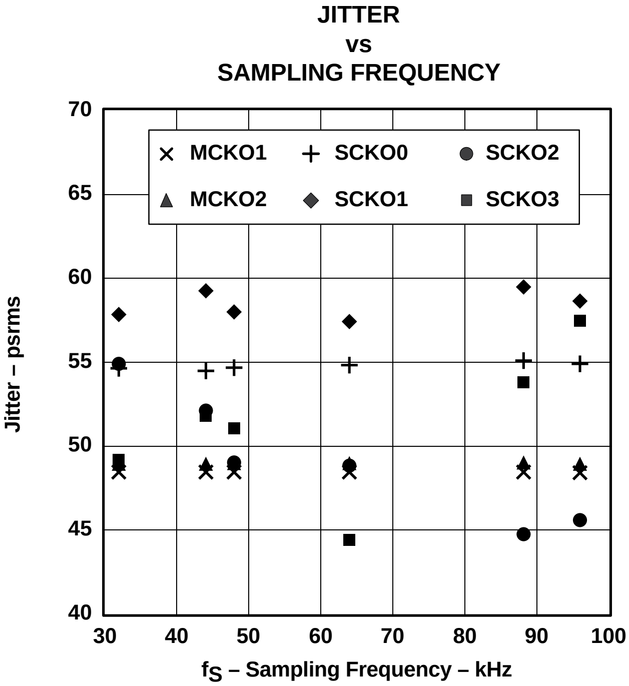


Figure 1

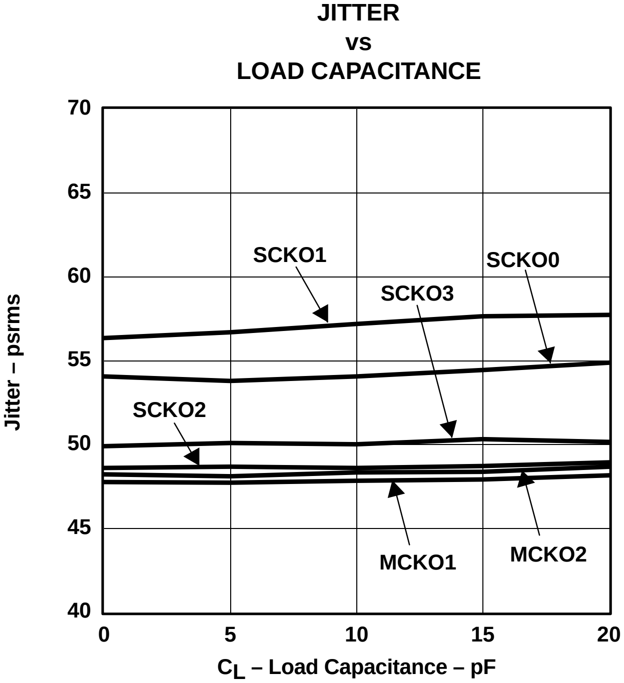


Figure 2

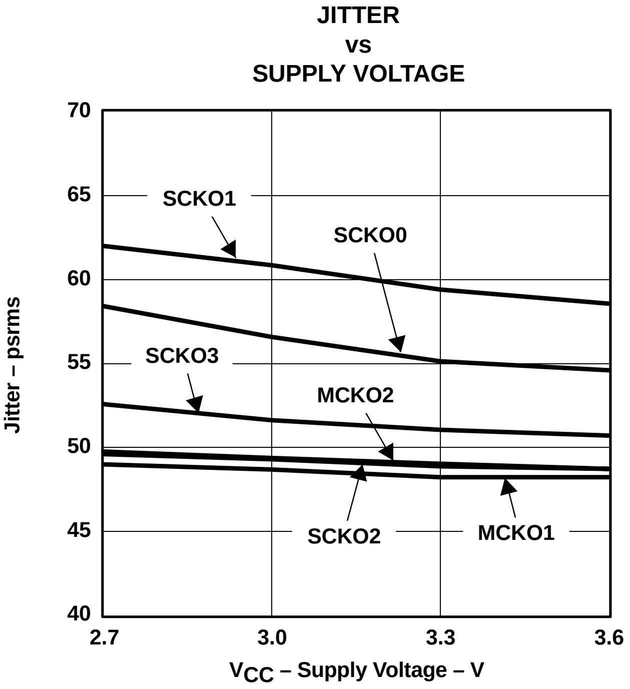


Figure 3

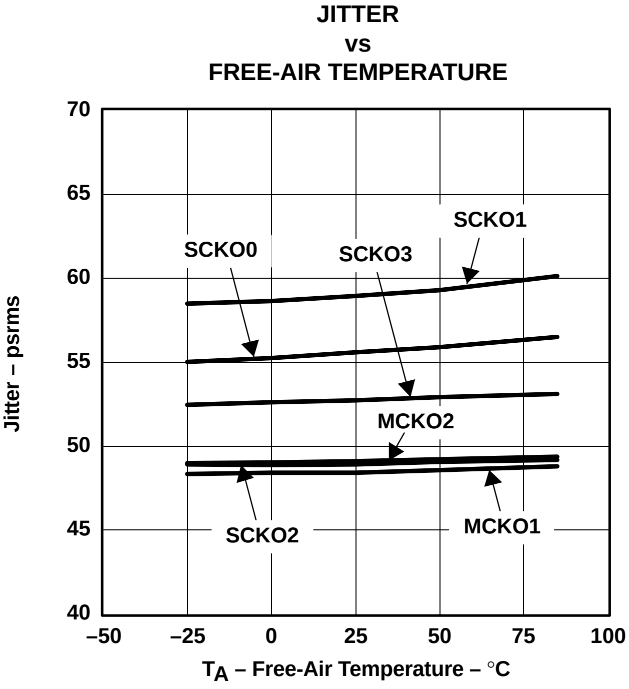


Figure 4

NOTE: All specifications at T_A = 25°C, $V_{DD}1–3$ (= V_{DD}) = V_{CC} = +3.3 V, f_M = 27 MHz, crystal oscillation, C_1, C_2 = 15 pF, default frequency (33.8688 MHz for SCKO0, 36.864 MHz for SCKO1, 256 f_S and 384 f_S of 48 kHz for SCKO2 and SCKO3), C_L = 20 pF on measurement pin, unless otherwise noted.

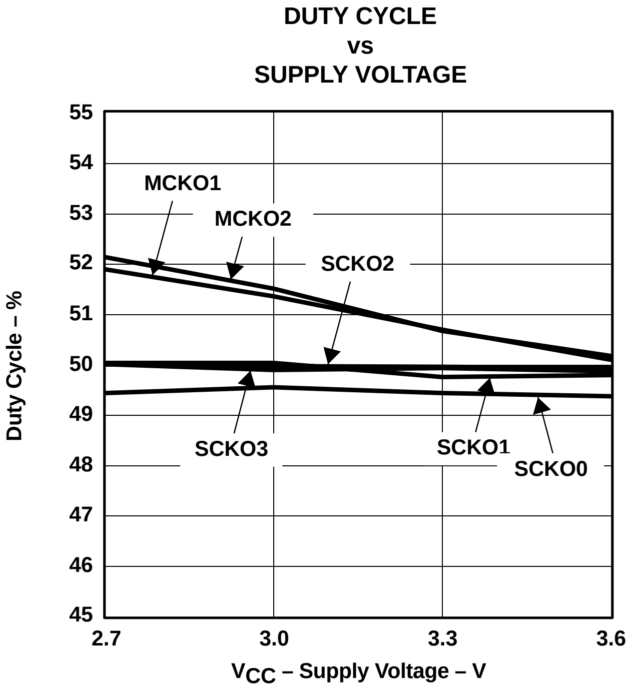


Figure 5

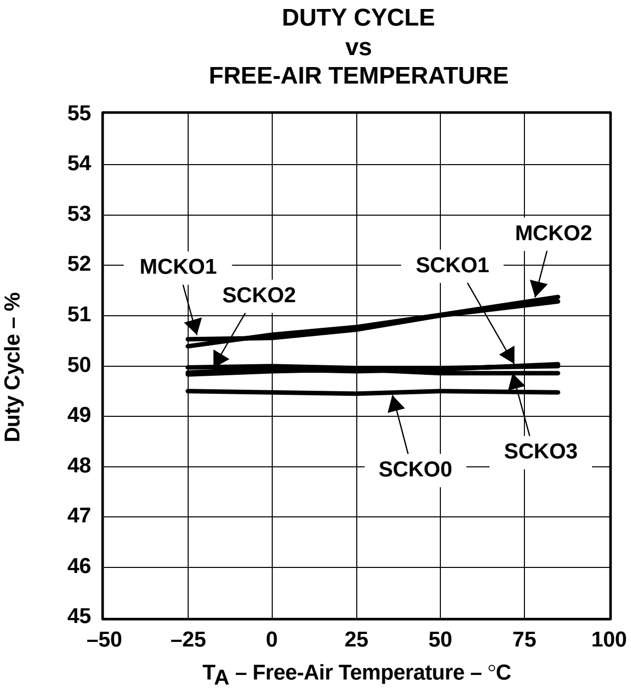


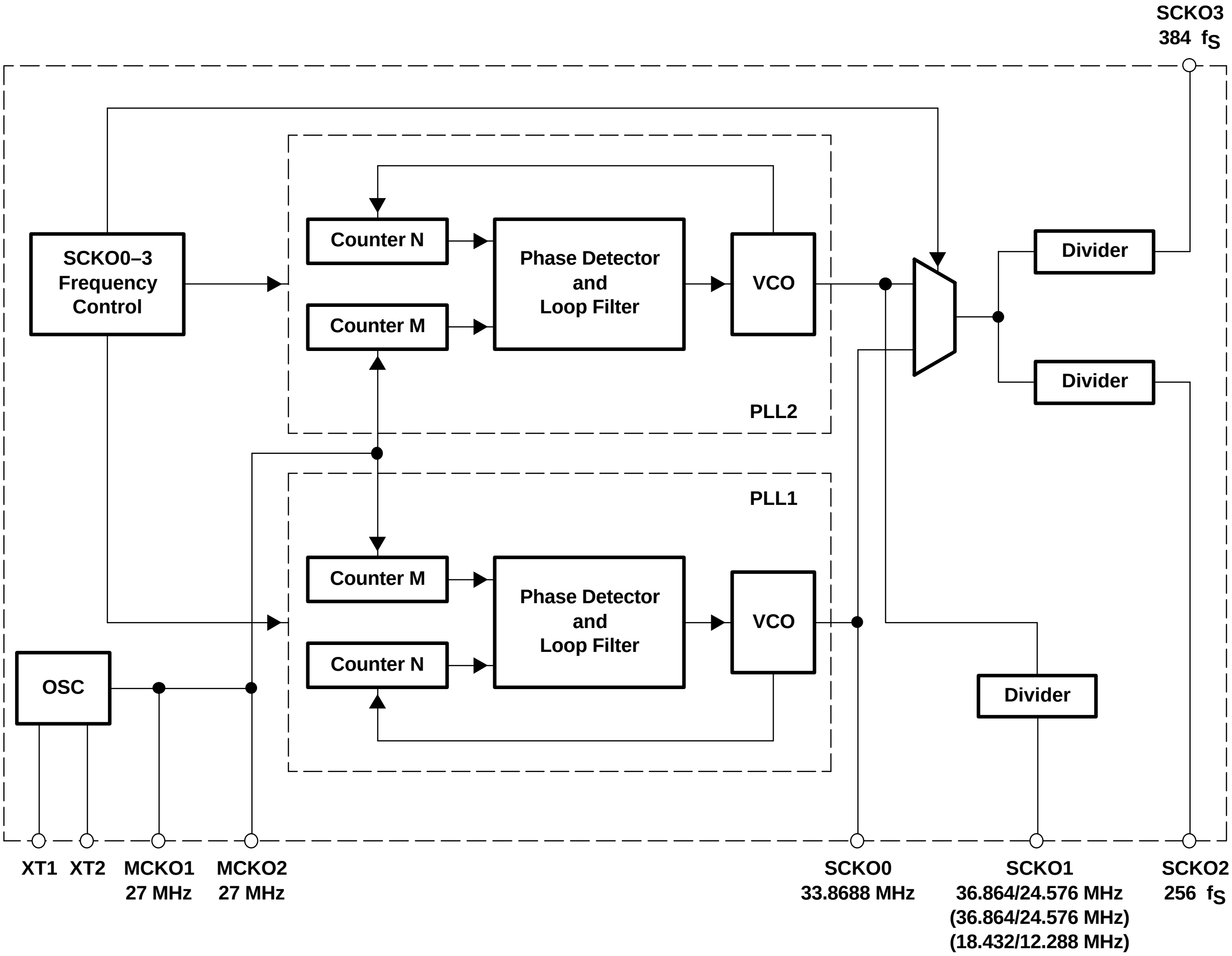
Figure 6

NOTE: All specifications at T_A = 25°C, V_{DD}1–3 (= V_{DD}) = V_{CC} = +3.3 V, f_M = 27 MHz, crystal oscillation, C_1, C_2 = 15 pF, default frequency (33.8688 MHz for SCKO0, 36.864 MHz for SCKO1, 256 f_S and 384 f_S of 48 kHz for SCKO2 and SCKO3), C_L = 20 pF on measurement pin, unless otherwise noted.

THEORY OF OPERATION

MASTER CLOCK AND SYSTEM CLOCK OUTPUT

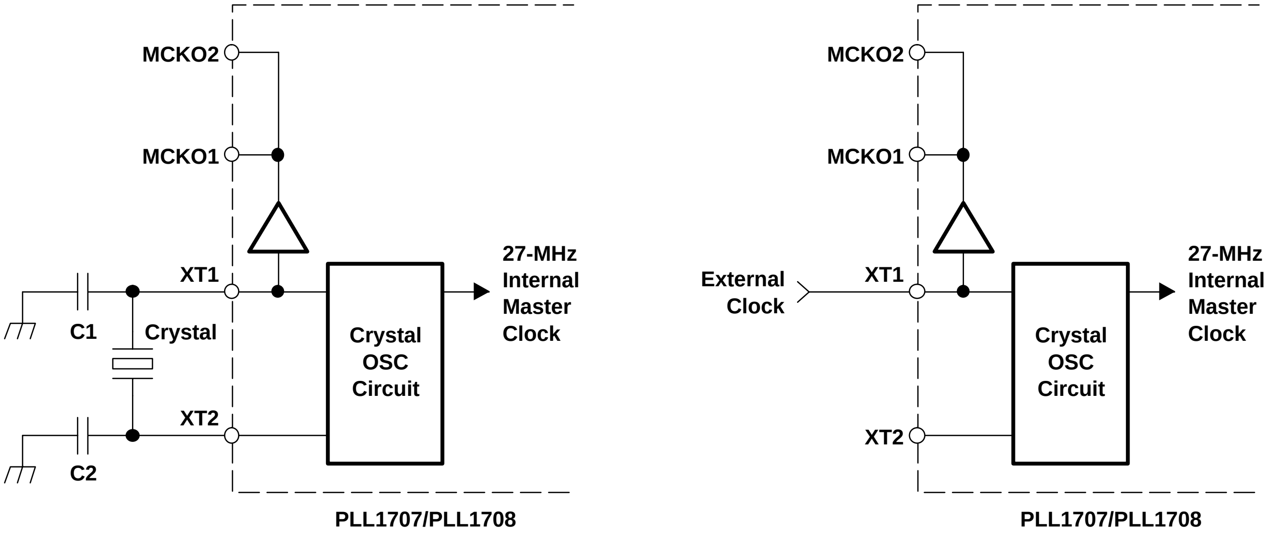
The PLL1707/8 consists of a dual PLL clock and master clock generator which generates four system clocks and two buffered 27-MHz clocks from a 27-MHz master clock. Figure 7 shows the block diagram of the PLL1707/8. The PLL is designed to accept a 27-MHz master clock.


SCKO3
384 fS
SCKO0–3 Frequency Control
Counter N
Counter M
Phase Detector and Loop Filter
VCO
PLL2
PLL1
Counter M
Counter N
Phase Detector and Loop Filter
VCO
Divider
Divider
Divider
OSC
XT1
XT2
MCKO1 27 MHz
MCKO2 27 MHz
SCKO0 33.8688 MHz
SCKO1 36.864/24.576 MHz (36.864/24.576 MHz) (18.432/12.288 MHz)
SCKO2 256 fS

( ): PLL1708

Figure 7. Block Diagram

The master clock can be either a crystal oscillator placed between XT1 (pin 10) and XT2 (pin 11), or an external input to XT1. If an external master clock is used, XT2 must be open. Figure 8 illustrates possible system clock connection options, and Figure 9 illustrates the 27-MHz master clock timing requirement.

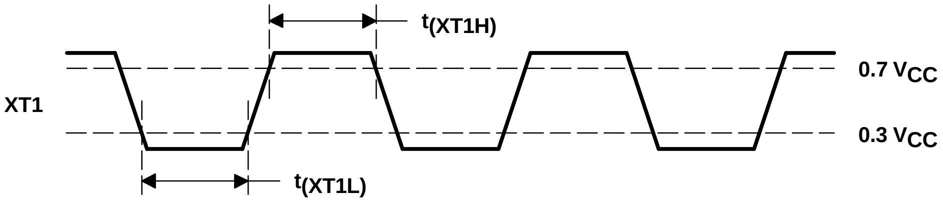

MCKO2
MCKO1
XT1
C1
Crystal
XT2
C2
Crystal OSC Circuit
27-MHz Internal Master Clock
PLL1707/PLL1708
MCKO2
MCKO1
External Clock
XT1
XT2
Crystal OSC Circuit
27-MHz Internal Master Clock
PLL1707/PLL1708

C1, C2 = 10 pF to 33 pF

Crystal Resonator Connection

External Clock Input Connection

Figure 8. Master Clock Generator Connection Diagram


$t_{(XT1H)}$
XT1
0.7 V_{CC}
0.3 V_{CC}
$t_{(XT1L)}$

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
Master clock pulse duration HIGH	$t_{(XT1H)}$	10		ns
Master clock pulse duration LOW	$t_{(XT1L)}$	10		ns

Figure 9. External Master Clock Timing Requirement

The PLL1707/8 provides a very low-jitter, high-accuracy clock. SCKO0 outputs a fixed 33.8688-MHz clock, SCKO1 outputs 256 $f_{S,}$ 384 f_S 512 $f_{S,}$ or 768 f_S (f_S = 48 kHz) which is selected by hardware or software control. The output frequency of the remaining clocks is determined by the sampling frequency (f_S) under hardware or software control. SCKO2 and SCKO3 output 256-f_S and 384-f_S system clocks, respectively. Table 2 shows each sampling frequency which can be programmed. The system clock output frequencies for programmed sampling frequencies are shown in Table 3. The half sampling frequencies on SCKO2 and SCKO3 and 256 f_S and 384 f_S on SCKO1 are supported only on the PLL1708.

Table 1. Generated System Clock SCKO1 Frequency

f_S	SCKO1 FREQUENCY
256 f_S[†]	12.288 MHz
384 f_S[†]	18.432 MHz
512 f_S	24.576 MHz
768 f_S	36.864 MHz

[†] PLL1708 only

Table 2. Sampling Frequencies

SAMPLING RATE	SAMPLING FREQUENCY (kHz)		
Half sampling frequencies†	16	22.05	24
Standard sampling frequencies	32	44.1	48
Double sampling frequencies	64	88.2	96

† PLL1708 only

Table 3. Sampling Frequencies and System Clock Output Frequencies

SAMPLING FREQUENCY (kHz)	SAMPLING RATE	256 f_S SCKO2 (MHZ)	384 f_S SCKO3 (MHZ)
16†	Half	4.096	6.144
22.05†	Half	5.6448	8.4672
24†	Half	6.144	9.216
32	Standard	8.192	12.288
44.1	Standard	11.2896	16.9344
48	Standard	12.288	18.432
64	Double	16.384	24.576
88.2	Double	22.5792	33.8688
96	Double	24.576	36.864

† PLL1708 only

Response time from power on (or applying the clock to XT1) to SCKO settling time is typically 3 ms. Delay time from sampling frequency change to SCKO settling is 300 ns maximum. Figure 10 illustrates SCKO transient timing in the PLL1708.

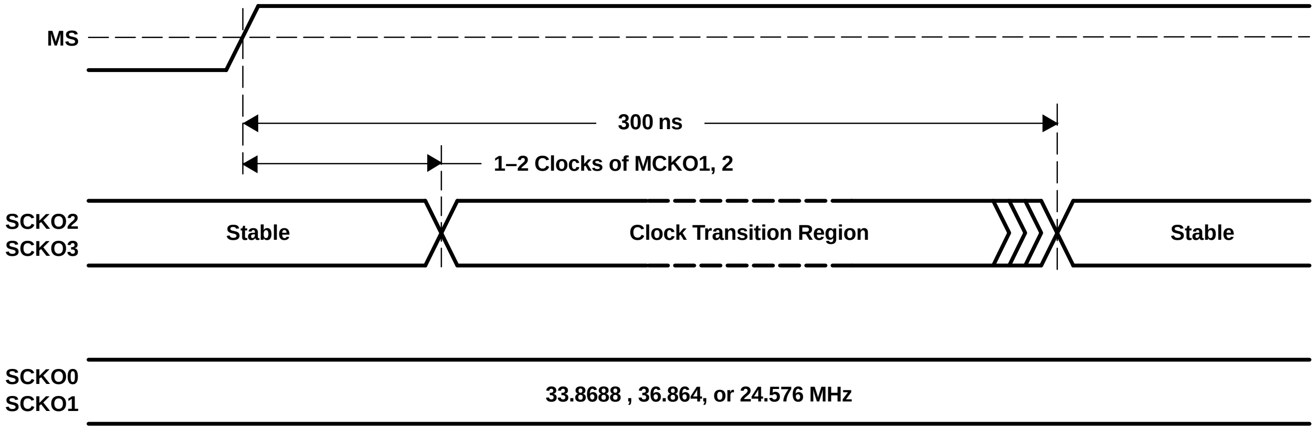


Figure 10. System Clock Transient Timing

The delay time for hardware control to use SR, FS2, FS1, or CSEL is 150 ns maximum. Figure 11 illustrates SCKO transient timing in the PLL1707. Clock transient timing is not synchronized with the SCKOs. External buffers are recommended on all output clocks in order to avoid degrading the jitter performance of the PLL1707/8.

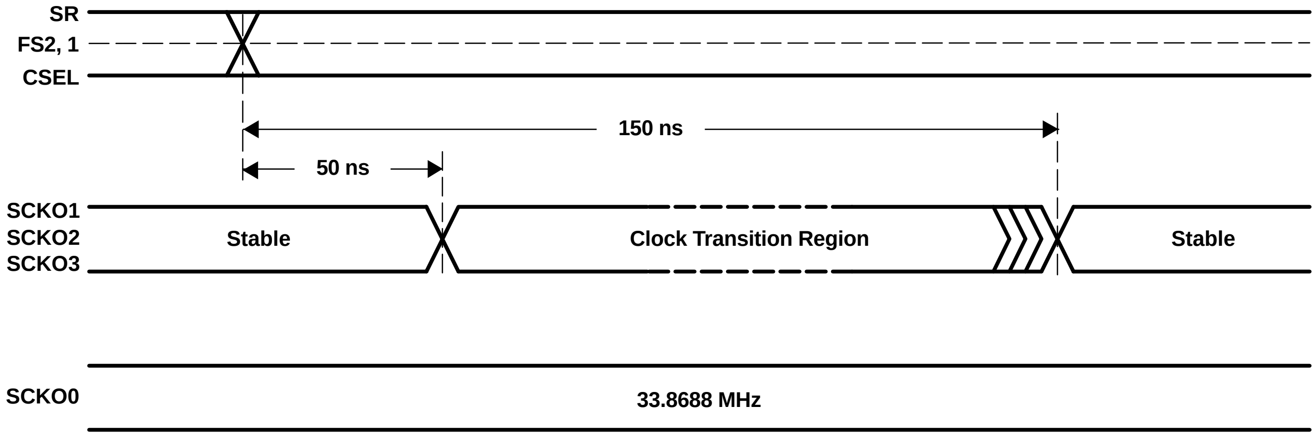

SR
FS2, 1
CSEL
150 ns
50 ns
SCKO1
SCKO2
SCKO3
Stable
Clock Transition Region
Stable
SCKO0
33.8688 MHz

Figure 11. SCKO Transient Timing

POWER-ON RESET

The PLL1707/8 has an internal power-on reset circuit. The mode register of the PLL1708 is initialized with default settings by power-on reset. Throughout the reset period, all clock outputs are enabled with the default settings after power-up time. Initialization by internal power-on reset is done automatically during 1024 master clocks at V_{DD} > 2.0 V (TYP). Power-on reset timing is shown in Figure 12.

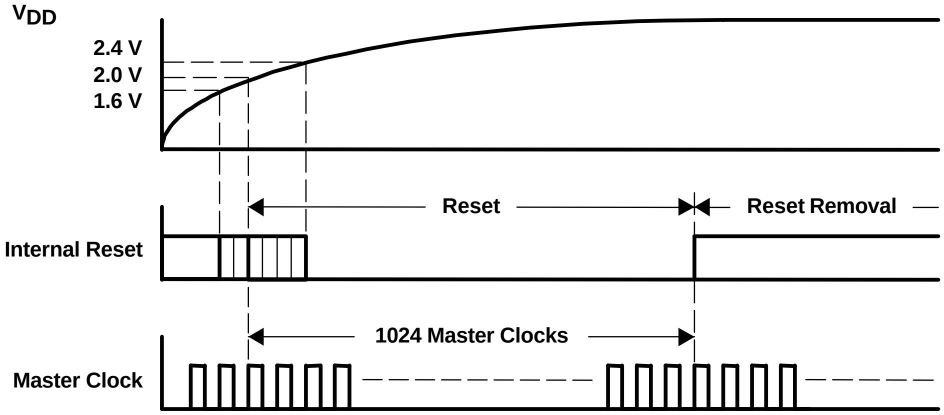

V_{DD}
2.4 V
2.0 V
1.6 V
Reset
Reset Removal
Internal Reset
1024 Master Clocks
Master Clock

Figure 12. Power-On Reset Timing

FUNCTION CONTROL

The built-in functions of the PLL1707 can be controlled in the parallel mode (hardware mode), which uses SR (pin 7), FS1 (pin 5) and FS2 (pin 6). The PLL1708 can be controlled in the serial mode (software mode), which has a three-wire interface using MS (pin 7), MC (pin 6), and MD (pin 5). The selectable functions are shown in Table 4.

Table 4. Selectable Functions

SELECTABLE FUNCTION	PARALLEL MODE	SERIAL MODE
Sampling frequency select (32 kHz, 44.1 kHz, 48 kHz)	Yes	Yes
Sampling rate select (standard/double)	Yes	Yes
Sampling rate select (half)	No	Yes
Each clock output enable/disable	No	Yes
Power down	No	Yes
SCKO1 configuration	No	Yes

PLL1707 (Parallel Mode)

In the parallel mode, the following functions can be selected:

Sampling Frequency Group Select

The sampling frequency group can be selected by FS1 (pin 5) and FS2 (pin 6).

FS2 (PIN 6)	FS1 (PIN 5)	SAMPLING FREQUENCY
LOW	LOW	48 kHz
LOW	HIGH	44.1 kHz
HIGH	LOW	32 kHz
HIGH	HIGH	Reserved

Sampling Rate Select

The sampling rate can be selected by SR (pin 7)

SR (PIN 7)	SAMPLING RATE
LOW	Standard
HIGH	Double

System Clock SCKO1 Frequency Select

System clock SCKO1 frequency can be selected by CSEL (pin 12).

CSEL (PIN 12)	SCKO1 FREQUENCY
LOW	36.864 MHz
HIGH	24.576 MHz

PLL1708 (Serial Mode)

The built-in functions of the PLL1708 are shown in Table 5. These functions are controlled using the MS, MC, and MD serial control signals.

Table 5. Selectable Functions

SELECTABLE FUNCTION	DEFAULT
Sampling frequency select (32 kHz, 44.1 kHz, 48 kHz)	48-kHz group
Sampling rate select (half, standard, double)	Standard
Each clock output enable/disable	Enabled
Power down	Disabled
SCKO1 configuration	36.864 MHz, 24.576 MHz

Program-Register Bit Mapping

The built-in functions of the PLL1708 are controlled through a 16-bit program register. This register is loaded using MD, MC and MS. After the 16 data bits are clocked in using the rising edge of MC, MS is used to latch the data into the register. Table 6 shows the bit mapping of the register. The serial mode control format and control data input timing are shown in Figure 13 and Figure 14, respectively.

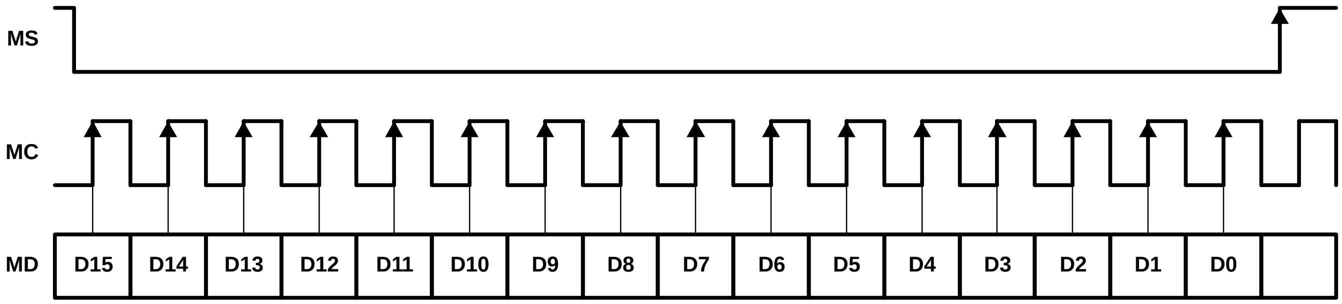
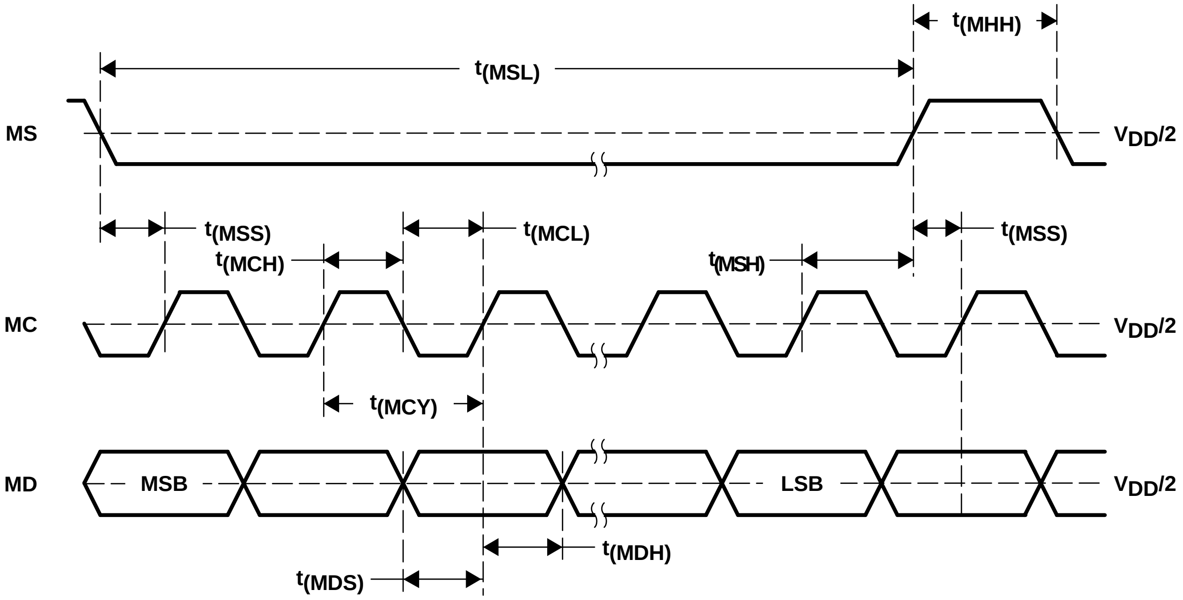

MS
MC
MD
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0

Figure 13. Serial Mode Control Format


t(MHH)
t(MSL)
MS
VDD/2
t(MSS)
t(MCL)
t(MCH)
t(MSH)
t(MSS)
MC
VDD/2
t(MCY)
MD
MSB
LSB
VDD/2
t(MDH)
t(MDS)

DESCRIPTION	SYMBOL	MIN	TYP	MAX	UNIT
MC pulse cycle time	$t_{(MCY)}$	100			ns
MC pulse duration LOW	$t_{(MCL)}$	40			ns
MC pulse duration HIGH	$t_{(MCH)}$	40			ns
MD hold time	$t_{(MDH)}$	40			ns
MD setup time	$t_{(MDS)}$	40			ns
MS low-level time	$t_{(MSL)}$	16			MC clocks(1)
MS high-level time	$t_{(MHH)}$	200			ns
MS hold time(2)	$t_{(MSH)}$	40			ns
MS setup time(3)	$t_{(MSS)}$	40			ns

(1) MC clocks: MC clock period
(2) MC rising edge for LSB to MS rising edge
(3) MS rising edge to the next MC rising edge. If the MC clock is stopped after the LSB, any MS rise time is accepted.

Figure 14. Control Data Input Timing

Mode Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	0	CE6	CE5	CE4	CE3	CE2	CE1	SR2	SR1	FS2	FS1

Table 6. Mode Register Mapping

REGISTER	BIT NAME	DESCRIPTION
Mode control	CE6	MCKO2 output enable/disable
	CE5	MCKO1 output enable/disable
	CE4	SCKO1 output enable/disable
	CE3	SCKO3 output enable/disable
	CE2	SCKO2 output enable/disable
	CE1	SCKO0 output enable/disable
	SR[2:1]	Sampling rate select
	FS[2:1]	Sampling frequency select

FS[2:1]: Sampling Frequency Group Select

FS2	FS1	SAMPLING FREQUENCY
0	0	48 kHz (default)
0	1	44.1 kHz
1	0	32 kHz
1	1	Reserved

SR[2:1]: Sampling Rate Select

SR2	SR1	SAMPLING RATE
0	0	Standard (default)
0	1	Double
1	0	Half
1	1	Reserved

CE [6:1]: Clock Output Control

CE1–CE6	CLOCK OUTPUT CONTROL
0	Clock output disable
1	Clock output enable (default)

While all the bits of CE [6:1] are 0, the PLL1708 goes into the power-down mode, all dynamic operation including PLLs and the oscillator halts, but serial mode control is enabled for resumption.

Configuration Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	1	1	RSV	RSV	RSV	RSV	RSV	CFG1	RSV	RSV	RSV	RSV

Table 7. Configuration Register Mapping

REGISTER	BIT NAME	DESCRIPTION
Configuration	RSV	Reserved, must be 0
	CFG1	SCKO1 configuration

CFG1: SCKO1 Configuration Control

CFG1	CONFIGURATION 1
0	36.864 MHz, 24.576 MHz for SCKO1 (default)
1	18.432 MHz, 12.288 MHz for SCKO1

The system clock SCKO1 frequency can be selected by CSEL (pin 12) and CFG1 (register).

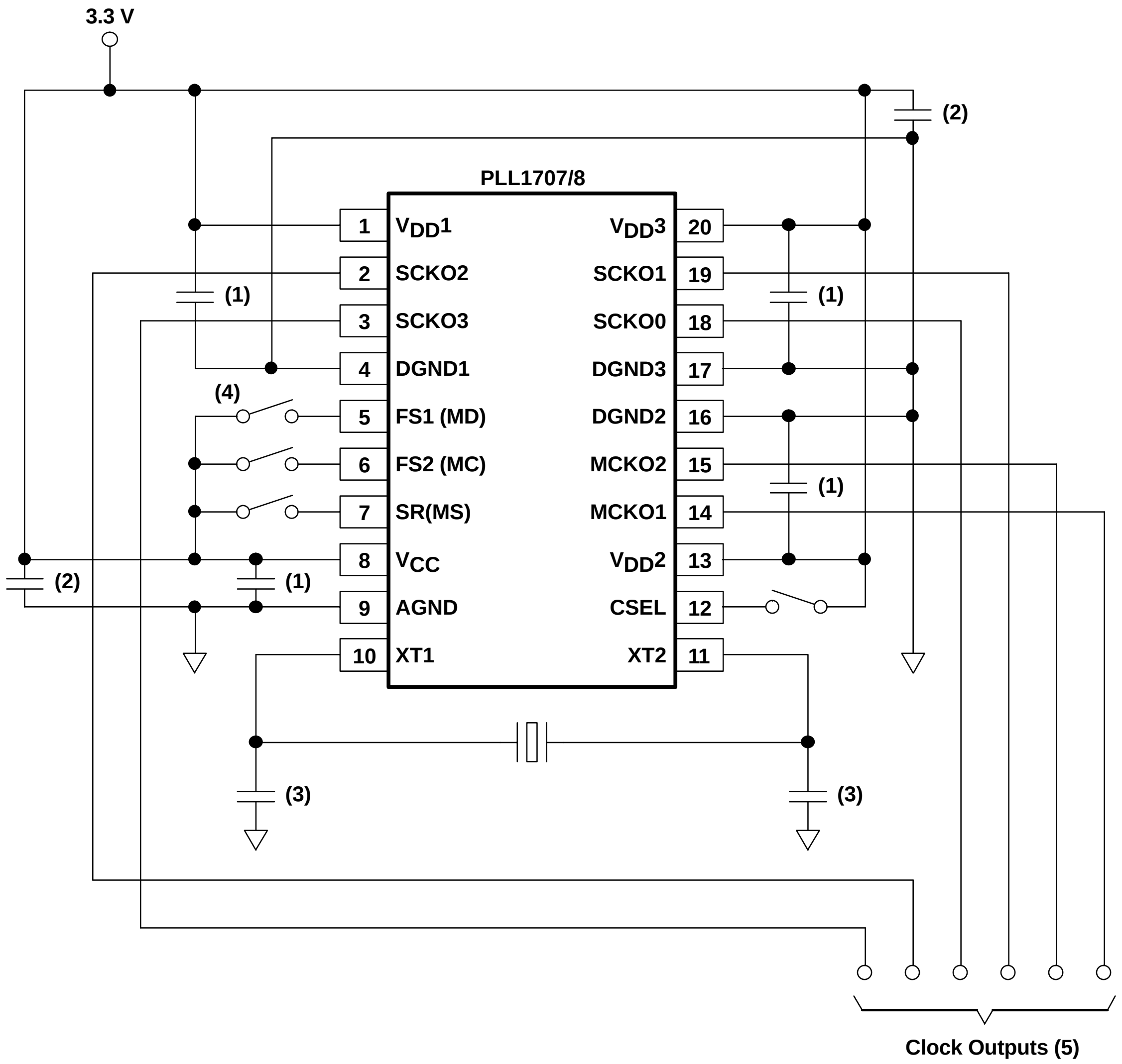
CFG1 (REGISTER)	CSEL (PIN 12)	SCKO1
0	LOW	36.864 MHz
0	HIGH	24.576 MHz
1	LOW	18.432 MHz
1	HIGH	12.288 MHz

CONNECTION DIAGRAM

Figure 15 shows the typical connection circuit for the PLL1707. There are four grounds for digital and analog power supplies. However, the use of one common ground connection is recommended to avoid latch-up or other power-supply-related troubles. Power supplies should be bypassed as close as possible to the device.

MPEG-2 APPLICATIONS

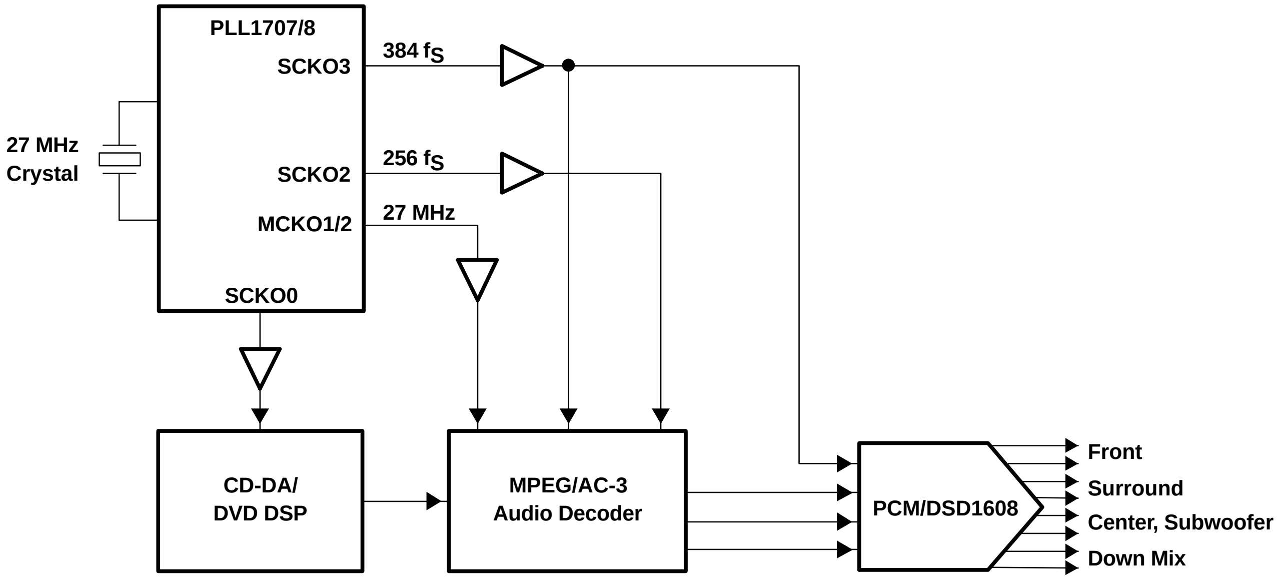
Typical applications for the PLL1707/8 are MPEG-2 based systems such as DVD recorders, HDD recorders, DVD players, DVD add-on cards for multimedia PCs, digital HDTV systems, and set-top boxes. The PLL1707/8 provides audio system clocks for a CD-DA DSP, DVD DSP, Karaoke DSP, ADC(s), and DAC(s) from a 27-MHz video clock.


3.3 V
(2)
PLL1707/8
1 VDD1
2 SCKO2
3 SCKO3
4 DGND1
5 FS1 (MD)
6 FS2 (MC)
7 SR(MS)
8 VCC
9 AGND
10 XT1
20 VDD3
19 SCKO1
18 SCKO0
17 DGND3
16 DGND2
15 MCKO2
14 MCKO1
13 VDD2
12 CSEL
11 XT2
(1)
(4)
(3)
Clock Outputs (5)

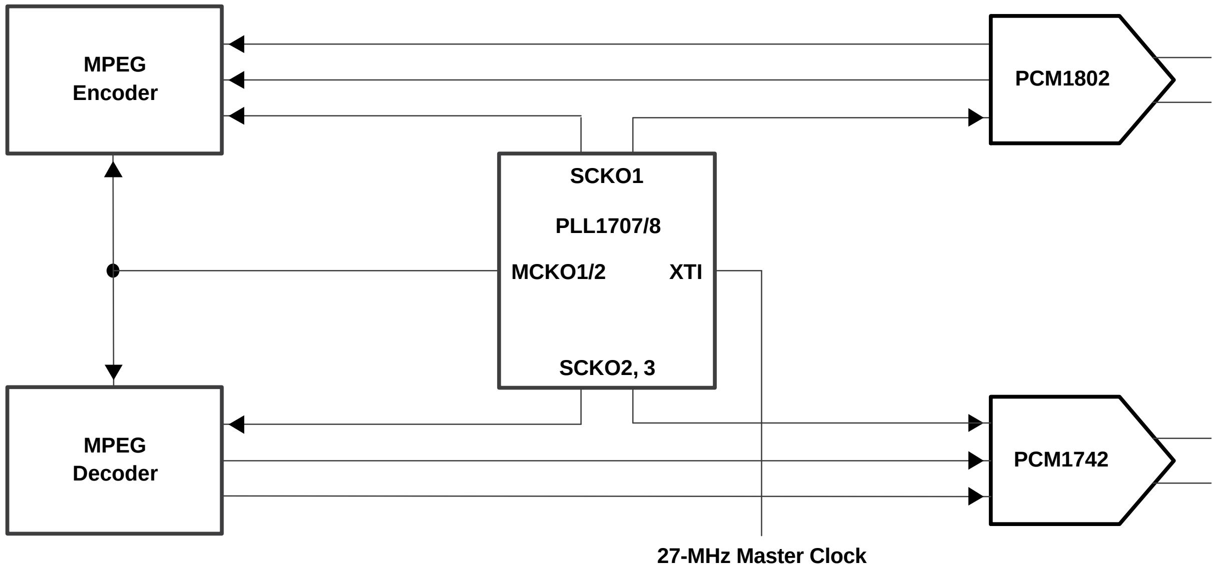
(1) 0.1-µF ceramic capacitor typical, depending on quality of power supply and pattern layout
(2) 10-µF aluminum electrolytic capacitor typical, depending on quality of power supply and pattern layout
(3) 27-MHz quartz crystal and 10–33 pF × 2 ceramic capacitors, which generate the appropriate amplitude of oscillation on XT1/XT2
(4) This connection is for PLL1707 (parallel mode); when PLL1708 (serial mode) is to be used, control pins must be connected to serial interfaced controller.
(5) For good jitter performance, minimize the load capacitance on the clock output. It is recommended to drive the clock outputs through buffers, especially if there are heavy loads on SCKO0 and SCKO1, and to minimize mutual interference by separating them or inserting a guard pattern between them.

Figure 15. Typical Connection Diagram

BLOCK DIAGRAM OF DVD PLAYER APPLICATION


PLL1707/8
SCKO3
SCKO2
MCKO1/2
SCKO0
27 MHz
Crystal
384 fS
256 fS
27 MHz
CD-DA/
DVD DSP
MPEG/AC-3
Audio Decoder
PCM/DSD1608
Front
Surround
Center, Subwoofer
Down Mix

BLOCK DIAGRAM OF HDD+DVD RECORDER APPLICATION


MPEG
Encoder
PCM1802
SCKO1
PLL1707/8
MCKO1/2
XTI
SCKO2, 3
MPEG
Decoder
PCM1742
27-MHz Master Clock

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PLL1707DBQ	ACTIVE	SSOP	DBQ	20	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PLL1707	Samples
PLL1707DBQG4	ACTIVE	SSOP	DBQ	20	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PLL1707	Samples
PLL1707DBQR	ACTIVE	SSOP	DBQ	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PLL1707	Samples
PLL1707DBQRG4	ACTIVE	SSOP	DBQ	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PLL1707	Samples
PLL1708DBQ	ACTIVE	SSOP	DBQ	20	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PLL1708	Samples
PLL1708DBQG4	ACTIVE	SSOP	DBQ	20	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PLL1708	Samples
PLL1708DBQR	ACTIVE	SSOP	DBQ	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PLL1708	Samples
PLL1708DBQRG4	ACTIVE	SSOP	DBQ	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PLL1708	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF PLL1707 :

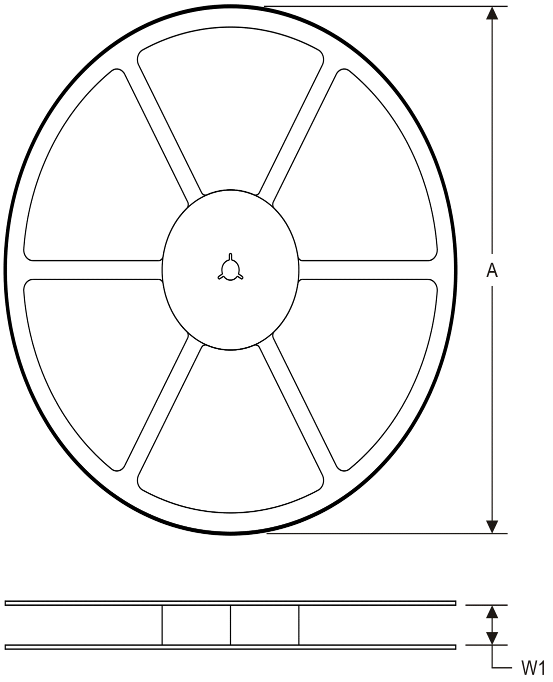
- Automotive: PLL1707-Q1

NOTE: Qualified Version Definitions:

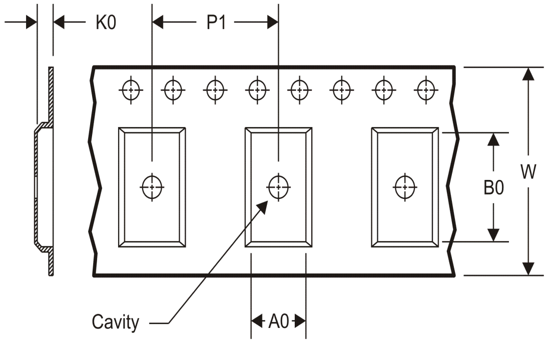
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



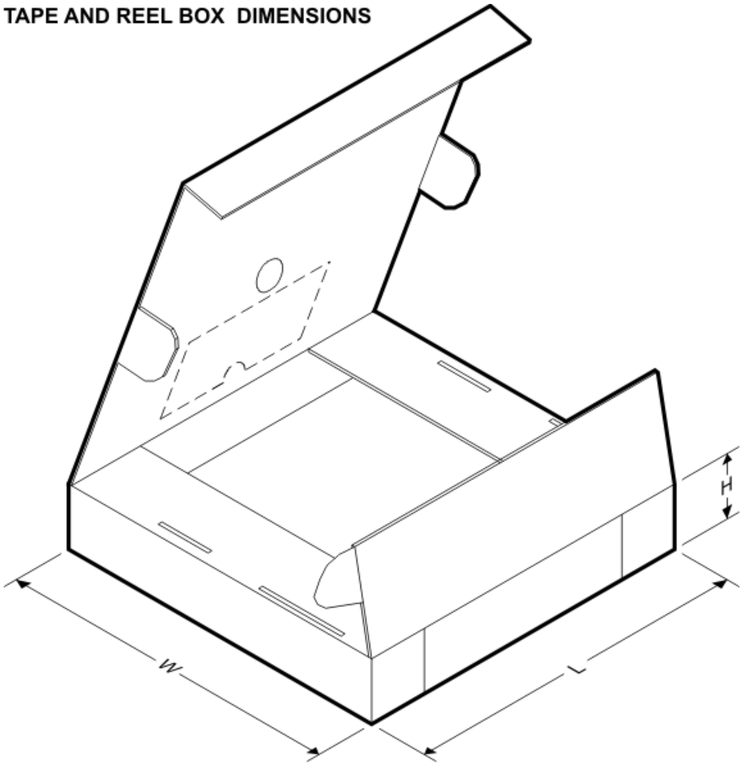
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PLL1707DBQR	SSOP	DBQ	20	2000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
PLL1708DBQR	SSOP	DBQ	20	2000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

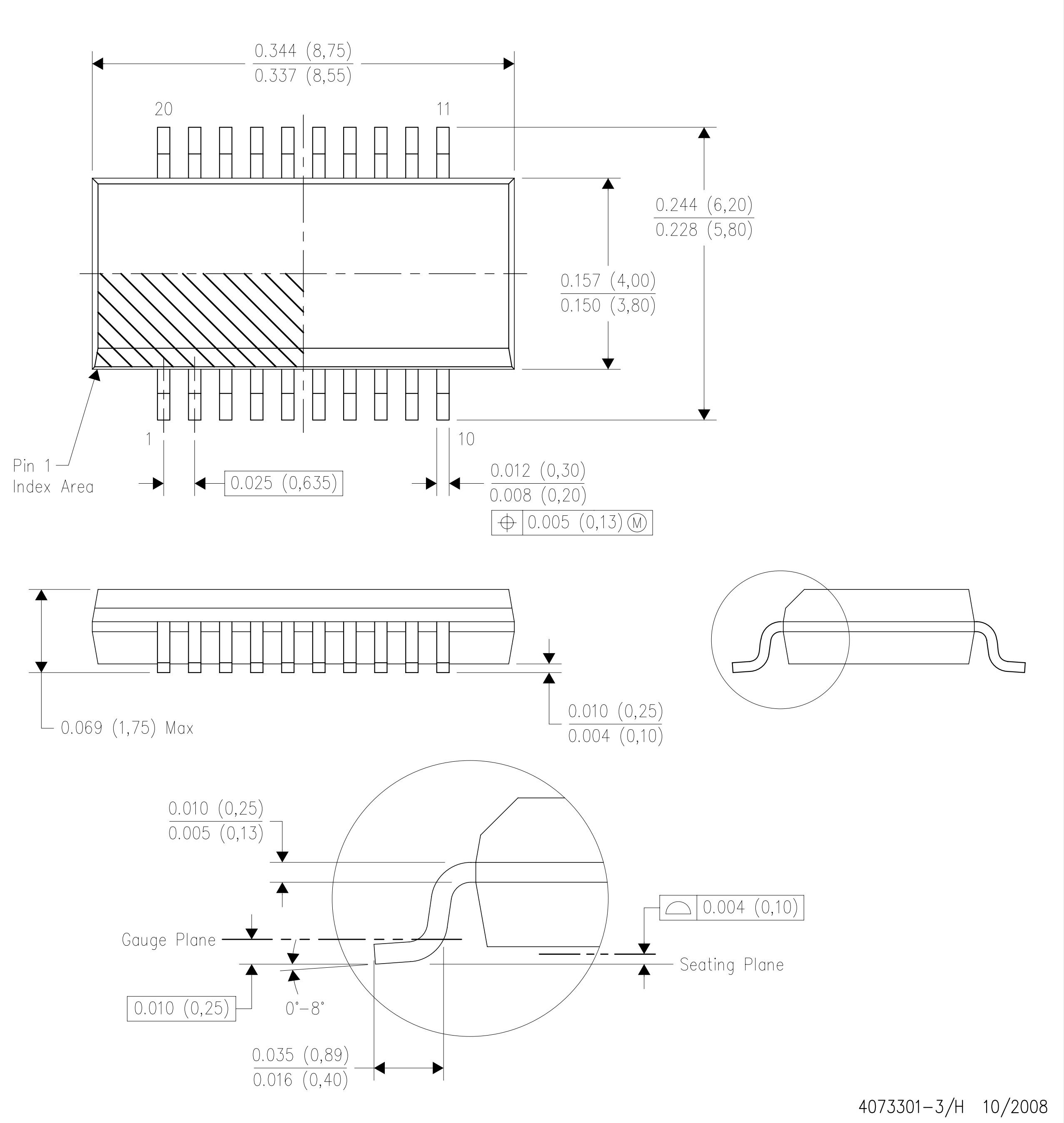
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

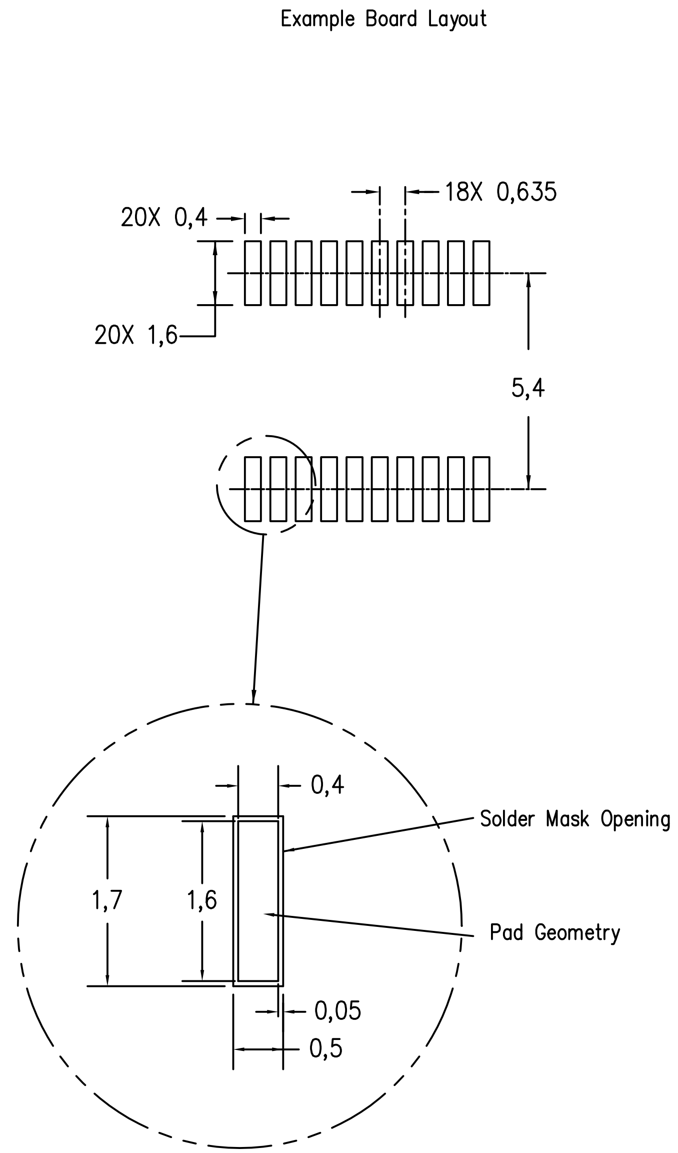
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PLL1707DBQR	SSOP	DBQ	20	2000	367.0	367.0	38.0
PLL1708DBQR	SSOP	DBQ	20	2000	367.0	367.0	38.0

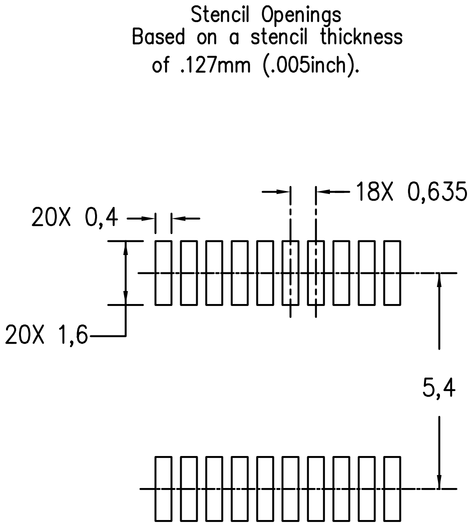
DBQ (R-PDSO-G20) PLASTIC SMALL-OUTLINE PACKAGE


0.344 (8,75)
0.337 (8,55)
20
11
0.244 (6,20)
0.228 (5,80)
0.157 (4,00)
0.150 (3,80)
1
10
Pin 1
Index Area
0.025 (0,635)
0.012 (0,30)
0.008 (0,20)
0.005 (0,13) M
0.069 (1,75) Max
0.010 (0,25)
0.004 (0,10)
0.010 (0,25)
0.005 (0,13)
Gauge Plane
0.010 (0,25)
0°–8°
0.004 (0,10)
Seating Plane
0.035 (0,89)
0.016 (0,40)
4073301-3/H 10/2008

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO-137 variation AD.

DBQ (R–PDSO–G20) PLASTIC SMALL OUTLINE PACKAGE


Example Board Layout
20X 0,4
18X 0,635
20X 1,6
5,4
0,4
Solder Mask Opening
1,7
1,6
Pad Geometry
0,05
0,5


Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
20X 0,4
18X 0,635
20X 1,6
5,4

4210335–3/D 03/14

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

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