TUSB1310A USB 3.0 Transceiver

Not Recommended for New Designs

1 Device Overview

1.1 Features

- Universal Serial Bus (USB)
  - Single Port 5.0-Gbps USB 3.0 Physical Layer Transceiver
    - One 5.0-Gbps SuperSpeed Connection
    - One 480-Mbps HS/FS/LS Connection
  - Fully Compliant With USB 3.0 Specification, Revision 1.0
  - Supports 3+ Meters USB 3.0 Cable Length
  - Fully Adaptive Equalizer to Optimize Receiver Sensitivity
  - PIPE to Link-Layer Controller
    - Supports 16-Bit SDR Mode at 250 MHz
    - Compliant With PHY Interface for the USB Architectures (PIPE), Version 3.0
  - ULPI to Link-Layer Controller
    - Supports 8-Bit SDR Mode at 60 MHz
    - Supports Synchronous Mode and Low-Power Mode
    - Compliant With UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1
- General Features
  - IEEE 1149.1 JTAG Support
  - IEEE 1149.6 JTAG support for the SuperSpeed Port
  - Operates on One Reference Clock of 40 MHz
  - 3.3-, 1.8-, and 1.1-V Supply Voltages
  - 1.8-V PIPE and ULPI I/O
  - Available in Lead-Free 175-Ball 12- × 12-nF NFBGA Package (ZAY)

1.2 Applications

- Surveillance Cameras
- Digital Still Cameras
- Multimedia Handsets
- Phones and Smartphones
- Portable Media Players
- Personal Navigation Devices
- Audio Docks
- Video- and Wireless-IP Phones
- Software Defined Radios

1.3 Description

The TUSB1310A device is one port, 5.0-Gbps USB 3.0 physical layer transceiver that operates off of one reference clock, which is provided by either a crystal or an external reference clock. The reference clock frequencies are selectable from 20, 25, 30, and 40 MHz. The TUSB1310A device provides the clock to the USB controller. The use of one reference clock allows the TUSB1310A device to provide a cost-effective USB 3.0 solution with few external components and a low implementation cost.

The USB controller interfaces to the TUSB1310A device through a PIPE (SuperSpeed) and a ULPI (USB 2.0) interface. The 16-bit PIPE operates off of a 250-MHz interface clock. The ULPI supports 8-bit operations with a 60-MHz interface clock.

USB 3.0 reduces active and idle power consumption with improved power-management features. The low-power states of the TUSB1310A device are controlled by the USB controller through the PIPE interface.

SuperSpeed USB uses existing USB software infrastructure by keeping the existing software interfaces and software drivers intact. In addition, SuperSpeed USB retains backward compatibility with USB 2.0 based products by using the same form-factor Type-A connector and cables. Existing USB 2.0 devices work with new USB 3.0 hosts and new USB 3.0 devices with work with legacy USB 2.0 hosts.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB1310A	NFBGA (175)	12.00 mm × 12.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

1.4 Functional Block Diagram

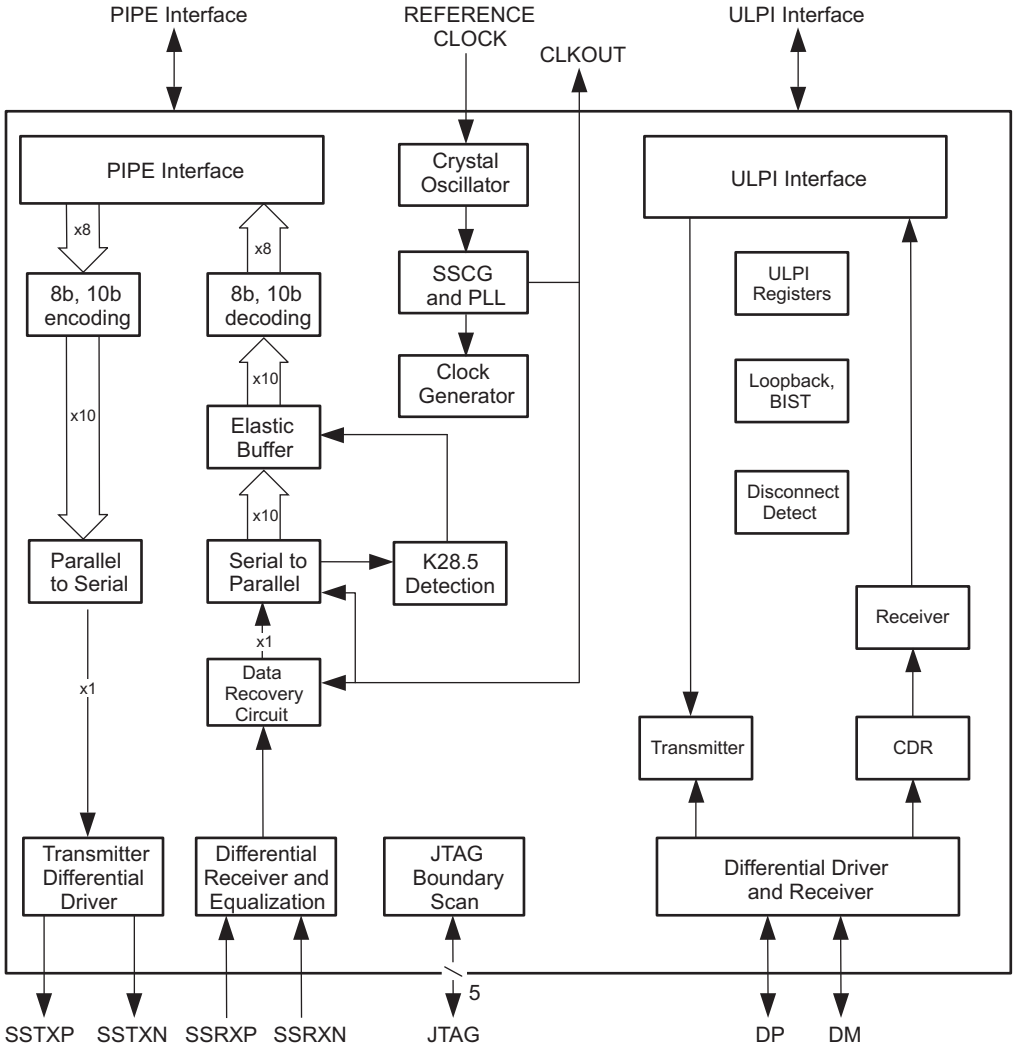

Figure 1-1. Functional Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (August 2015) to Revision G	Page
• Changed the device to *Not Recommended for New Designs*	1
• Changed sentence From: "The SuperSpeed USB contains SSTXP/SSTXN and SSRXP/SSRXP..." To: "The SuperSpeed USB contains SSTXP/SSTXN and SSRXP/SSRXN..." in the *Overview* section	20

Changes from Revision E (July 2012) to Revision F	Page
• Added *Pin Configuration and Functions* section, storage temperature to the *Absolute Maximum Ratings* table, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added parameter names to the *DC Characteristics for 1.8-V Digital I/O* table	14

3 Pin Configuration and Functions

Figure 3-1 shows the 175-pin ZAY plastic ball grid array (NFBGA) pin assignments.

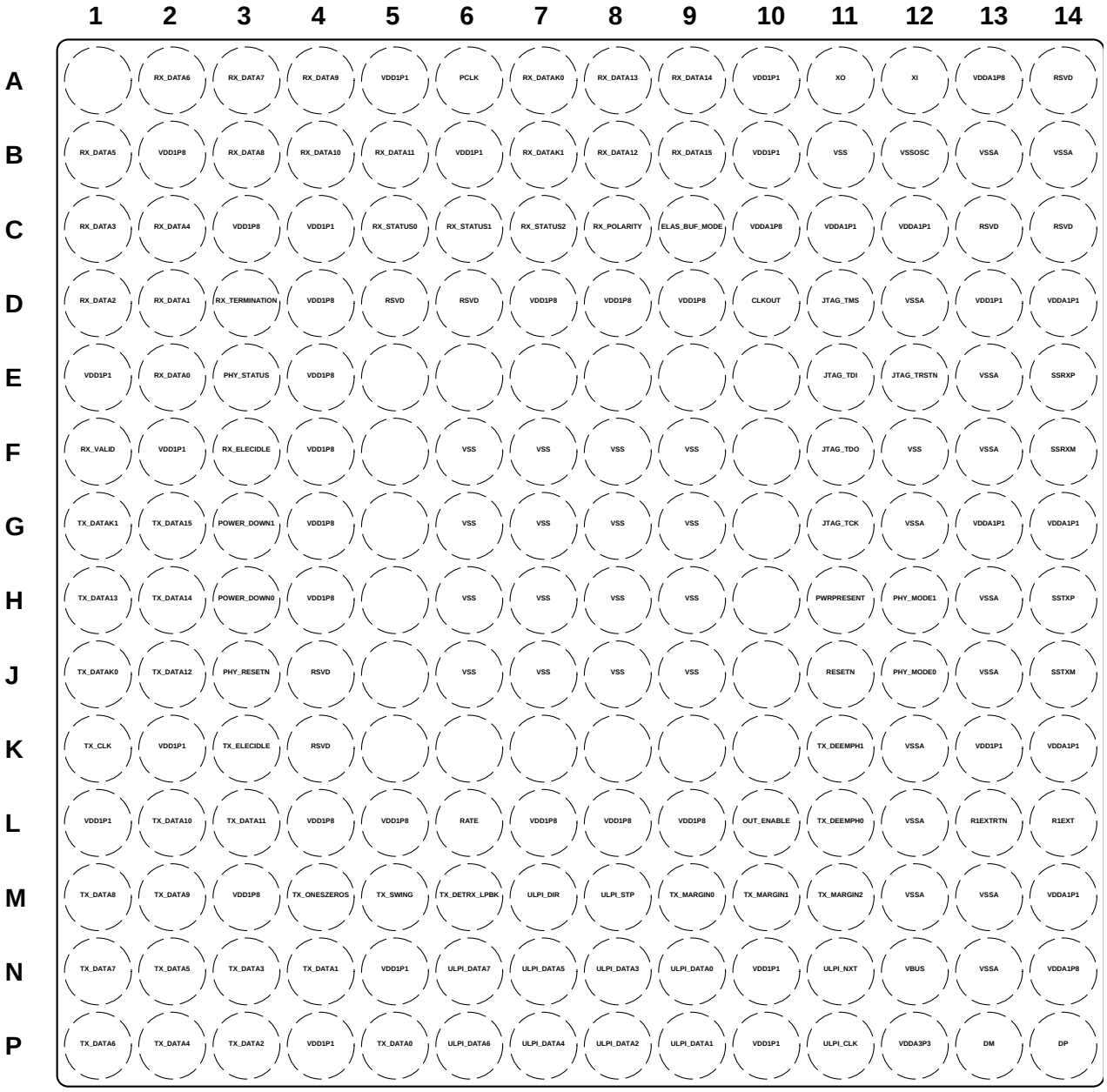


Figure 3-1. 175-Pin ZAY NFBGA (Top View)

3.1 Pin Attributes

Table 3-1. Pin Types

TYPE	DESCRIPTION
I	Input
O	Output
I/O	Input/output
PD, PU	Internal pullup, internal pulldown
S	Strapping pin
P	Power supply
G	Ground

3.2 Configuration Pins

The configuration pins are not latched by RESETN.

Table 3-2. Configuration Pins

SIGNAL NAME	TYPE	PIN NO.	MODE NAME	DESCRIPTION
PHY_MODE1	I, PD	H12	USB	Must be set to 0. Operates as USB 3.0 transceiver.
PHY_MODE0	I, PU	J12	USB	Must be set to 1. Operates as USB 3.0 transceiver.

3.3 Signal Descriptions

3.3.1 PIPE

The TUSB1310A supports 16-bit SDR mode with a 250-MHz clock.

Table 3-3. PIPE Signal Descriptions

SIGNAL NAME	TYPE	BALL NO.	DESCRIPTION
TX_CLK	I	K1	TX_DATA and TX_DATAK clock for source synchronous PIPE. This clock frequency is the same as PCLK frequency. The rising edge of the clock is the reference for all signals.
TX_DATA15	I	G2	Parallel USB SuperSpeed data input bus. The 16 bits represent 2 symbols of transmit data where TX_DATA7-0 is the first symbol to be transmitted, and TX_DATA15-8 is the second symbol.
TX_DATA14		H2	
TX_DATA13		H1	
TX_DATA12		J2	
TX_DATA11		L3	
TX_DATA10		L2	
TX_DATA9		M2	
TX_DATA8		M1	
TX_DATA7		N1	
TX_DATA6		P1	
TX_DATA5		N2	
TX_DATA4		P2	
TX_DATA3		N3	
TX_DATA2		P3	
TX_DATA1		N4	
TX_DATA0		P5	
TX_DATAK1	I	G1	Data/Control for the symbols of transmit data. TX_DATAK0 corresponds to the low-byte of TX_DATA, TX_DATAK1 to the upper byte.
TX_DATAK0		J1	

Table 3-3. PIPE Signal Descriptions (continued)

SIGNAL NAME	TYPE	BALL NO.	DESCRIPTION
PCLK	O	A6	Parallel interface data clock. All data movement across the parallel PIPE is synchronous to this clock. This clock operates at 250 MHz. The rising edge of the clock is the reference for all signals.
RX_DATA15	O	B9	Parallel USB SuperSpeed data output bus. The 16 bits represent 2 symbols of receive data where RX_DATA7-0 is the first symbol received, and RX_DATA15-8 is the second.
RX_DATA14		A9	
RX_DATA13		A8	
RX_DATA12		B8	
RX_DATA11		B5	
RX_DATA10		B4	
RX_DATA9		A4	
RX_DATA8		B3	
RX_DATA7		A3	
RX_DATA6		A2	
RX_DATA5		B1	
RX_DATA4		C2	
RX_DATA3		C1	
RX_DATA2		D1	
RX_DATA1		D2	
RX_DATA0		E2	
RX_DATAK1	O	B7	Data/Control for the symbols of receive data. RX_DATAK0 corresponds to the low-byte of RX_DATA, RX_DATAK1 to the upper byte. A value of zero indicates a data byte; a value of 1 indicates a control byte.
RX_DATAK0		A7	
RX_VALID	O	F1	Active High. Indicates symbol lock and valid data on RX_DATA and RX_DATAK.

Table 3-3. PIPE Signal Descriptions (continued)

SIGNAL NAME	TYPE	BALL NO.	DESCRIPTION
CONTROL AND STATUS SIGNALS			
PHY_RESETN	I, PU	J3	Active Low. Resets the transmitter and receiver. This signal is asynchronous.
TX_DETRX_LPBK	I, PD	M6	Active High. Used to tell the PHY to begin a receiver detection operation or to begin loopback.
TX_ELECIDLE	I	K3	Active High. Forces TX output to electrical idle depending on the power state.
RX_ELECIDLE	S, I/O, PD	F3	Active High. While deasserted with the PHY in P0, P1, P2, or P3, indicates detection of LFPS.
RX_STATUS2	O	C7	Encodes receiver status and error codes for the received data stream when receiving data.
RX_STATUS1		C6	
RX_STATUS0		C5	

BIT 2	BIT 1	BIT 0	DESCRIPTION
0	0	0	Received data OK
0	0	1	1 SKP ordered set added
0	1	0	1 SKP ordered set removed
0	1	1	Receiver detected
1	0	0	8B/10B decode error
1	0	1	Elastic buffer overflow
1	1	0	Elastic buffer underflow. This error code is not used if the elasticity buffer is operating in the nominal buffer empty mode.
1	1	1	Receive disparity error

POWER_DOWN1	I	G3	Power up and down the transceiver power states.
POWER_DOWN0		H3	

BIT 1	BIT 0	DESCRIPTION
0	0	P0, normal operation
0	1	P1, low recovery time latency, power saving state
1	0	P2, longer recovery time latency, low-power state
1	1	P3, lowest power state

When transitioning from P3 to P0, the signaling is asynchronous.

PHY_STATUS	S, I/O, PD	E3	Active High. Used to communicate completion of several PHY functions including power management state transitions, rate change, and receiver detection. When this signal transitions during entry and exit from P3 and PCLK is not running, then the signaling is asynchronous.
PWRPRESENT	O	H11	Indicates the presence of VBUS

Table 3-3. PIPE Signal Descriptions (continued)

SIGNAL NAME	TYPE	BALL NO.	DESCRIPTION
CONFIGURATION PINS			
TX_ONESZEROS	I, PD	M4	Active High. Used only when transmitting USB compliance pat-terns CP7 or CP8. Causes the transmitter to transmit an alternating sequence of 50 to 250 ones and 50 to 250 zeros—regardless of the state of the TX_DATA interface.
TX_DEEMPH1	I, PD, PU	K11	Selects transmitter de-emphasis. When the MAC changes, the TUSB1310A starts to transmit with the new setting within 128 ns.
TX_DEEMPH0		L11	**BIT 1** / **BIT 0** / **DESCRIPTION** 0 / 0 / –6-dB de-emphasis 0 / 1 / –3.5-dB de-emphasis 1 / 0 / No de-emphasis 1 / 1 / Reserved
TX_MARGIN2	I, PD	M11	Selects transmitter voltage levels
TX_MARGIN1		M10	**BIT 2** / **BIT 1** / **BIT 0** / **TX_SWING** / **DESCRIPTION** 0 / 0 / 0 / 0 / Normal operating range 800 mV to 1200 mV 0 / 0 / 0 / 1 / Normal operating range 400 mV to 700 mV 0 / 0 / 1 / 0 / 800 mV to 1200 mV 0 / 0 / 1 / 1 / 400 mV to 700 mV 0 / 1 / 0 / 0 / 700 mV to 900 mV 0 / 1 / 0 / 1 / 300 mV to 500 mV 0 / 1 / 1 / 0 / 400 mV to 600 mV 0 / 1 / 1 / 1 / 200 mV to 400 mV 1 / Don't care / 0 / 200 mV to 400 mV 1 / Don't care / 1 / 100 mV to 200 mV
TX_MARGIN0		M9	
TX_SWING	I, PD	M5	Controls transmitter voltage swing level 0: Full swing 1: Half swing
RX_POLARITY	I, PD	C8	Active High. Tells PHY to do a polarity inversion on the received data. Inverted data show up on RX_DATA15-0 within 20 PCLK clocks after RX_POLARITY is asserted. 0: PHY does no polarity inversion 1: PHY does polarity inversion
RX_TERMINATION	I, PD	D3	Controls presence of receiver terminations 0: Terminations removed 1: Terminations present
RATE	I, PU	L6	Controls the link signaling rate The RATE is always 1
ELAS_BUF_MODE	I, PD	C9	Selects elasticity buffer operating mode 0: Nominal half full buffer mode 1: Nominal empty buffer mode

3.3.2 ULPI

The ULPI (ultra low pin count interface) is a low pin count USB PHY to a Link-Layer Controller interface. The ULPI consists of the interface and the ULPI registers. The TUSB1310A device is always the master of the ULPI bus.

Table 3-4. ULPI Signal Descriptions

SIGNAL NAME	TYPE	BALL NO.	DESCRIPTION
ULPI_CLK	O	P11	60-MHz interface clock. All ULPI signals are synchronous to ULPI_CLK. The ULPI_CLK is always a 60-MHz output of the TUSB1310A device. In low-power mode, the ULPI_CLK is not driven.
ULPI_DATA7	S, I/O, PD	N6	Data bus. Driven to 00h by the Link when the ULPI bus is idle. 8-bit data timed on rising edge of ULPI_CLK
ULPI_DATA6		P6	
ULPI_DATA5		N7	
ULPI_DATA4		P7	
ULPI_DATA3		N8	
ULPI_DATA2		P8	
ULPI_DATA1		P9	
ULPI_DATA0		N9	
ULPI_DIR	O	M7	Controls the direction of the ULPI_DATA bus 0: ULPI_DATA lines are inputs 1: ULPI_DATA lines are outputs
ULPI_STP	S, I, PU	M8	Active High. The Link must assert ULPI_STP to signal the end of a USB transmit packet or a register write operation. The ULPI_STP signal must be asserted in the cycle after the last data byte is presented on the bus. The ULPI_STP has an internal weak pullup to safeguard against false commands on the ULPI_DATA lines.
ULPI_NXT	O	N11	Active High. The PHY asserts ULPI_NXT to throttle all data types, except register read data and the RX CMD. The PHY also asserts ULPI_NXT and ULPI_DIR simultaneously to indicate USB receive activity, if ULPI_DIR was previously low. The PHY is not allowed to assert ULPI_NXT during the first cycle of the TX CMD driven by the Link.

3.3.3 Clocking

Table 3-5. Clock Signal Name Descriptions

SIGNAL NAME	TYPE	BALL NO.	DESCRIPTION
XI	I	A12	Crystal Input. This pin is the clock reference input for the TUSB1310A. The TUSB1310A device supports either a crystal unit, or a 1.8-V clock input. Frequencies supported are 20, 25, 30, or 40 MHz.
XO	O	A11	Crystal output. If a 1.8-V clock input is connected to XI, XO must be left open.
CLKOUT	O	D10	OOBCLK is driven in U3 mode.

3.3.4 JTAG Interface

The JTAG Interface is used for board-level boundary scan. All digital IO support IEEE1149.1 boundary scan and SuperSpeed differential pairs support IEEE1149.6 boundary scan.

Table 3-6. JTAG Signal Name Descriptions

SIGNAL NAME	TYPE	BALL NO.	DESCRIPTION
JTAG_TCK	I, PU	G11	JTAG test clock
JTAG_TMS	I, PU	D11	JTAG test mode select
JTAG_TDI	I, PU	E11	JTAG test data input
JTAG_TRSTN	I, PD	E12	JTAG test asynchronous reset. Active Low. An external pulldown is required for normal operation.
JTAG_TDO	O	F11	JTAG test data output

3.3.5 Reset and Output Control Interface

Table 3-7. Reset and Output Control Signal Descriptions

SIGNAL NAME	TYPE	BALL NO.	DESCRIPTION
RESETN	I	J11	Active Low. Resets the transmitter and receiver. This signal is asynchronous.
OUT_ENABLE	I	L10	Active High. This can be connected to a 1.8-V power-on-reset signal on the PCB to avoid static current and signal contention during power up. 0: Disable all driver outputs while I/O powers are supplied, but internal control circuit powers are not present during power up. 1: Enable all driver outputs during normal operation.

3.3.6 Strap Options

Strapping pins are latched by reset deassertion in the TUSB1310A device.

Table 3-8. Strapping Options (1)

SIGNAL NAME	TYPE	BALL NO.	DESCRIPTION
XTAL_DIS (RX_ELECIDLE)	S, I/O, PD	F3	Selects an input clock source 0: Crystal Input 1: Clock Input
SSC_DIS (TX_MARGIN0)	S, I, PD	M9	Spread spectrum clocking disable 0: SSC enable 1: SSC disable
PIPE_16BIT (PHY_STATUS)	S, I/O, PD	E3	Selects PIPE 0: 16-bit PIPE SDR mode Must be 0 at reset.
ISO_START (ULPI_DATA7)	S, I/O, PD	N6	Active High. Puts PIPE into isolate mode. When in the isolate mode, TUSB1310A device does not respond to packet data present at TX_DATA15-0, TXDATAK1-0 inputs and presents a high impedance on the PCLK, RX_DATA15-0, RX_DATAK1-0, RX_VALID outputs. When in the isolate mode, the TUSB1310A device continues to respond to ULPI. When the isolate mode bit in ULPI register is cleared, the USB interfaces starts transmitting packet data on TX_DATA15-0 and driving PCLK, RX_DATA15-0, RX_DATA1-0, and RX_VALID.
ULPI_8BIT (ULPI_DATA6)	S, I/O, PD	P6	Selects ULPI data bus bit width 0: 8-bit ULPI SDR mode Must be set to 0.
REFCLKSEL1, REFCLKSEL0 (ULPI_DATA5, ULPI_DATA4)	S, I/O, PD	N7 P7	Select input reference clock frequency for on-chip oscillator 00: 20 MHz on XI 01: 25 MHz on XI 10: 30 MHz on XI 11: 40 MHz on XI

(1) Signals in green have double function just before reset and after reset.

3.3.7 USB Interfaces

Table 3-9. USB Interface Signal Name Descriptions

SIGNAL NAME	TYPE	BALL NO.	DESCRIPTION
SSTXP	O	H14	USB SuperSpeed transmitter differential pair
SSTXM		J14	
SSRXP	I	E14	USB SuperSpeed receiver differential pair
SSRXM		F14	
DP	I/O	P14	USB non-SuperSpeed differential pair
DM		P13	
VBUS	I	N12	USB VBUS pin Connected through an external voltage divider

3.3.8 Special Connect

Table 3-10. Special Connect Signal Descriptions

SIGNAL NAME	TYPE	BALL NO.	DESCRIPTION
R1EXT	O	L14	High precision external resistor used for calibration. The R1 value shall be 10 kΩ ±1% accuracy.
R1EXTRTN	I	L13	R1 ground reference. This pin is not connected to board ground.
VDDA1P1	P	M14	Needs a 1-µF bypass capacitor
RSVD	I/O	D6	Must be left open.
		D5	
		C13	
		C14	
		K4	
		J4	
		A14	

3.3.9 Power and Ground

Table 3-11. Power and Ground Signal Descriptions

SIGNAL NAME	TYPE	BALL NO.		DESCRIPTION
VDDA3P3	P	P12		Analog 3.3-V power supply
VDDA1P8	P	N14		Analog 1.8-V power supply
		A13		
		C10		
VDDA1P1	P	C12		Analog 1.1-V power supply
		K14		
		G13		
		G14		
		D14		
		C11		
VDD1P8	P	B2	C3	Digital IO 1.8-V power supply
		D4	D7	
		D8	D9	
		E4	F4	
		G4	H4	
		L5	L4	
		M3	L7	
		L8	L9	
VDD1P1	P	A5	A10	Digital 1.1-V power supply
		B6	B10	
		E1	F2	
		K2	L1	
		N5	P4	
		N10	P10	
		K13	D13	
		C4		

Table 3-11. Power and Ground Signal Descriptions (continued)

SIGNAL NAME	TYPE	BALL NO.		DESCRIPTION
VSSA	G	B14	B13	Analog ground
		J13	H13	
		F13	E13	
		K12	L12	
		G12		
		D12		
		N13		
		M12		
		M13		
VSSOSC	G	B12		Oscillator ground If using a crystal, this must not be connected to PCB ground plane. See Section 6.2.2 for guidelines. If using an oscillator, this must be connected to PCB ground.
VSS	G	F6	F7	Digital ground
		F8	F9	
		G6	G7	
		G8	G9	
		J6	J7	
		H6	H7	
		H8	H9	
		J8	J9	
		B11	F12	

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VDD1P1 steady-state supply voltage	–0.3	1.4	V
VDD1P8 steady-state supply voltage	–0.3	2.45	V
VDDA1P1 steady-state supply voltage	–0.3	1.4	V
VDDA1P8 steady-state supply voltage	–0.3	2.45	V
VDDA3P3 steady-state supply voltage	–0.3	3.8	V
Storage temperature	–55	150	°C

4.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDA3P3	Analog 3.3-supply voltage	2.97	3.3	3.63	V
VDDA1P8	Analog 1.8-supply voltage	1.71	1.8	1.98	V
VDDA1P1	Analog 1.1-supply voltage	1.045	1.1	1.155	V
VDD1P8	Digital IO 1.8-supply voltage	1.62	1.8	1.98	V
VDD1P1	Digital 1.1-supply voltage	1.045	1.1	1.155	V
VBUS	Voltage at VBUS PAD	0		1.155	V
T_A	Operating free-air temperature	–40		85	°C
T_J	Operating junction temperature	–40		105	°C

4.4 Device Power-Consumption Summary

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER	MIN	TYP	MAX	UNIT
VDDA3P3 power consumption		13		mW
VDDA1P8 power consumption		77		mW
VDDA1P1 power consumption		118		mW
VDD1P1 power consumption		98		mW
VDD1P8 power consumption		128		mW

(1) Power-consumption condition is transmitting and/or receiving (in U0) at 25°C and nominal voltages.

4.5 DC Characteristics for 1.8-V Digital I/O

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		0.65 V_{DDS}			V
V_{IL}	Low-level input voltage				0.35 V_{DDS}	V
V_{OH}	High-level output voltage	I_O = –2 mA, V_{DDS} = 1.62 V to 1.98 V, driver enabled, pullup or pulldown disabled	V_{DDS} – 0.45			V
		I_O = –2 mA, V_{DDS} = 1.4 V to 1.6 V, driver enabled, pullup or pulldown disabled	0.75 V_{DDS}			
V_{OL}	Low-level output voltage	I_O = 2 mA, V_{DDS} = 1.62 V to 1.98 V, driver enabled, pullup or pulldown disabled			0.45	V
		I_O = 2 mA, V_{DDS} = 1.4 V to 1.6 V, driver enabled, pullup or pulldown disabled			0.25 V_{DDS}	
V_{hys}	Input hysteresis		100	270		mV
I_I	Input current	Any receiver, including those with a pullup or pulldown. The pullup or pulldown must be disabled.			±1	µA
$I_{I(PUon)}$	Input current with pullup enabled	Receiver pullup only, pullup enabled (not inhibited), V_{PAD} = 0 V		–47 to –169		µA
		Receiver pullup only, pullup enabled (not inhibited)		–100		
I_{OZ}	Off-state output current	Driver only, driver disabled			±20	µA
I_Z	Total leakage current(1)				±20	µA
$V_{TX\_DIFF\_SS}$	SSTXP, SSTXN differential p-p TX voltage swing		0.8		1.2	V
$R_{TX\_DIFF\_DC}$	DC differential impedance		72		120	Ω
$V_{TX\_RCV\_DET}$	The amount of voltage change allowed during receiver detection				0.6	V
$C_{AC\_COUPLING}$	AC coupling capacitor		75		200	nF
RRX_DC	Receiver DC common-mode impedance		18		30	Ω
RRX_DIFF_DC	DC differential impedance		72		120	Ω
VRX_LFPS_DET	LFPS detect threshold		100		300	mV
VCM_AC_LFPS	LFPS common-mode voltage				100	mV
VCM_LFPS_active	LFPS common-mode voltage active				10	mV
VTX_DIFF_PP_LFPS	LFPS differential voltage		800		1200	mV

(1) I_Z is the total leakage current through the PAD connection of a driver/receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited.

4.6 Thermal Characteristics

THERMAL METRIC(1)		TUSB1310A ZAY (NFBGA) 175 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

4.7 Timing Characteristics

4.7.1 Power-Up and Reset Timing

The TUSB1310A device does not drive signals on any strapping pins before they are latched internally.

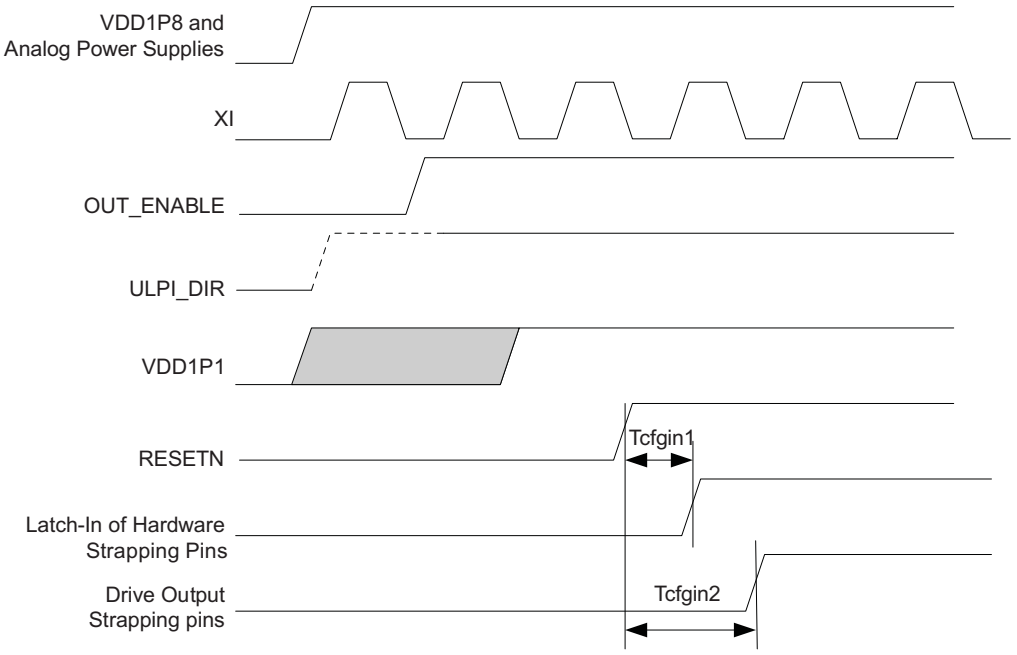


Figure 4-1. Power-Up and Reset Timing

Table 4-1. Power-Up and Reset Timing

		MIN	NOM	MAX	UNIT
Tcfgin1	Hardware configuration latch-in time from RESETN	0			ns
Tcfgin2	Time from RESETN to driver outputs on strapping pins	0			ns
	RESETN pulse width	1			µs
	RESETN to PHY_STATUS deassertion		300		µs

4.7.2 PIPE Transmit

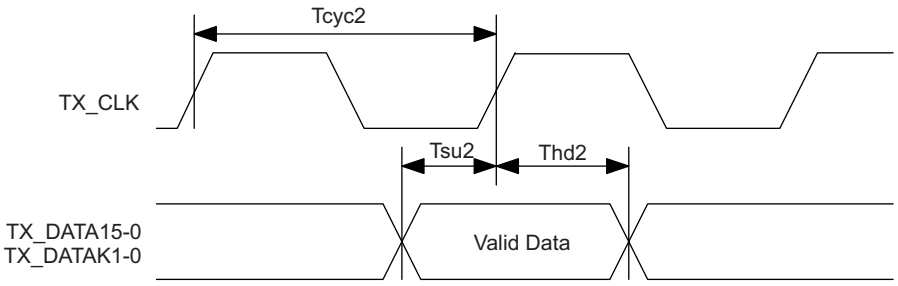


Figure 4-2. PIPE Transmit Timing

Table 4-2. PIPE Transmit Timing

		MIN	NOM	MAX	UNIT
Tcyc2	TX_CLK period		4		ns
Tdty2	TX_CLK duty cycle		50%		
Tsu2	Data setup to TX_CLK rise and TX_CLK fall (1)	1			ns
Thd2	Data hold to TX_CLK rise and TX_CLK fall (1)	0			ns

(1) This includes TX_DATA15-0, TX_DATAK1-0, TX_ONESZEROS, RATE, TX_DEEMPTH, TX_DETRX_LPBK, TX_ELECIDLE, TX_MARGIN, TX_SWING, RX_POLARITY, POWER_DOWN1-0.

4.7.3 PIPE Receive

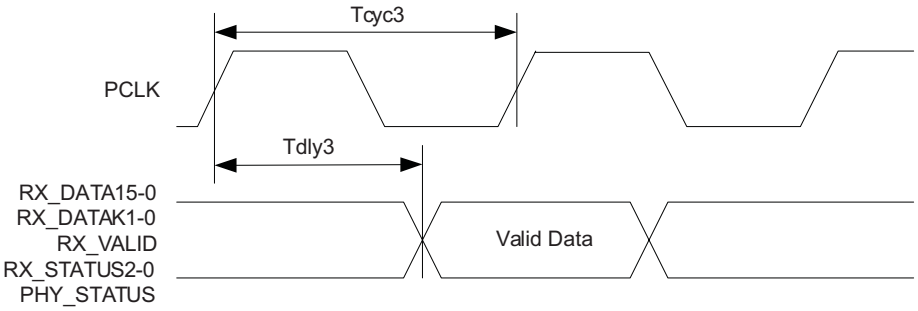


Figure 4-3. PIPE Receive Timing

Table 4-3. PIPE Receive Timing

		MIN	NOM	MAX	UNIT
Tcyc3	PCLK Period		4		ns
Tdty3	PCLK Duty Cycle		50%		
Tdly3	PCLK rise and fall to RX_DATA15-0, RX_DATAK1-0, RX_VALID, RX_STATUS2-0, PHY_STATUS Delay (1)(2)	1		2	ns

(1) Output Load max = 10 pF, min = 5 pF
(2) Timing is relative to the 50% transition point, not V_{IH} or V_{IL}.

4.7.4 ULPI Parameters

Table 4-4. ULPI Parameters

DESCRIPTION	NOTES	HS	FS	LS	UNIT
RX CMD delay	PHY pipeline delays	2 to 4	2 to 4	2 to 4	clocks
TX start delay		1 to 2	1 to 10	1 to 10	clocks
TX end delay		2 to 5			clocks
RX start delay		3 to 8			clocks
RX end delay		3 to 8	17 to 18	122 to 123	clocks
Transmit-Transmit (host only)	Link decision times	15 to 24	7 to 18	77 to 247	clocks
Receive-Transmit (host or peripheral)		1 to 14	7 to 18	77 to 247	clocks

4.7.5 ULPI Clock

Table 4-5. ULPI Clock Parameters

		MIN	NOM	MAX	UNIT
Fstart_8bit	Frequency (first transition) ±10%	54	60	66	MHz
Fsteady	Frequency (steady state) ±500 ppm	59.97	60	60.03	MHz
Dstart_8bit	Duty cycle (first transition) ±10%	40%	50%	60%	
Dsteady	Duty cycle (steady state) ±500 ppm	49.975%	50%	50.025%	
Tsteady	Time to reach steady state frequency and duty cycle after first transition			1.4	ms
Tstart_dev	Clock startup time after deassertion of SuspemdM – Peripheral			5.6	ms
Tstart_host	Clock startup time after deassertion of SuspemdM – Hold				ms
Tprep	PHY preparation time after first transition of input clock				µs
Tjitter	Jitter				ps
Trise, Tfall	Rise and fall time				ns

4.7.6 ULPI Transmit

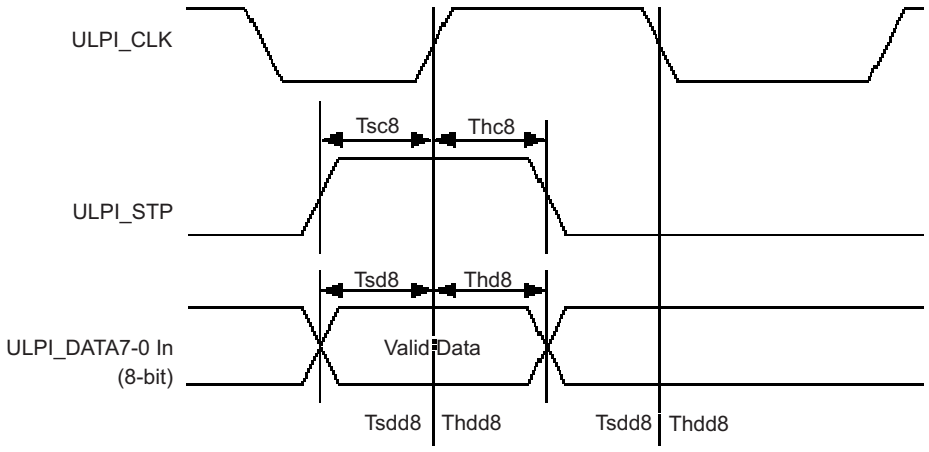


Figure 4-4. ULPI Transmit Timing

Table 4-6. ULPI Transmit Timing

		MIN	NOM	MAX	UNIT
Tsc8, Tsd8	ULPI_STP set-up time			6	ns
Thc8, Thd8	ULPI_STP hold time	0			ns

4.7.7 ULPI Receive Timing

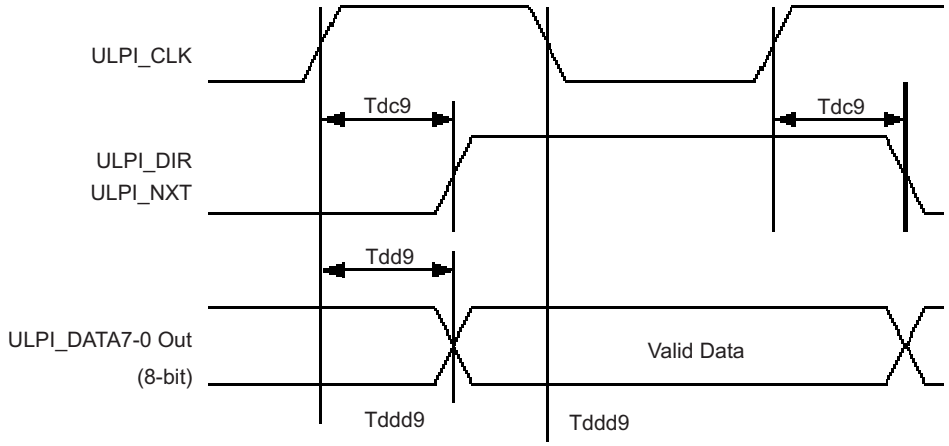


Figure 4-5. ULPI Receive Timing

Table 4-7. ULPI Receive Timing

		MIN	NOM	MAX	UNIT
Tdc9, Tdd9	ULPI_DIR/ULPI_NXT/ULPI_DATA7-0 (1)			9	ns

(1) Output Load MAX = 10 pF, MIN = 5 pF

4.8 Typical Characteristics

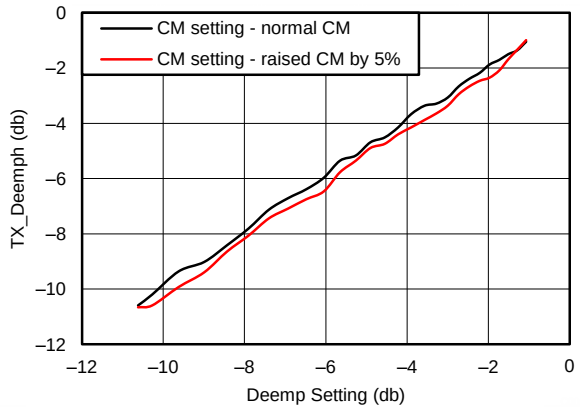


Figure 4-6. TX De-emphasis

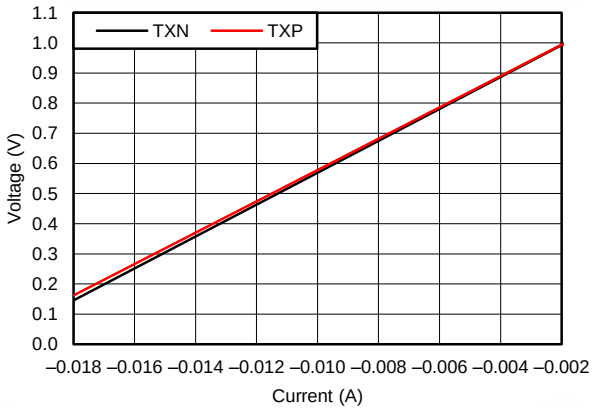


Figure 4-7. TX Termination I-V

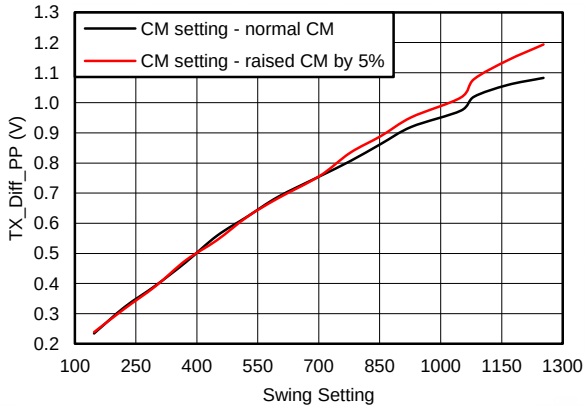


Figure 4-8. Diff TX Swing versus Swing Settings

5 Detailed Description

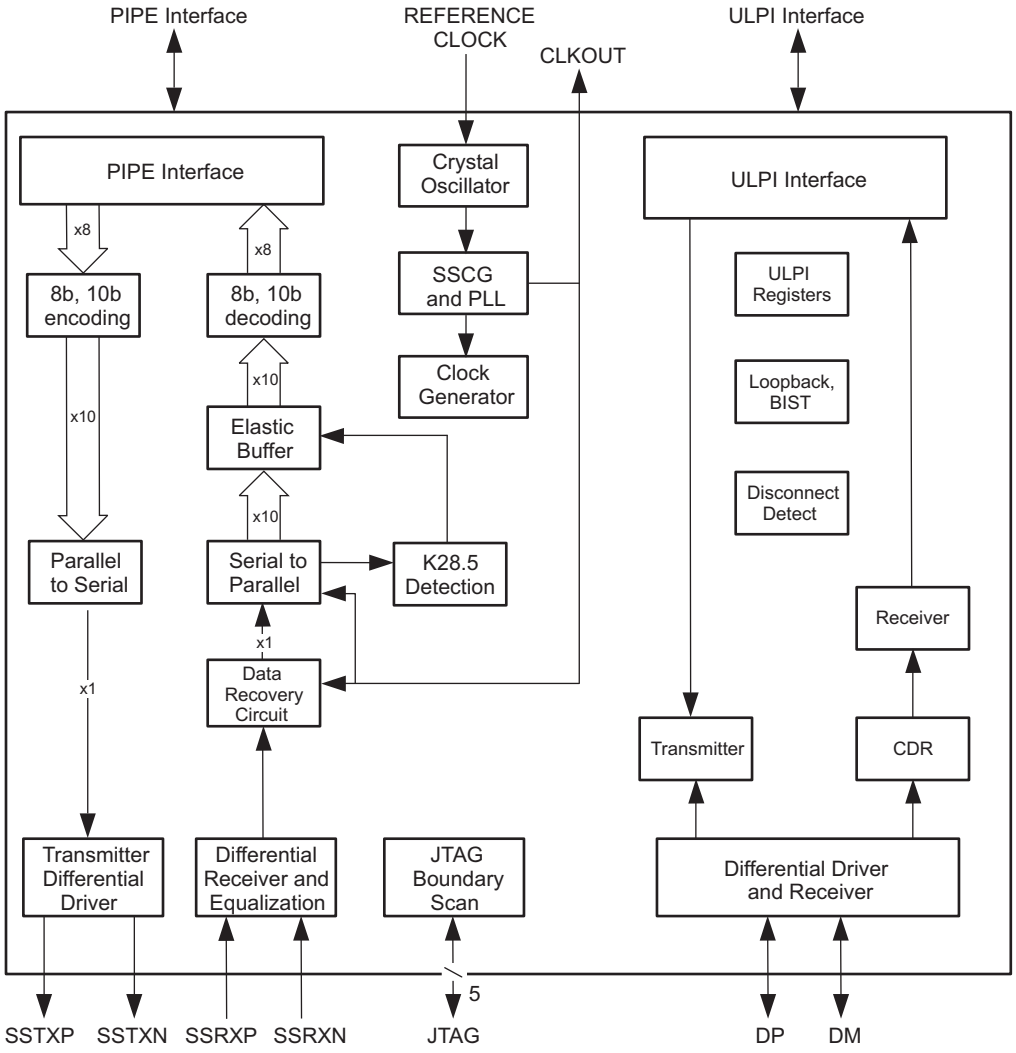
5.1 Overview

The USB physical layer handles the low-level USB protocol and signaling, which includes data serialization and deserialization, 8b/10b encoding, analog buffers, elastic buffers, and receiver detection. It shifts the clock domain of the data from the USB rate to one that is compatible with the link-layer controller.

The SuperSpeed USB contains SSTXP/SSTXN and SSRXP/SSRXN differential pairs and uses the PIPE to communicate with the link-layer controller. The Non-SuperSpeed USB has a DP/DM differential pair and communicates with the Link-Layer Controller through the ULPI. The reference clock of the TUSB1310A device is connected to an internal crystal oscillator, spread spectrum clock, and with a PLL, which provides clocks to all functional blocks and to the CLKOUT pin for the Link-Layer Controller.

A JTAG interface is used for IEEE1149.1 and IEEE1149.6 boundary scan.

5.2 Functional Block Diagram



5.3 Feature Description

5.3.1 Power On and Reset

The TUSB1310A device has two hardware reset pins, a chip reset RESETN and a logic reset PHY_RESETN. The RESETN is used only at Power On. The PHY_RESETN can be used as a functional reset. The ULPI register also has a software reset.

Until all power sources are supplied, the OUT_ENABLE pin can control the output driver enable. After all power sources are supplied, the chip reset RESETN and a ULPI soft reset is asserted by the Link Layer. The power-up sequence is described in Section 5.3.1.4.

5.3.1.1 RESETN and PHY_RESETN: Hardware Reset

The RESETN sets all internal states to initial values. The Link Layer must hold the PHY in reset through the RESETN until all power sources and the reference clock to the TUSB1310A device are stable. All pins used for strapping options must be set before RESETN deassertion as they are latched by reset deassertion. All strapping option pins have internal pullup or pulldown to set default values, but if any non-default values are desired, they need to be controlled externally by the Link-Layer Controller.

Table 5-1. Pin States in Chip Reset

PIPE CONTROL PIN NAME	STATE	VALUE
TX_DETRX_LPBK	Inactive	0
TX_ELECIDLE	Active	1
TX_ONESZEROS	Inactive	0
RX_POLARITY	Inactive	0
POWER_DOWN	U2	10b
TX_MARGIN2-0	Normal operating range	000b
TX_DEEMP	–3.5 dB	1
RATE	5.0 Gbps	1
TX_SWING	Full swing or half swing	0 or 1
RX_TERMINATION	Appropriate state	0 or 1

5.3.1.2 ULPI Reset: Software Reset

After power-up, the Link-Layer Controller must set the reset bit in ULPI register. It resets the core but does not reset the ULPI interface or the ULPI registers.

During the ULPI reset, the ULPI_DIR is deasserted. After the reset, the ULPI_DIR is asserted again and the TUSB1310A device sends an RX CMD update to the Link Layer. During the reset, the link must ignore signals on the ULPI_DATA7-0 and must not access the TUSB1310A.

5.3.1.3 OUT_ENABLE: Output Enable

Digital IO buffers use two power supplies, core VDD1P1 and IO VDD1P8. During power up, OUT_ENABLE must be asserted low for proper operation.

5.3.1.4 Power-Up Sequence

Figure 5-1 shows the power-up sequence.

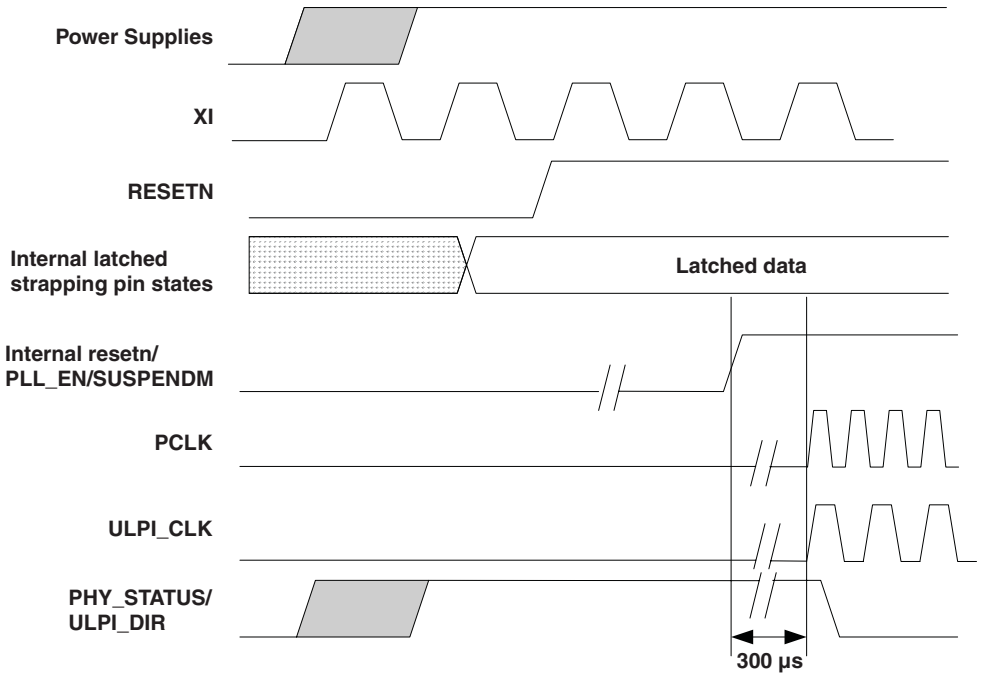


Figure 5-1. Power-Up Sequence

After proper power-supply sequencing, the reference clock on XI starts to operate. On the RESETN deassertion, REFCLKSEL1-0 is determined depending on the PHY_MODE pins, PLL is locked and the valid ULPI_CLK and the valid PCLK are driven.

After all stable clocks are provided, the TUSB1310A device allows the Link-Layer Controller to access by deasserting the ULPI_DIR. The Link-Layer Controller sets the Reset bit in the ULPI register. At the PIPE interface, the PHY_STATUS changes from high to low, which indicates that the TUSB1310A device is in the power state specified by the POWER_DOWN signal. After the PHY_STATUS change, the TUSB1310A device is ready for PIPE transactions.

5.3.2 Clocks

5.3.2.1 Clock Distribution

A source clock must be provided through XI or XO from an external crystal or from a square wave clock. The USB 3.0 PLL provides a clock to the PIPE that drives 250 MHz. The USB 2.0 PLL provides a 60-MHz clock to the ULPI.

5.3.2.2 Output Clock

The CLKOUT is used by the Link-Layer Controller or the MAC in low-power mode. A 120-MHz clock is available on the CLKOUT pin only in the USB U3 power state.

5.3.3 Power State Transition Time

The P1 to P0 transition time is the amount of time for the TUSB1310A device to return to P0 state, after having been in the P1 state. This time is measured from when the MAC sets the POWER_DOWN signals to P0 until the TUSB1310A device asserts PHY_STATUS. The TUSB1310A device asserts PHY_STATUS when it is ready to begin data transmission and reception.

The P2 to P0 transition time is the amount of time for the TUSB1310A device to return to the P0 state, after having been in the P2 state. This time is measured from when the MAC sets the POWER_DOWN signals to P0 until the TUSB1310A device asserts PHY_STATUS. The TUSB1310A device asserts PHY_STATUS when it is ready to begin data transmission and reception.

The P3 to P0 transition time is the amount of time for the TUSB1310A device to go to P0 state, after having been in the P3 state. Time is measured from when the MAC sets the POWER_DOWN signals to P0 until the TUSB1310A device deasserts PHY_STATUS. The TUSB1310A device asserts PHY_STATUS when it is ready to begin data transmission and reception.

5.3.4 Power Management

The SuperSpeed USB power state transition is controlled by the PIPE POWER_DOWN[1-0] and the Non-SuperSpeed USB power state is transitioned by setting suspendM bit in the ULPI Function control register through the ULPI or by asserting the ULPI_STP.

5.3.4.1 USB Power Management

The USB 3.0 specification improves power consumption by defining four power states, U0, U1, U2, and U3 while the PIPE specification defines P0, P1, P2 and P3. The POWER_DOWN pin states are mapped to LTSSM states as described in Table 5-2. For all power state transitions, the Link-Layer Controller must not begin any operational sequences or further power state transitions until the TUSB1310A device has indicated that the internal state transition is completed.

Table 5-2. Power States

PIPE POWER STATE	USB POWER STATE	PCLK	PLL	TRANSMITTING	RECEIVING	PHY_STATUS
P0	U0, all other LTSSM states	On	On	Active or Idle or LFPS	Active or Idle	One cycle assertion
P1	U1	On	On	Idle or LFPS	Idle	One cycle assertion
P2	U2, RxDetect, SS.Inactive	On	On	Idle or LFPS or RxDetect	Idle	One cycle assertion
P3	U3, SS.disabled	Off. The PIPE is in an asynchronous mode.	Off	LFPS or RxDetect	Idle	PHY_STATUS is asserted before PCLK is turned off and deasserted when PCLK is fully off.

When the Link-Layer Controller must transmit LFPS in P1, P2, or P3 state, it must deassert TX_ELECIDLE. The TUSB1310A device generates valid LFPS until the TX_ELECIDLE is asserted. The Link-Layer Controller must assert TX_ELECIDLE before transitioning to P0.

When RX_ELECIDLE is deasserted in P0, P1, P2, or P3, the TUSB1310A device receiver monitors for LFPS except during reset or when RX_TERMINATION is removed for electrical idle.

When the TUSB1310A device is in P0 and is actively transmitting; only RX_POLARITY can be asserted.

Table 5-3. PIPE Control Pin Matrix

POWER STATE	TX_DETRX_LPBK	TX_ELECIDLE	DESCRIPTION
P0	0	0	Transmitting data on TX_DATA
	0	1	Not transmitting and is in electrical idle
	1	0	Goes into loopback mode
	1	1	Transmits LFPS signaling
P1	Don't care	0	Transmits LFPS signaling
		1	Not transmitting and is in electrical idle
P2	Don't care	0	Transmits LFPS signaling
	0	1	Idle
	1	1	Does a receiver detection operation
P3	Don't care	0	Transmits LFPS signaling
		1	Does a receiver detection operation

5.3.5 Receiver Status

The TUSB1310A device has an elastic buffer for clock tolerance compensation, the Link Partner detection, and some received data error detections. The receive data status from SSRXP/SSRXN differential pair presents on RX_STATUS2-0. If an error occurs during a SKP ordered-set (a set of symbols transmitted as a group), the error signaling has precedence. If more than one error occurs on a received byte, the errors have the following priority:

1. 8B/10B decode error
2. Elastic buffer overflow
3. Elastic buffer underflow (cannot occur in nominal empty buffer model)
4. Disparity error

5.3.5.1 Clock Tolerance Compensation

The receiver contains an elastic buffer used to compensate for differences in frequencies between bit rates at the two ends of a Link. The elastic buffer must be capable of holding enough symbols to handle worst case differences in frequency and worst case intervals between SKP ordered-sets. A SKP order-set is a set of symbols transmitted as a group. The SKP ordered-sets allows the receiver to adjust the data stream being received prevent the elastic buffer from either overflowing or under-flowing due to any clock tolerance differences.

The TUSB1310A device supports two models, nominal half-full buffer model and nominal empty-buffer mode. For the nominal half-full buffer model, the TUSB1310A device monitors the receive data stream. When a SKP ordered-set is received, the TUSB1310A device adds or removes one SKP order set from each SKP to manage its elastic buffer to keep the buffer as close to half full as possible. Only full SKP ordered sets are added or removed. When a SKP order set is added, the TUSB1310A device asserts an *Add SKP* code (001b) on the RX_STATUS for one clock cycle. When a SKP order set is removed, the RX_STATUS has a *Remove SKP* code (010b).

For the nominal empty-buffer model, the TUSB1310A device tries to keep the elasticity buffer as close to empty as possible. When no SKP ordered sets have been received, the TUSB1310A device is required to insert SKP ordered sets into the received data stream.

Table 5-4. RX_STATUS: SKP

RX_STATUS2-0	SKP ADDITION OR REMOVAL	LENGTH
001b	1 SKP Ordered Set added	One clock cycle
010b	1 SKP Ordered Set removed	

5.3.5.2 Receiver Detection

TX_DETRX_LPBK starts a receiver detection operation to determine if there is a receiver at the other end of the link. When the receiver detect sequence completes, the PHY_STATUS is asserted for one clock and drives the RX_STATUS signals to the appropriate code. When the TX_DETRX_LPBK signal is asserted, the Link-Layer Controller must leave the signal asserted until the PHY_STATUS pulse. When receiver detection is performed in P3, the PHY_STATUS shows the appropriate receiver detect value until the TX_DETRX_LPBK is deasserted.

Table 5-5. RX_STATUS: Receiver Detection

RX_STATUS2-0	DETECTED CONDITION	LENGTH
000b	Receiver not present	One clock cycle
011b	Receiver present	

5.3.5.3 8b/10b Decode Errors

When the TUSB1310A device detects an 8b/10b decode error, it asserts a SUB symbol in the data on the RX_DATA where the bad byte occurred. In the same clock cycle that the SUB symbol is asserted on the RX_DATA, the 8b/10b decode error code (100b) is asserted on the RX_STATUS. An 8b/10b decoding error has priority over all other receiver error codes and could mask out a disparity error occurring on the other byte of data being clocked onto the RX_DATA with the SUB symbol.

Table 5-6. 8b/10b Decode Errors

RX_STATUS2-0	DETECTED ERROR	LENGTH
100b	8B/10B Decode Error	Clock cycles during the effected byte is transferred on RX_DATA15-0

5.3.5.4 Elastic Buffer Errors

When the elastic buffer overflows, data is lost during the reception of the data. The elastic buffer overflow error code (101b) is asserted on the RX_STATUS on the PCLK cycle the omitted data would have been asserted. The data asserted on the RX_DATA is still valid data, the elastic buffer overflow error code on the RX_STATUS just marks a discontinuity point in the data stream being received.

When the elastic buffer underflows, SUB symbols are inserted into the data stream on the RX_DATA to fill the holes created by the gaps between valid data. For every PCLK cycle a SUB symbol is asserted on the RX_DATA, an elastic buffer underflow error code (111b) is asserted on the RX_STATUS. In nominal empty-buffer mode, SKP ordered sets are transferred on RX_DATA and the underflow is not signaled.

Table 5-7. Elastic Buffer Errors

RX_STATUS2-0	DETECTED ERROR	LENGTH
101b	Elastic Buffer overflow	Clock cycles the omitted data would have appeared
110b	Elastic Buffer underflow	Clock cycles during the SUB symbol presence on RX_DATA15-0

5.3.5.5 Disparity Errors

When the TUSB1310A device detects a disparity error, it asserts a disparity error code (111b) on the RX_STATUS in the same PCLK cycle it asserts the erroneous data on the RX_DATA. The disparity code does not discern which byte on the RX_DATA is the erroneous data.

Table 5-8. Disparity Errors

RX_STATUS2-0	DETECTED ERROR	LENGTH
111b	Disparity Error	Clock cycles during the effected byte is transferred on RX_DATA15-0

5.3.6 Loopback

The TUSB1310A device begins an internal-loopback operation from SSRXP/SSRXN differential pairs to SSTXP/SSTXN differential pairs when the TX_DETRX_LPBK is asserted while holding TX_ELECIDLE deasserted. The TUSB1310A device stops transmitting data to the SSTXP/SSTXN signaling pair from the TX_DATA and begins transmitting on the SSTXP/SSTXN signaling pair the data received at the SSRXP/SSRXN signaling pair. This data is not routed through the 8b/10b coding/encoding paths. While in the loopback operation, the received data is still sent to the RX_DATA. The data sent to the RX_DATA is routed through the 10b/8b decoder.

The TX_DETRX_LPBK deassertion terminates the loopback operation and returns to transmitting TX_DATA over the SSTXP/SSTXN signaling pair. The TUSB1310A device only transitions out of loopback on detection of LFPS signaling by transitioning to P2 state and starting the LFPS handshake.

5.3.7 Adaptive Equalizer

The adaptive equalizer dynamically adjusts the forward gain and peaking of the analog equalizer to minimize the jitter at the cross over point of the eye diagram, which allows for greater jitter tolerance in the RX.

5.4 Device Functional Modes

USB 3.0 is a physical SuperSpeed bus combined in parallel with a physical USB 2.0, according to the USB 3.0 Specification. Each PHY operates independently on a separate data bus. Following this specification, the USB architecture of the TUSB1310A device achieves different working modes. Simultaneous operation of USB 3.0 and USB 2.0 modes is not allowed for peripheral devices.

5.4.1 USB 3.0 Mode

At an electrical level, each SuperSpeed differential link is initialized by enabling its receiver termination. The transmitter is responsible for detecting the far end receiver termination as an indication of a bus connection and informing the link layer so the connect status can be factored into link operation and management. The SuperSpeed link is disabled, for example, when the low impedance receiver termination of a port is removed.

5.4.2 USB 2.0 Mode

When the TUSB1310A is connected to an electrical environment that only supports high-speed, full-speed, or low-speed connections, the SuperSpeed USB 3.0 connectivity is disabled. In this case, the USB 2.0 capabilities are compliant with the USB 2.0 specification.

5.4.3 ULPI Modes

The TUSB1310A device supports synchronous mode and low-power mode. The default mode is synchronous mode.

The synchronous mode is a normal operation mode. The ULPI_DATA are synchronous to ULPI_CLK. The low-power mode is used during power down and no ULPI_CLK. The TUSB1310A device sets ULPI_DIR to output and drives LineState signals and interrupts.

Table 5-9. ULPI Synchronous and Low-Power Mode Functions

SYNCHRONOUS	LOW POWER
ULPI_CLK(OUT)	
ULPI_DATA7(I/O)	
ULPI_DATA6(I/O)	
ULPI_DATA5(I/O)	
ULPI_DATA4(I/O)	

Table 5-9. ULPI Synchronous and Low-Power Mode Functions (continued)

SYNCHRONOUS	LOW POWER
ULPI_DATA3(I/O)	ULPI_INT (OUT)
ULPI_DATA2(I/O)	
ULPI_DATA1(I/O)	ULPI_LINESTATE1(OUT)
ULPI_DATA0(I/O)	ULPI_LINE_STATE0 (OUT)
ULPI_DIR(OUT)	
ULPI_STP(IN)	
ULPI_NXT(OUT)	

5.5 Register Maps

Table 5-10. Register Definitions

ACCESS CODE	EXPANDED NAME	DESCRIPTION
Rd	Read	Register can be read. Read-only if this is the only mode given.
Wr	Write	Pattern on the data bus is written over all bits of the register.
S	Set	Pattern on the data bus is OR'd with and written into the register.
C	Clear	Pattern on the data bus is a mask. If a bit in the mask is set, then the corresponding register bit is set to zero (cleared).

The TUSB1310A device contains the ULPI registers consisting of an immediate register set and an extended register set.

Table 5-11. Register Map

REGISTER NAME	ADDRESS (6 BITS)			
	Rd	Wr	Set	Clr
IMMEDIATE REGISTER SET				
Vendor ID Low	00h			
Vendor ID High	01h			
Product ID Low	02h			
Product ID High	03h			
Function Control	04h–06h	04h	05h	06h
Interface Control	07h–09h	07h	08h	09h
OTG Control	0Ah–0Ch	0Ah	0Bh	0Ch
USB Interrupt Enable Rising	0Dh–0Fh	0Dh	0Eh	0Fh
USB Interrupt Enable Falling	10h–12h	10h	11h	12h
USB Interrupt Status	13h	13h		
USB Interrupt Latch	14h	14h		
Debug	15h			
Scratch Register	16h–18h	16h	17h	18h
Reserved	19h–2Eh			

5.5.1 Vendor ID and Product ID (00h-03h)

Table 5-12. Vendor ID and Product ID

ADDRESS	BITS	NAME	ACCESS	RESET	DESCRIPTION
00h	7:00	Vendor ID Low	Rd	51h	Lower byte of vendor ID supplied by USB-IF
01h	7:00	Vendor ID High	Rd	04h	Upper byte of vendor ID supplied by USB-IF
02h	7:00	Product ID Low	Rd	10h	Lower byte of vendor ID supplied by vendor
03h	7:00	Product ID High	Rd	13h	Upper byte of vendor ID supplied by vendor

5.5.2 Function Control (04h-06h)

Address: 04h-06h (Read), 04h (Write), 05h (Set), 06h (Clear)

Table 5-13. Function Control

BITS	NAME	ACCESS	RESET	DESCRIPTION
1:0	XcvrSelect	Rd, Wr, S, C	1h	Selects the required transceiver speed 00b : Enable HS transceiver 01b: Enable FS transceiver 10b: Enable LS transceiver 11b: Enable FS transceiver for LS packets (FS preamble is automatically prepended)
2	TermSelect	Rd, Wr, S, C	0	Controls the internal 1.5-kΩ pullup resister and 45-Ω HS terminations. Control over bus resistors changes depending on XcvrSelect, OpMode, DpPulldown and DmPulldown. Because low speed peripherals never support full speed or hi-speed, providing the 1.5 kΩ on DM for low speed is optional.
4:3	OpMode	Rd, Wr, S, C	00	Selects the required bit encoding style during transmit 00 : Normal operation 01: Nondriving 10: Disable bit-stuff and NRZI encoding 11: Do not automatically add SYNC and EOP when transmitting. Must be used only for HS packets.
5	Reset	Rd, Wr, S, C	0	Active High transceiver reset. After the Link sets this bit, the TUSB1310A device must assert the ULPI_DIR and reset the ULPI. When the reset is completed, the PHY deasserts the ULPI_DIR and automatically clears this bit. After deasserting the ULPI_DIR, the PHY must re-assert the ULPI_DIR and send an RX CMD update on the Link-Layer Controller. The Link-Layer Controller must wait for the ULPI_DIR to deassert before using the ULPI bus. Does not reset the ULPI or ULPI register set.
6	SuspendM	Rd, Wr, S, C	1h	Active low PHY suspend. Put the TUSB1310A device into low-power mode. The PHY can power down all blocks except the full speed receiver, OTG com-parators, and the ULPI pins. The PHY must automatically set this bit to 1 when low-power mode is exited. 0: Low-power mode 1: Powered
7	Reserved	Rd	0	Reserved

5.5.3 Interface Control (07h-09h)

Address: 07-09h (Read), 07h (Write), 08h (Set), 09h (Clear)

Table 5-14. Interface Control

BITS	NAME	ACCESS	RESET	DESCRIPTION
0	Reserved	Rd	0b	Reserved, only write a 0 to this bit
1	Reserved	Rd	0b	Reserved, only write a 0 to this bit
2	Reserved	Rd	0h	Reserved
3	ClockSuspendM	Rd, Wr, S, C	0b	Active low clock suspend. Valid only in serial mode. Powers down the internal clock circuitry only. Valid only when SuspendM = 1. The TUSB1310A device must ignore ClockSuspend when SuspendM = 0. By default, the clock is not be powered in serial mode. 0 : Clock is not powered in serial mode 1 : Clock is powered in serial mode
6:4	Reserved	Rd	0h	Reserved
7	Interface Protect Disable	Rd, Wr, S, C	0	Controls internal pull-ups and pull-downs on both the ULPI_STP and the ULPI_DATA for protecting the ULPI when the Link-Layer Controller puts the signals to tri-state value. 0 Enables the pullup and pulldown 1 Disables the pullup and pulldown

5.5.4 OTG Control

Address: 0Ah-0Ch (Read), 0Ah (Write), 0Bh (Set), 0Ch (Clear). Controls UTMI+ OTG functions of the PHY.

Table 5-15. OTG Control Register

BITS	NAME	ACCESS	RESET	DESCRIPTION
0	Reserved	Rd	0b	This bit is not implemented and returns a 0b when read
1	DpPulldown	Rd, Wr, S, C	1b	Enables the 15-kΩ pulldown resistor on D+ 0 Pulldown resistor not connected to D+ 1 Pulldown resistor connected to D+
2	DmPulldown	Rd, Wr, S, C	1h	Enables the 15-kΩ pulldown resistor on D– 0 Pulldown resistor not connected to D– 1 Pulldown resistor connected to D–
7:3	Reserved	Rd	0h	These bits are not implemented and return zeros when read

5.5.5 USB Interrupt Enable Rising (0Dh-0Fh)

Address: 0D-0Fh (Read), 0Dh (Write), 0Eh (Set), 0Fh (Clear)

Table 5-16. USB Interrupt Enable Rising

BITS	NAME	ACCESS	RESET	DESCRIPTION
0	Hostdisconnect Rise	Rd, Wr, S, C	1b	Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b).

5.5.6 USB Interrupt Enable Falling (10h-12h)

Address: 10-12h (Read), 10h (Write), 11h (Set), 12h (Clear)

Table 5-17. USB Interrupt Enable Falling

BITS	NAME	ACCESS	RESET	DESCRIPTION
0	Hostdisconnect Fall	Rd, Wr, S, C	1b	Generate an interrupt event notification when Host-disconnect changes from high to low. Applicable only in host.

5.5.7 USB Interrupt Status (13h)

Address: 13h (Read-only)

Table 5-18. USB Interrupt Status

BITS	NAME	ACCESS	RESET	DESCRIPTION
0	Hostdisconnect Fall	Rd, Wr, S, C	1b	Generate an interrupt event notification when Host-disconnect changes from high to low. Applicable only in host.

5.5.8 USB Interrupt Latch (14h)

Address: 14h (Read-only with auto-clear)

Table 5-19. USB Interrupt Latch

BITS	NAME	ACCESS	RESET	DESCRIPTION
0	Hostdisconnect Fall	Rd, Wr, S, C	1b	Set to 1b by the PHY when an unmasked event occurs on Host-disconnect. Cleared when this register is read. Applicable only in host mode.

5.5.9 Debug (15h)

Address: 15h (Read-only)

Table 5-20. Debug

BITS	NAME	ACCESS	RESET	DESCRIPTION
0	LineState0	Rd	0	Contains the current value of LineState0
1	LineState1	Rd	0	Contains the current value of LineState1
7:2	Reserved	Rd	0	Reserved

5.5.10 Scratch Register (16-18h)

Address: 16-18h (Read), 16h (Write), 17h (Set), 18h (Clear)

Table 5-21. Scratch Register

BITS	NAME	ACCESS	RESET	DESCRIPTION
7:0	Scratch	Rd, Wr, S, C	00	Empty register byte for testing purposes. Software can read, write, set, and clear this register and the TUSB1310A device functionality is not be affected.

6 Application, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

Texas Instruments' TUSB1310A device is a single port, 5.0-Gbps USB 3.0 physical layer transceiver that is available in a lead-free, 175-ball, 12-mm × 12-mm NFBGA package (ZAY). The link controller interfaces to the TUSB1310A device are through a PIPE (16-bit wide operating at 250 MHz) and a ULPI (8-bit wide operating at 60 MHz) interface. The USB connector interfaces to the TUSB1310A device through a USB 3.0 SuperSpeed USB differential pair (TX and RX) and USB 2.0 differential pair (DP/DM).

6.2 Typical Application

Figure 6-1 represents a typical implementation of the TUSB1310A USB 3.0 physical layer transceiver that operates off of a single crystal or an external reference clock. The reference frequencies are selectable from 20, 25, 30, and 40 MHz. The TUSB1310A device provides a clock to the USB link layer controllers. The single reference clock allows the TUSB1310A device to provide a cost effective USB 3.0 solution with few external components and a minimum implementation cost.

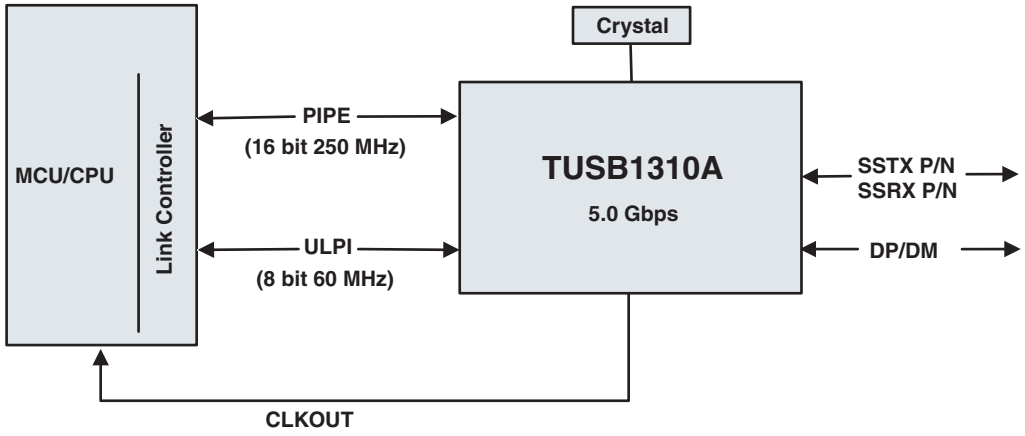


Figure 6-1. Typical Application Schematic

6.2.1 Design Requirements

6.2.1.1 Clock Source Requirements

6.2.1.1.1 Clock Source Selection Guide

Reference clock jitter is an important parameter. Jitter on the reference clock degrades both the transmit eye and receiver jitter tolerance, no matter how clean the rest of the PLL is, thereby impairing system performance. Additionally, a particularly jittery reference clock may interfere with PLL lock detection mechanism, forcing the lock detector to issue an unlock signal. A good quality, low jitter reference clock is required to achieve compliance with supported USB 3.0 standards. For example, USB 3.0 specification requires the random jitter (RJ) component of either RX or TX to be 2.42 ps (random phase jitter calculated after applying jitter transfer function [JTF]). As the PLL typically has a number of additional jitter components, the reference clock jitter must be considerably below the overall jitter budget.

6.2.1.1.2 Oscillator

If an external clock source is used, XI must be tied to the clock source and XO must be left floating.

Table 6-1. Oscillator Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency tolerance	Operational temperature			±50	ppm
Frequency stability	1 year aging			±50	ppm
Rise and Fall time	20% to 80%			6	nsec
Reference clock R_J with JTF (1 sigma) (1)(2)			0.8		psec
Reference clock T_J with JTF (total p-p) (2)(3)			25		psec
Reference clock jitter (absolute p-p) (4)			50		psec

(1) Sigma value assuming Gaussian distribution
(2) After application of JTF
(3) Calculated as $14.1 \times R_J + D_J$
(4) Absolute phase jitter (p-p)

6.2.1.1.3 Crystal

Either a 20-MHz, 25-MHz, 30-MHz, or 40-MHz crystal can be selected. A parallel, 20-pF load crystal must be used if a crystal source is used.

Table 6-2. Crystal Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency tolerance	Operational temperature			±50	ppm
Frequency stability	1 year aging			±50	ppm
Load capacitance		12	20	24	pF

6.2.2 Detailed Design Procedure

6.2.2.1 Chip Connection on PCB

Components must be placed close to the TUSB1310A device to reduce the trace length of the interface between the components and the TUSB1310A. If external capacitors cannot accommodate a close placement, shielding to ground is recommended.

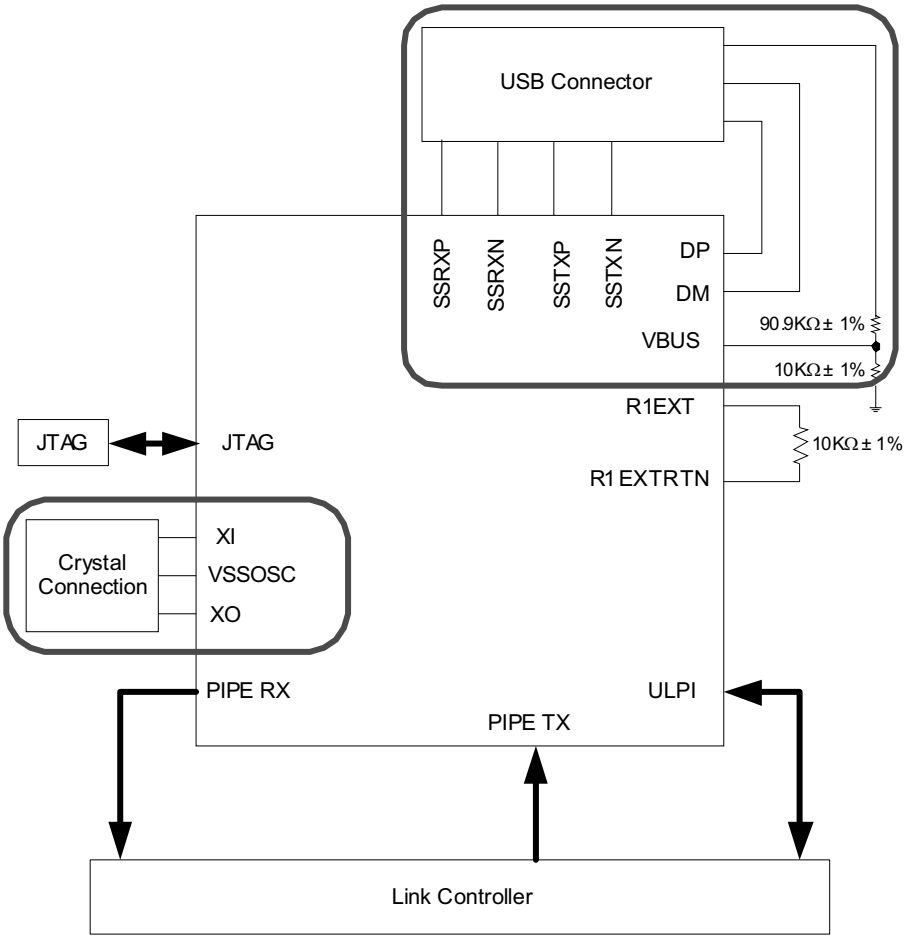


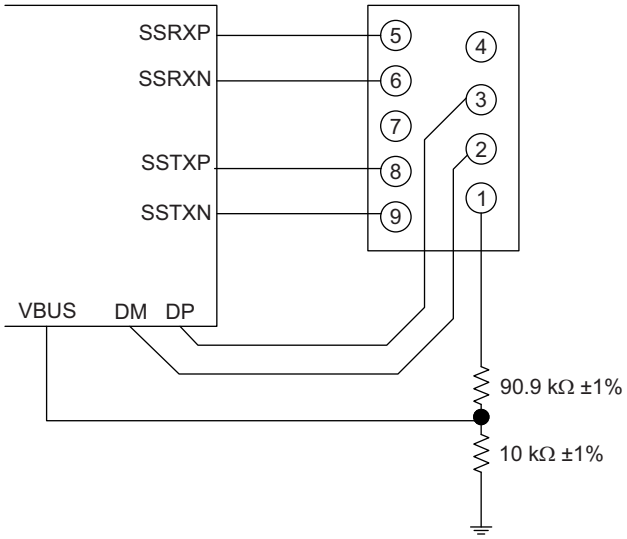
Figure 6-2. Analog Pin Connections

6.2.2.1.1 USB Connector Pins Connection

The following rules apply for differential pair signals (DP/DM, SSTXP/SSTXN, and SSRXP/SSRXN):

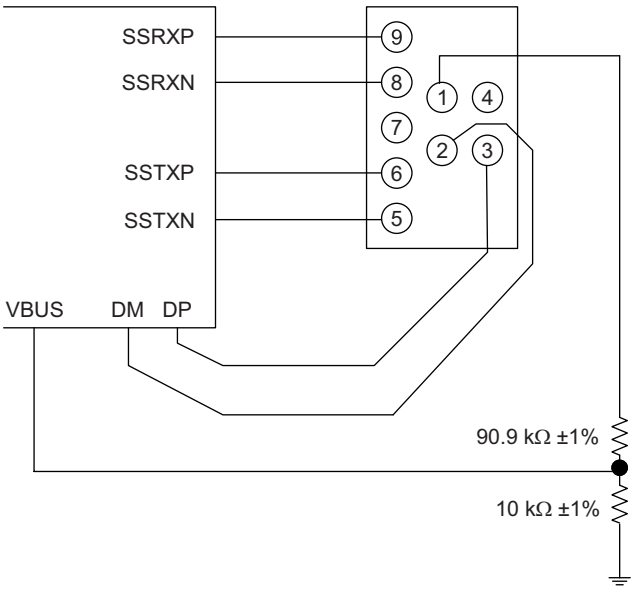
- Keep as short as possible
- Must be trace-length matched and parallelism must be maintained
- Minimize vias and corners
- Avoid crossing plane splits and stubs

Figure 6-3 and Figure 6-4 are for visual reference only.



Pin#	Signal Name
1	VBUS
2	DM
3	DP
4	GND
5	SSRXN
6	SSRXP
7	GND_DRAIN
8	SSTXN
9	SSTXP

Figure 6-3. USB Standard-A Connector Pin Connection



Pin#	Signal Name
1	VBUS
2	DM
3	DP
4	GND
5	SSTXN
6	SSTXP
7	GND_DRAIN
8	SSRXN
9	SSRXP

Figure 6-4. USB Standard-B Connector Pin Connection

6.2.2.1.2 Clock Connections

The TUSB1310A device supports an external oscillator source or a crystal unit. If a clock is provided to XI instead of a crystal, XO is left open. Otherwise, if a crystal is used, the connection must adhere to the following guidelines.

Because XI and XO are coupled to other leads and supplies on the PCB, it is important to keep them as short as possible and away from any switching leads. It is also recommended to minimize the capacitance between XI and XO. This can be accomplished by connecting the VSSOSC lead to the two external capacitors CL1 and CL2 and shielding them with the clean ground lines. The VSSOSC must not be connected to PCB ground.

Load capacitance (C_{LOAD}) of the crystal varying with the crystal vendors is the total capacitance value of the entire oscillation circuit system as seen from the crystal. It includes two external capacitors CL1 and CL2 in Figure 6-5. The trace length between the decoupling capacitors and the corresponding power pins on the TUSB1310A device must be minimized. It is also recommended that the trace length from the capacitor pad to the power or ground plane be minimized.

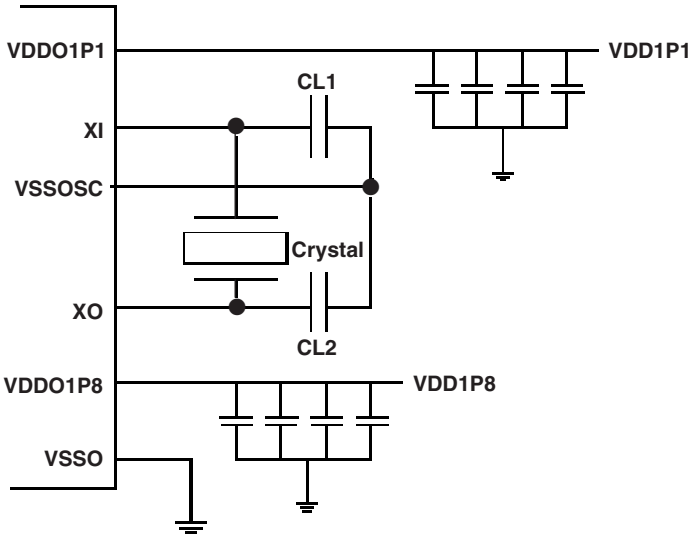


Figure 6-5. Typical Crystal Connections

6.2.3 Application Curve

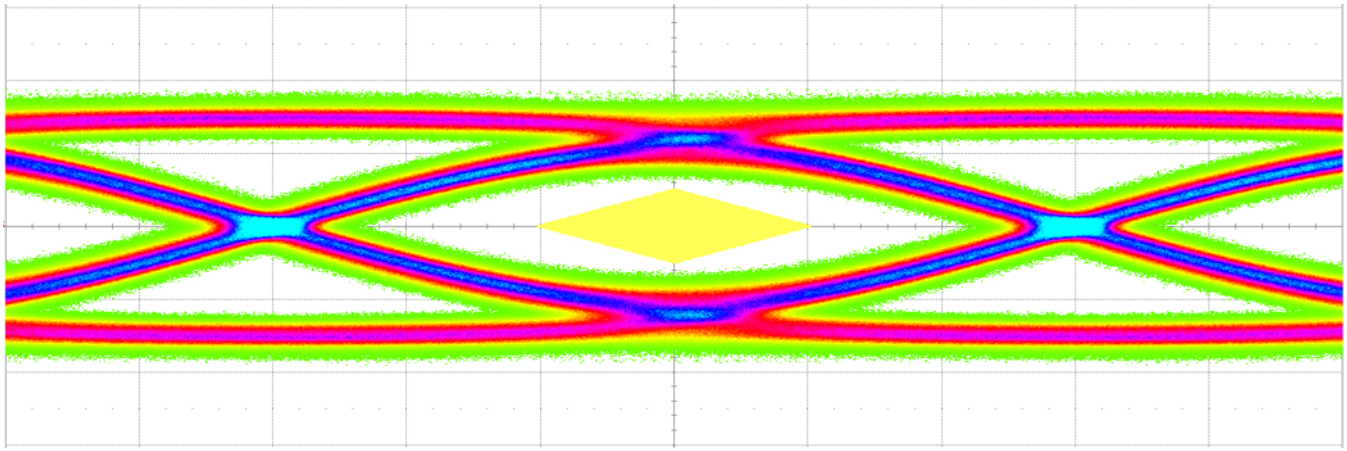


Figure 6-6. Super Speed Eye Diagram

6.2.4 Layout

6.2.4.1 Layout Guidelines

6.2.4.1.1 High-Speed Differential Routing

1. The high-speed differential pair (USB_DM and USB_DP) is connected to a type A USB connecter.
2. The differential pair traces should be routed with 90 Ω ±15% differential impedance.
3. The high-speed signal pair should be trace length matched.
4. Max trace length mismatch between high speed USB signal pairs should be no greater than 150 mils.
5. Keep total trace length to a minimum, if routing longer than eight inches contact TI to address signal integrity concerns.
6. Route differential traces first.
7. Route the differential pairs on the top or bottom layers with the minimum amount of vias possible.
8. No termination or coupling caps are required.
9. If a common mode choke is required then place the choke as close as possible to the USB connector signal pins.
10. Likewise ESD clamps should also be placed as close as possible to the USB connector signal pins (closer than the choke).
11. For more detailed information, refer to *USB 2.0 Board Design and Layout Guidelines* (SPRAAR7), which describes general PCB design and layout guidelines for the USB 2.0 differential pair (DP/DM).

6.2.4.1.2 SuperSpeed Differential Routing

1. SuperSpeed consists of two differential routing pairs: a transmit pair (USB_SSTXM and USB_SSTXP) and a receive pair (USB_SSRXM and USB_SSRXP).
2. Each differential pair trace must be routed with 90 Ω ±15% differential impedance.
3. The high-speed signal pair must be trace-length matched. Maximum trace length mismatch between SuperSpeed USB signal pairs must be no greater than 5 mils. The total length for each differential pair can be no longer than eight inches, which is based on the SuperSpeed USB compliance channel specification and must be avoided if at all possible. TI recommends that the SuperSpeed differential pairs be as short as possible.
4. The transmit differential pair does not have to be the same length as the receive differential pair. Keep total trace length to a minimum. Route differential traces first. Route the differential pairs on the top or bottom layers with the minimum amount of vias possible.
5. The transmitter differential pair requires 0.1-µF coupling capacitors for proper operation. The package or case size of these capacitors must be no larger than 0402. C-packs are not allowed. The capacitors must be placed symmetrically as close as possible to the USB connector signal pins.
6. If a common mode choke is required, place the choke as close as possible to the USB connector signal pins (closer than the transmitter capacitors).
7. Likewise, ESD clamps must also be placed as close as possible to the USB connector signal pins (closer than the choke and transmitter capacitors).

8. It is permissible to swap the plus and minus on either or both of the SuperSpeed differential pairs, which may be necessary to prevent the differential traces from crossing over one another. However, it is not permissible to swap the transmitter differential pair with the receive differential pair.
9. It is recommended to use a 2010 pad for the inside pins, provided no pad is used for adjacent pins. Instead, use a pad on one of the inside pins for the next pad route the trace between the outer pins to a via. There is enough space to route a 3.78-mil trace between the outside pads while leaving 5-mil spacing between the trace and pad; it is then possible to increase the trace width to 4 mils after the breakout.
10. In Figure 6-7 the red pads are USB_SS_RXP/USB_SS_RXN and the blue pads are USB_SS_TXP/USB_SS_TXN.

6.2.4.2 Layout Example

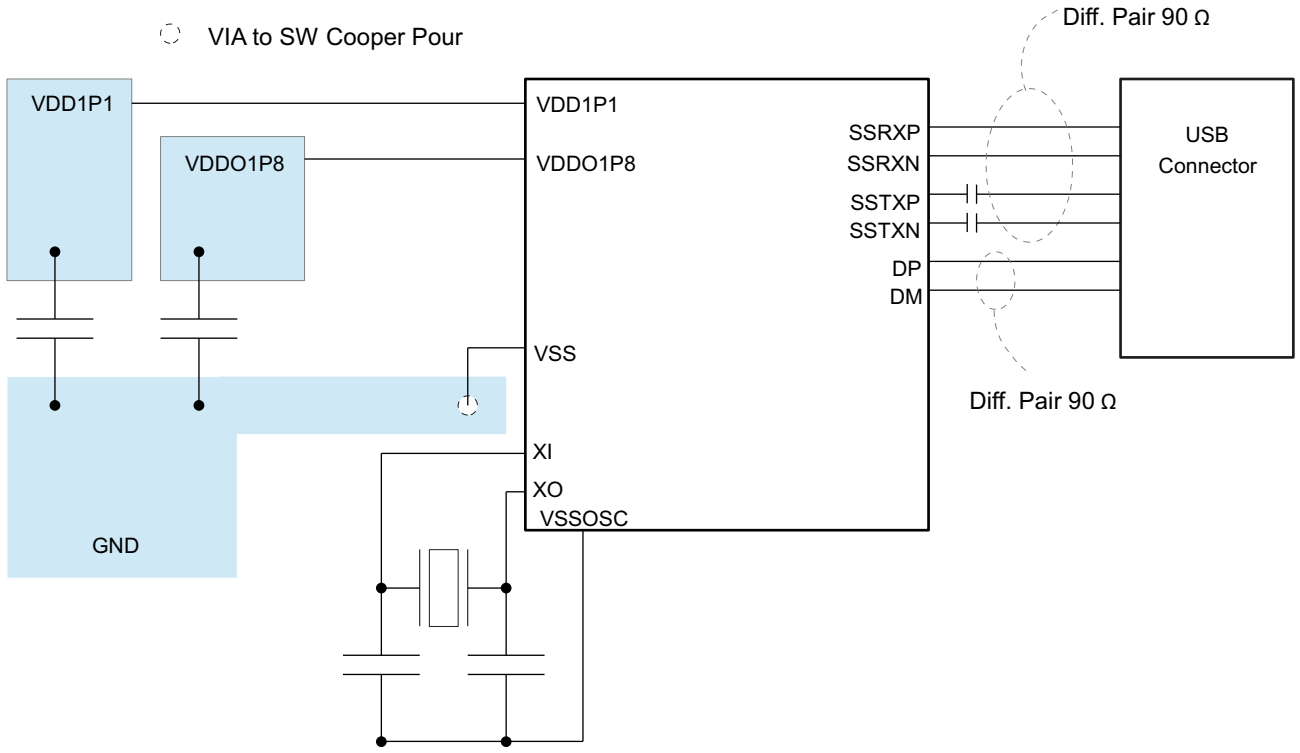


Figure 6-7. Layout Example

6.3 Power Supply Recommendations

6.3.1 1.1-V and 1.8-V Digital Supply

The TUSB1310A requires 1.1-V and 1.8-V digital power sources. Both VDD1P1 and VDD1P8 supplies must have 0.1-μF bypass capacitors to VSS (ground) in order for proper operation. The recommendation is one capacitor for each power terminal. Place the capacitor as close as possible to the terminal on the device and keep trace length to a minimum. Smaller value capacitors like 0.01-μF are also recommended on the digital supply terminals. When placing and connecting all bypass capacitors, high-speed board design rules must be followed.

6.3.2 1.1-V, 1.8-V and 3.3-V Analog Supplies

Because circuit noise on the analog power terminals must be minimized, a Pi-type filter is recommended for each supply. Analog power terminals must have a 0.1-μF bypass capacitor connected to VSSA (ground) for proper operation. Place the capacitor as close as possible to the terminal on the device and keep trace length to a minimum. Smaller value capacitors (0.01-μF) are also recommended on the analog supply terminals.

6.3.3 Capacitor Selection Recommendations

When selecting bypass capacitors for the TUSB1310A device, X7R-type capacitors are recommended. The frequency versus impedance curves, quality, stability, and cost of these capacitors make them a logical choice for most computer systems.

The selection of bulk capacitors with low-ESR specifications is recommended to minimize low frequency power supply noise. Today, the best low-ESR bulk capacitors are radial leaded aluminum electrolytic capacitors. These capacitors typically have ESR specifications that are less than 0.01 Ω at 100 kHz. Also, several manufacturers sell D-size surface mount specialty polymer solid aluminum electrolytic capacitors with ESR specifications slightly higher than 0.01 Ω at 100 kHz. Both of these bulk capacitor options significantly reduce low frequency power supply noise and ripple.

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

The following documents describe the TUSB1310A transceiver. Copies of these documents are available on the Internet at www.ti.com.

(SPRAAR7) *High-Speed Interface Layout Guidelines*

(SPRAA99) *nFBGA Packaging*

(SLLU123) *TUSB1310 Implementation Guide*

(SLLZ063) *TUSB1310A Errata*

7.1.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

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7.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.4 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB1310AZAY	NRND	NFBGA	ZAY	175	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	TUSB1310A	
TUSB1310AZAYR	NRND	NFBGA	ZAY	175	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	TUSB1310A	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

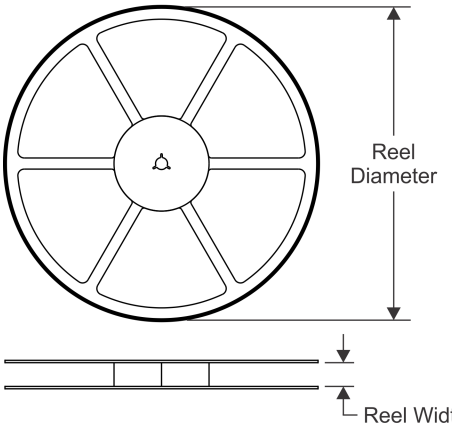
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

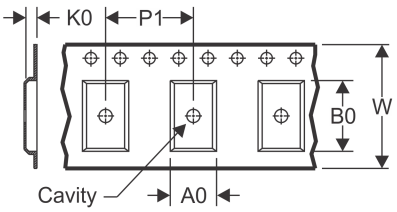
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

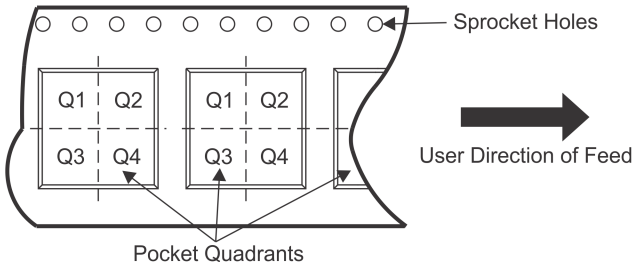


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

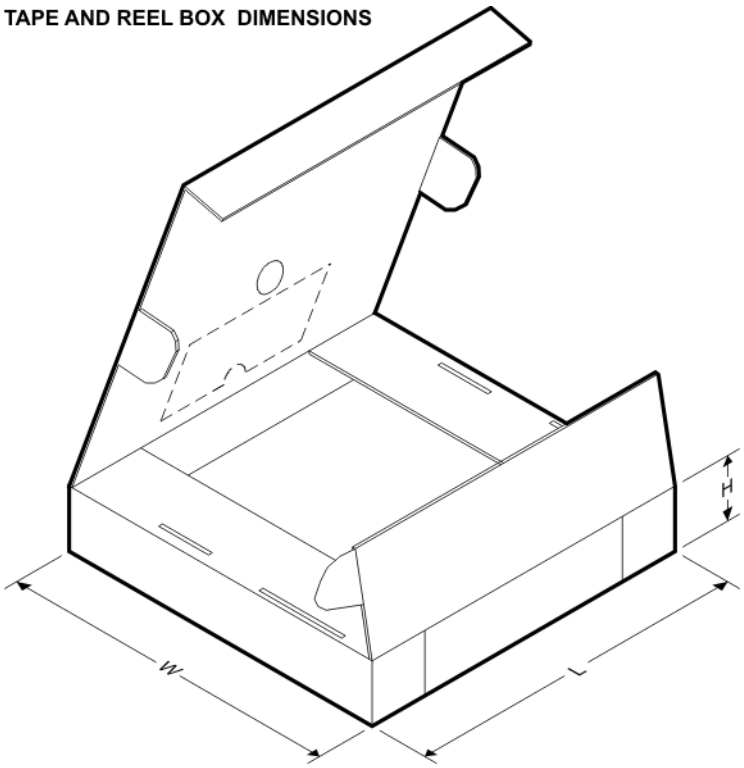
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB1310AZAYR	NFBGA	ZAY	175	1000	330.0	24.4	12.35	12.35	2.3	16.0	24.0	Q1

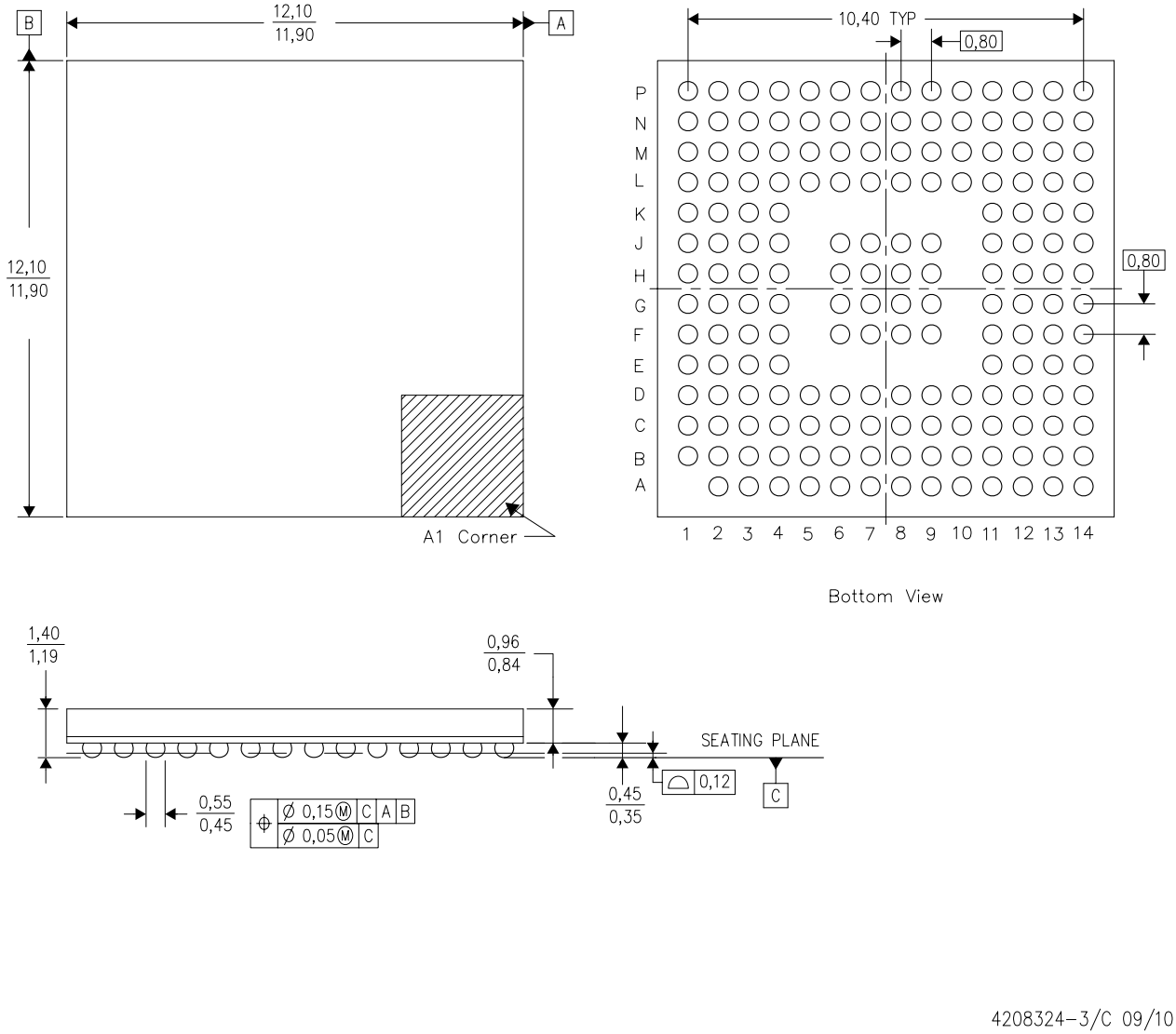
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB1310AZAYR	NFBGA	ZAY	175	1000	336.6	336.6	41.3

ZAY (S–PBGA–N175) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

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