OZ9939

LCDM Inverter Controller

FEATURES

- Negative PWM dimming polarity
- Constant operating frequency
- Drives positive/negative-impedance lamps during ignition
- High drive current for external MOSFETs
- User-defined ignition time and shutdown delay time
- Multiple mode dimming control
- Built-in intelligence for ignition and normal operation of CCFLs
- Built-in open-lamp protection and over-voltage protection for backlight system
- Optimized soft-start function

ORDERING INFORMATION

Part Number	Temp Range	Package
OZ9939G	-20°C to 85°C	16-pin SOIC
OZ9939GN	-20°C to 85°C	16-pin SOIC Lead-Free
OZ9939IG	-40°C to 85°C	16-pin SOIC
OZ9939IGN	-40°C to 85°C	16-pin SOIC Lead-Free
OZ9939D	-20°C to 85°C	16-pin DIP
OZ9939DN	-20°C to 85°C	16-pin DIP Lead-Free

GENERAL DESCRIPTION

The OZ9939 is a high performance, cost-effective CCFL (Cold Cathode Fluorescent Lamp) controller designed for driving large-size Liquid Crystal Display (LCD) applications requiring 2 to 6 CCFLs.

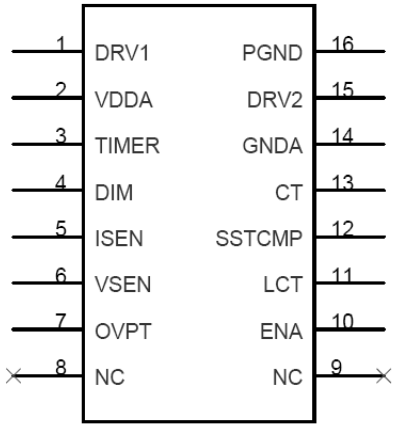
The controller converts unregulated DC voltages into a nearly sinusoidal lamp voltage and current waveforms.

The OZ9939 provides two drive signals for most power conversion topologies while maintaining high-efficiency operation. The PWM controller provides a soft-start operation, current and voltage regulation, over-voltage and over-current protection, high drive capability and multiple dimming functions (internal PWM or external PWM or analog dimming functions).

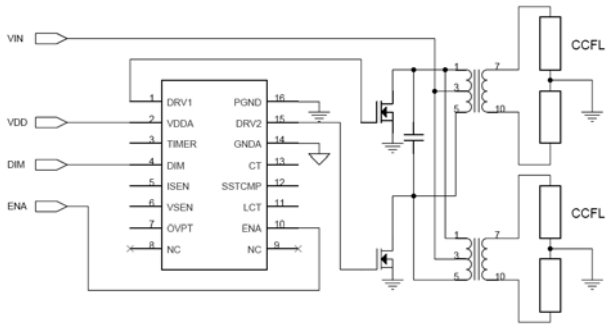
The control logic provides a regulated ignition voltage and appropriate protection features for over-voltage or over-current conditions.

The OZ9939 offers a high level of integration, while maintaining flexibility and high-efficiency operation that reduces external component heating, resulting in higher reliability and longer CCFL life. The proprietary design technique provides a simple, low-cost system solution.

PIN DIAGRAM



SIMPLIFIED APPLICATION CIRCUIT



PIN DESCRIPTION

Pin No.	Names	Description
1	DRV1	Drive output
2	VDDA	Supply voltage input
3	TIMER	Timing capacitor to set striking time and shutdown delay time
4	DIM	Analog dimming or Internal LPWM dimming or external PWM pulse input for dimming function
5	ISEN	Current sense feedback
6	VSEN	Voltage sense feedback
7	OVPT	Over-voltage/ over-current protection threshold setting pin
8	NC	No connection
9	NC	No connection
10	ENA	ON/OFF control of IC
11	LCT	Timing capacitor to set internal PWM dimming frequency and also a pin for analog dimming selection
12	SSTCMP	Capacitor for soft start time and loop compensation
13	CT	Timing resistor and capacitor for operation and striking frequency
14	GNDA	Ground for analog signals
15	DRV2	Drive output
16	PGND	Ground for power paths

ABSOLUTE MAXIMUM RATINGS(1)

Input Voltage VDDA	7.0V
GNDA	+/- 0.3V
Signal Inputs	-0.3V to VDDA +0.3V

Operating Temp.	OZ9939	OZ9939I
	-20°C to 85°C	-40°C to 85°C

Operating Junction Temp.	125°C
Storage Temp.	-55°C to 150°C

RECOMMENDED OPERATING RANGE

VDDA - Input Voltage	4.5V to 5.5V
f_{op} - Operating Frequency	20KHz to 150KHz
Analog Dimming Range	0.7V to 2.1V
Thermal Impedance (θ_{J-A}) - 16-pin SOP - 16-pin DIP	 86 °C/W 56 °C/W

Note (1): The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The "Electrical Characteristics" table defines the conditions for actual device operation. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Conditions		Limits		Unit
		VDDA=5V; Ta=25°C R_{CT} =39Kohm, C_{CT}=470pF R_{LCT} =3.3Mohm, C_{LCT}=4.7nF	Min	Typ	Max	
Supply Current						
Stand By	I_{dds}	ENA=0V		2.0	5.0	μA
Operating	I_{dd}	Capacitance at DRV1 & DRV2=2nF	1.5	2.0	2.5	mA
Soft Start						
Current Source	ISSTCMP		1.83	2.29	2.75	μA
Under Voltage Lockout						
Lock Out	UVLO	VDDA 5V→0V			3.2	V
Resume	UVLO	VDDA 0V→5V	4.0			V
Reference Voltage						
ISEN Reference Voltage		ISEN=SSTCMP	1.12	1.18	1.23	V
		Temperature Coefficient		360		ppm/ °C
VSEN Reference Voltage During Striking		VSEN=SSTCMP	2.78	2.92	3.06	V
		Temperature Coefficient		310		ppm/ °C
Driver Frequency						
Striking	f_{str}		62.6	65.8	69.0	KHZ
		Temperature Coefficient		290		ppm/ °C
Normal Operation	F_{op}		50.0	52.0	54.0	kHz
		Temperature Coefficient		110		ppm/ °C
Timer and Protection						
Striking Current Source		ISEN =0V	2.3	2.9	3.5	uA
Open Lamp and Over Voltage Protection Current Source		SSTCMP > 3.3V or VSEN>OVPT	8.0	10.0	12.0	uA
Protection Release Threshold			2.60	2.81	3.02	V
Drivers						
DRV1/2 Source	Ron			12	18	Ω
DRV1/2 Sink	Ron			5	9	Ω
Maximum Duty Cycle			45			%

ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Symbol	Test Conditions		Limits		Unit
		VDDA=5V; Ta=25°C R_{CT} =39Kohm, C_{CT}=470pF R_{LCT} =3.3Mohm, C_{LCT}=4.7nF	Min	Typ	Max	
PWM Dimming Control						
LCT Frequency			194	200	206	Hz
ENA Threshold						
On					2.0	V
Off			1.0			V

FUNCTIONAL BLOCK DIAGRAM

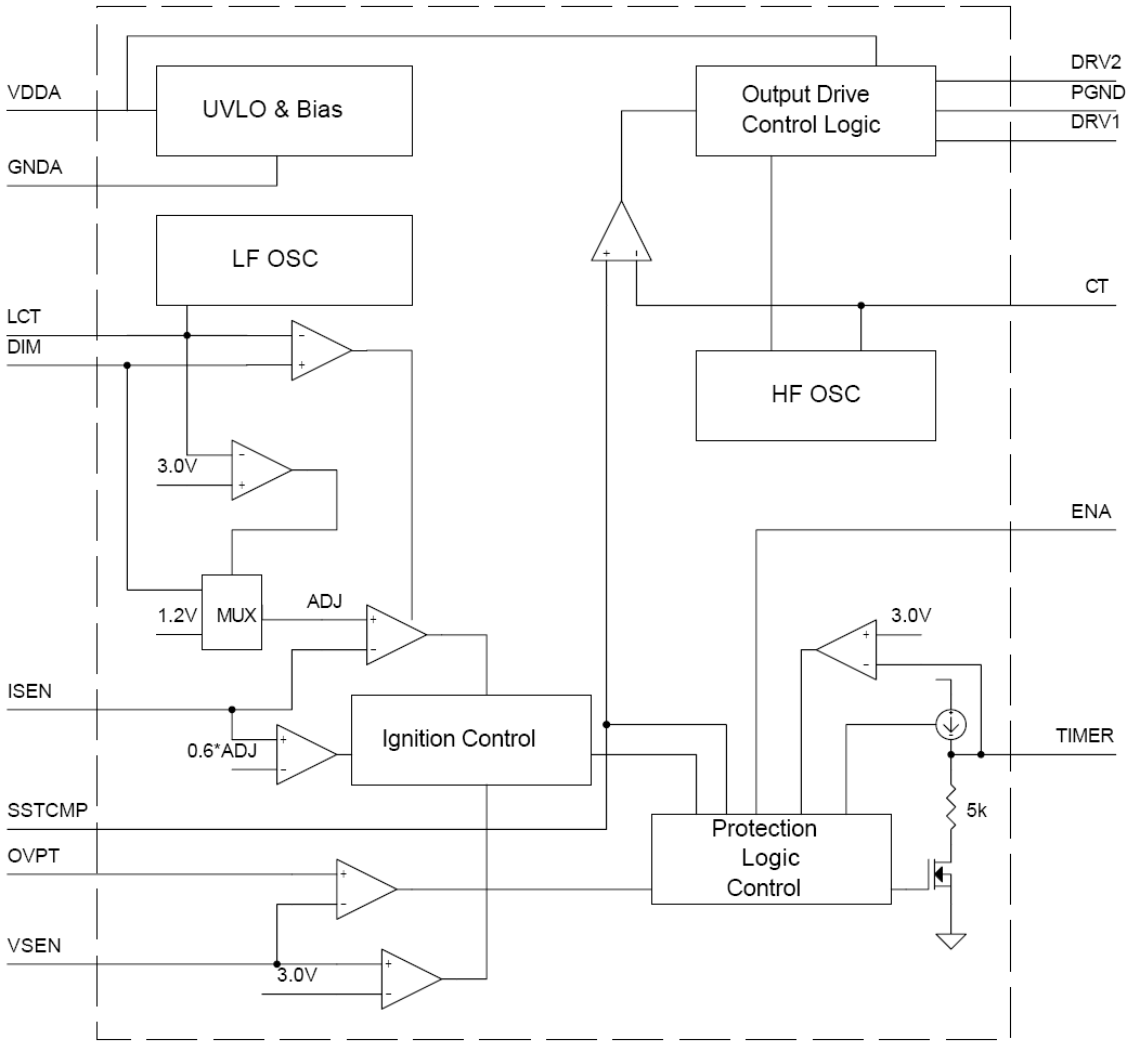


Figure 1

FUNCTIONAL DESCRIPTION

1. Power Conversion

The OZ9939 controller is designed to suit various power conversion topologies and provides symmetrical drive pulses to the tank circuit that includes the transformer(s), output capacitors and the CCFL/panel load that yields quasi-sinusoidal CCFL voltage and current waveforms. High efficiency operation of the OZ9939 yields lower heat dissipation for the inverter system resulting in higher reliability.

To illustrate the controller functions, refer to Figures 1 and 2 on pages 5 and 8, respectively for the following sections.

2. Enable

Applying a voltage level greater than 2V to ENA (pin 10) enables the IC. A voltage less than 1V will disable the IC.

3. Soft-Start (SST)

Utilizing a patented multi-task technique, the soft-start function and the loop compensation function are combined to provide a good start-up characteristic. Connecting an external capacitor to SSTCMP (pin 12) provides the functions. In the start-up mode, current charges capacitor C13 connected to SSTCMP. The voltage at the capacitor controls the gradual increase in power to the transformer and subsequently to the output load. This reduces in-rush current and provides reliable operation to the CCFL.

4. Ignition

When the VDDA voltage exceeds the under-voltage lockout threshold, the IC is enabled an internal striking timer is activated.

The approximate striking frequency is calculated by the following equation.

$$f_{st} = \frac{3812/\ R_{CT}\ [K\Omega] + 26}{4\ *C_{CT}[pF]}\ X1000\ [KHz]$$

5. Aged CCFL Ignition

OZ9939 provides a striking timer function to ensure that any aged, slow-turn-on CCFL is provided with sufficient voltage and time to ignite. The transformer output voltage is sensed at VSEN (Pin 6). When the voltage at VSEN reaches a threshold of approximately 3.0V, the IC regulates the output voltage at the transformer secondary. If the lamps are not ignited when the voltage at TIMER (pin 3) reaches a threshold of approximately 3V, the IC will shutdown and latch

The approximate striking time is calculated by the following equation.

$$T_{str}\ [Sec]\ = C_{TIMER}\ [uF]$$

To resume normal operation, toggle the ENA signal or reset VDDA.

6. Normal Operation

Once the lamps are ignited and the voltage at ISEN (pin 5) is >0.7V, the IC enters the normal operation mode and the PWM dimming control is activated.
The operating frequency is determined by resistor (R9) and capacitor (C9) connected to CT (pin 13). The control loop regulates the average current through the lamps by adjusting the duty cycle of the output drives. Constant frequency operation eliminates interference with the inverter and LCD panel that often occurs in a variable frequency inverter system. The peak and valley of the CT waveform are 2V and 0V respectively.

The approximate operating frequency is calculated by the following equation.

$$f_{op} = \frac{9.53\ x10^{5}}{R_{CT}\ [K\Omega]*C_{CT}[pF]}\ [KHz]$$

7. Open Lamp Protection

If a CCFL is removed or damaged during normal operation, the voltage at SSTCMP (pin 12) rises rapidly. When the voltage at SSTCMP reaches a threshold of approximately 2.5V, a current source charges the capacitor (C17) connected to TIMER (pin 3). Once the voltage level at the TIMER pin reaches a threshold of approximately 3V, the drive outputs shut down and latch.

The shutdown delay feature avoids inverter shutdown due to a VIN transient or if a lamp has a positive impedance characteristic.

The approximate shutdown delay time is calculated by the following equation.

$T_d\ [Sec] = 0.33\ XC_{TIMER}\ [uF]$

To resume operation, toggle the ENA signal or restart VDDA.

8. Over-Voltage and Over-Current Protection

Over-voltage and over-current protection are monitored by the voltage on VSEN (pin 6). During normal operation, if a CCFL is damaged or removed, the voltage at VSEN (pin 6) increases. Once the voltage at VSEN exceeds the user-defined, preset voltage set by OVPT (pin 7), the driver output duty cycle is regulated and the shutdown delay timer is activated. OVPT sets the overall protection threshold voltage that is lower than ~3V (VSEN threshold). Once the voltage at TIMR pin reaches ~3V, the IC will shut down and latch. OVPT voltage setting is determined by a resistor divider (R13 and R16) connected to the OVPT.

The approximate shutdown delay time is calculated by the following equation.

T_d [Sec] = 0.33 XC_{TIMER} [uF]

To resume operation, toggle the PWM signal or restart VDDA.

9. Dimming Control

A built-in function enables the user to select one of the following dimming controls: analog, internal LPWM or external PWM signal.

Analog dimming control is activated when the voltage to LCT (pin 11) is greater than 3V. A voltage of 0.5V to 1.25V applied to DIM (pin 4) controls the amplitude of the lamp current.

Internal LPWM dimming control is determined by resistor R8 and capacitor C14 connected to LCT. The low frequency sawtooth waveform is compared with the voltage at DIM to generate the LPWM signal. The peak and valley of the waveform are 1.5V and 0.1V respectively.
The frequency is approximated by the following equation:

$$f_{LOSC} = \frac{3102}{R_{LCT}\,[M\Omega]*C_{LCT}[nF]} \quad [Hz]$$

With negative PWM dimming polarity, the LPWM duty cycle will be 100% when DIM pin voltage is lower than 0.1V. LCD panel will have maximum brightness. When DIM pin voltage is higher than 1.5V, the LPWM duty cycle will be 0%. LCD panel will be totally dark.

External PWM dimming is implemented by setting LCT to a DC voltage between 0.5V to 1.0V using a resistor divider (R8 and R17) between VDDA and GND. Apply the external PWM pulse to DIM (pin 4).
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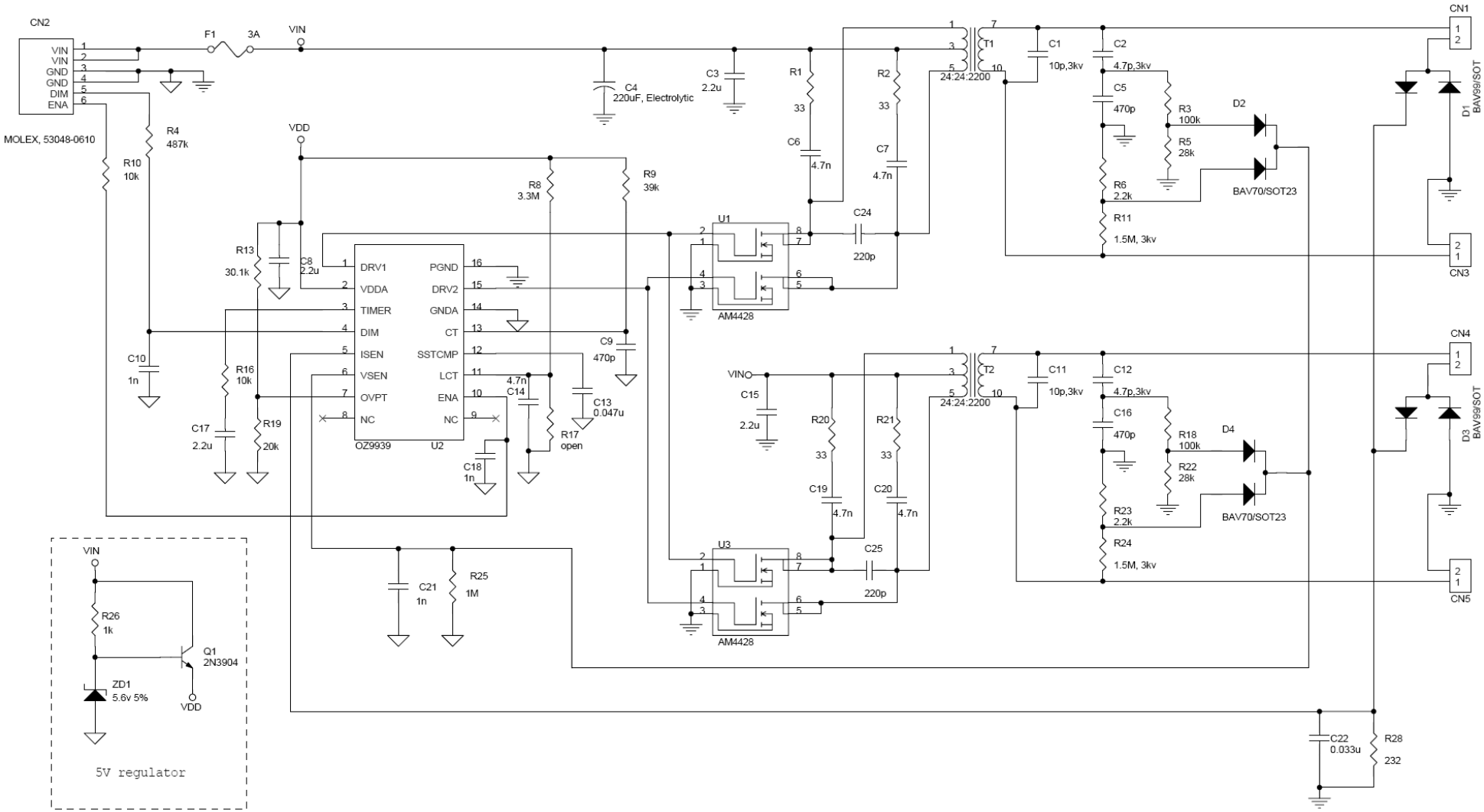
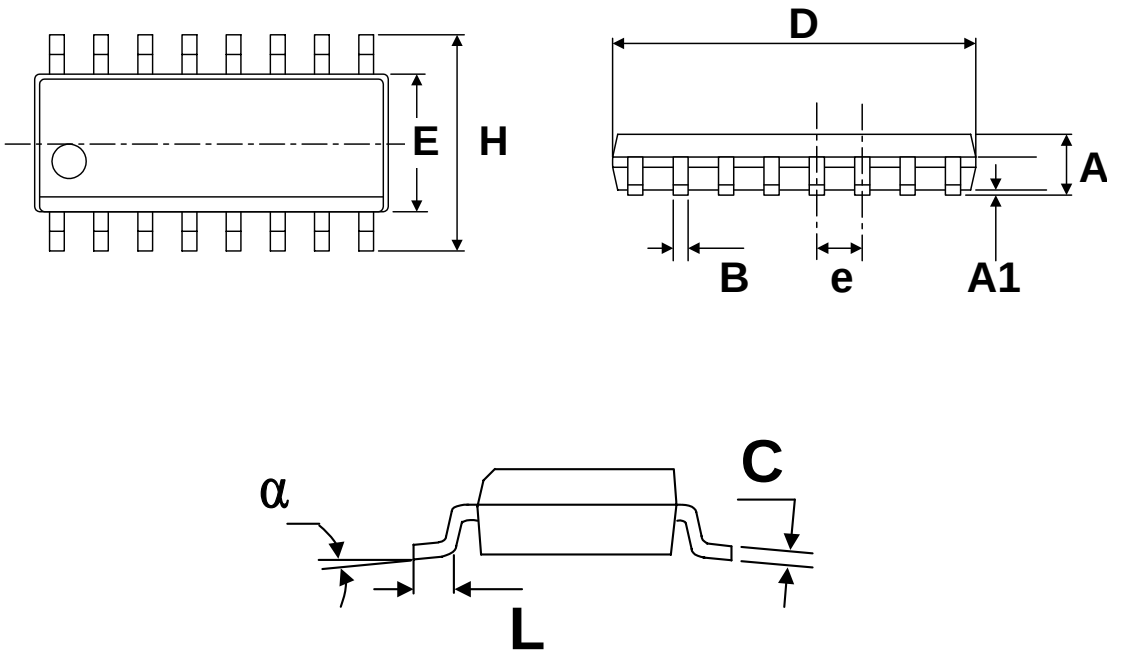
REFERENCE APPLICATION CIRCUIT



VIN: 10.8V---13.2V
ENA: 0V---1.0V, disable. 2.0V---5.0V, Enable
DIM: 0V---1.3V; 0V, maximum brightness; 1.3V, minimum brightness

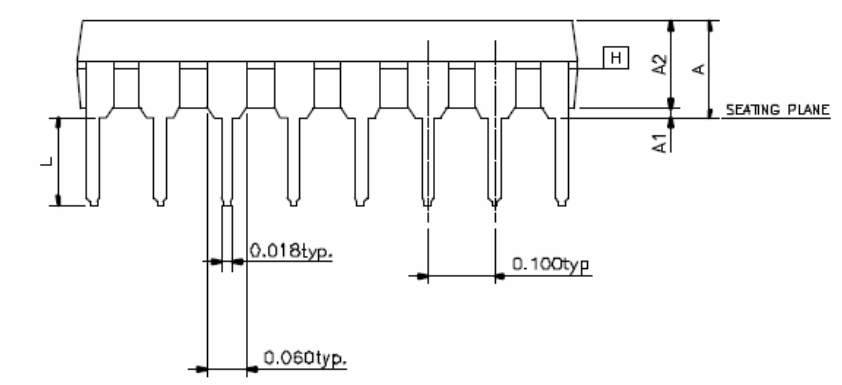
Figure 2

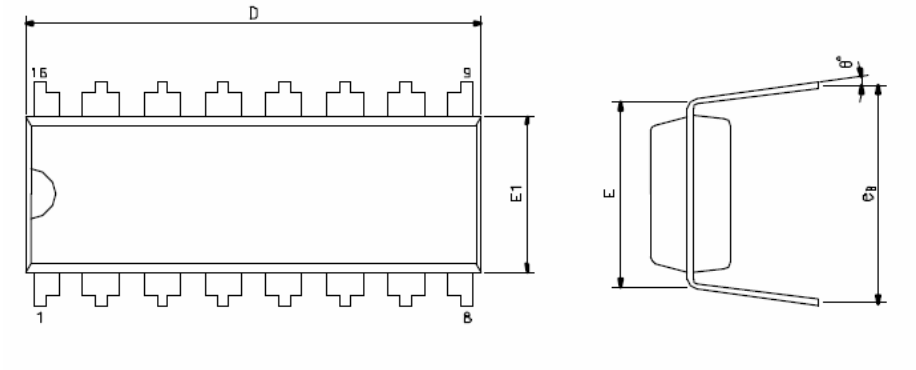
PACKAGE INFORMATION – 16-PIN SOP: OZ9939G (150mil)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	**0.0532**	**0.0688**	**1.35**	**1.75**
A1	**0.0040**	**0.0098**	**0.10**	**0.25**
B	**0.013**	**0.020**	**0.33**	**0.51**
C	**0.0075**	**0.0098**	**0.19**	**0.25**
D	**0.3859**	**0.3937**	**9.80**	**10.00**
E	**0.1497**	**0.1574**	**3.80**	**4.00**
e	**0.050 BCS.**		**1.27 BCS.**	
H	**0.2284**	**0.2440**	**5.80**	**6.20**
L	**0.016**	**0.050**	**0.40**	**1.27**
α	**0°**	**8°**	**0°**	**8°**

PACKAGE INFORMATION – 16-PIN DIP: OZ9939D (300mil)





SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	0.735	0.755	0.775
E	0.300 BSC.		
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ°	0	7	15

UNIT : INCH

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