LM6211 Low Noise, RRO Operational Amplifier with CMOS Input and 24V Operation

Check for Samples: LM6211

FEATURES

(Typical 24V Supply Unless Otherwise Noted)

- **Supply Voltage Range 5V to 24V**
- **Input Referred Voltage Noise 5.5 nV/√Hz**
- **Unity Gain Bandwidth 20 MHz**
- **1/f Corner Frequency 400 Hz**
- **Slew Rate 5.6 V/µs**
- **Supply Current 1.05 mA**
- **Low Input Capacitance 5.5 pF**
- **Temperature Range -40°C to 125°C**
- **Total Harmonic Distortion 0.01% @ 1 kHz, 600Ω**
- **Output Short Circuit Current 25 mA**

APPLICATIONS

- **PLL Loop Filters**
- **Low Noise Active Filters**
- **Strain Gauge Amplifiers**
- **Low Noise Microphone Amplifiers**

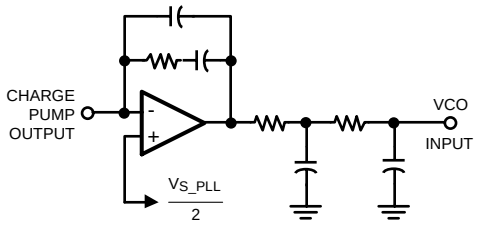
DESCRIPTION

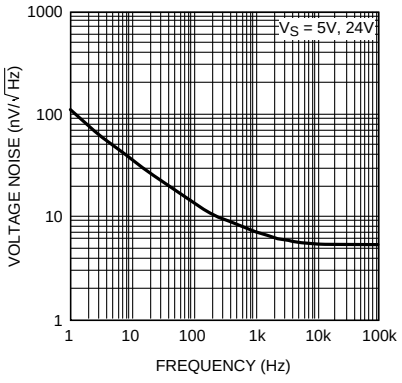
The LM6211 is a wide bandwidth, low noise op amp with a wide supply voltage range and a low input bias current. The LM6211 operates with a single supply voltage of 5V to 24V, is unity gain stable, has a ground-sensing CMOS input stage, and offers rail-to-rail output swing.

The LM6211 is designed to provide optimal performance in high voltage, low noise systems. The LM6211 has a unity gain bandwidth of 20 MHz and an input referred voltage noise density of 5.5 nV/√Hz at 10 kHz. The LM6211 achieves these specifications with a low supply current of only 1 mA. The LM6211 has a low input bias current of 2.3 pA, an output short circuit current of 25 mA and a slew rate of 5.6 V/us. The LM6211 also features a low common-mode input capacitance of 5.5 pF which makes it ideal for use in wide bandwidth and high gain circuits. The LM6211 is well suited for low noise applications that require an op amp with very low input bias currents and a large output voltage swing, like active loop-filters for wide-band PLLs. A low total harmonic distortion, 0.01% at 1 kHz with loads as high as 600Ω, also makes the LM6211 ideal for high fidelity audio and microphone amplifiers.

The LM6211 is available in the small SOT-23 package, allowing the user to implement ultra-small and cost effective board layouts.

Typical Application





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	Human Body Model	2000V
	Machine Model	200V
V_{IN} Differential		±0.3V
Supply Voltage ($V_S = V^+ – V^–$)		25V
Voltage at Input/Output pins		V^+ +0.3V, $V^–$ −0.3V
Storage Temperature Range		−65°C to +150°C
Junction Temperature(4)		+150°C
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering Lead Temp. (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human Body Model is 1.5 kΩ in series with 100 pF. Machine Model is 0Ω in series with 200 pF.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings(1)

Temperature Range		−40°C to +125°C
Supply Voltage ($V_S = V^+ – V^–$)		5V to 24V
Package Thermal Resistance (θ_{JA}(2))	5-Pin SOT-23	178°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

5V Electrical Characteristics(1)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5V, $V^–$ = 0V, $V_{CM} = V_O = V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V		0.1	±2.5 **±2.8**	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0.5V(4)		2		µV/C
I_B	Input Bias Current	V_{CM} = 0.5V(5)(6)		0.5	5 **10**	pA **nA**
I_{OS}	Input Offset Current	V_{CM} = 0.5V		0.1		pA
CMRR	Common Mode Rejection Ratio	0 V ≤ V_{CM} ≤ 3V **0.4 V ≤ V_{CM} ≤ 2.3 V**	83 **70**	98		dB
PSRR	Power Supply Rejection Ratio	V^+ = 5V to 24V, V_{CM} = 0.5V	85 **78**	98		dB
		V^+ = 4.5V to 25V, V_{CM} = 0.5V	80	95		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 65 dB **CMRR ≥ 60 dB**	0 **0**		3.3 **2.4**	V

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using the Statistical Quality Control (SQC) method.
(3) Typical values represent the most likely parametric norm at the time of characterization.
(4) Offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.
(6) Input bias current is ensured by design.

5V Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
A_{VOL}	Large Signal Voltage Gain	V_O = 0.35V to 4.65, R_L = 2 kΩ to $V^+/2$	82 **80**	110		dB
		V_O = 0.25V to 4.75, R_L = 10 kΩ to $V^+/2$	85 **82**	110		
V_O	Output Swing High	R_L = 2 kΩ to $V^+/2$		50	150 **165**	mV from rail
		R_L = 10 kΩ to $V^+/2$		20	85 **90**	
	Output Swing Low	R_L = 2 kΩ to $V^+/2$		39	150 **170**	
		R_L = 10 kΩ to $V^+/2$		13	85 **90**	
I_{OUT}	Output Short Circuit Current	Sourcing to $V^+/2$ V_{ID} = 100 mV[7]	13 **10**	16		mA
		Sinking to $V^+/2$ V_{ID} = −100 mV[7]	20 **10**	30		
I_S	Supply Current			0.96	1.10 **1.25**	mA
SR	Slew Rate	A_V = +1, 10% to 90%[8]		5.5		V/µs
GBW	Gain Bandwidth Product			17		MHz
e_n	Input-Referred Voltage Noise	f = 10 kHz		5.5		nV/√Hz
		f = 1 kHz		6.0		
i_n	Input-Referred Current Noise	f = 1 kHz		0.01		pA/√Hz
THD	Total Harmonic Distortion	A_V = 2, R_L = 600Ω to $V^+/2$		0.01		%

(7) The device is short circuit protected and can source or sink its limit currents continuously. However, care should be taken such that when the output is driving short circuit currents, the inputs do not see more than ±0.3V differential voltage.
(8) Slew rate is the average of the rising and falling slew rates.

24V Electrical Characteristics[1]

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 24V, V^- = 0V, $V_{CM} = V_O = V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V		0.25	±2.7 **±3.0**	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0.5V[4]		±2		µV/C
I_B	Input Bias Current	V_{CM} = 0.5V[5] [6]		2	25 **10**	pA **nA**
I_{OS}	Input Offset Current	V_{CM} = 0.5V		0.1		pA
CMRR	Common Mode Rejection Ratio	0 ≤ V_{CM} ≤ 21V **0.4 ≤ V_{CM} ≤ 20V**	85 **70**	105		dB
PSRR	Power Supply Rejection Ratio	V^+ = 5V to 24V, V_{CM} = 0.5V	85 **78**	98		dB
		V^+ = 4.5V to 25V, V_{CM} = 0.5V	80	98		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 65 dB **CMRR ≥ 60 dB**	0 **0**		21.5 **20.5**	V

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using the Statistical Quality Control (SQC) method.
(3) Typical values represent the most likely parametric norm at the time of characterization.
(4) Offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.
(6) Input bias current is ensured by design.

24V Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 24V, V^- = 0V, $V_{CM} = V_O = V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
A_{VOL}	Large Signal Voltage Gain	V_O = 1.5V to 22.5V, R_L = 2 kΩ to $V^+/2$	82 **77**	120		dB
		V_O = 1V to 23V, R_L = 10 kΩ to $V^+/2$	85 **82**	120		
V_O	Output Swing High	R_L = 2 kΩ to $V^+/2$		212	400 **520**	mV from rail
		R_L = 10 kΩ to $V^+/2$		48	150 **165**	
	Output Swing Low	R_L = 2 kΩ to $V^+/2$		150	350 **420**	
		R_L = 10 kΩ to $V^+/2$		38	150 **170**	
I_{OUT}	Output Short Circuit Current	Sourcing to $V^+/2$ V_{ID} = 100 mV[7]	20 **15**	25		mA
		Sinking to $V^+/2$ V_{ID} = −100 mV [7]	30 **20**	38		
I_S	Supply Current			1.05	1.25 **1.40**	mA
SR	Slew Rate	A_V = +1, V_O = 18 V_{PP} 10% to 90%[8]		5.6		V/µs
GBW	Gain Bandwidth Product			20		MHz
e_n	Input-Referred Voltage Noise	f = 10 kHz		5.5		nV/√Hz
		f = 1 kHz		6.0		
i_n	Input-Referred Current Noise	f = 1 kHz		0.01		pA/√Hz
THD	Total Harmonic Distortion	A_V = 2, R_L = 2 kΩ to $V^+/2$		0.01		%

(7) The device is short circuit protected and can source or sink its limit currents continuously. However, care should be taken such that when the output is driving short circuit currents, the inputs do not see more than ±0.3V differential voltage.
(8) Slew rate is the average of the rising and falling slew rates.

Connection Diagram

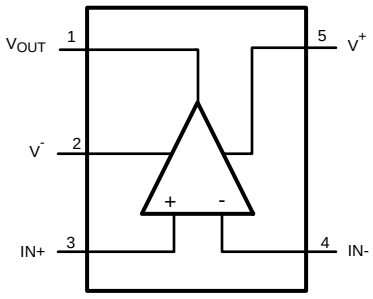


Figure 1. 5-Pin SOT-23 - Top View

Typical Performance Characteristics

Unless otherwise specified, T_A = 25°C, V_S = 24V, $V^+ = V_S$, V^- = 0 V, $V_{CM} = V_S/2$.

Supply Current vs. Supply Voltage

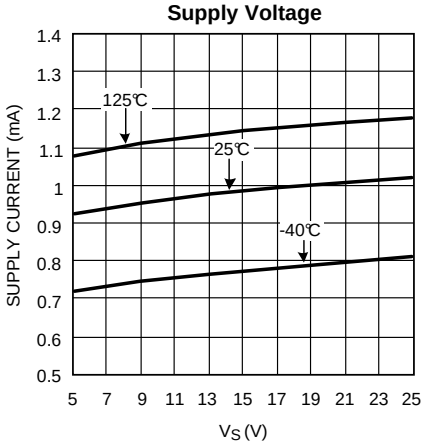


Figure 2.

V_{OS} vs. Supply Voltage

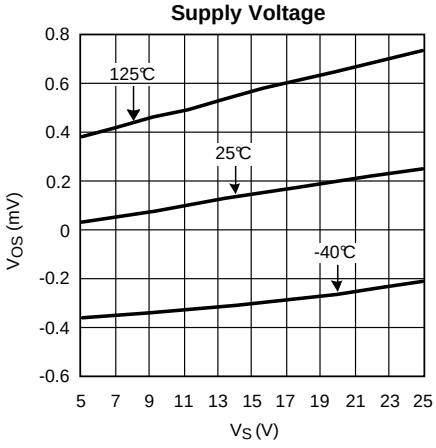


Figure 3.

V_{OS} vs. V_{CM}

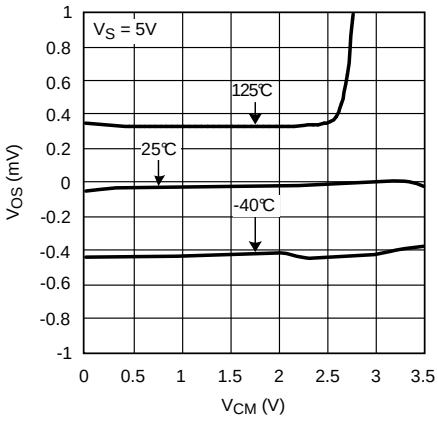


Figure 4.

V_{OS} vs. V_{CM}

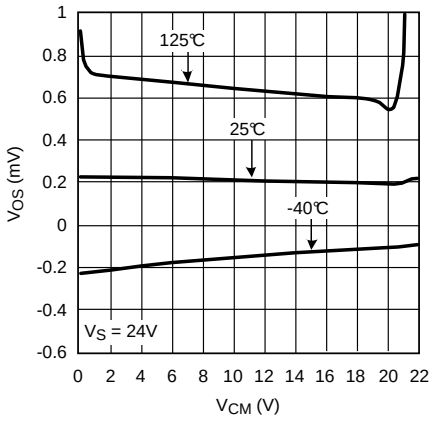


Figure 5.

Input Bias Current vs. V_{CM}

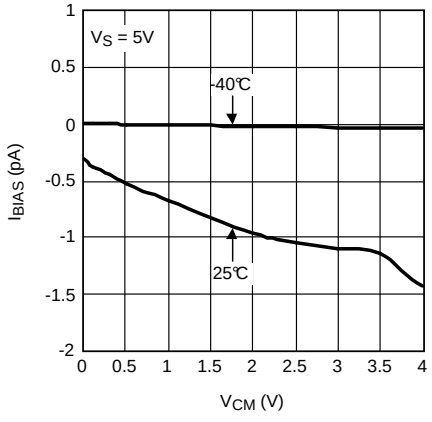


Figure 6.

Input Bias Current vs. V_{CM}

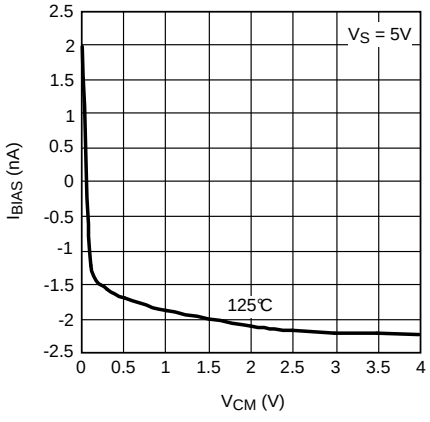


Figure 7.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V_S = 24V, $V^+ = V_S$, V^- = 0 V, $V_{CM} = V_S/2$.

Input Bias Current vs. V_{CM}

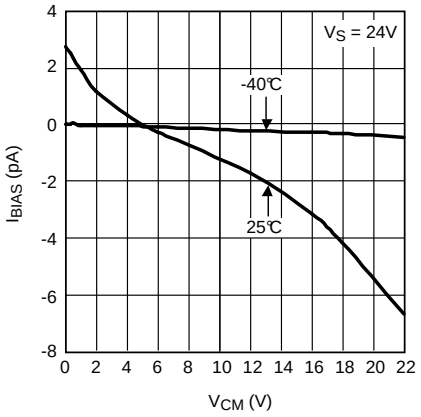


Figure 8.

Input Bias Current vs. V_{CM}

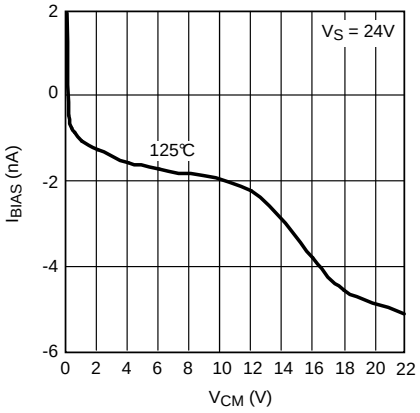


Figure 9.

Sourcing Current vs. Supply Voltage

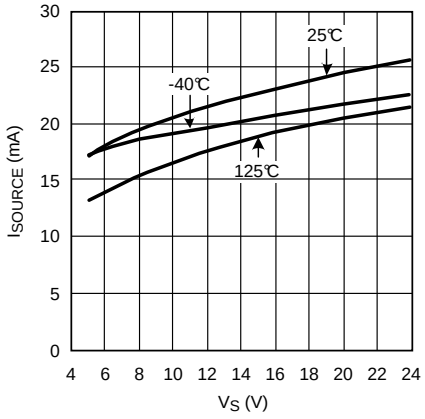


Figure 10.

Sinking Current vs. Supply Voltage

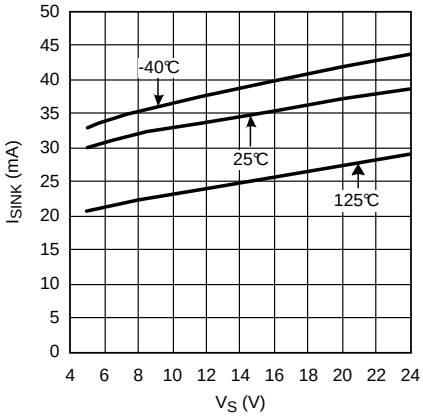


Figure 11.

Positive Output Swing vs. Supply Voltage

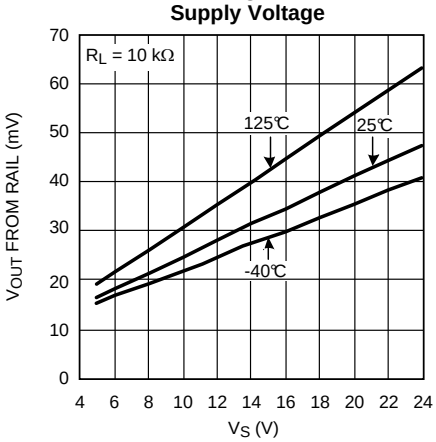


Figure 12.

Negative Output Swing vs. Supply Voltage

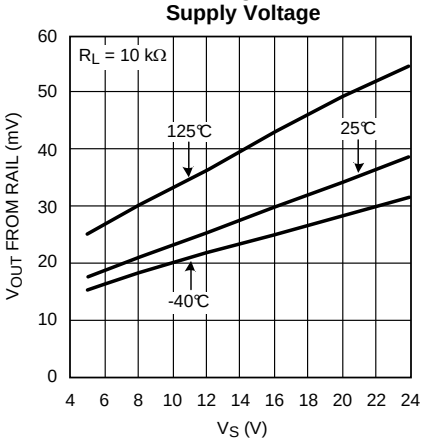


Figure 13.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V_S = 24V, $V^+ = V_S$, $V^- = 0$ V, $V_{CM} = V_S/2$.

Positive Output Swing vs. Supply Voltage

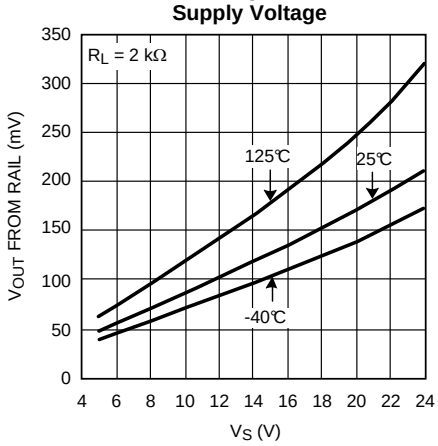


Figure 14.

Negative Output Swing vs. Supply Voltage

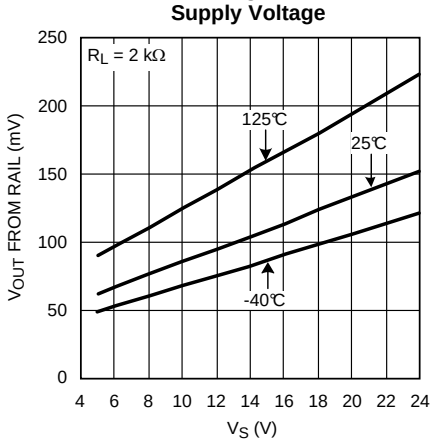


Figure 15.

Sourcing Current vs. Output Voltage

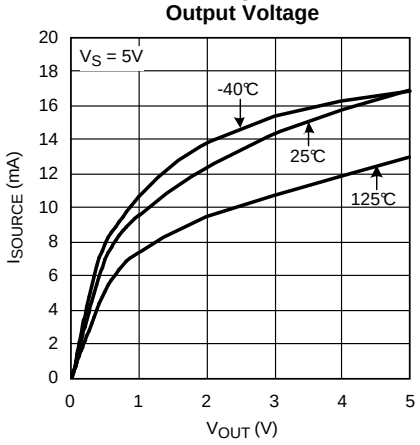


Figure 16.

Sinking Current vs. Output Voltage

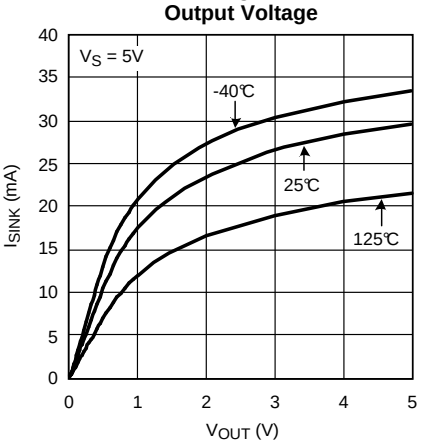


Figure 17.

Sourcing Current vs. Output Voltage

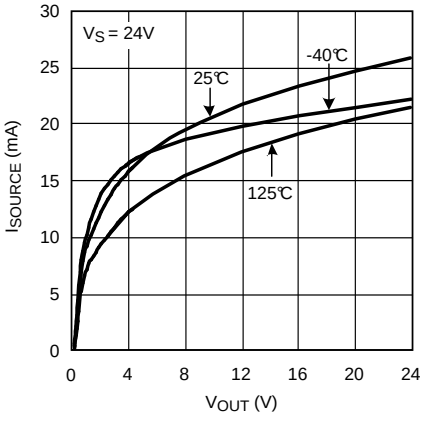


Figure 18.

Sinking Current vs. Output Voltage

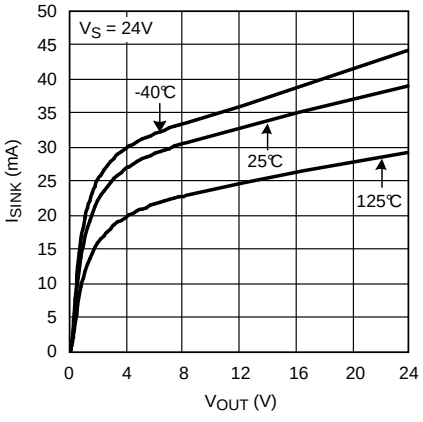


Figure 19.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V_S = 24V, $V^+ = V_S$, V^- = 0 V, $V_{CM} = V_S/2$.

Open Loop Gain and Phase with Resistive Load

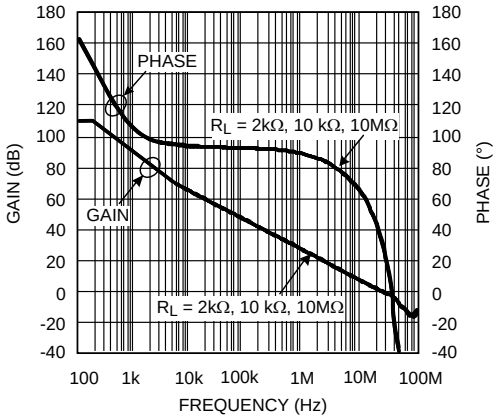


Figure 20.

Open Loop Gain and Phase with Capacitive Load

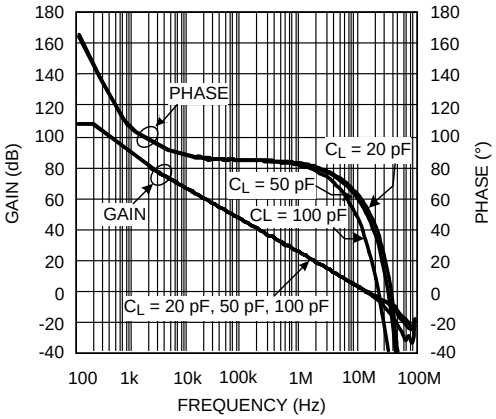


Figure 21.

Input Referred Voltage Noise vs. Frequency

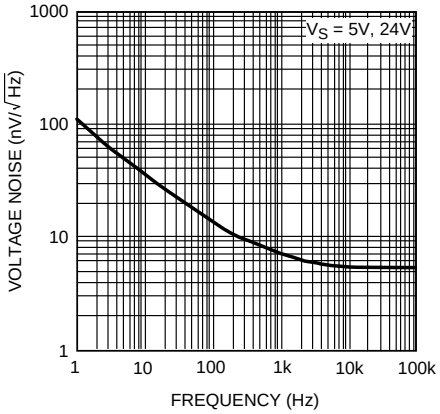


Figure 22.

THD+N vs. Frequency

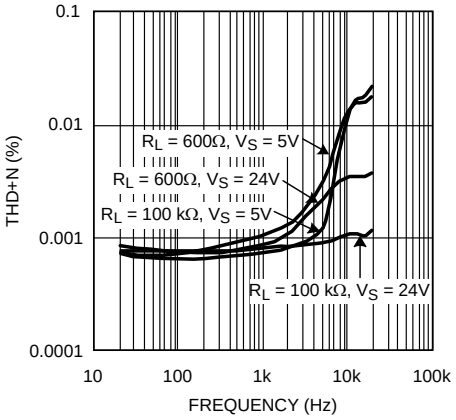


Figure 23.

THD+N vs. Output Amplitude

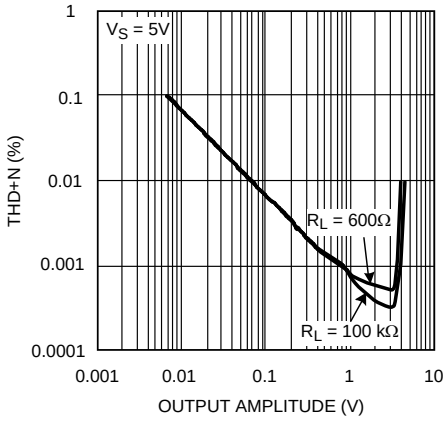


Figure 24.

THD+N vs. Output Amplitude

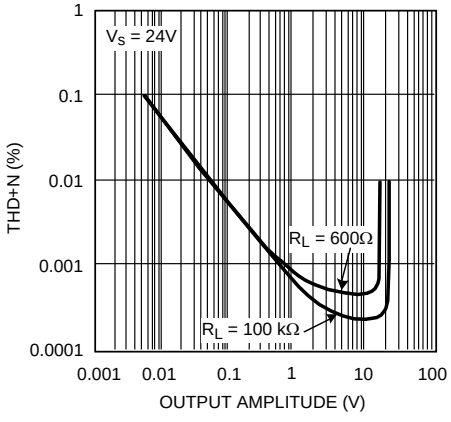


Figure 25.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V_S = 24V, $V^+ = V_S$, $V^- = 0$ V, $V_{CM} = V_S/2$.

Slew Rate vs. Supply Voltage

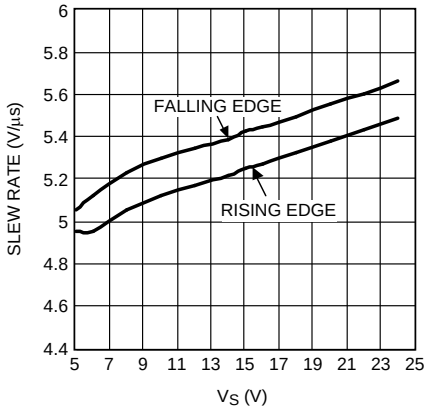


Figure 26.

Overshoot and Undershoot vs. Capacitive Load

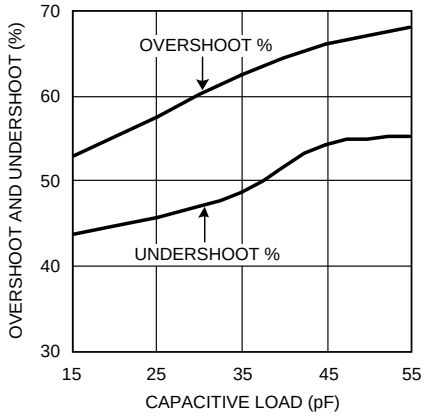


Figure 27.

Small Signal Transient Response

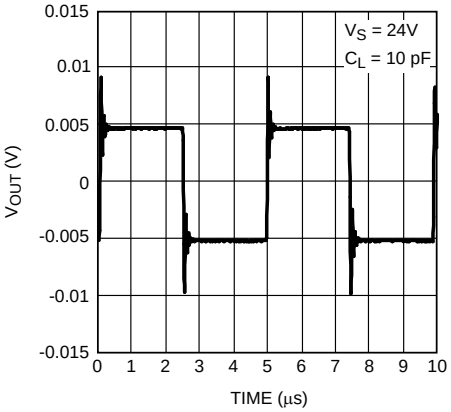


Figure 28.

Large Signal Transient Response

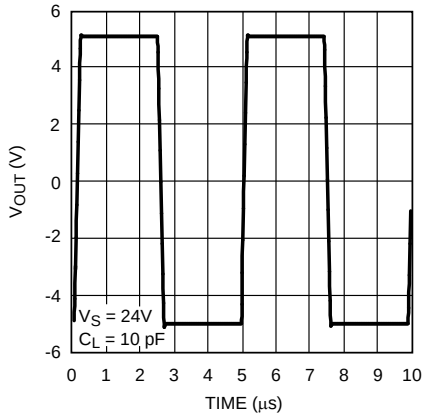


Figure 29.

Phase Margin vs. Capacitive Load (Stability)

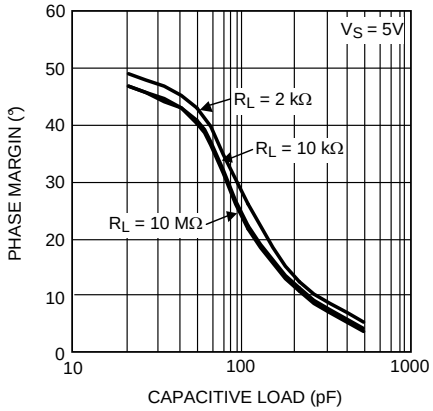


Figure 30.

Phase Margin vs. Capacitive Load (Stability)

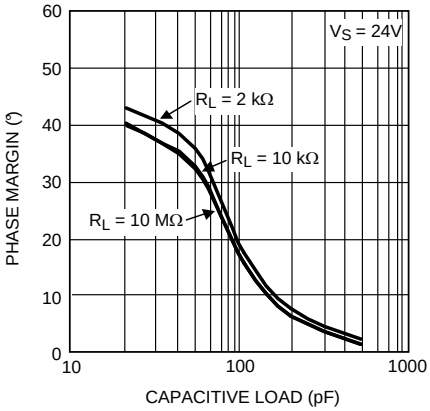


Figure 31.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V_S = 24V, $V^+ = V_S$, $V^- = 0$ V, $V_{CM} = V_S/2$.

Closed Loop Output Impedance vs. Frequency

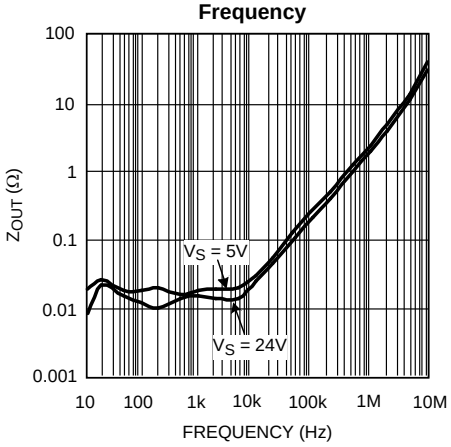


Figure 32.

PSRR vs. Frequency

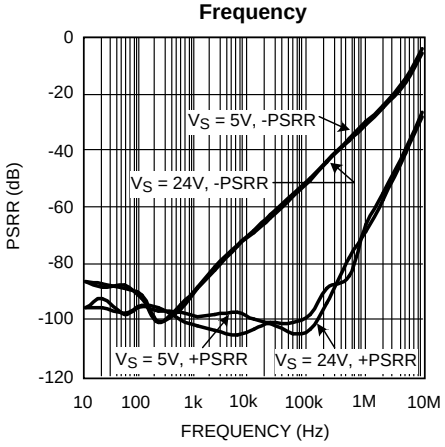


Figure 33.

CMRR vs. Frequency

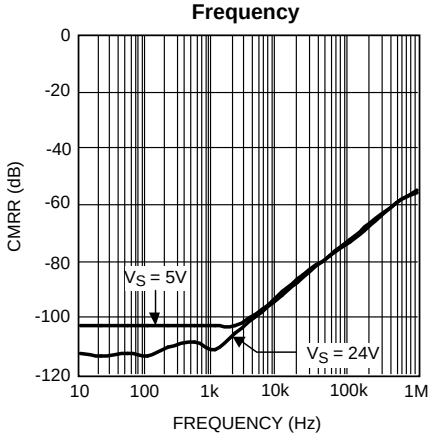


Figure 34.

APPLICATION NOTES

ADVANTAGES OF THE LM6211

High Supply Voltage, Low Power Operation

The LM6211 has performance ensured at supply voltages of 5V and 24V. The LM6211 is ensured to be operational at all supply voltages between 5V and 24V. In this large range of operation, the LM6211 draws a fairly constant supply current of 1 mA, while providing a wide bandwidth of 20 MHz. The wide operating range makes the LM6211 a versatile choice for a variety of applications ranging from portable instrumentation to industrial control systems.

Low Input Referred Noise

The LM6211 has very low flatband input referred voltage noise, 5.5 nV/$\sqrt{Hz}$. The 1/f corner frequency, also very low, is about 400 Hz. The CMOS input stage allows for an extremely low input current (2 pA) and a very low input referred current noise (0.01 pA/$\sqrt{Hz}$). This allows the LM6211 to maintain signal fidelity and makes it ideal for audio, wireless or sensor based applications.

Low Input Bias Current and High Input Impedance

The LM6211 has a CMOS input stage, which allows it to have very high input impedance, very small input bias currents (2 pA) and extremely low input referred current noise (0.01 pA/$\sqrt{Hz}$). This level of performance is essential for op amps used in sensor applications, which deal with extremely low currents of the order of a few nanoamperes. In this case, the op amp is being driven by a sensor, which typically has a source impedance of tens of MΩ. This makes it essential for the op amp to have a much higher impedance.

Low Input Capacitance

The LM6211 has a comparatively small input capacitance for a high voltage CMOS design. Low input capacitance is very beneficial in terms of driving large feedback resistors, required for higher closed loop gain. Usually, high voltage CMOS input stages have a large input capacitance, which when used in a typical gain configuration, interacts with the feedback resistance to create an extra pole. The extra pole causes gain-peaking and can compromise the stability of the op amp. The LM6211 can, however, be used with larger resistors due to its smaller input capacitance, and hence provide more gain without compromising stability. This also makes the LM6211 ideal for wideband transimpedance amplifiers, which require a wide bandwidth, low input referred noise and low input capacitance.

RRO, Ground Sensing and Current Limiting

The LM6211 has a rail-to-rail output stage, which provides the maximum possible output dynamic range. This is especially important for applications requiring a large output swing, like wideband PLL synthesizers which need an active loop filter to drive a wide frequency range VCO. The input common mode range includes the negative supply rail which allows direct sensing at ground in a single supply operation. The LM6211 also has a short circuit protection circuit which limits the output current to about 25 mA sourcing and 38 mA sinking, and allows the LM6211 to drive short circuit loads indefinitely. However, while driving short circuit loads care should be taken to prevent the inputs from seeing more than ±0.3V differential voltage, which is the absolute maximum differential input voltage.

Small Size

The small footprint of the LM6211 package saves space on printed circuit boards, and enables the design of smaller and more compact electronic products. Long traces between the signal source and the op amp make the signal path susceptible to noise. By using a physically smaller package, the LM6211 can be placed closer to the signal source, reducing noise pickup and enhancing signal integrity

STABILITY OF OP AMP CIRCUITS

Stability and Capacitive Loading

The LM6211 is designed to be unity gain stable for moderate capacitive loads, around 100 pF. That is, if connected in a unity gain buffer configuration, the LM6211 will resist oscillation unless the capacitive load is higher than about 100 pF. For higher capacitive loads, the phase margin of the op amp reduces significantly and it tends to oscillate. This is because an op amp cannot be designed to be stable for high capacitive loads without either sacrificing bandwidth or supplying higher current. Hence, for driving higher capacitive loads, the LM6211 needs to be externally compensated.

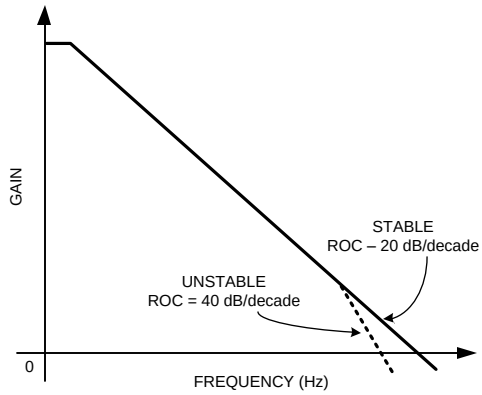


Figure 35. Gain vs. Frequency for an Op Amp

An op amp, ideally, has a dominant pole close to DC, which causes its gain to decay at the rate of 20 dB/decade with respect to frequency. If this rate of decay, also known as the rate of closure (ROC), remains at 20 dB/decade at the unity gain bandwidth of the op amp, the op amp is stable. If, however, a large capacitance is added to the output of the op amp, it combines with the output impedance of the op amp to create another pole in its frequency response before its unity gain frequency (Figure 35). This increases the ROC to 40 dB/decade and causes instability.

In such a case a number of techniques can be used to restore stability to the circuit. The idea behind all these schemes is to modify the frequency response such that it can be restored to a ROC of 20 dB/decade, which ensures stability.

In the Loop Compensation

Figure 36 illustrates a compensation technique, known as 'in the loop' compensation, that employs an RC feedback circuit within the feedback loop to stabilize a non-inverting amplifier configuration. A small series resistance, R_S, is used to isolate the amplifier output from the load capacitance, C_L, and a small capacitance, C_F, is inserted across the feedback resistor to bypass C_L at higher frequencies.

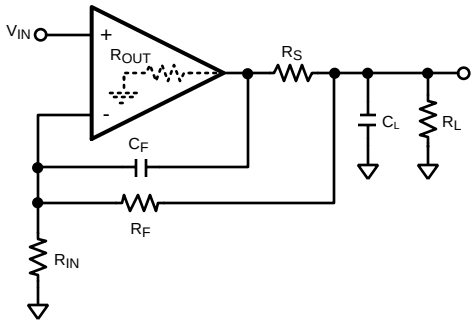


Figure 36. In the Loop Compensation

The values for R_S and C_F are decided by ensuring that the zero attributed to C_F lies at the same frequency as the pole attributed to C_L. This ensures that the effect of the second pole on the transfer function is compensated for by the presence of the zero, and that the ROC is maintained at 20 dB/decade. For the circuit shown in Figure 36 the values of R_S and C_F are given by Equation 1. Table 1 shows different values of R_S and C_F that need to be used for maintaining stability with different values of C_L, as well as the phase margins to be expected. R_F and R_{IN} are assumed to be 10 kΩ, R_L is taken as 2 kΩ, while R_{OUT} is taken to be 60Ω.

$$R_S = \frac{R_{OUT}R_{IN}}{R_F}$$

$$C_F = \left(\frac{R_F + 2R_{IN}}{RF^2}\right) C_L R_{OUT} \quad (1)$$

Table 1.

C_L (pF)	R_S (Ω)	C_F (pF)	Phase Margin (°)
250	60	4.5	39.8
300	60	5.4	49.5
500	60	9	53.1

Although this methodology provides circuit stability for any load capacitance, it does so at the price of bandwidth. The closed loop bandwidth of the circuit is now limited by R_S and C_F.

Compensation by External Resistor

In some applications it is essential to drive a capacitive load without sacrificing bandwidth. In such a case, in the loop compensation is not viable. A simpler scheme for compensation is shown in Figure 37. A resistor, R_{ISO}, is placed in series between the load capacitance and the output. T110his introduces a zero in the circuit transfer function, which counteracts the effect of the pole formed by the load capacitance, and ensures stability.

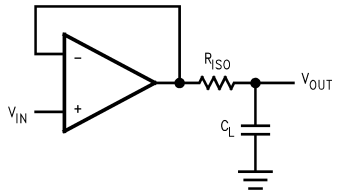


Figure 37. Compensation By Isolation Resistor

The value of R_{ISO} to be used should be decided depending on the size of C_L and the level of performance desired. Values ranging from 5Ω to 50Ω are usually sufficient to ensure stability. A larger value of R_{ISO} will result in a system with lesser ringing and overshoot, but will also limit the output swing and the short circuit current of the circuit.

Stability and Input Capacitance

In certain applications, for example I-V conversion, transimpedance photodiode amplification and buffering the output of current-output DAC, capacitive loading at the input of the op amp can endanger stability. The capacitance of the source driving the op amp, the op amp input capacitance and the parasitic/wiring capacitance contribute to the loading of the input. This capacitance, C_{IN}, interacts with the feedback network to introduce a peaking in the closed loop gain of the circuit, and hence causes instability.

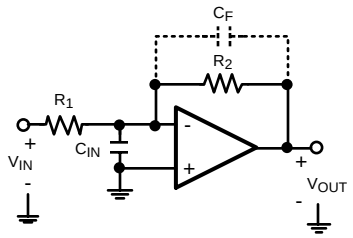


Figure 38. Compensating for Input Capacitance

This peaking can be eliminated by adding a feedback capacitance, C_F, as shown in Figure 38. This introduces a zero in the feedback network, and hence a pole in the closed loop response, and thus maintains stability. An optimal value of C_F is given by Equation 2. A simpler approach is to select $C_F = (R_1/R_2)C_{IN}$ for a 90° phase margin. This approach, however, limits the bandwidth excessively.

Typical Applications

ACTIVE LOOP FILTER FOR PLLs

A typical phase locked loop, or PLL, functions by creating a negative feedback loop in terms of the phase of a signal. A simple PLL consists of three main components: a phase detector, a loop filter and a voltage controlled oscillator (VCO). The phase detector compares the phase of the output of the PLL with that of a reference signal, and feeds the error signal into the loop filter, thus performing negative feedback. The loop filter performs the important function of averaging (or low-pass filtering) the error and providing the VCO with a DC voltage, which allows the VCO to modify its frequency such that the error is minimized. The performance of the loop filter affects a number of specifications of the PLL, like its frequency range, locking time and phase noise.

Since a loop filter is a very noise sensitive application, it is usually suggested that only passive components be used in its design. Any active devices, like discrete transistors or op amps, would add significantly to the noise of the circuit and would hence worsen the in-band phase noise of the PLL. But newer and faster PLLs, like TI's LMX2430, have a power supply voltage of less than 3V, which limits the phase-detector output of the PLL. If a passive loop filter is used with such circuits, then the DC voltage that can be provided to the VCO is limited to couple of volts. This limits the range of frequencies for which the VCO, and hence the PLL, is functional. In certain applications requiring a wider operating range of frequencies for the PLL, like set-top boxes or base stations, this level of performance is not adequate and requires active amplification, hence the need for active loop filters.

An active loop filter typically consists of an op amp, which provides the gain, accompanied by a three or four pole RC filter. The non-inverting input of the op amp is biased to a fixed value, usually the mid-supply of the PLL, while a feedback network provides the gain as well as one, or two, poles for low pass filtering. Figure 39 illustrates a typical active loop filter.

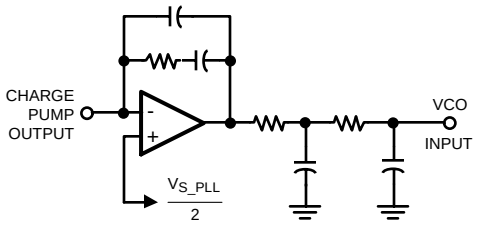


Figure 39. A Typical Active Loop Filter

Certain performance characteristics are essential for an op amp if it is to be used in a PLL loop filter. Low input referred voltage and current noise are essential, as they directly affect the noise of the filter and hence the phase noise of the PLL. Low input bias current is also important, as bias current affects the level of 'reference spurs', artifacts in the frequency spectrum of the PLL caused by mismatch or leakage at the output of the phase detector. A large input and output swing is beneficial in terms of increasing the flexibility in biasing the op amp. The op amp can then be biased such that the output range of the PLL is mapped efficiently onto the input range of the VCO.

With a CMOS input, ultra low input bias currents (2 pA) and low input referred voltage noise (5.5 nV/$\sqrt{Hz}$), the LM6211 is an ideal op amp for using in a PLL active loop filter. The LM6211 has a ground sensing input stage, a rail-to-rail output stage, and an operating supply range of 5V - 24V, which makes it a versatile choice for the design of a wide variety of active loop filters.

Figure 41 shows the LM6211 used with the LMX2430 to create an RF frequency synthesizer. The LMX2430 detects the PLL output, compares it with its internal reference clock and outputs the phase error in terms of current spikes. The LM6211 is used to create a loop filter which averages the error and provides a DC voltage to the VCO. The VCO generates a sine wave at a frequency determined by the DC voltage at its input. This circuit can provide output signal frequencies as high as 2 GHz, much higher than a comparative passive loop filter. Compared to a similar passive loop filter, the LM6211 doesn't add significantly to the phase noise of the PLL, except at the edge of the loop bandwidth, as shown in Figure 40. A peaking of loop gain is expected, since the loop filter is deliberately designed to have a wide bandwidth and a low phase margin so as to minimize locking time.

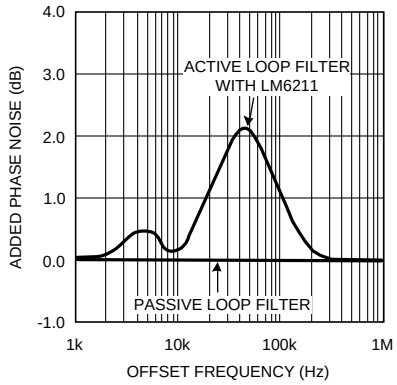


Figure 40. Effect of LM6211 on Phase Noise of PLL

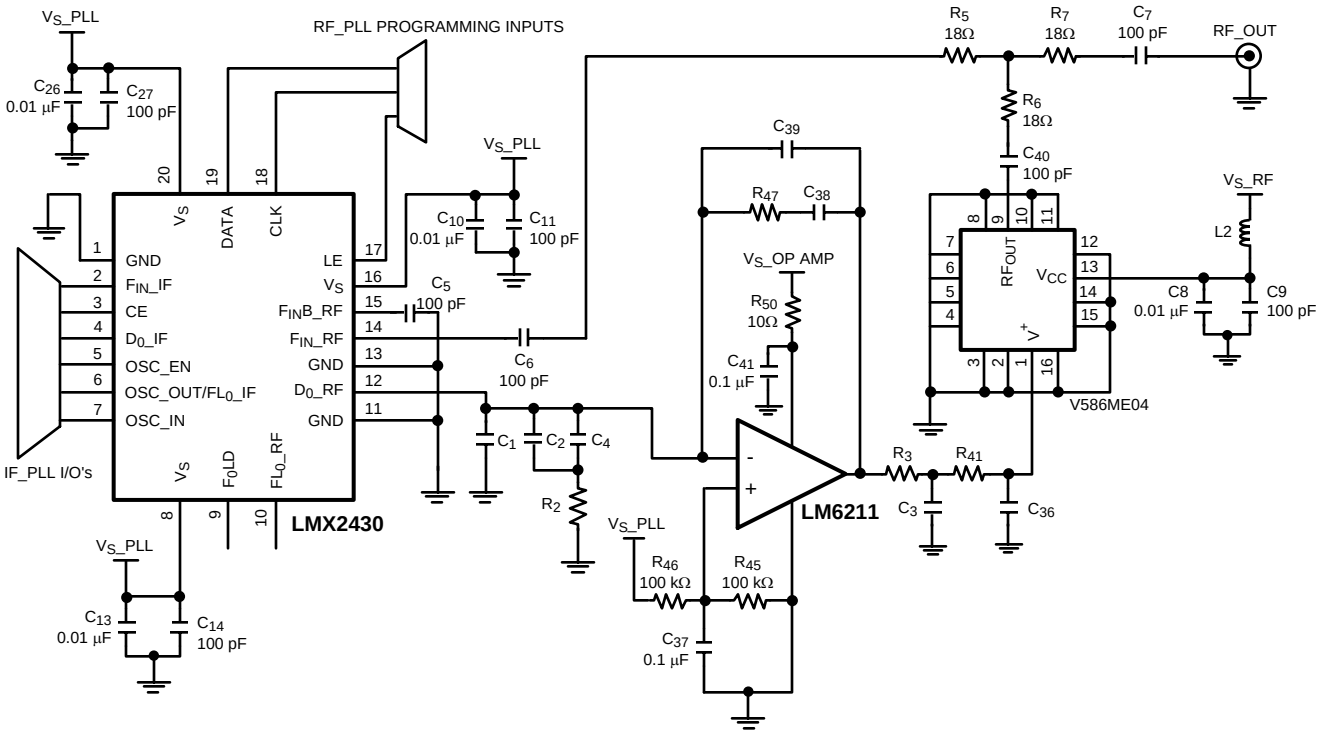


Figure 41. LM6211 in the Active Loop Filter for LMX2430

ADC INPUT DRIVER

A typical application for a high performance op amp is as an ADC driver, which delivers the analog signal obtained from sensors and actuators to ADCs for conversion to the digital domain and further processing. Important requirements in this application are a slew rate high enough to drive the ADC input and low input referred voltage and current noise. If an op amp is used with an ADC, it is critical that the op amp noise does not affect the dynamic range of the ADC. The LM6211, with low input referred voltage and current noise, provides a great solution for this application. For example, the LM6211 can be used to drive an ADS121021, a 12-bit ADC from TI. If it provides a gain of 10 to a maximum input signal amplitude of 100 mV, for a bandwidth as wide as 100 kHz, the average noise seen at the input of the ADC is only 44.6 µVrms. Hence the dynamic range of the ADC, measured in Effective Number of Bits or ENOB, is only reduced by 0.3 bits, despite amplifying the input signal by a gain of 10. Low input bias currents and high input impedance also help as they prevent the loading of the sensor and allow the measurement system to function over a large range.

Figure 42 shows a circuit for monitoring fluid pressure in a hydraulic system, in which the LM6211 is used to sense the error voltage from the pressure sensor. Two LM6211 amplifiers are used to make a difference amplifier which senses the error signal, amplifies it by a gain of 100, and delivers it to the ADC input. The ADC converts the error voltage into a pressure reading to be displayed and drives the DAC, which changes the voltage driving the resistance bridge sensor. This is used to control the gain of the pressure measurement circuit, such that the range of the sensor can be modified to obtain the best resolution possible.

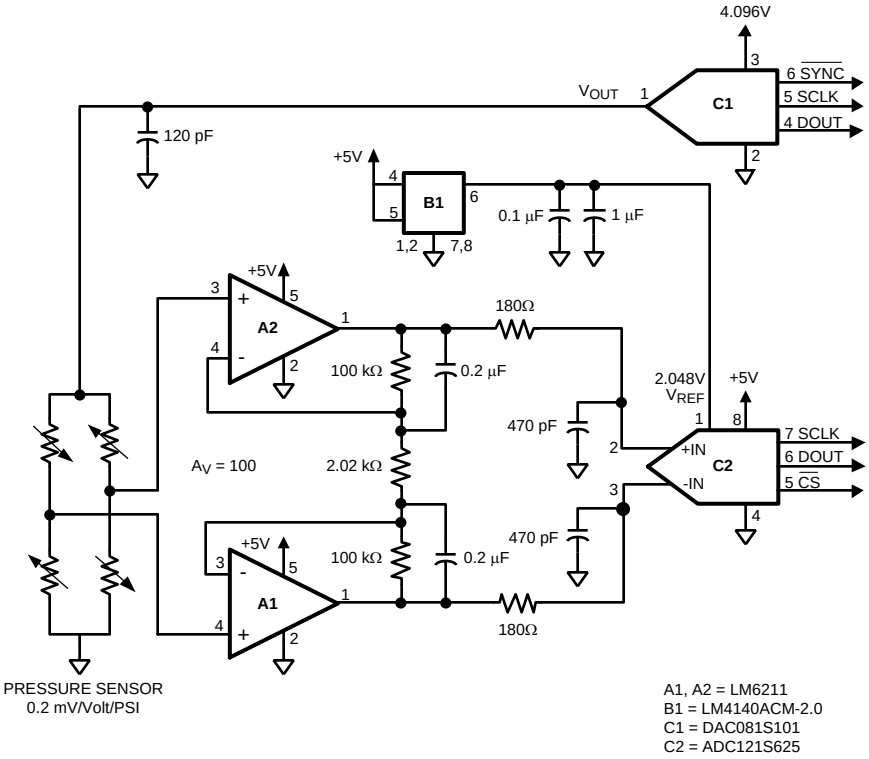


Figure 42. Hydraulic Pressure Monitoring System

DAC OUTPUT AMPLIFIER

Op amps are often used to improve a DAC's output driving capability. High performance op amps are required as I-V converters at the outputs of high resolution current output DACs. Since most DACs operate with a single supply of 5V, a rail-to-rail output swing is essential for this application. A low offset voltage is also necessary to prevent offset errors in the waveform generated. Also, the output impedance of DACs is quite high, more than a few kΩ in some cases, so it is also advisable for the op amp to have a low input bias current. An op amp with a high input impedance also prevents the loading of the DAC, and hence, avoids gain errors. The op amp should also have a slew rate which is fast enough to not affect the settling time of the DAC output.

The LM6211, with a CMOS input stage, ultra low input bias current, a wide bandwidth (20 MHz) and a rail-to-rail output swing for a supply voltage of 24V is an ideal op amp for such an application. Figure 43 shows a typical circuit for this application. The op amp is usually expected to add another time constant to the system, which worsens the settling time, but the wide bandwidth of the LM6211 (20 MHz) allows the system performance to improve without any significant degradation of the settling time.

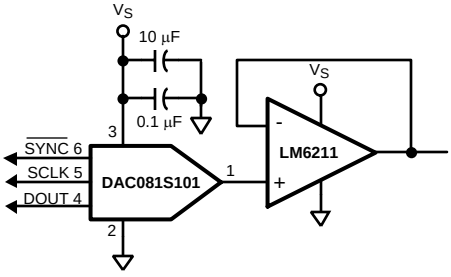


Figure 43. DAC Driver Circuit

AUDIO PREAMPLIFIER

With low input referred voltage noise, low supply voltage and low supply current, and low harmonic distortion, the LM6211 is ideal for audio applications. Its wide unity gain bandwidth allows it to provide large gain over a wide frequency range and it can be used to design a preamplifier to drive a load of as low as 600Ω with less than 0.001% distortion. Two amplifier circuits are shown in Figure 44 and Figure 45. Figure 44 is an inverting amplifier, with a 10 kΩ feedback resistor, R_2, and a 1 kΩ input resistor, R_1, and hence provides a gain of −10. Figure 45 is a non-inverting amplifier, using the same values for R_1 and R_2, and provides a gain of 11. In either of these circuits, the coupling capacitor C_{C1} decides the lower frequency at which the circuit starts providing gain, while the feedback capacitor C_F decides the frequency at which the gain starts dropping off. Figure 46 shows the frequency response of the circuit in Figure 44 with different values of C_F.

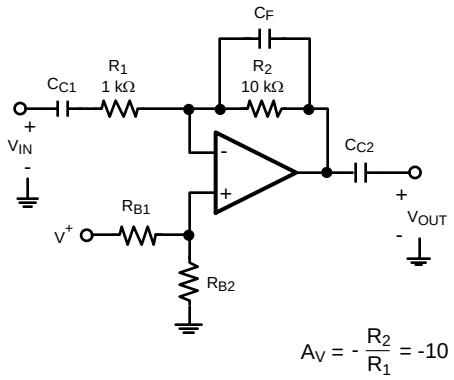


Figure 44. Inverting Audio Amplifier

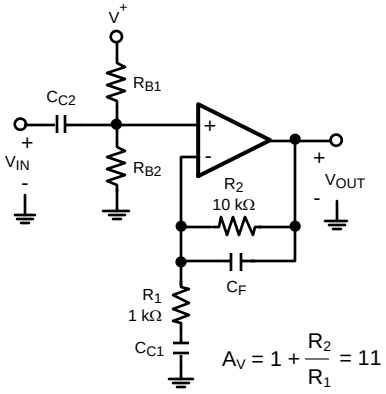


Figure 45. Non-Inverting Audio Preamplifier

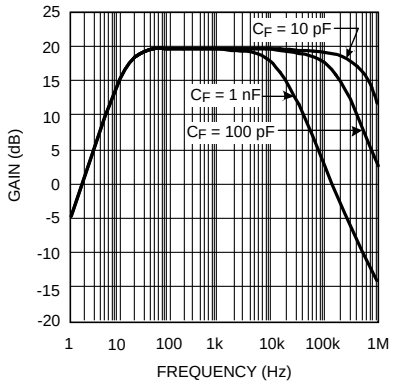


Figure 46. Frequency Response of the Non-Inverting Preamplifier

TRANSIMPEDANCE AMPLIFIER

A transimpedance amplifier converts a small input current into a voltage. This current is usually generated by a photodiode. The transimpedance gain, measured as the ratio of the output voltage to the input current, is expected to be large and wide-band. Since the circuit deals with currents in the range of a few nA, low noise performance is essential. The LM6211, being a CMOS input op amp, provides a wide bandwidth and low noise performance while drawing very low input bias current, and is hence ideal for transimpedance applications.

A transimpedance amplifier is designed on the basis of the current source driving the input. A photodiode is a very common capacitive current source, which requires transimpedance gain for transforming its miniscule current into easily detectable voltages. The photodiode and amplifier's gain are selected with respect to the speed and accuracy required of the circuit. A faster circuit would require a photodiode with lesser capacitance and a faster amplifier. A more sensitive circuit would require a sensitive photodiode and a high gain. A typical transimpedance amplifier is shown in Figure 47. The output voltage of the amplifier is given by the equation $V_{OUT} = -I_{IN}R_F$. Since the output swing of the amplifier is limited, R_F should be selected such that all possible values of I_{IN} can be detected.

The LM6211 has a large gain-bandwidth product (20 MHz), which enables high gains at wide bandwidths. A rail-to-rail output swing at 24V supply allows detection and amplification of a wide range of input currents. A CMOS input stage with negligible input current noise and low input voltage noise allows the LM6211 to provide high fidelity amplification for wide bandwidths. These properties make the LM6211 ideal for systems requiring wide-band transimpedance amplification.

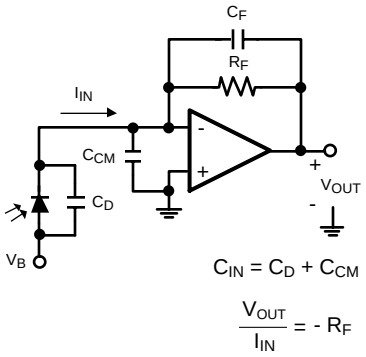


Figure 47. Photodiode Transimpedance Amplifier

The following parameters are used to design a transimpedance amplifier: the amplifier gain-bandwidth product, A_0; the amplifier input capacitance, C_{CM}; the photodiode capacitance, C_D; the transimpedance gain required, R_F; and the amplifier output swing. Once a feasible R_F is selected using the amplifier output swing, these numbers can be used to design an amplifier with the desired transimpedance gain and a maximally flat frequency response. The input common-mode capacitance with respect to V_{CM} for the LM6211 is give in Figure 48.

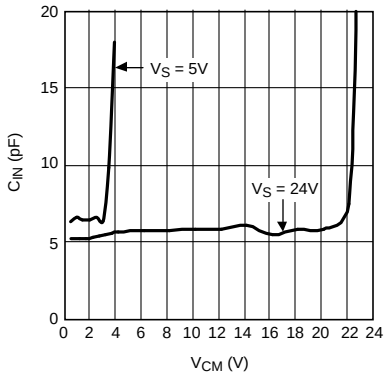


Figure 48. Input Common-Mode Capacitance vs. V_{CM}

An essential component for obtaining a maximally flat response is the feedback capacitor, C_F. The capacitance seen at the input of the amplifier, C_{IN}, combined with the feedback resistor, R_F, generates a phase lag which causes gain-peaking and can destabilize the circuit. C_{IN} is usually just the sum of C_D and C_{CM}. The feedback capacitor C_F creates a pole, f_P in the noise gain of the circuit, which neutralizes the zero in the noise gain, f_Z, created by the combination of R_F and C_{IN}. If properly positioned, the noise gain pole created by C_F can ensure that the slope of the gain remains at 20 dB/decade till the unity gain frequency of the amplifier is reached, thus ensuring stability. As shown in Figure 50, f_P is positioned such that it coincides with the point where the noise gain intersects the op amp's open loop gain. In this case, f_P is also the overall 3 dB frequency of the transimpedance amplifier. The value of C_F needed to make it so is given by Equation 2. A larger value of C_F causes excessive reduction of bandwidth, while a smaller value fails to prevent gain peaking and maintain stability.

$$C_F = \frac{1 + \sqrt{1 + 4\pi R_F C_{IN} A_0}}{2\pi R_F A_0} \tag{2}$$

Calculating C_F from Equation 2 can sometimes return unreasonably small values (<1 pF), especially for high speed applications. In these cases, it is often more practical to use the circuit shown in Figure 49 in order to allow more reasonable values. In this circuit, the capacitance C_F' is (1+ R_B/R_A) times the effective feedback capacitance, C_F. A larger capacitor can now be used in this circuit to obtain a smaller effective capacitance.

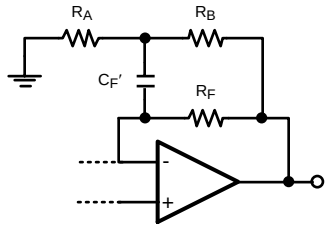


Figure 49. Modifying C_F

For example, if a C_F of 0.5 pF is needed, while only a 5 pF capacitor is available, R_B and R_A can be selected such that R_B/R_A = 9. This would convert a C_F' of 5 pF into a C_F of 0.5 pF. This relationship holds as long as R_A << R_F

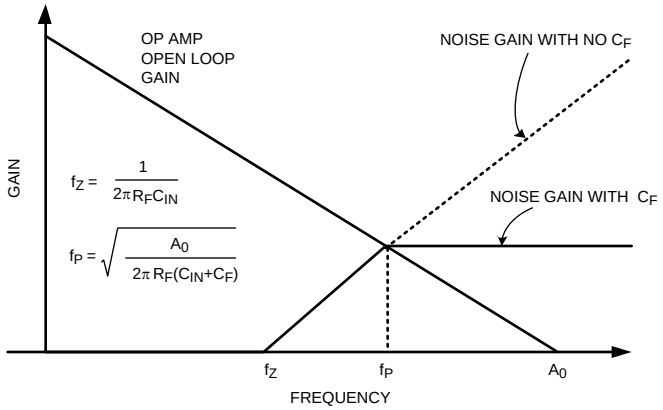


Figure 50. Method for C_F selection

SENSOR INTERFACES

The low input bias current and low input referred noise of the LM6211 make it ideal for sensor interfaces. These circuits are required to sense voltages of the order of a few µV, and currents amounting to less than a nA, and hence the op amp needs to have low voltage noise and low input bias current. Typical applications include infra-red (IR) thermometry, thermocouple amplifiers and pH electrode buffers. Figure 51 is an example of a typical circuit used for measuring IR radiation intensity, often used for estimating the temperature of an object from a distance. The IR sensor generates a voltage proportional to I, which is the intensity of the IR radiation falling on it. As shown in Figure 51, K is the constant of proportionality relating the voltage across the IR sensor (V_{IN}) to the radiation intensity, I. The resistances R_A and R_B are selected to provide a high gain to amplify this voltage, while C_F is added to filter out the high frequency noise.

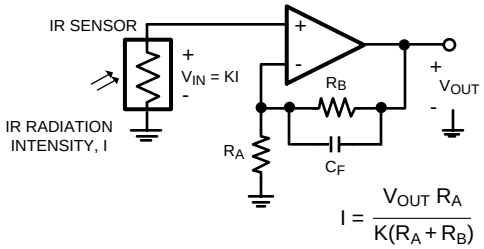


Figure 51. IR Radiation Sensor

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM6211 MDC	ACTIVE	DIESALE	Y	0	400	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-40 to 85		Samples
LM6211MF	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	AT1A	
LM6211MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AT1A	Samples
LM6211MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AT1A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

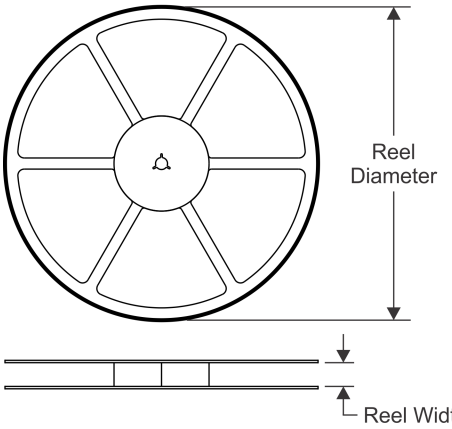
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

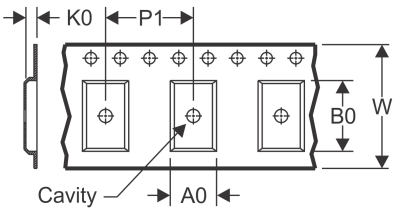
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

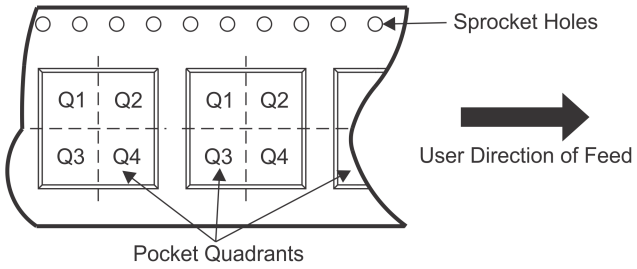


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

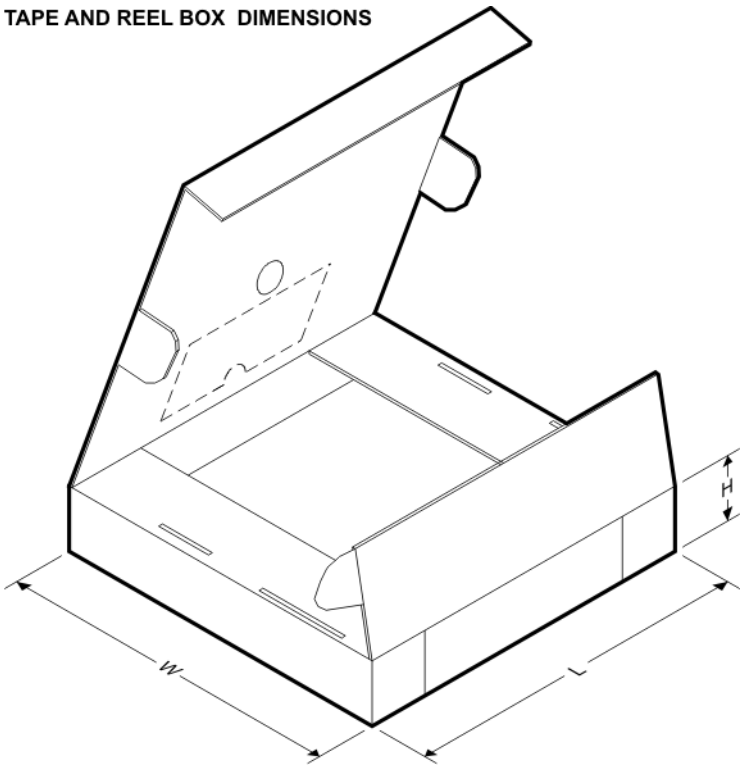
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM6211MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM6211MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM6211MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

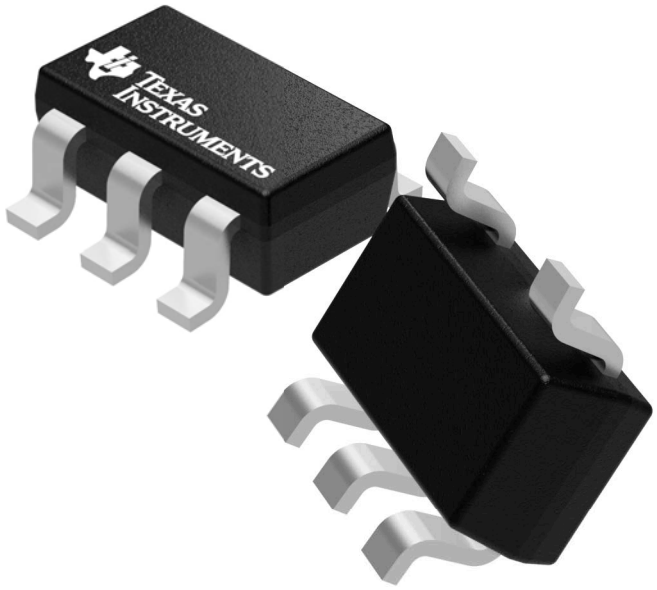


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM6211MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM6211MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM6211MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



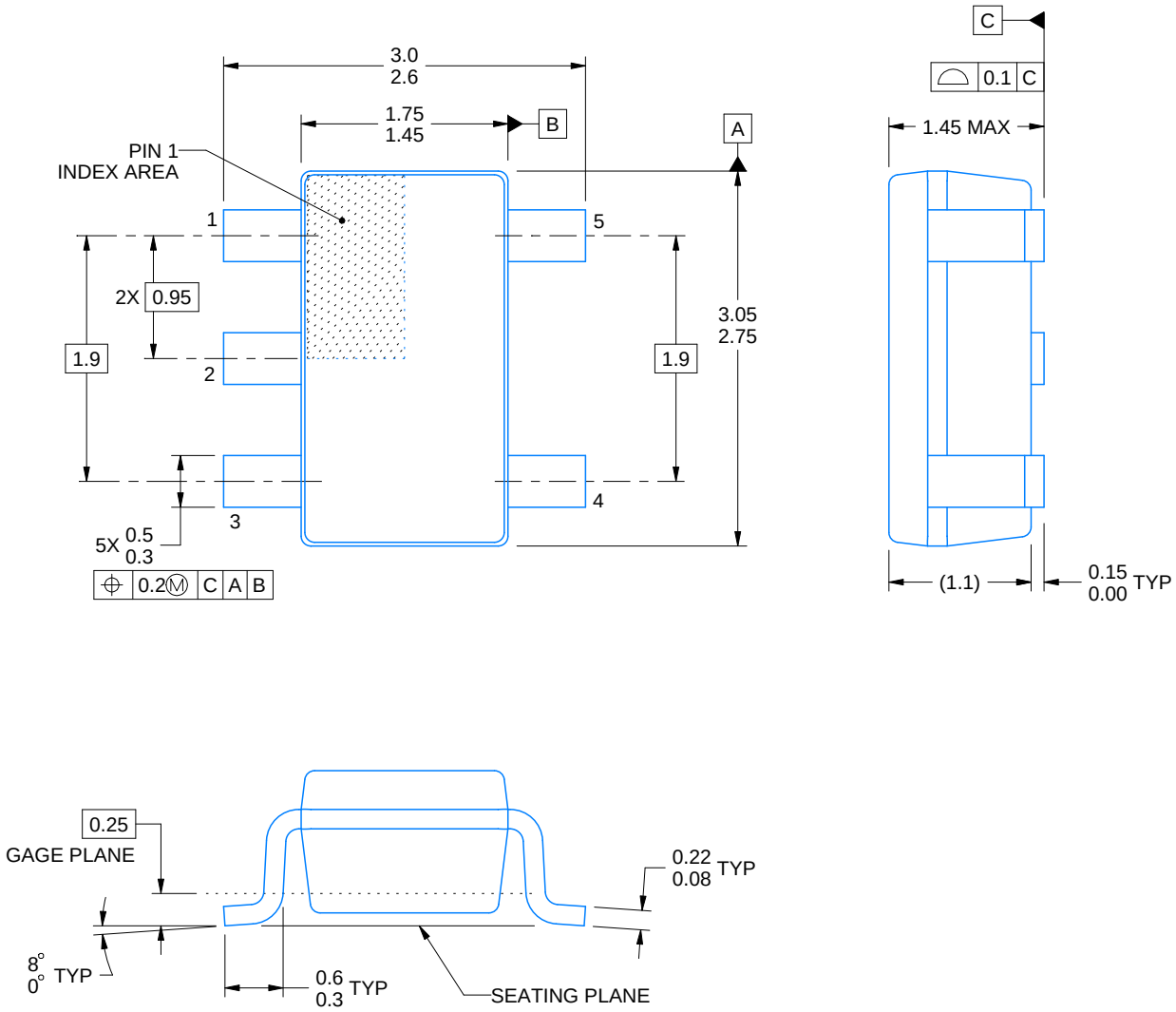
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

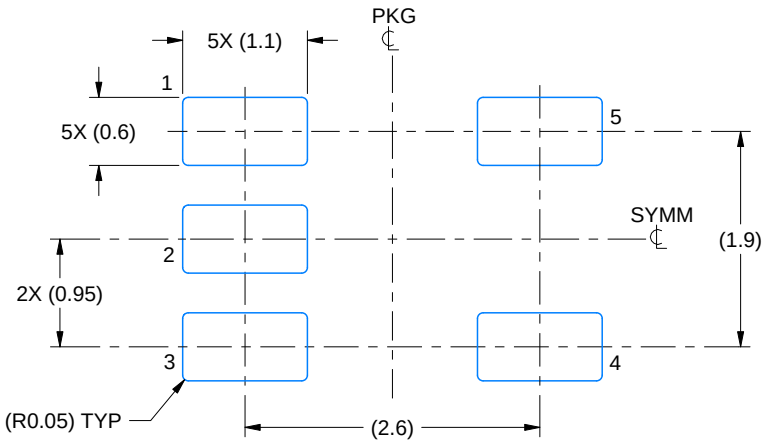
SMALL OUTLINE TRANSISTOR



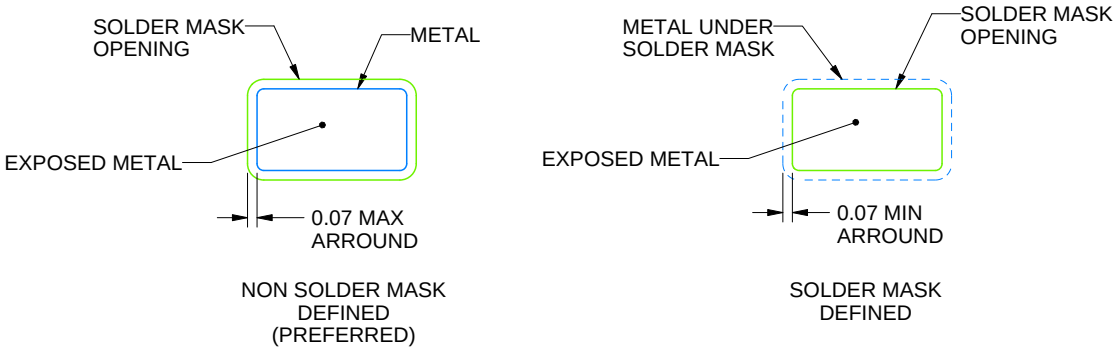
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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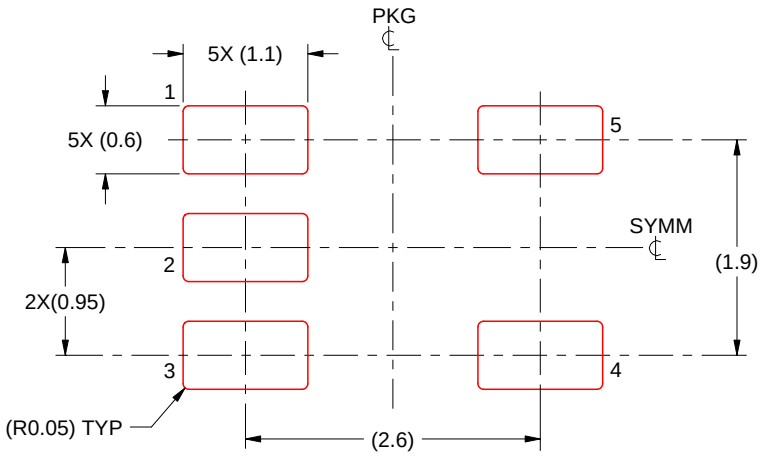
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

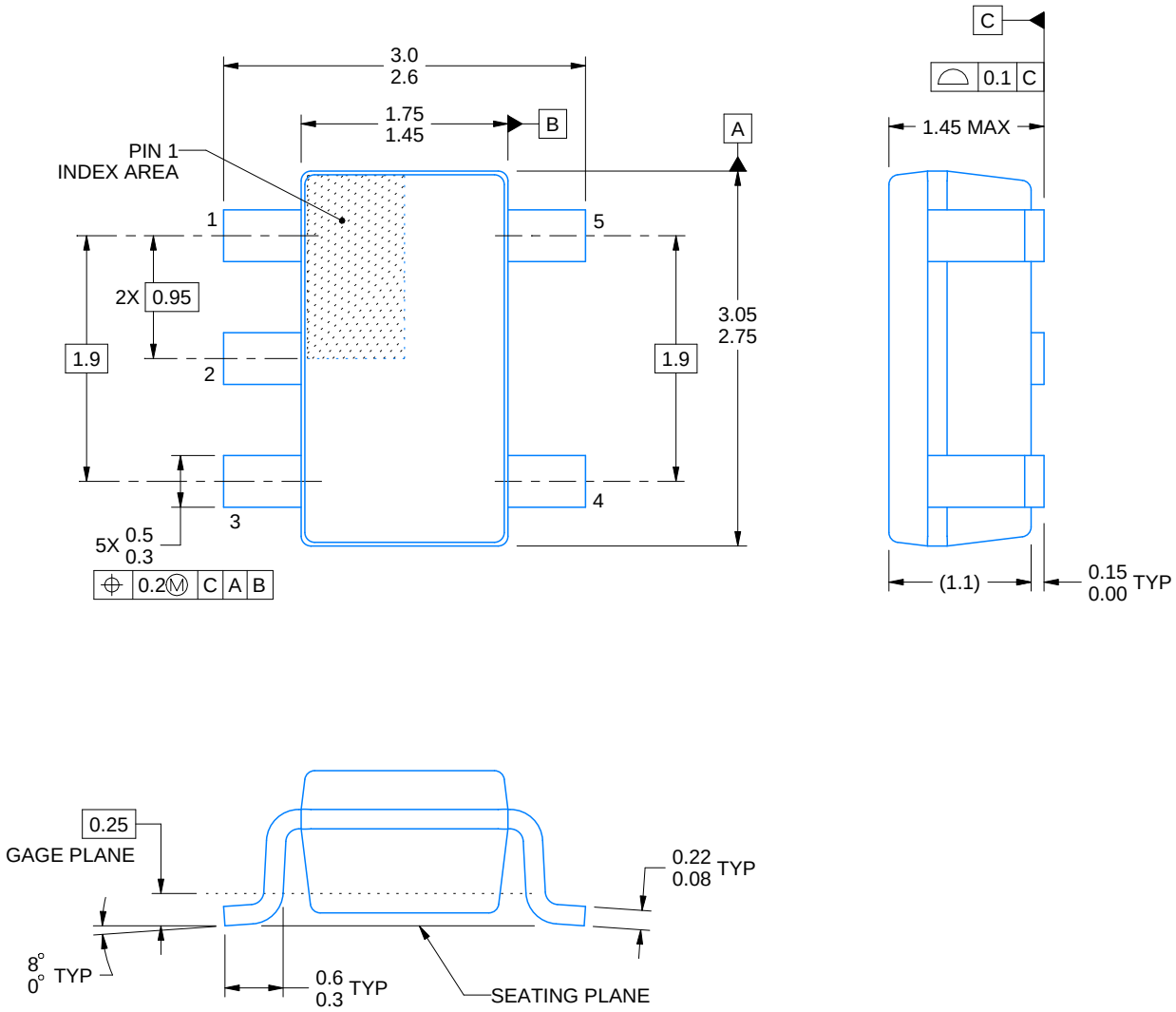
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/C 04/2017

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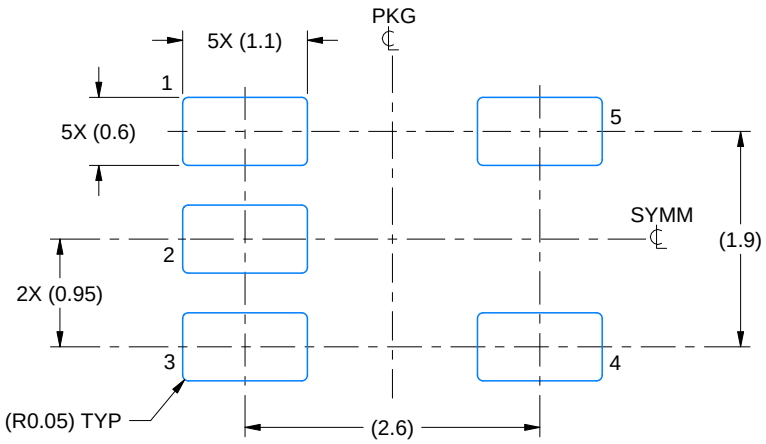
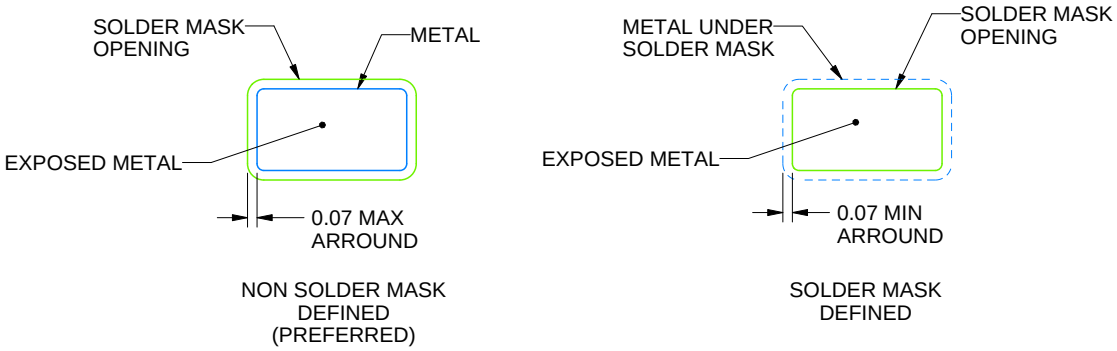


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

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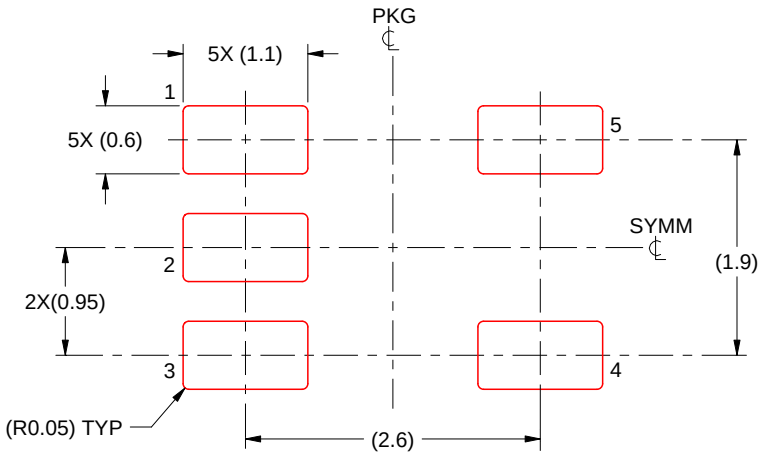

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

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7. Board assembly site may have different recommendations for stencil design.

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