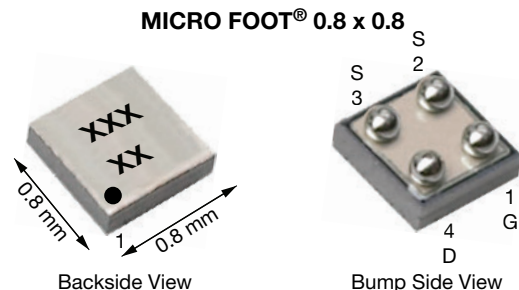


N-Channel 8 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (TYP.)
8	0.054 at V _{GS} = 4.5 V	3.5	4.3 nC
	0.060 at V _{GS} = 2.5 V	3.3	
	0.068 at V _{GS} = 1.8 V	3.1	
	0.086 at V _{GS} = 1.5 V	2.3	
	0.135 at V _{GS} = 1.2 V	1	



Marking Code: xx = AB
xxx = Date/Lot traceability code

Ordering Information:
Si8802DB-T2-E1 (lead (Pb)-free and halogen-free)

FEATURES

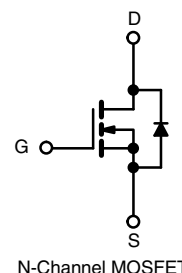
- TrenchFET® power MOSFET
- Small 0.8 mm x 0.8 mm outline area
- Low 0.4 mm max. profile
- Low On-resistance
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load switch with low voltage drop
- Load switch for 1.2 V, 1.5 V, 1.8 V power lines
- Smart phones, tablet PCs, portable media players



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V _{DS}	8	V
Gate-Source Voltage		V _{GS}	± 5	
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	3.5 ^a	A
	T _A = 70 °C		2.8 ^a	
	T _A = 25 °C		3 ^b	
	T _A = 70 °C		2.4 ^b	
Pulsed Drain Current (t = 300 μs)		I _{DM}	15	
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	0.7 ^a	
	T _A = 25 °C		0.4 ^b	
Maximum Power Dissipation	T _A = 25 °C	P _D	0.9 ^a	W
	T _A = 70 °C		0.6 ^a	
	T _A = 25 °C		0.5 ^b	
	T _A = 70 °C		0.3 ^b	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +150	°C
Soldering Recommendations (Peak Temperature) ^c			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	TYPICAL	MAXIMUM
Maximum Junction-to-Ambient ^{a, d}	t ≤ 5 s	R _{thJA}	105	135
Maximum Junction-to-Ambient ^{b, e}			200	260

Notes

- Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.
- Surface mounted on 1" x 1" FR4 board with minimum copper, t = 5 s.
- Refer to IPC/JEDEC® (J-STD-020), no manual or hand soldering.
- Maximum under steady state conditions is 185 °C/W.
- Maximum under steady state conditions is 330 °C/W.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	8	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	7	-	mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J		-	-2.1	-	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.35	-	0.7	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 5 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 8 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 8 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	10	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 1 A	-	0.044	0.054	Ω
		V _{GS} = 2.5 V, I _D = 1 A	-	0.049	0.060	
		V _{GS} = 1.8 V, I _D = 0.5 A	-	0.055	0.068	
		V _{GS} = 1.5 V, I _D = 0.2 A	-	0.060	0.086	
		V _{GS} = 1.2 V, I _D = 0.1 A	-	0.080	0.135	
Forward Transconductance ^a	g _{fs}	V _{DS} = 4 V, I _D = 1 A	-	13	-	S
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} = 4 V, V _{GS} = 4.5 V, I _D = 1 A	-	4.3	6.5	nC
Gate-Source Charge	Q _{gs}		-	0.44	-	
Gate-Drain Charge	Q _{gd}		-	0.72	-	
Gate Resistance	R _g	f = 1 MHz	-	3.5	-	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 4 V, R _L = 4 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	5	10	ns
Rise Time	t _r		-	15	30	
Turn-Off Delay Time	t _{d(off)}		-	22	40	
Fall Time	t _f		-	7	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _A = 25 °C	-	-	0.7	A
Pulse Diode Forward Current	I _{SM}		-	-	15	
Body Diode Voltage	V _{SD}	I _S = 1 A, V _{GS} = 0 V	-	0.7	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 1 A, di/dt = 100 A/μs, T _J = 25 °C	-	20	40	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	5	10	nC
Reverse Recovery Fall Time	t _a		-	14	-	ns
Reverse Recovery Rise Time	t _b		-	60	-	

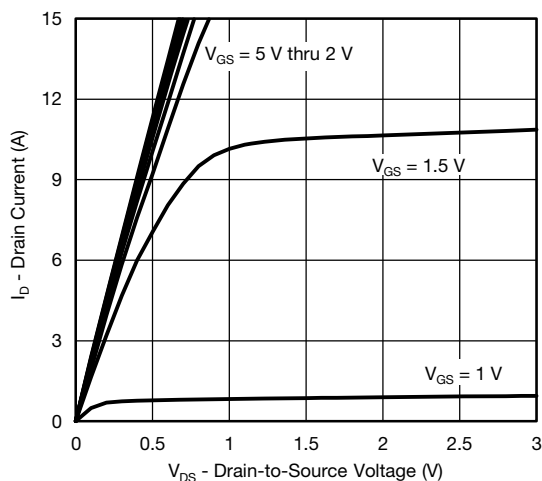
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

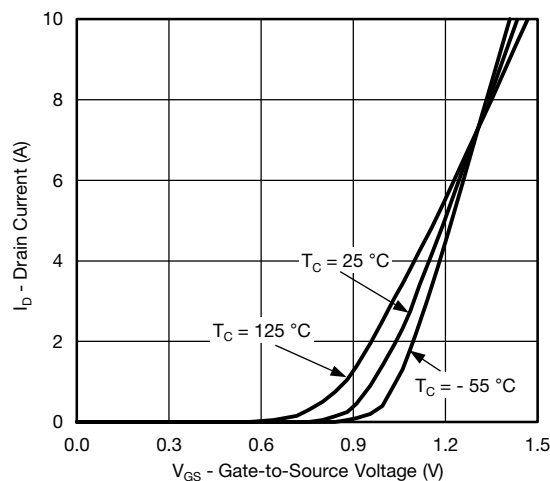
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



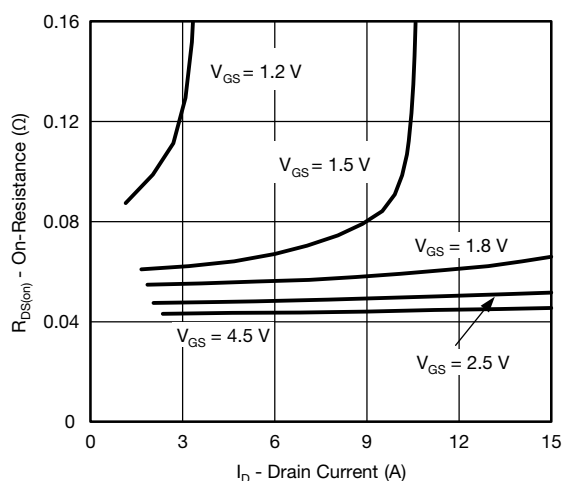
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



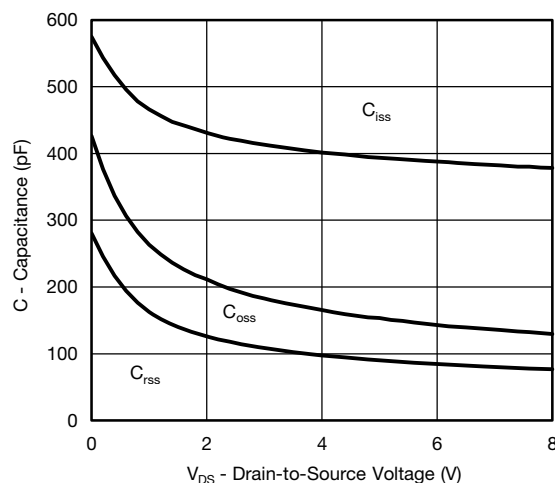
Output Characteristics



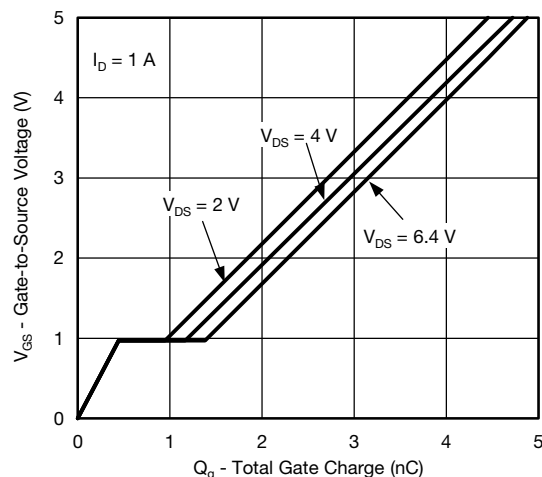
Transfer Characteristics



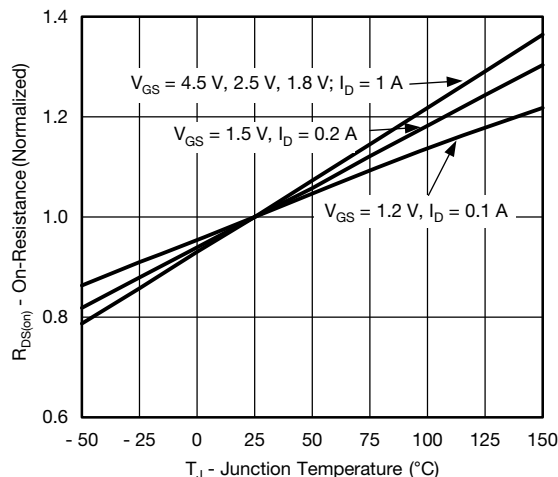
On-Resistance vs. Drain Current



Capacitance



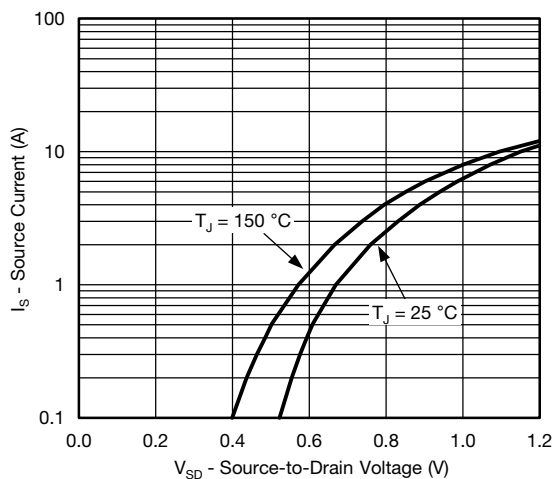
Gate Charge



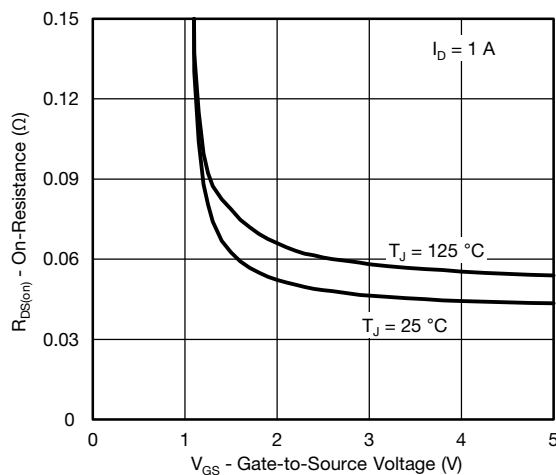
On-Resistance vs. Junction Temperature



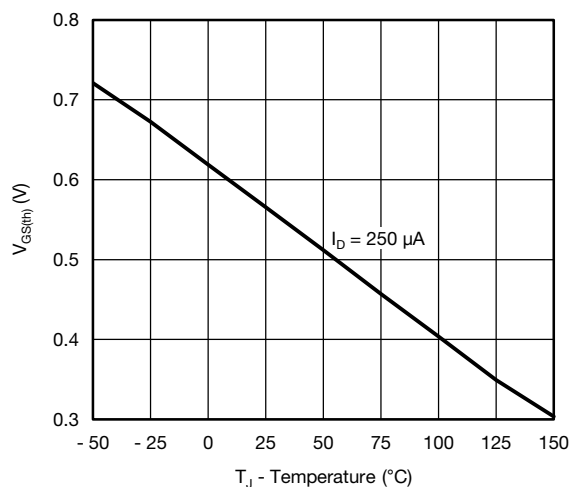
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



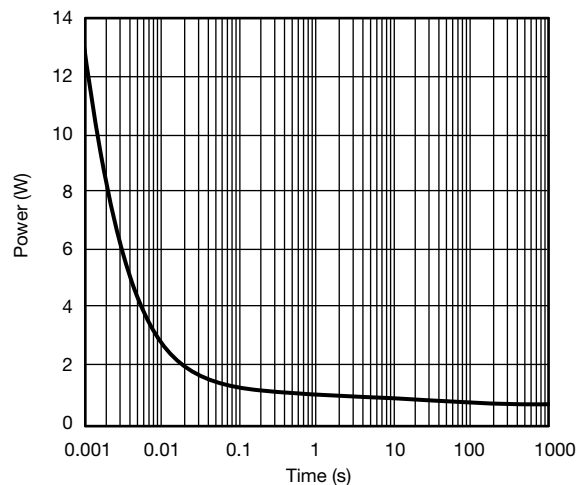
Source-Drain Diode Forward Voltage



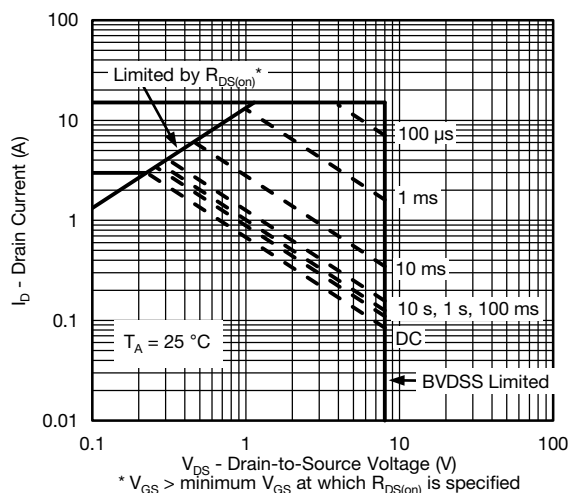
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



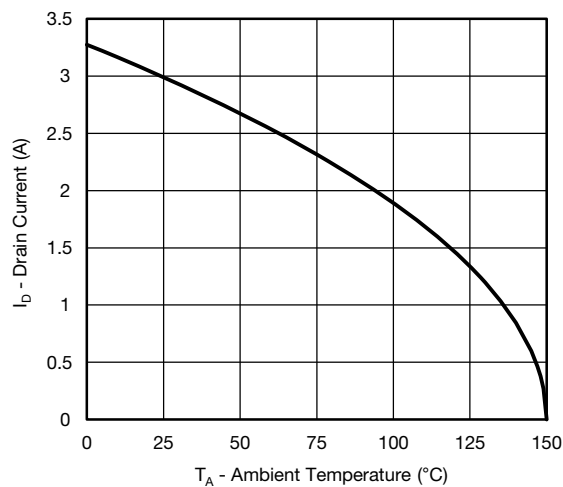
Single Pulse Power (Junction-to-Ambient)



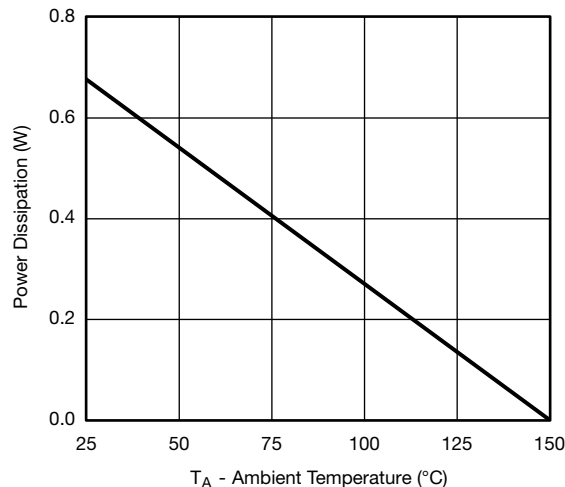
Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



Power Derating

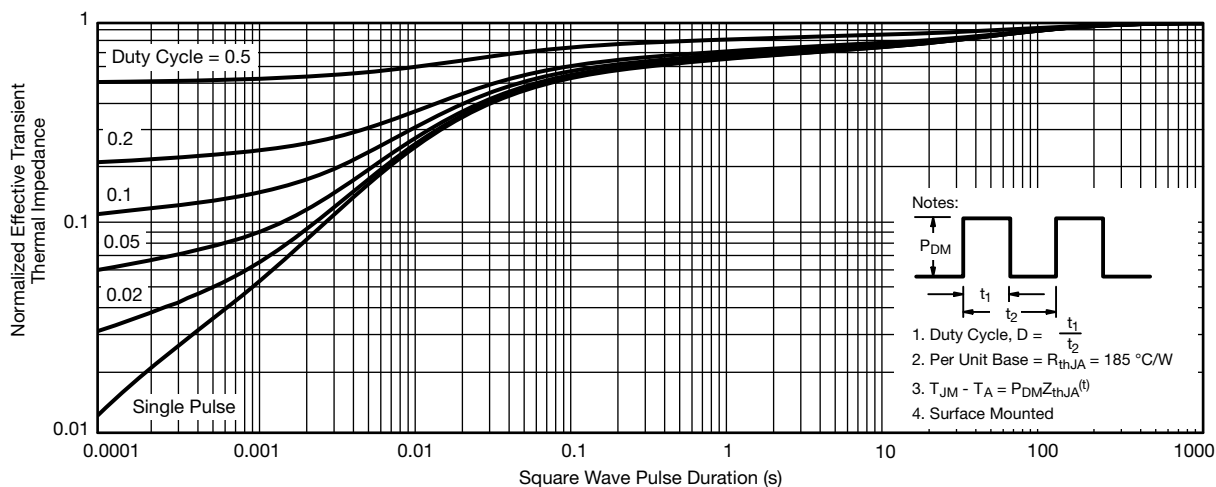
Note

When mounted on 1" x 1" FR4 with full copper.

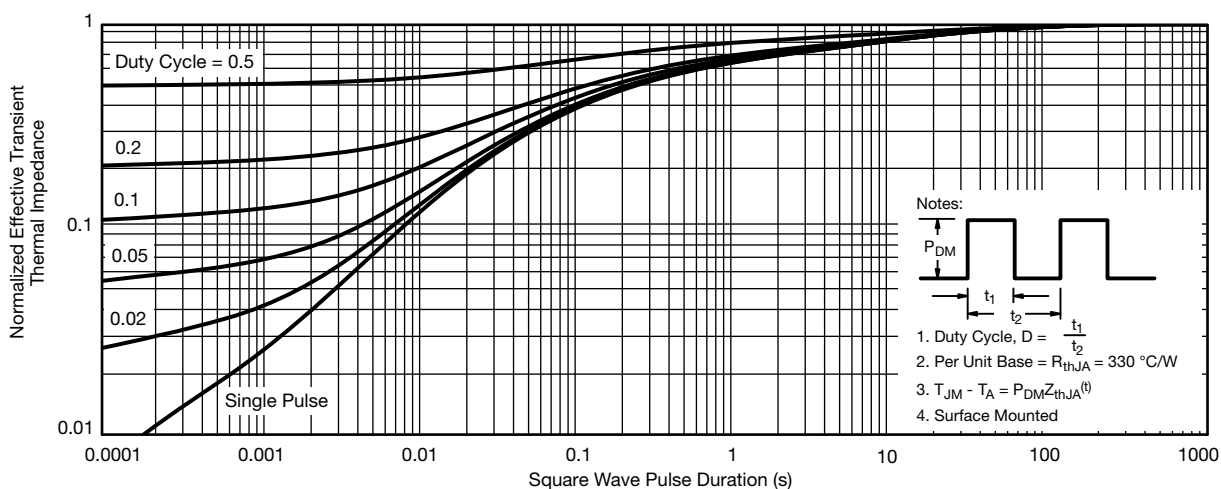
* The power dissipation P_D is based on $T_{J(max)} = 150\text{ }^{\circ}\text{C}$, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient (On 1" x 1" FR4 Board with Maximum Copper)

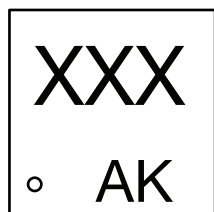


Normalized Thermal Transient Impedance, Junction-to-Ambient (On 1" x 1" FR4 Board with Minimum Copper)

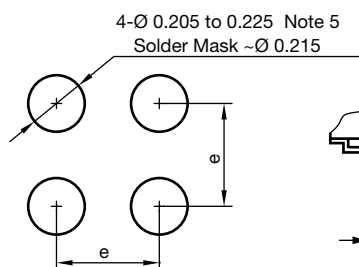
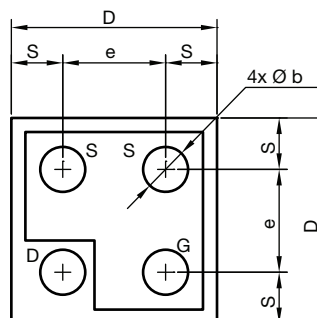
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67999.



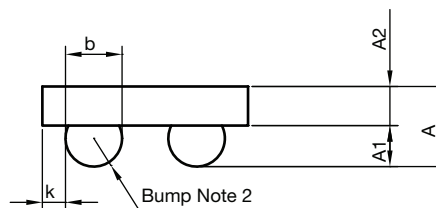
MICRO FOOT®: 4-Bump (0.8 mm x 0.8 mm, 0.4 mm Pitch)



Mark on Backside of die



Note 4



Notes

- (1) Laser mark on the backside surface of die
- (2) Bumps are 95.5 % Sn,3.8 % Ag,0.7 % Cu
- (3) "i" is the location of pin 1
- (4) "b1" is the diameter of the solderable substrate surface, defined by an opening in the solder resist layer solder mask defined.
- (5) Non-solder mask defined copper landing pad.

DIM.	MILLIMETERS ^a			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.328	0.365	0.402	0.0129	0.0144	0.0158
A1	0.136	0.160	0.184	0.0053	0.0062	0.0072
A2	0.192	0.205	0.218	0.0076	0.0081	0.0086
b	0.200	0.220	0.240	0.0078	0.0086	0.0094
b1	0.175			0.0068		
e	0.400			0.0157		
S	0.160	0.180	0.200	0.0062	0.0070	0.0078
D	0.720	0.760	0.800	0.0283	0.0299	0.0314
K	0.040	0.070	0.100	0.0015	0.0027	0.0039

Note

- a. Use millimeters as the primary measurement.

ECN: T15-0053-Rev. A, 16-Feb-15
DWG: 6033



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