

SN74S1051

12-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

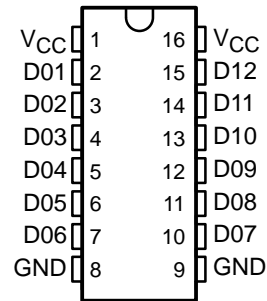
SDLS018B – SEPTEMBER 1990 – REVISED MARCH 2003

- Designed to Reduce Reflection Noise
- Repetitive Peak Forward Current to 200 mA
- 12-Bit Array Structure Suited for Bus-Oriented Systems

description/ordering information

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 12-bit high-speed Schottky diode array suitable for clamping to V_{CC} and/or GND.

D, N, NS, OR PW PACKAGE
(TOP VIEW)

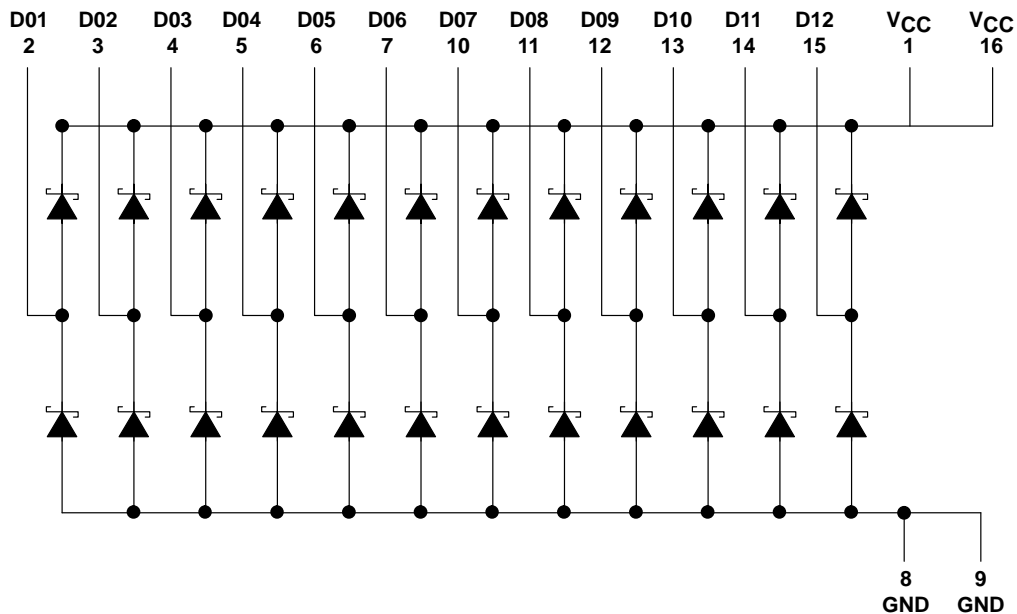


ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74S1051N	SN74S1051N
	SOIC – D	Tube	SN74S1051D	S1051
		Tape and reel	SN74S1051DR	
	SOP – NS	Tape and reel	SN74S1051NSR	74S1051
TSSOP – PW	Tape and reel	SN74S1051PWR	S1051	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

schematic diagrams



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated

SN74S1051

12-BIT SCHOTTKY BARRIER DIODE

BUS-TERMINATION ARRAY

SDLS018B – SEPTEMBER 1990 – REVISED MARCH 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady-state reverse voltage, V_R	7 V
Continuous forward current, I_F : Any D terminal from GND or to V_{CC}	50 mA
Total through all GND or V_{CC} terminals	170 mA
Repetitive peak forward current‡, I_{FRM} : Any D terminal from GND or V_{CC}	200 mA
Total through all GND or V_{CC} terminals	1 A
Package thermal impedance, θ_{JA} (see Note 1): D package	73°C/W
N package	67°C/W
NS package	64°C/W
PW package	108°C/W
Operating free-air temperature range	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ These values apply for $t_w \leq 100 \mu s$, duty cycle $\leq 20\%$.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
V_F	Static forward voltage	To V_{CC}	$I_F = 18 \text{ mA}$	0.85	1.05	V	
			$I_F = 50 \text{ mA}$	1.05	1.3		
		From GND	$I_F = 18 \text{ mA}$	0.75	0.95		
			$I_F = 50 \text{ mA}$	0.95	1.2		
V_{FM}	Peak forward voltage		$I_F = 200 \text{ mA}$	1.45		V	
I_R	Static reverse current	To V_{CC}	$V_R = 7 \text{ V}$			5	μA
		From GND			5		
C_t	Total capacitance	$V_R = 0 \text{ V}, f = 1 \text{ MHz}$		8	16	pF	
		$V_R = 2 \text{ V}, f = 1 \text{ MHz}$		4	8		

§ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ C$.

NOTE 2: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
I_x	Internal crosstalk current	Total I_F current = 1 A,	See Note 3	0.8	2	mA	
		Total I_F current = 198 mA,	See Note 3	0.02	0.2		

§ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ C$.

NOTE 3: I_x is measured under the following conditions with one diode static, all others switching:

Switching diodes: $t_w = 100 \mu s$, duty cycle = 20%

Static diode: $V_R = 5 \text{ V}$

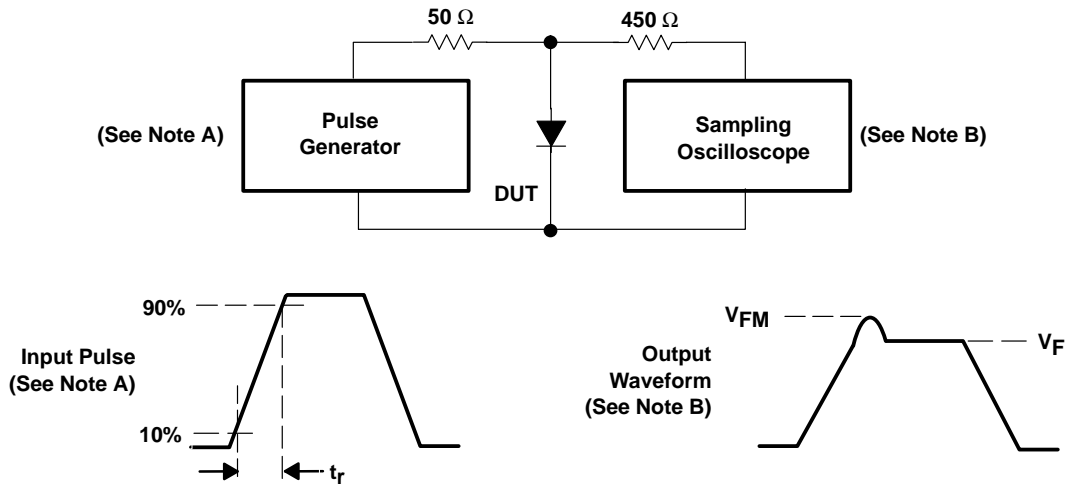
The static diode input current is the internal crosstalk current, I_x .

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
t_{rr}	Reverse recovery time	$I_F = 10 \text{ mA}, I_{RM(REC)} = 10 \text{ mA}, I_{R(REC)} = 1 \text{ mA}, R_L = 100 \Omega$				8	16	ns	

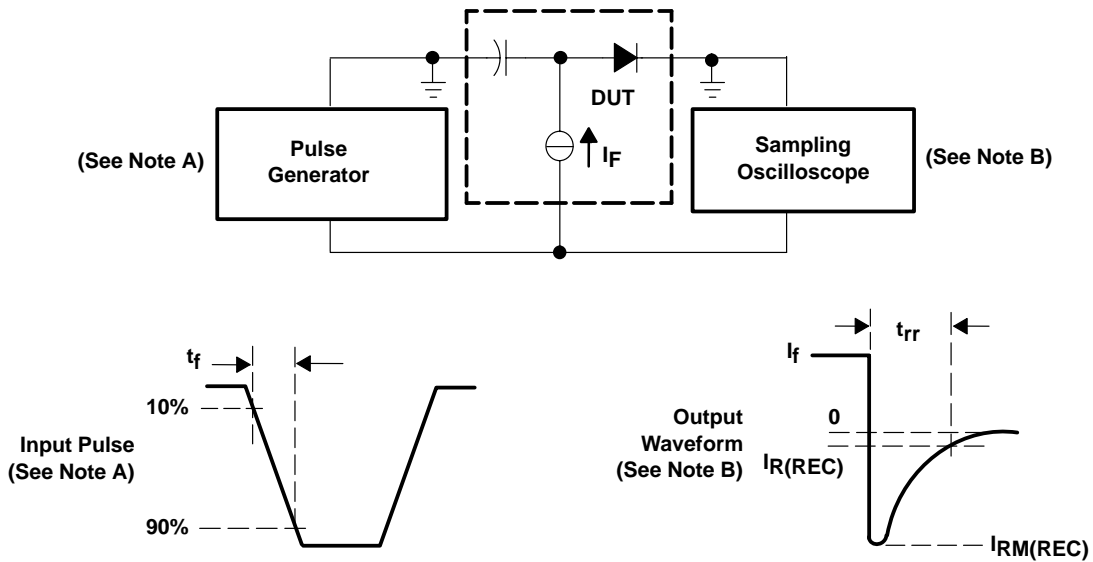


PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: $t_r = 20$ ns, $Z_O = 50$ Ω , freq = 500 Hz, duty cycle = 1%.
 B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \leq 350$ ps, $R_i = 50$ Ω , $C_i \leq 5$ pF.

Figure 1. Forward Recovery Voltage



- NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: $t_f = 0.5$ ns, $Z_O = 50$ Ω , $t_w \geq 50$ ns, duty cycle = 1%.
 B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \leq 350$ ps, $R_i = 50$ Ω , $C_i \leq 5$ pF.

Figure 2. Reverse Recovery Time

SN74S1051 12-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

SDLS018B – SEPTEMBER 1990 – REVISED MARCH 2003

APPLICATION INFORMATION

Large negative transients at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.) or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74S1051 diode termination array helps suppress negative transients caused by transmission-line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split-resistor or Thevenin-equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver reduce negative transients, but they also can increase propagation delays down the line because a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current when the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients is tracked by the current-voltage characteristic curve for that diode. Typical current-versus-voltage curves for the SN74S1051 are shown in Figures 3 and 4.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 5 was evaluated. The resulting waveforms with and without the diode are shown in Figure 6.

The maximum effectiveness of the diode arrays in suppressing negative transients occurs when the diode arrays are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

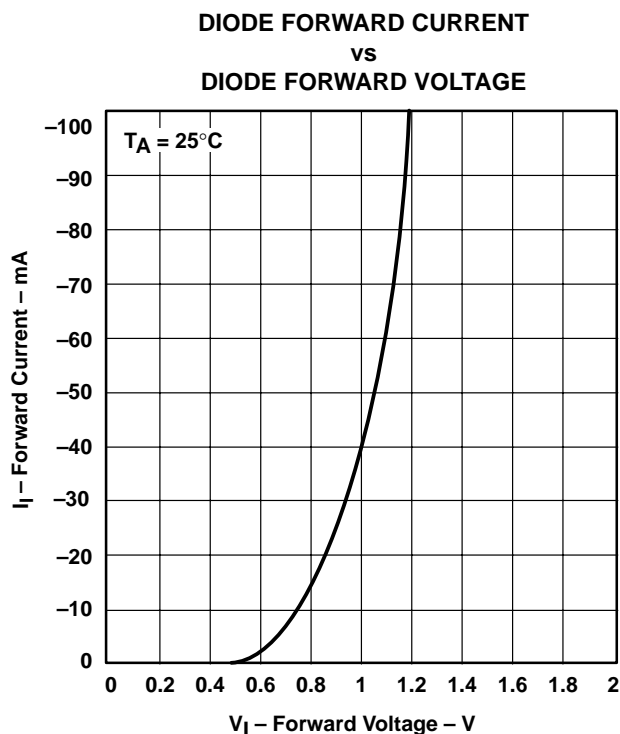
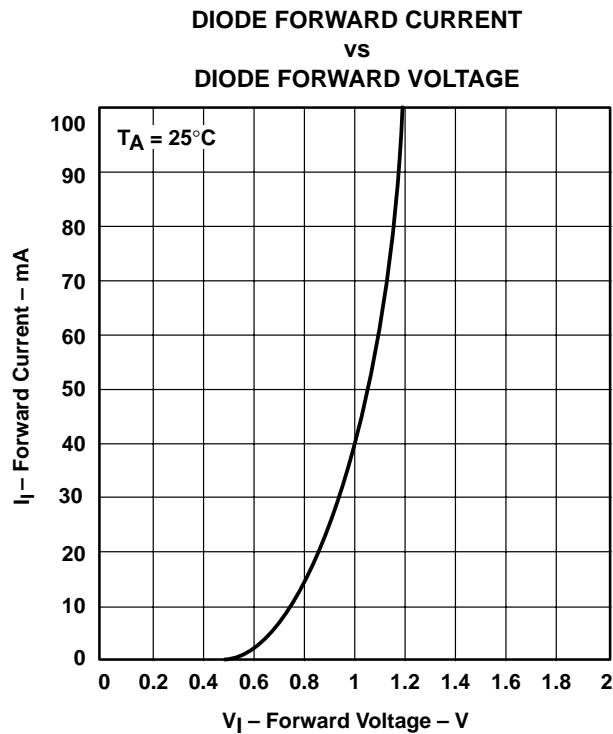


Figure 3. Typical Input Current vs Input Voltage
(Lower Diode)



**Figure 4. Typical Input Current vs Input Voltage
(Upper Diode)**

SN74S1051
12-BIT SCHOTTKY BARRIER DIODE
BUS-TERMINATION ARRAY

SDLS018B – SEPTEMBER 1990 – REVISED MARCH 2003

APPLICATION INFORMATION

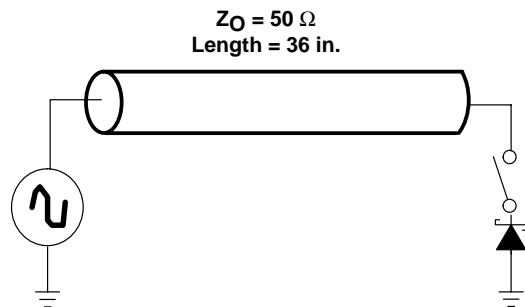


Figure 5. Diode Test Setup

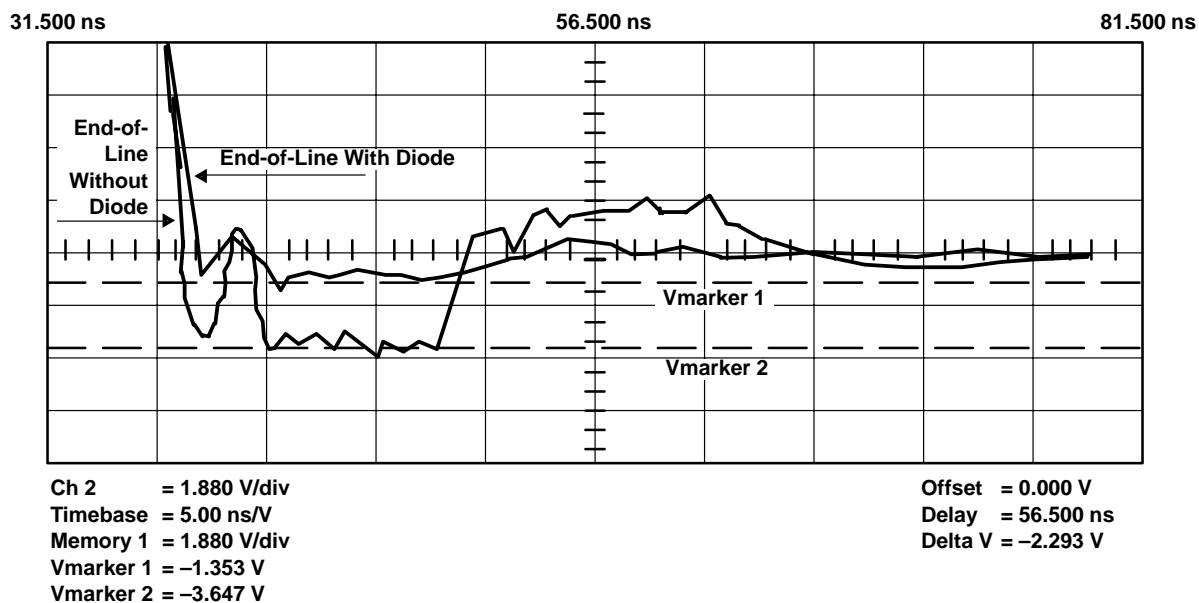


Figure 6. Reduction of Negative Transients at the End of a Transmission Line

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74S1051D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S1051	Samples
SN74S1051DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S1051	Samples
SN74S1051DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S1051	Samples
SN74S1051N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S1051N	Samples
SN74S1051NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74S1051	Samples
SN74S1051PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S1051	Samples
SN74S1051PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S1051	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74S1051DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74S1051NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74S1051PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74S1051DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74S1051NSR	SO	NS	16	2000	367.0	367.0	38.0
SN74S1051PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.