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FDMC2610

July 2016

N-Channel UltraFET Trench[®] MOSFET 200V, 9.5A, 200m Ω

Features

- Max $r_{DS(on)}$ = 200m Ω at V_{GS} = 10V, I_D = 2.2A
- Max $r_{DS(on)}$ = 215m Ω at V_{GS} = 6V, I_D = 1.5A
- Low Profile 1mm Max in a Power 33
- RoHS Compliant

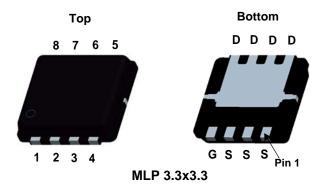


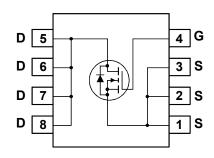
General Description

This N-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced Power Trench process. It has been optimized for power management applications.

Application

■ DC - DC Conversion





MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter			Ratings	Units
V _{DS}	Drain to Source Voltage			200	V
V _{GS}	Gate to Source Voltage			±20	V
	Drain Current -Continuous (Silicon limited)	T _C = 25°C		9.5	
I_D	-Continuous	T _A = 25°C	(Note 1a)	2.2	Α
	-Pulsed			15	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	6	mJ
D	Power Dissipation	T _C = 25°C		42	W
P_{D}	Power Dissipation	T _A = 25°C	(Note 1a)	2.1	VV
T _I , T _{STG}	Operating and Storage Junction Temperature Ra	ange		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a	60	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC2610	FDMC2610	MLP 3.3x3.3	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Chara	acteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	200			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250μA, referenced to 25°C		199		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 160V,$ $V_{GS} = 0V$ $T_{J} = 125^{\circ}C$			1 100	μА
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2	3.2	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250μA, referenced to 25°C		-9.9		mV/°C
		$V_{GS} = 10V, I_D = 2.2A$		175	200	
r _{DS(on)}	Drain to Source On Resistance	$V_{GS} = 6V, I_D = 1.5A$		188	215	mΩ
		$V_{GS} = 10V$, $I_D = 2.2A$, $T_J = 125$ °C		347	397	
9 _{FS}	Forward Transconductance	$V_{DS} = 5V, I_{D} = 2.2A$		7		S

Dynamic Characteristics

C _{iss}	Input Capacitance	\\ - 400\\ \\ - 0\\	720	960	pF
C _{oss}	Output Capacitance	V _{DS} = 100V, V _{GS} = 0V, f = 1MHz	41	55	pF
C _{rss}	Reverse Transfer Capacitance	f = 1MHz	12	20	pF
R_g	Gate Resistance	f = 1MHz	0.7		Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		17	31	ns
t _r	Rise Time	$V_{DD} = 100V, I_D = 2.2A$	13	24	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10V$, $R_{GEN} = 24\Omega$	29	47	ns
t _f	Fall Time		16	29	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0V \text{ to } 10V \ V_{DD} = 100V$	12.3	18	nC
Q _{gs}	Gate to Source Gate Charge	I _D = 2.2A	3		nC
Q _{gd}	Gate to Drain "Miller" Charge		3.6		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0V, I _S = 2.2A (Note 2)	0	.8	1.2	V
t _{rr}	Reverse Recovery Time	I _F = 2.2A, di/dt = 100A/μs	6	9	104	ns
Q _{rr}	Reverse Recovery Charge		1	14	171	nC

Notes: 1. $R_{\theta JA}$ is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 60°C/W when mounted on a 1 in² pad of 2 oz copper



b. 135°C/W when mounted on a minimum pad of 2 oz copper

- 2: Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.
- 3. Starting T_J = 25 °C; N-ch: L = 3 mH, I_{AS} = 2 A, V_{DD} = 200 V, V_{GS} = 10 V.

Typical Characteristics T_J = 25°C unless otherwise noted.

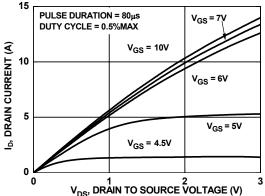
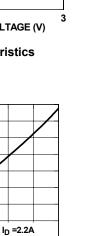


Figure 1. On-Region Characteristics

PULSE DURATION = 80µs

DUTY CYCLE = 0.5%MAX



V_{GS} = 10V

Figure 3. Normalized On-Resistance vs Junction Temperature

T_J, JUNCTION TEMPERATURE (°C)

. -75 -50 -25 0 25 50 75 100 125 150

NORMALIZED

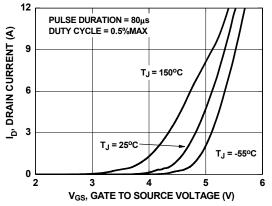


Figure 5. Transfer Characteristics

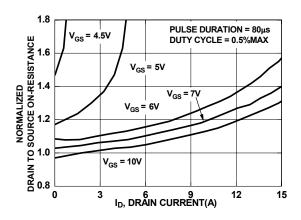


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

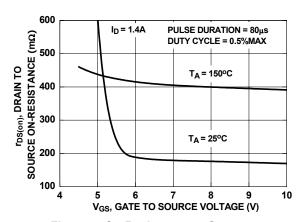


Figure 4. On-Resistance vs Gate to Source Voltage

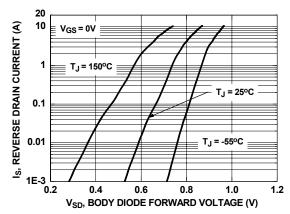


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted.

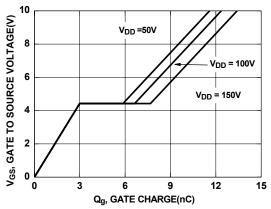


Figure 7. Gate Charge Characteristics

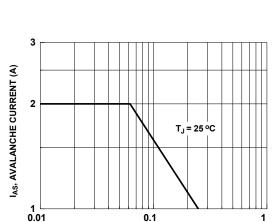


Figure 9. Unclamped Inductive Switching Capability

t_{AV}, TIME IN AVALANCHE (ms)

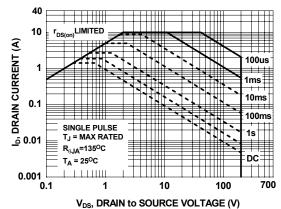


Figure 11. Forward Bias Safe Operating Area

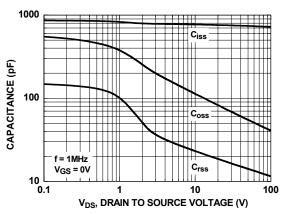


Figure 8. Capacitance vs Drain to Source Voltage

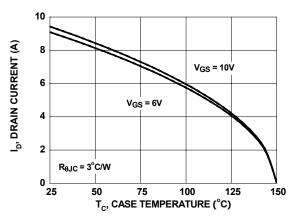


Figure 10. Maximum Continuous Drain Current vs Case Temperature

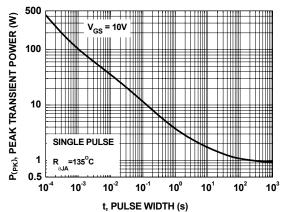


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted.

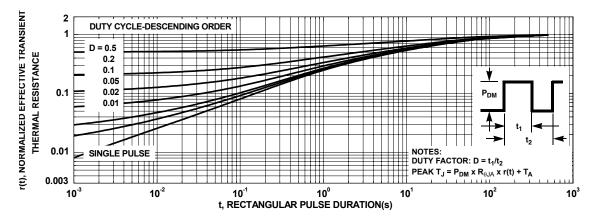
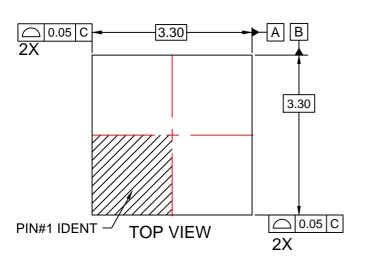
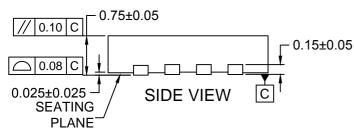
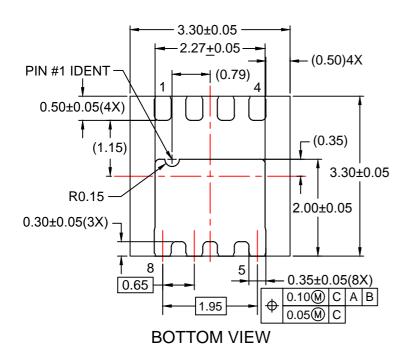
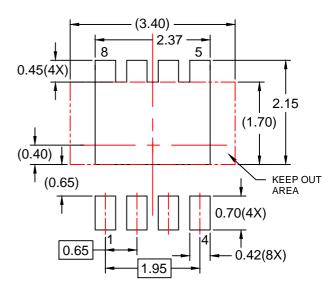


Figure 13. Transient Thermal Response Curve









RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Srev3.



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