High and Low Side Driver

General Description

The PN7113 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels based on P_SUB P_EPI process. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications.

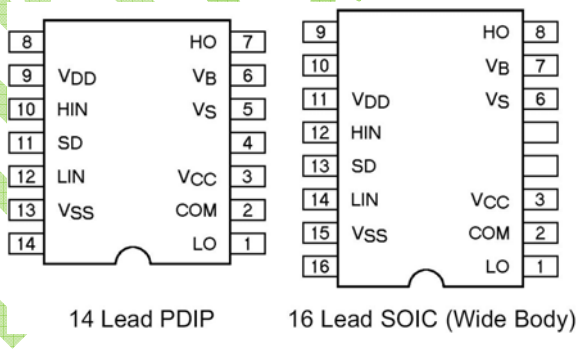
Features

- Fully operational to +600 V
- 3.3 V logic compatible
- Floating channel designed for bootstrap operation
- Gate drive supply range from 10 V to 20 V
- UVLO for both channels
- 3.0A output current
- Separate logic supply range from 3.3 V to 20 V
- -5V negative Vs ability
- maximum working frequency is up to 100KHz
- Matched propagation delay for both channels
- 14-Lead PDIP or 16-Lead SOIC package

Applications

- High and medium-power motor driver
- Power MOSFET or IGBT driver
- Lighting ballast

Package



14 Lead PDIP　　16 Lead SOIC (Wide Body)

Typical Application Circuit

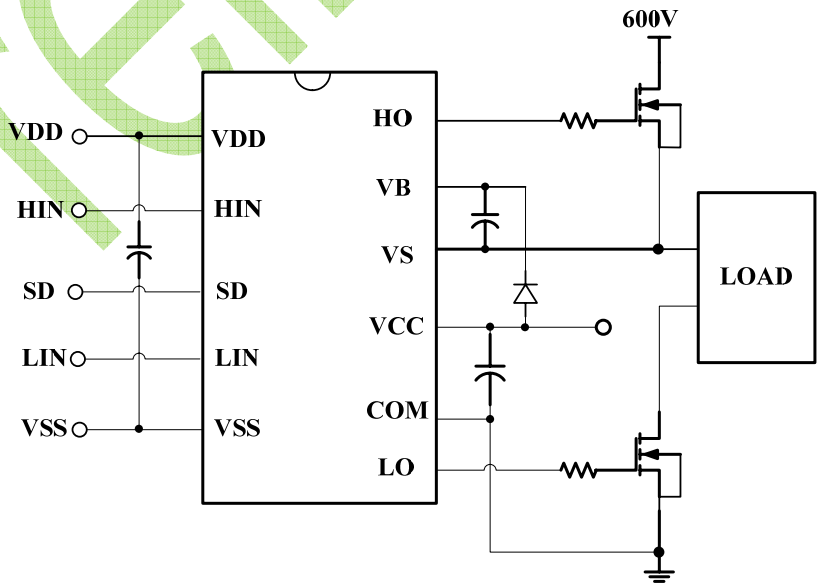


Figure1. Typical Application Circuit

Pin Description

PIN NO.	PIN NAME	PIN FUNCTION
1	VDD	Logic supply
2	HIN	Logic input for high side gate driver output (HO), in phase
3	SD	Logic input for shutdown
4	LIN	Logic input for low side gate driver output (LO), in phase
5	VSS	Logic ground
6	VB	High side floating supply
7	HO	High side gate drive output
8	VS	High side floating supply return
9	VCC	Low side supply
10	LO	Low side gate drive output
11	COM	Low side return

Functional Block Diagram

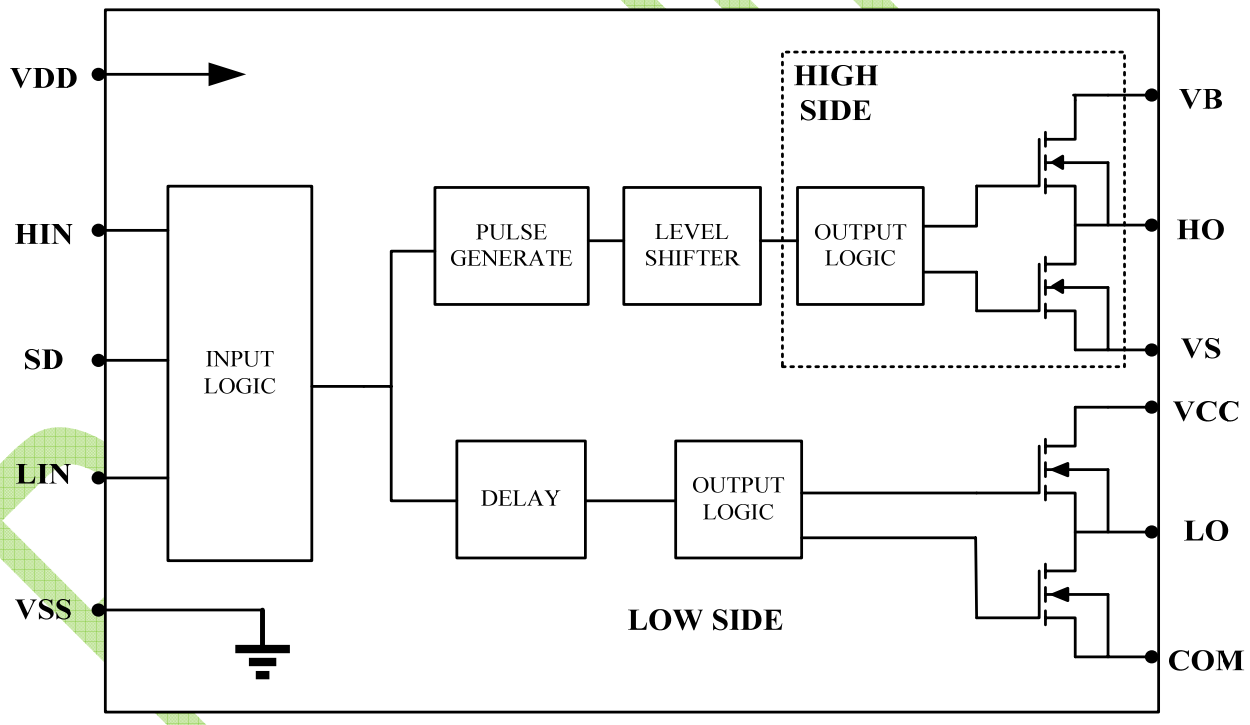


Figure2 Functional Block Diagram

Absolute Maximum Ratings [Note1]

Symbol	Definition	MIN.	MAX.	Units
VB	High side floating supply	-0.3	625	V
VS	High side floating supply return	VB - 25	VB + 0.3	
VHO	High side gate drive output	VS -0.3	VB + 0.3	
VCC	Low side supply	-0.3	25	
VLO	Low side gate drive output	-0.3	VCC + 0.3	
VDD	Logic supply	-0.3	VSS + 25	
VSS	Logic ground	VCC-25	VCC + 0.3	
VIN	Logic input for high side	VSS-0.3	VDD + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	--	55	V/ns
P_D	Package Power Dissipation @ TA ≤25°C (14 Lead DIP)	--	1.6	W
	(14 Lead DIP w/o Lead 4)	--	1.5	
	(16 Lead DIP w/o Leads 5 & 6)	--	1.6	
	(16 Lead SOIC)	--	1.25	
R_qJA	Thermal Resistance Junction to Ambient (14 Lead DIP)	--	75	°C /W
	(14 Lead DIP w/o Lead 4)	--	85	
	(16 Lead DIP w/o Leads 5 & 6)	--	75	
	(16 Lead SOIC)	--	100	
TJ	Junction Temperature	--	150	°C
TS	Storage Temperature	-55	150	
TL	Lead Temperature (Soldering, 10 seconds)	--	300	

Note 1: Exceeding these ratings may damage the device.

Recommended Operating Conditions

Symbol	Definition	MIN.	MAX.	Units
VB	High side floating supply	V_S+10	V_S+20	V
VS	High side floating supply return	-	600	
VHO	High side gate drive output	VS	VB	
VCC	Low side supply	10	20	
VLO	Low side gate drive output	0	VCC	
VDD	Logic supply	Vss+3	Vss+20	
VSS	Logic ground	-5	5	
HIN	Logic input for high side	VSS	VDD	
LIN	Logic input for low side	VSS	VDD	

Dynamic Electrical Characteristics

VBIAS (VCC, VBS, VDD) = 15V, CL = 1000 pF, TA = 25°C and VSS = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

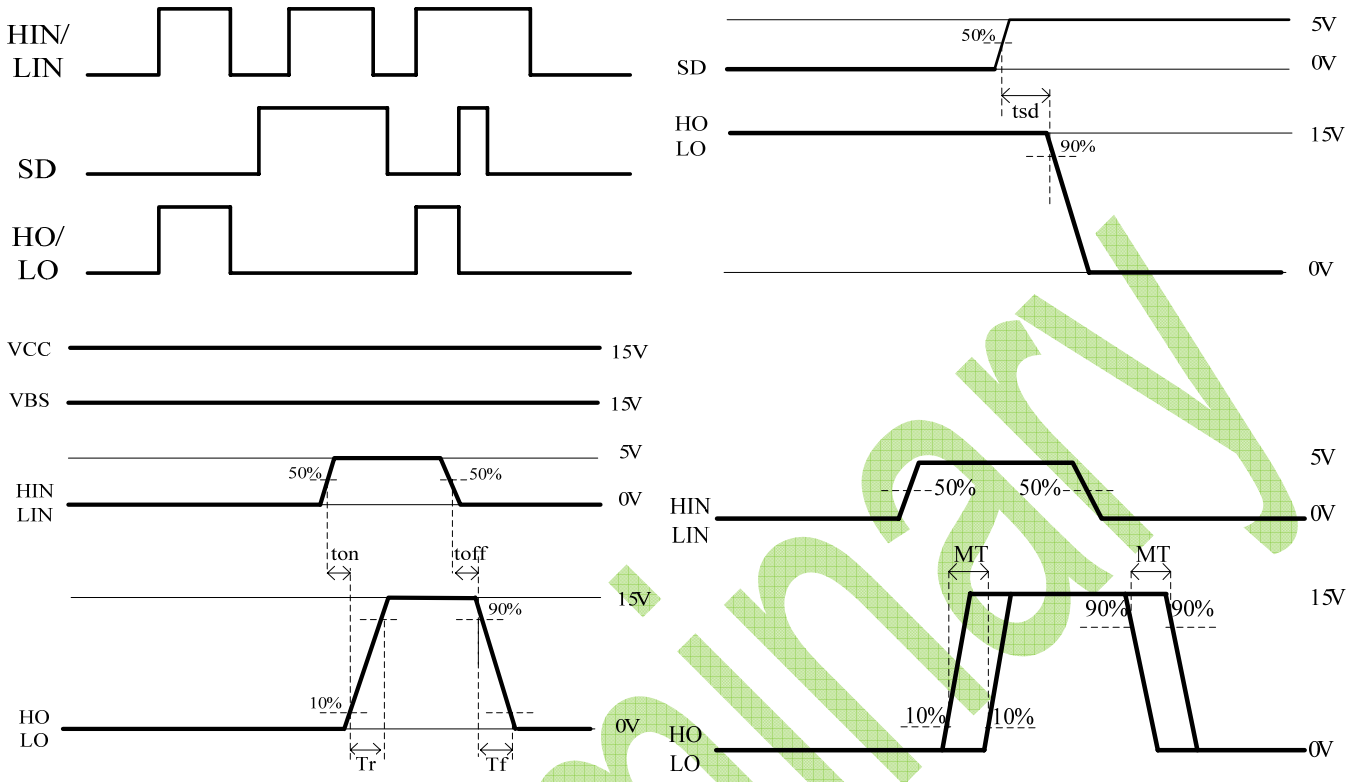
Symbol	Definition	TYP.	MAX.	Units
ton_H	High side turn-on propagation delay	130	140	ns
$toff_H$	High side turn-off propagation delay	135	150	
ton_L	Low side turn-on propagation delay	120	130	
$toff_L$	Low side turn-off propagation delay	115	125	
MT	Turn-on delay matching	16	20	
	Turn-off delay matching	16	20	
Tr	Turn-on rise time	26	30	
Tf	Turn-off fall time	24	30	

Static Electrical Characteristics

VBIAS (VCC, VBS, VDD) = 15V, TA = 25°C and VSS = COM unless otherwise specified. The VIN, VTH and IIN parameters are referenced to VSS and are applicable to all three logic input leads: HIN, LIN and SD. The VO and IO parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	MIN.	TYP.	MAX.	Units
VIH	Logic “1” input voltage	8.5	-	-	V
VIL	Logic “0” input voltage	-	-	6.2	
VOH	High level output voltage, V_{BIAS} - V_O	-	1.3	-	
VOL	Low level output voltage, V_O	-	0.1	-	
IQCC	Quiescent VCC supply current	-	-	124	uA
IQBS	Quiescent VBS supply current	-	74	-	uA
IN+	Logic “1” input bias current	-	-	19	
IN-	Logic “0” input bias current	-	24	-	
VBSU+	VBS supply UVLO threshold	-	8.6	-	V
VBSU-		-	8.2	-	
VCCU+	VCC supply UVLO threshold	-	8.5	-	
VCCU-		-	8.2	-	**A**
IO+	Source pulsed current(PW<10us)		3.0		
IO-	Sink pulsed current(PW<10us)		3.0		

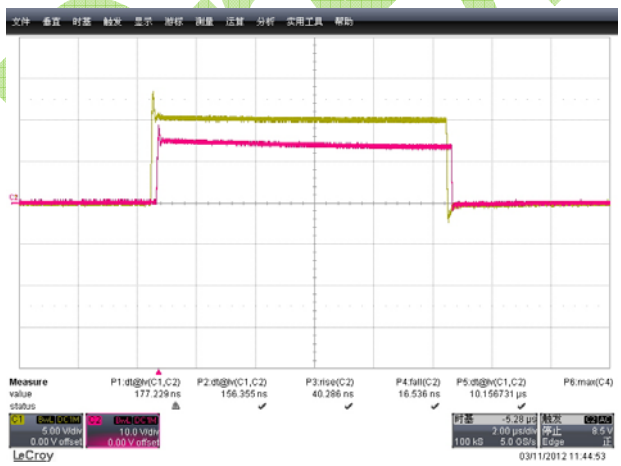
Logic Function & Timing Spec



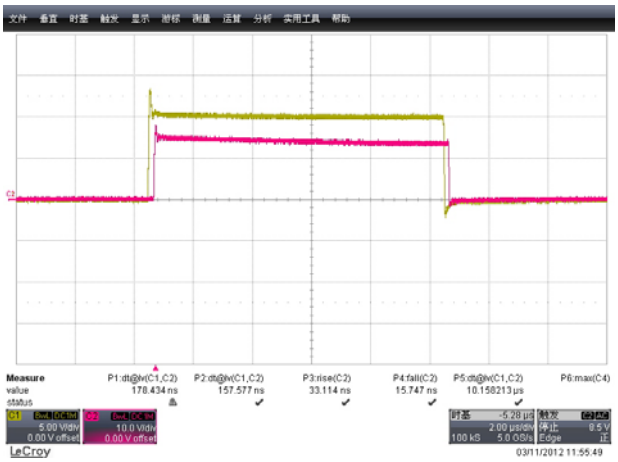
Typical Performance Characteristics

VDD=10V, VCC=15V, VB=15V, VS=0V

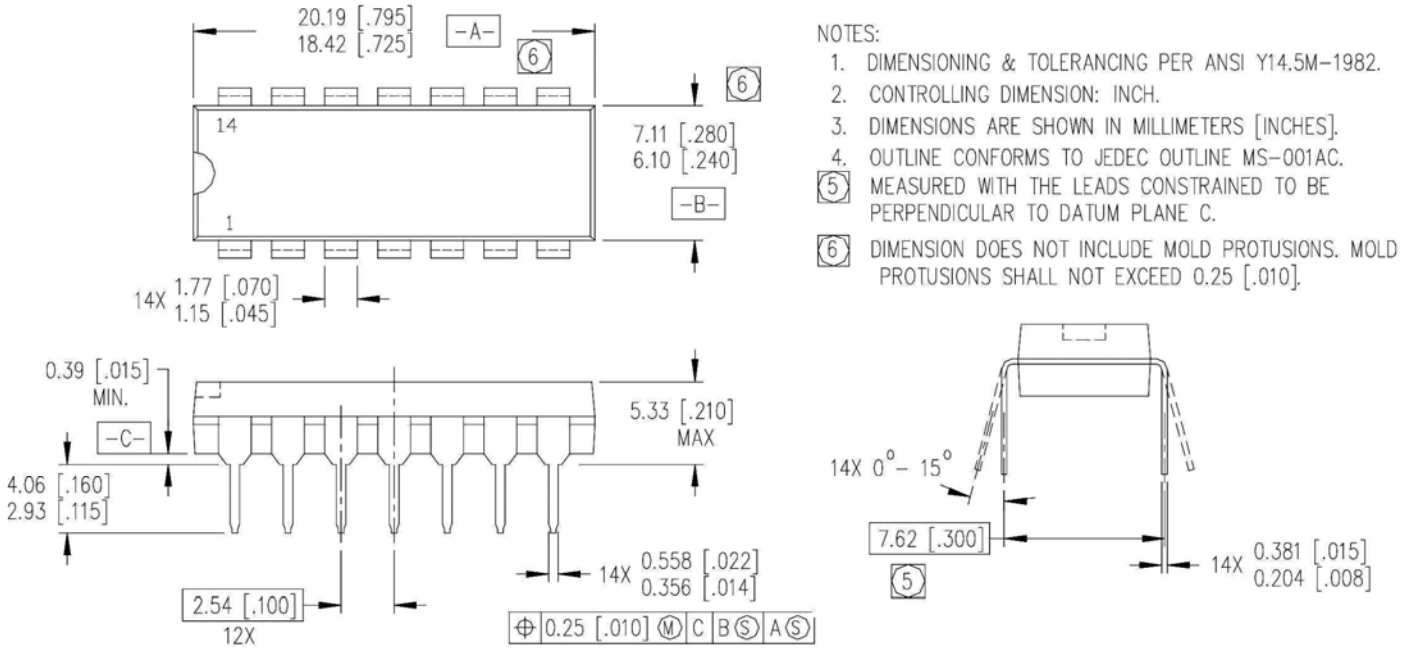
Low Side



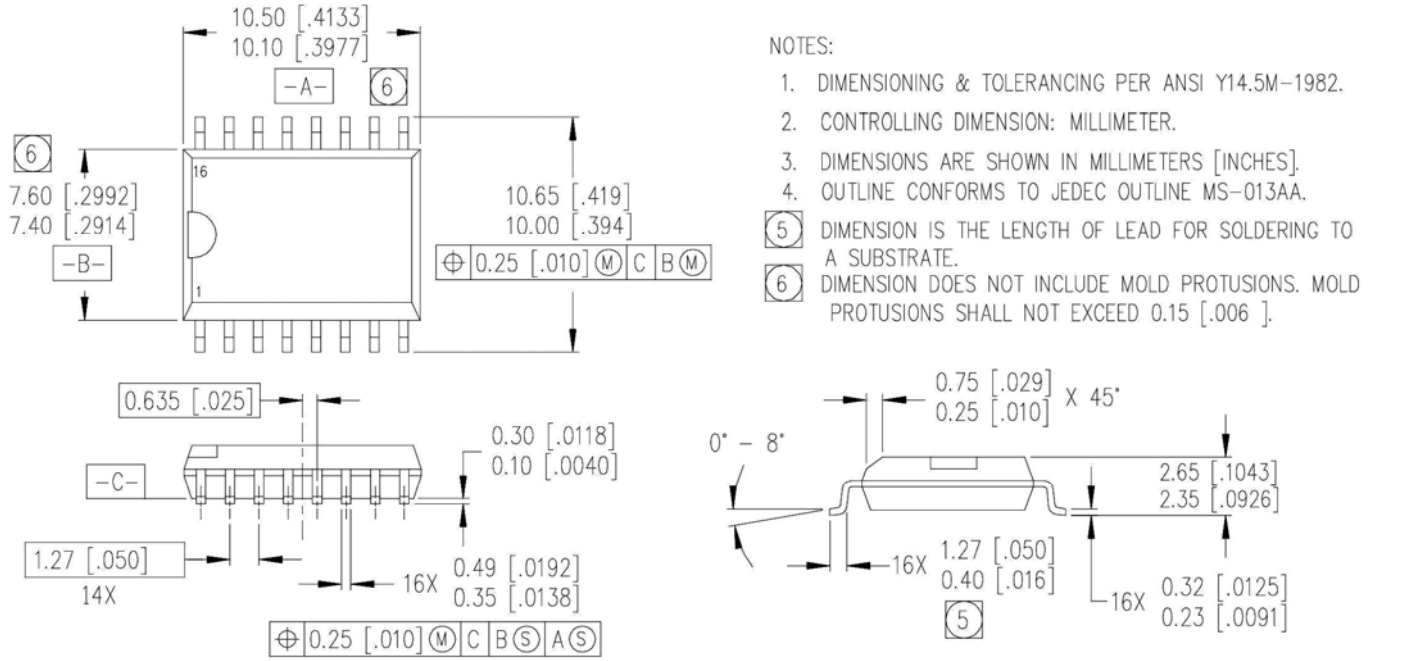
High Side



Package Information



14-Lead PDIP



16-Lead SOIC (wide body)

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