A7602E-H&A7608SA-H Hardware Design

LTE Module

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Version History

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1 Introduction

This document describes the electronic specifications, RF specifications, interfaces, mechanical characteristics and testing results of the SIMCom module. With the help of this document and other software application notes/user guides, users can understand and use module to design and develop applications quickly.

1.1 Product Outline

Aimed at the global market, the module support GSM, WCDMA, LTE-TDD and LTE-FDD. Users can choose the module according to the wireless network configuration. The supported radio frequency bands are described in the following table.

Table 1: Module Frequency Bands

Standard	Frequency bands	Module	
		A7602E-H	A7608SA-H
GSM	850MHz		✓
	900MHz	✓	✓
	1800MHz	✓	✓
	1900MHz		✓
WCDMA	BAND1	✓	✓
	BAND2		✓
	BAND5		✓
	BAND8	✓	✓
LTE-FDD	LTE-FDD B1	✓	✓
	LTE-FDD B2		✓
	LTE-FDD B3	✓	✓
	LTE-FDD B4		✓
	LTE-FDD B5	✓	✓
	LTE-FDD B7	✓	✓
	LTE-FDD B8	✓	✓
	LTE-FDD B20	✓	✓
	LTE-FDD B28		✓
	LTE-FDD B66		✓
LTE-TDD	LTE TDD B34		
	LTE TDD B38	✓	✓

	LTE TDD B39		
	LTE TDD B40	✓	✓
	LTE TDD B41	✓	✓
Category	/	CAT4	CAT4
GNSS	/	Optional	Optional
Aux ANT	/	Optional	Optional

With a small physical dimension of 30*30*2.5 mm and with the functions integrated, the module can meet almost any space requirement in users' applications, such as smart phone, PDA, industrial handhold, machine-to-machine and vehicle application, etc.

1.2 Hardware Interfaces Overview

The interfaces are described in detail in the next chapter include:

- Power Supply
- USB2.0 Interface
- UART Interfaces
- MMC/SD Interface
- USIM Interface
- GPIOs
- ADC
- Two channels LDO Power Output
- PCM Interface
- SPI Interface
- I2C Interface
- Analog Audio Interface

Table 2: Module Function List

Function	Support
USB2.0	✓
UART	✓
SDC3.0	✓
USIM	✓
ADC	✓
PCM	✓
SPI	✓
I2C	✓
Analog Audio	✓
GPIOs	✓
GNSS	Optional
MAIN ANT	✓
AUX ANT	Optional
GNSS ANT	✓

1.3 Hardware Block Diagram

The block diagram of the module is shown in the figure below.

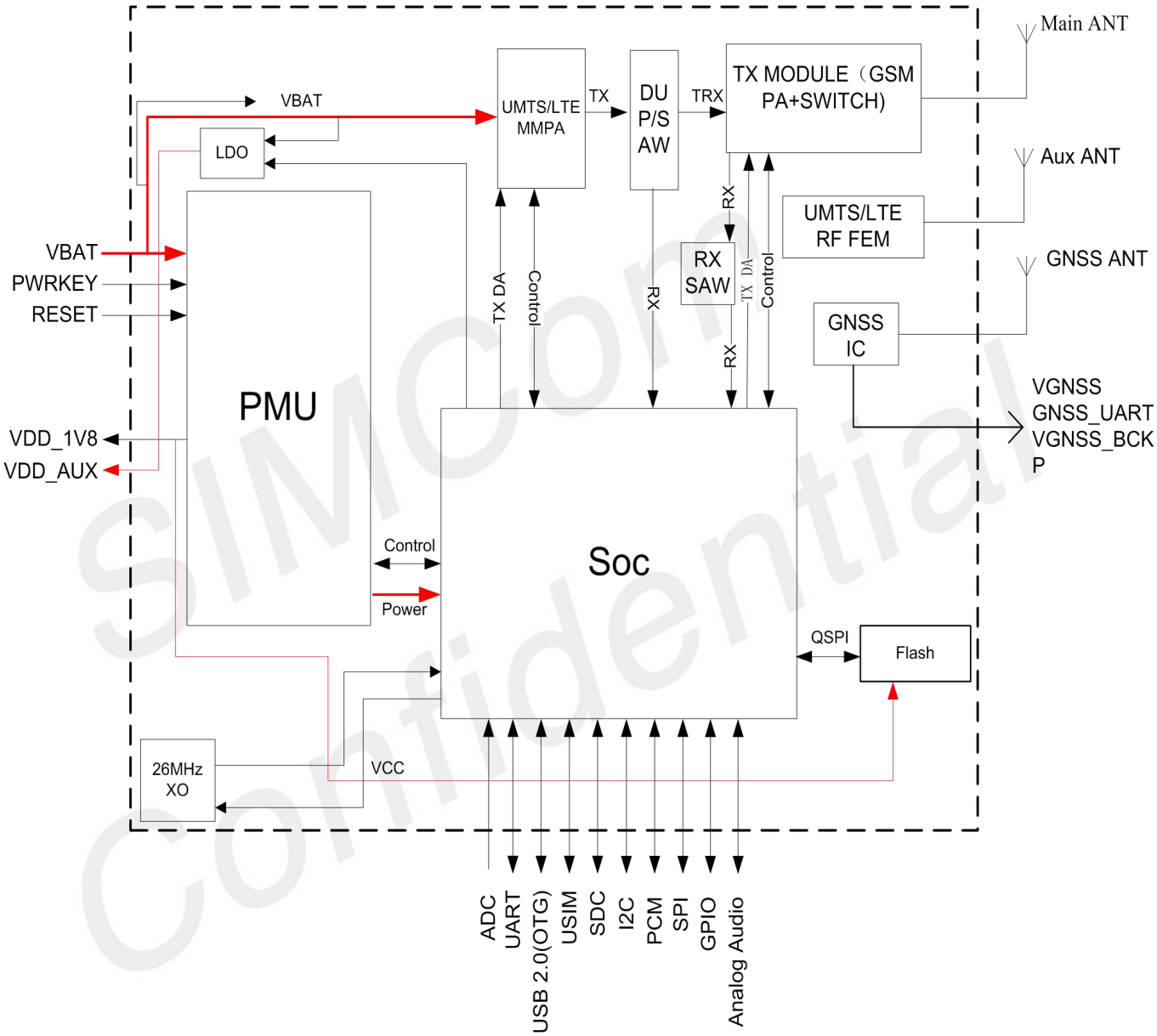

Figure 1: Module Block Diagram

1.4 Functional Overview

Table 3: General Features

Feature	Implementation
Power supply	Single supply voltage 3.4～4.2 V， recommend 3.8 V.
Power saving	Current in sleep mode : <5 mA
Radio frequency bands	Please refer to the table 1
Transmitting power	GSM/GPRS power class: --GSM850: 4 (2W) --EGSM900: 4 (2W) --DCS1800: 1 (1W) --PCS1900: 1 (1W) EDGE power class: --GSM850: E2 (0.5W) --EGSM900: E2 (0.5W) --DCS1800: E1 (0.4W) --PCS1900: E1 (0.4W) UMTS power class: --WCDMA :3 (0.25W) LTE power class: 3 (0.25W)
Data Transmission Throughput	GPRS multi-slot class 12 EDGE multi-slot class 12 UMTS R99 speed: 384 kbps DL/UL HSPA+: 5.76 Mbps(UL), 42 Mbps(DL) HSDPA/HSUPA: 2.2 Mbps(UL), 2.8 Mbps(DL) LTE-FDD CAT4 ：150 Mbps (DL)，50 Mbps (UL) LTE-TDD CAT4 ：130 Mbps (DL)，35 Mbps (UL)
Antenna	GSM/UMTS/LTE main antenna. UMTS/LTE auxiliary antenna GNSS antenna
GNSS	GNSS engine (GPS,GLONASS and BD) Protocol: NMEA
SMS	MT, MO, CB, Text and PDU mode SMS storage: USIM card or ME(default) Transmission of SMS alternatively over CS or PS.
USIM interface	Support identity card: 1.8 V / 3 V
USIM application toolkit	Support SAT class 3, GSM 11.14 Release 98 Support USAT
Phonebook management	Support phonebook types: DC,MC,RC,SM,ME,FD,ON,LD,EN
Audio feature	Support PCM interface Only support PCM master mode and short frame sync, 16-bit linear data formats

UART interfaces	**MAIN UART:** A full modem serial port by default Baud rate: 9600 bps to 3.6Mbps(default:115200 bps) Can be used as the AT commands or data stream channel Support RTS/CTS hardware handshake Multiplex ability according to GSM 07.10 Multiplexer Protocol **Debug UART:** Used for Software console and log output Baud rate: 9600 bps to 3.6 Mbps(default:115200 bps) **GNSS UART：** Used for GNSS communication Baud rate: 9600 bps to 921600 bps(default:9600 bps)
eMMC/SD	Support eMMC and SD Cards with 2.85 V on SD port
USB	USB2.0 high speed interface
Firmware upgrade	Firmware upgrade over USB interface
Physical characteristics	Size:30*30*2.5 mm Weight:5.7 g
Temperature range	Normal operation temperature: -30 °C to +80 °C Extended operation temperature: -40 °C to +85 °C* Storage temperature -45 °C to +90 °C

NOTE

Module is able to make and receive voice calls, data calls, SMS and make GPRS/UMTS/HSPA+/LTE traffic in -40 ℃ ~ +85 ℃. The performance will be reduced slightly from the 3GPP specifications if the temperature is outside the normal operating temperature range and still within the extreme operating temperature range.

2 Package Information

2.1 Pin Assignment Overview

All functions of the module will be provided through 172 pads that will be connected to the customers' platform. The following Figure is a high-level view of the pin assignment of the module.

The module supports 2 kinds of OS, and the pad name is different with different OS, following figure shows the Rtos series module PIN MAP.

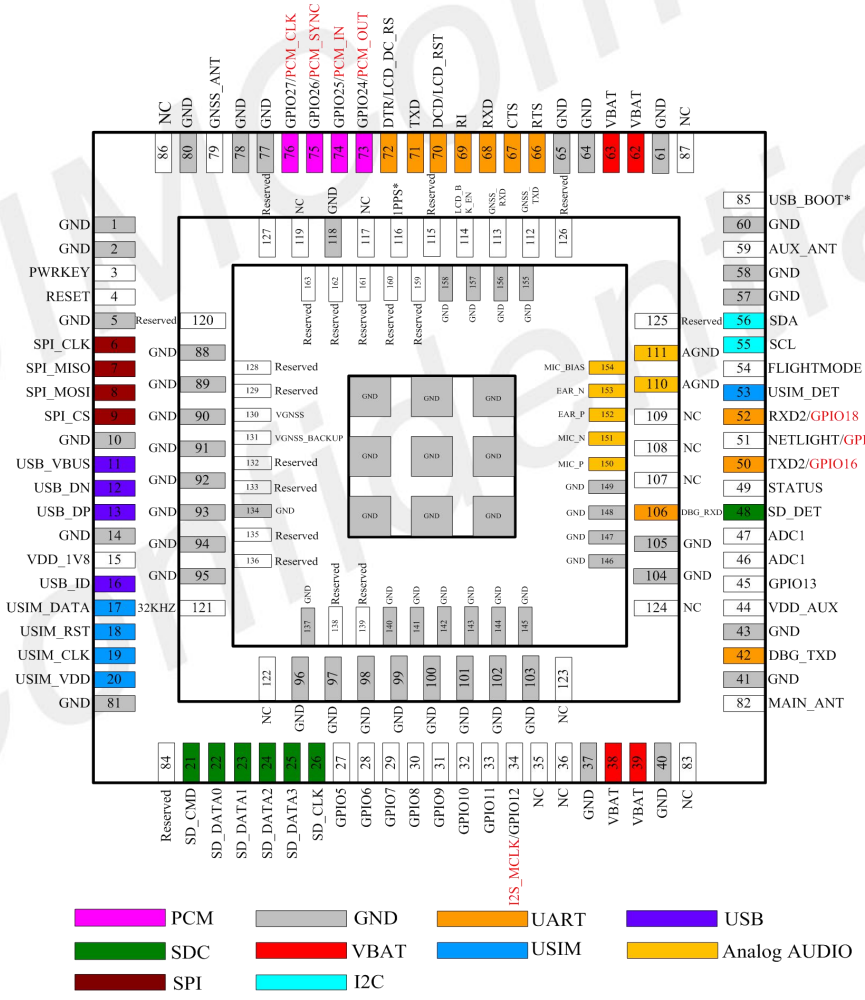

Figure 2: Pin Assignment Overview

Table 4: Pin Definition

PIN No	PIN Name	PIN No	PIN Name
1	GND	2	GND
3	PWRKEY	4	RESET
5	GND	6	SPI_CLK
7	SPI_MISO	8	SPI_MOSI
19	SPI_CS	10	GND
11	USB_VBUS	12	USB_DN
13	USB_DP	14	GND
15	VDD_1V8	16	USB_ID
17	USIM_DATA	18	USIM_RST
19	USIM_CLK	20	USIM_VDD
21	SD_CMD	22	SD_DATA0
23	SD_DATA1	24	SD_DATA2
25	SD_DATA3	26	SD_CLK
27	GPIO5	28	GPIO6
29	GPIO7	30	GPIO8
31	GPIO9	32	GPIO10
33	GPIO11	34	I2S_MCLK/GPIO12
35	NC	36	NC
37	GND	38	VBAT
39	VBAT	40	GND
41	GND	42	DBG_TXD
43	GND	44	VDD_AUX
45	GPIO13	46	ADC1
47	ADC1	48	SD_DET
49	STATUS	50	TXD2/GPIO16
51	NETLIGHT/GPIO17	52	RXD2/GPIO18
53	USIM_DET	54	FLIGHTMODE
55	SCL	56	SDA
57	GND	58	GND
59	AUX_ANT	60	GND
61	GND	62	VBAT
63	VBAT	64	GND
65	GND	66	RTS
67	CTS	68	RXD
69	RI	70	DCD/LCD_RST
71	TXD	72	DTR/LCD_DC_RS
73	GPIO24/PCM_OUT	74	GPIO25/PCM_IN
75	GPIO26/PCM_SYNC	76	GPIO27/PCM_CLK
77	GND	78	GND
79	GNSS_ANT	80	GND

81	GND	82	MAIN_ANT
83	NC	84	Reserved
85	USB_BOOT*	86	NC
87	NC	88	GND
89	GND	90	GND
91	GND	92	GND
93	GND	94	GND
95	GND	96	GND
97	GND	98	GND
99	GND	100	GND
101	GND	102	GND
103	GND	104	GND
105	GND	106	DBG_RXD
107	NC	108	NC
109	NC	110	AGND
111	AGND	112	GNSS_TXD
113	GNSS_RXD	114	LCD_BK_EN
115	Reserved	116	1PPS*
117	NC	118	GND
119	NC	120	Reserved
121	32KHZ*	122	NC
123	NC	124	NC
125	Reserved	126	Reserved
127	Reserved	128	Reserved
129	Reserved	130	VGNSS
131	VGNSS_BACKUP	132	Reserved
133	Reserved	134	GND
135	Reserved	136	Reserved
137	GND	138	Reserved
139	Reserved	140	GND
141	GND	142	GND
143	GND	144	GND
145	GND	146	GND
147	GND	148	GND
149	GND	150	MIC_P
151	MIC_N	152	EAR_P
153	EAR_N	154	MIC_BIAS
155	GND	156	GND
157	GND	158	GND
159	Reserved	160	Reserved
161	Reserved	162	Reserved

163	Reserved	**164**	GND
165	GND	**166**	GND
167	GND	**168**	GND
169	GND	**170**	GND
171	GND	**172**	GND

NOTE

Before the normal power on, the USB_BOOT cannot be pull down to ground, otherwise module will not be powered up normally.

2.2 Pin Description

Table 5: IO Parameters Definition

PI	Power input
PO	Power output
AI	Analog input
AIO	Analog input/output
I/O	Bidirectional input /output
DI	Digital input
DO	Digital output
DIO	Digital input/output
DOH	Digital output with high level
DOL	Digital output with low level
PU	Pull up
PD	Pull down

Table 6: Electric Feature

Power domain	Symbol	Description	Min	Typ	Max
P3	1.8 V				
	VOH	Output high	1.6 V	-	1.8 V
	VOL	Output low	0 V	-	0.2 V
	VIH	Input high	1.26 V	1.8 V	2.0 V
	VIL	Input low	-0.3 V	0 V	0.54 V
	Rpu	Pull-up resiter	55 KΩ	79 KΩ	121 KΩ
	Rpd	Pull-down resiter	51 KΩ	87 KΩ	169 KΩ
P5,P8	1.8 V				
	VOH	Output high	1.6 V	-	1.8 V
	VOL	Output low	0 V	-	0.2 V
	VIH	Input high	1.26 V	1.8 V	2.0 V
	VIL	Input low	-0.3 V	-	0.54 V
	Rpu	Pull-up resiter	55 KΩ	79 KΩ	121 KΩ
	Rpd	Pull-down resiter	51 KΩ	87 KΩ	169 KΩ
	3.0 V				
	VOH	Output high	2.4 V	-	-

Table 7: Pin Description

Pin Name	Pin No.	Power Domain	Defalt Stats	Description	Comment
Power supply					
VBAT	38,39,62,63	-	PI	Power supply for the module.	Power supply, voltage range: 3.4 ~ 4.2 V.
VDD_AUX	44	-	PO	LDO power output for other external circuits with Max 150 mA current output. Its output voltage is 2.85 V fixed.	If unused, keep it open.
VDD_1V8	15	-	PO	1.8 V output with Max 50 mA current output for external circuit, such as level shift circuit.	If unused, keep it open.
GND	1,2,5,10,14,37,40,41,43,57,58,60,61,64,65,77,78,80,81,88~105,118,134,137,140~149,155~158,164~172	-	-	Ground	
RESERVED	84,115,120,125~129,132,133,135,136,138,139,159~163	-	-		Keep these pins unconnected
NC	35,36,83,86,87,107~109,117,119,122~124	-	-		Keep these pins unconnected
PWRKEY	3	-	DI,PU	System power on/off control input, active low.	It has been pulled up to VBAT via 50 KΩ resistor internally.
RESET	4	-	DI, PU	System reset control input, active low.	It has been pulled up to VBAT via 50 KΩ resistor internally.
SD Interface					
SD_CMD	21	P8	DIO,PU	SD Card Bidirectional command/response signal.	The power domain of SD I/O pins depends on P8. If unused, keep them open.
SD_DATA0	22	P8	DIO,PU	SD Card Bidirectional data signal bit 0.	
SD_DATA1	23	P8	DIO,PU	SD Card Bidirectional data signal bit 1.	
SD_DATA2	24	P8	DIO,PU	SD Card Bidirectional data	

				signal bit 2.	
SD_DATA3	25	P8	DIO,PU	SD Card Bidirectional data signal bit 3.	
SD_CLK	26	P8	DO, PD	SD Card clock.	
SD_DET	48	P3	DI, PU	SD hot-plug detect.	Default: GPIO Optional: SD card detecting input. H: SD card is removed L: SD card is inserted. Pull it up to VDD_EXT with a 100 kΩ resistor.If unused, keep it open.
USIM Interface					
USIM_DATA	17	P5	DIO,PU	USIM Card data.	which has been pulled up via 4.7 KΩ resistor to USIM_VDD internally. Do not pull it up or down externally.
USIM_RST	18	P5	DO,PU	USIM Card reset.	
USIM_CLK	19	P5	DO, PU	USIM Card clock.	
USIM_VDD	20	-	PO	USIM Card power supply.	its output Voltage depends on USIM card type automatically. Its output current is up to 50 mA.
USIM_DET	53	P3	DI,PU	USIM Card hot-plug detect.	Default: GPIO Optional: USIM card detecting input. H: USIM is removed L: USIM is inserted
USB Interface					
USB_VBUS	11	-	AI	Valid USB detection input with 3.6~5.25 V detection voltage.	For USB connection detection only, not power supply.
USB_DN	12	-	AIO	Negative line of the differential, bi-directional USB signal.	Requires differential impedance of 90 Ω. USB 2.0 supports downward compatibility.
USB_DP	13	-	AIO	Positive line of the differential, bi-directional USB signal.	
USB_ID	16	-	DI,PU	USB ID input.	Keep it open.
MAIN UART					
TXD	71	P3	DO,PU	Transmit data.	

RXD	68	P3	DI,PU	Receive data	
RTS	66	P3	DO,PU	DTE request to send.	
CTS	67	P3	DI,PU	DCE clear to send.	
RI	69	P3	DO,PU	Ring Indicator	
DCD	70	P3	DO,PU	Data carrier detect.	
DTR	72	P3	DI,PU	Data terminal ready, sleep mode control.	
GNSS UART					
TXD2	50	P3	DO,PU	Transmit data for GNSS communication.	
RXD2	52	P3	DI,PU	Receive data for GNSS communication.	
Debug UART					
DBG_TXD	42	P3	DO,PU	Transmit data for debug.	Print Kernel log
DBG_RXD	106	P3	DI, PU	Receive data for debug.	
PCM Interface					
PCM_OUT	73	P3	DO,PD	PCM data output.	If unused, please keep them open.
PCM_IN	74	P3	DI,PD	PCM data input.	
PCM_SYNC	75	P3	DO,PD	PCM data frame sync signal.	
PCM_CLK	76	P3	DO,PD	PCM data bit clock.	
I2S_MCLK	34	P3	DO,PD	I2S MCLK.	
SPI Interface					
SPI_CLK	6	P3	DO,PD	SPI clock output	
SPI_MISO	7	P3	DI,PD	SPI master in/slave out data	
SPI_MOSI	8	P3	DO,PD	SPI master out/slave in data	
SPI_CS	9	P3	DO,PD	SPI chip-select output	
LCD Control Interface					
LCD_DC_RS	72	P3	DO,PU	LCD data/command select	If unused, please keep them open.
LCD_RST	70	P3	DO,PU	LCD reset	
LCD_BK_EN	114	P3	DO,PD	LCD Backlight control	
I2C Interface					
SCL	55	P3	OD,PU	I2C serial clock output	It has been pulled up to VDD_1V8 via 2.2 KΩ resistor internally. If unused, keep them open.
SDA	56	P3	OD,PU	I2C serial data input/output	
Analog Audio Interface					
AGND	110,111	-	PI	Analog Ground	
MIC_P	150	-	AI	Microphone input positive	
MIC_N	151	-	AI	Microphone input negative	
EAR_P	152	-	AO	Earphone output positive	
EAR_N	153	-	AO	Earphone output negative	
MIC_BIAS	154	-	PO	Microphone bias voltage	

GNSS Control Interface					
VGNSS	130	-	PI	GNSS supply voltage	Power supply, voltage range: 1.7 ~ 1.9 V.
VGNSS_BACK UP	131	-	PI	GNSS backup battery	Power supply, voltage range: 1.4 ~ 3.6 V.
GNSS_TXD	112	-	DO	GNSS NMEA data port	
GNSS_RXD	113	-	DI	GNSS NMEA data port	
1PPS*	116	-	-	-	In developing
GPIO Interface					
GPIO5	27	P3	DIO,PU	General input/output 5	If unused, please keep them open.
GPIO6	28	P3	DIO,PU	General input/output 6	
GPIO7	29	P3	DIO,PU	General input/output 7	
GPIO8	30	P3	DIO,PU	General input/output 8	
GPIO9	31	P3	DIO,PU	General input/output 9	
GPIO10	32	P3	DIO,PU	General input/output 10	
GPIO11	33	P3	DIO,PD	General input/output 11	
GPIO12	34	P3	DIO,PD	General input/output 12	
GPIO13	45	P3	DIO,PU	General input/output 13	
GPIO17	51	P3	DIO,PD	General input/output 17	
GPIO24	73	P3	DIO,PD	General input/output 24	
GPIO25	74	P3	DIO,PD	General input/output 25	
GPIO26	75	P3	DIO,PD	General input/output 26	
GPIO27	76	P3	DIO,PD	General input/output 27	
RF Interface					
MAIN _ANT	82		AIO	MAIN antenna soldering pad	
GNSS_ANT	79		AI	GNSS antenna soldering pad	
AUX_ANT	59		AI	Auxiliary antenna soldering pad	
Other Interface					
ADC1	46,47	-	AI	Analog-digital converter input 1.	Max input voltage 1.8V
STATUS	49		DO,PU	Indicates the module's operation status.	
NETLIGHT	51	P3	DO,PD	LED control output as network status indication.	
FLIGHTMODE	54	P3	DI,PD	Flight Mode control input. High level(or open): Normal Mode Low level: Flight Mode	
USB_BOOT*	85	P3	DI,PD	Forces the module to enter emergency download mode	
32KHZ*	121	-	DO,PD		In developing

2.3 Mechanical Information

The following figure shows the package outline drawing of module.

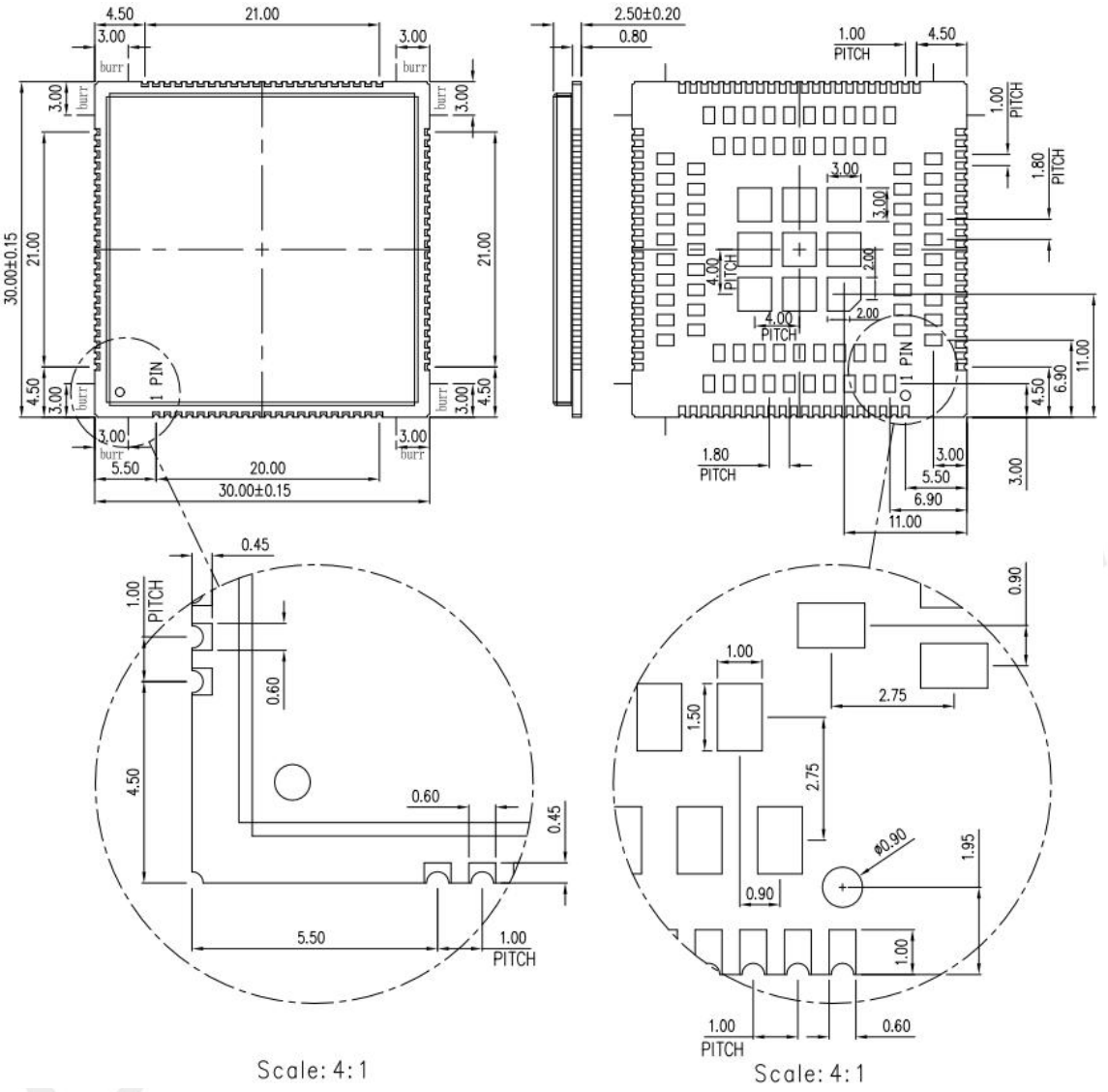

Figure 3: Mechanical Dimensions (Unit: mm)

2.4 Footprint Recommendation

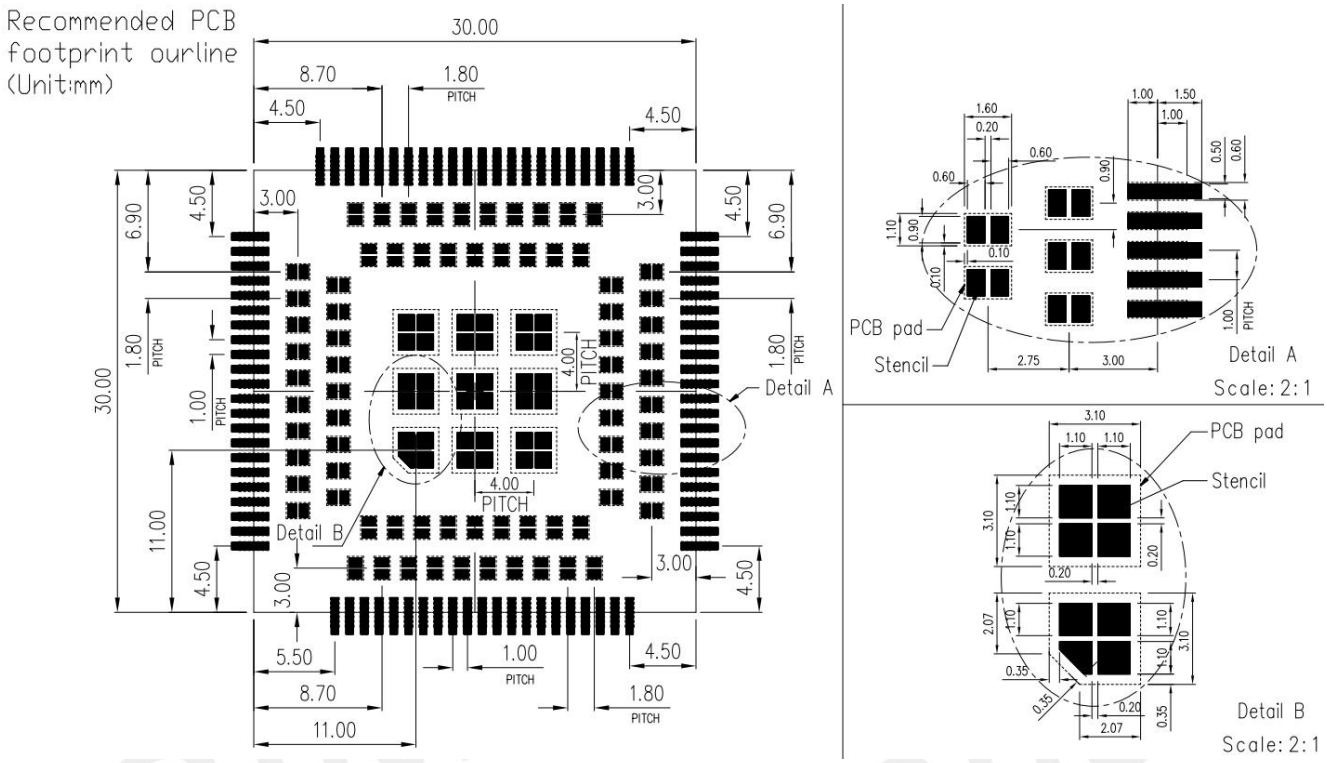

Figure 4: Footprint Recommendation (Unit: mm)

3 Interface Application

3.1 Power Supply

The power supply pins of module include 4 pins (pin 62&63, pin 38&39) named VBAT.

The 4 VBAT pads supply the power to RF and baseband circuits directly.
On VBAT pads, the ripple current up to 2 A typically, due to GSM/GPRS emission burst (every 4.615 ms), may cause voltage drop. So the power supply for these pads must be able to provide sufficient current up to more than 2 A in order to avoid the voltage drop is more than 300 mV.

The following figure shows the VBAT voltage ripple wave at the maximum power transmit phase.

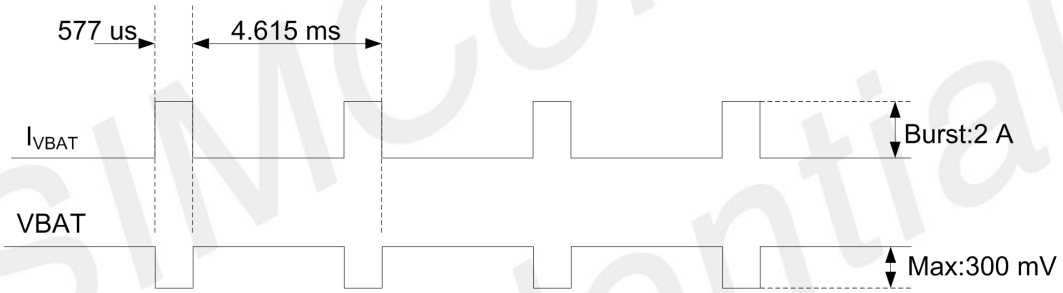

Figure 5: VBAT Voltage Drop during Burst Emission (GSM/GPRS)

NOTE

The test condition: The voltage of power supply for VBAT is 3.8 V, Cd=100 μF tantalum capacitor (ESR=0.7 Ω) and Cf=100 nF (Please refer to Figure 6 application circuit).

Table 8: VBAT Electronic Characteristic

Symbol	Description	Min.	Typ.	Max.	Unit
VBAT	Module power voltage	3.4	3.8	4.2	V
$I_{VBAT(peak)}$	Module power peak current in normal mode.	-	2	-	A
$I_{VBAT(average)}$	Module power average current in normal mode	Please refer to the table 34			
$I_{VBAT\ (sleep)}$	Power supply current in sleep mode				
$I_{VBAT\ (power-off)}$	Module power current in power off mode.			30	uA

3.1.1 Power Supply Design Guide

Make sure that the voltage on the VBAT pins will never drop below 3.4 V, even during a transmit burst, when current consumption may rise up to 2 A. If the voltage drops below 3.4 V, the RF performance may be affected.

NOTE

If the power supply for VBAT pins can support up to 2 A, more than 300 uF capacitors are recommended. Otherwise users must use a total of 1000 uF capacitors typically, in order to avoid of the voltage drop more than 300 mV.

Some multi-layer ceramic chip (MLCC) capacitors (0.1/1 uF) with low ESR in high frequency band can be used for EMC.

These capacitors should be put as close as possible to VBAT pads. Also, users should keep VBAT trace on circuit board wider than 2 mm to minimize PCB trace impedance. The following figure shows the recommended circuit. Recommend part of FB101 is BLM21PG300SN1D or MPZ2012S221A。

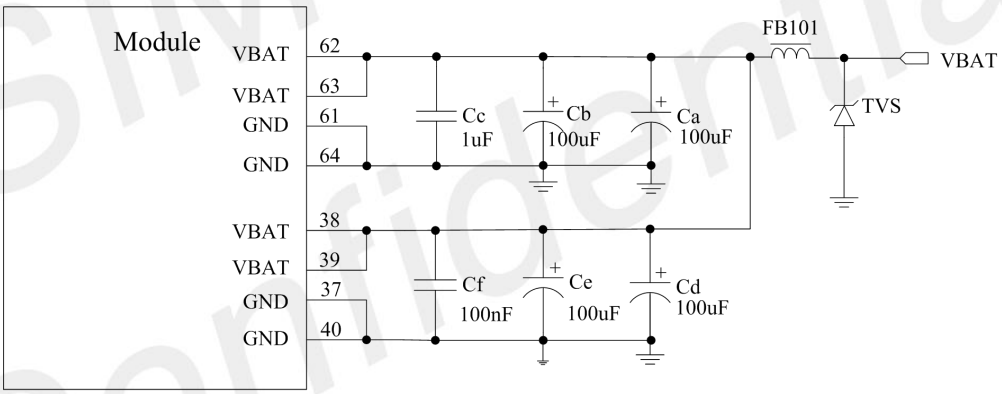

Figure 6: Power Supply Application Circuit

In addition, in order to guard for ESD or surge protection, it is suggested to use a TVS to protect the module.

NOTE

Customer could only power pin 62, 63 or only power pin 38, 39, for these pins are connected inside the module.

Table 9: Recommended TVS List

No	Manufacturer	Part Number	Reverse Stand-Off Voltage	Package
1	Js-ele	ESDBW5V0A1	5 V	DFN1006-2L
2	Prisem	PESDHC2FD4V5BH	4.5 V	DFN1006-2L
3	Way-on	WS05DPF-B	5 V	DFN1006-2L
4	Will semi	ESD5611N	5 V	DFN1006-2L
5	Will semi	ESD56151W05	5 V	SOD-323
6	Way-on	WS4.5DPV	4.5 V	DFN1610-2L

3.1.2 Recommended Power Supply Circuit

It is recommended that a switching mode power supply or a linear regulator power supply is used. It is important to make sure that all the components used in the power supply circuit can resist a peak current up to 2 A.

The following figure shows the linear regulator reference circuit with 5 V input and 3.8 V output.

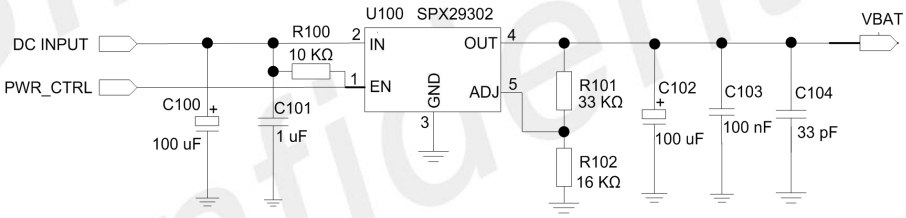

Figure 7: Linear Regulator Reference Circuit

If there is a big voltage difference between input and output for VBAT power supply, or the efficiency is extremely important, then a switching mode power supply will be preferable. The following figure shows the switching mode power supply reference circuit.

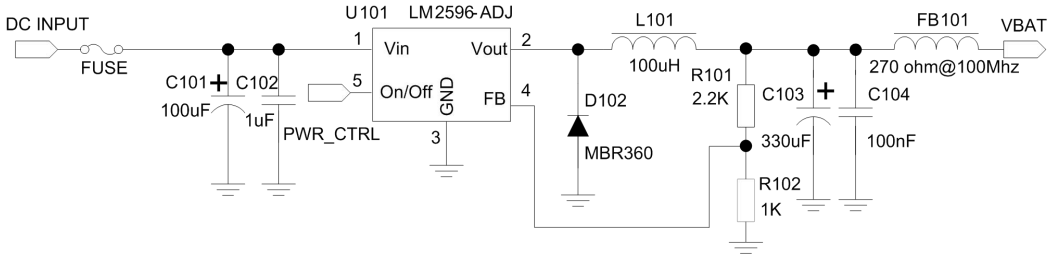

Figure 8: Switching Mode Power Supply Reference Circuit

NOTE

1. The Switching Mode power supply solution for VBAT must be chosen carefully against Electro Magnetic Interference and ripple current from depraving RF performance.
2. If the DC input is 12 V, customer must select a buck circuit to get better power efficiency.

3.1.3 Voltage Monitor*

To monitor the VBAT voltage, the AT command “AT+CBC” can be used.

For monitoring the VBAT voltage outside or within a special range, the AT command “AT+CVALARM” can be used to enable the under-voltage warning function.

If users need to power off module, when the VBAT voltage is out of a range, the AT command “AT+CPMVT” can be used to enable under-voltage power-off function.

NOTE

1. Under-voltage warning function and under-voltage power-off function are disabled by default. For more information about these AT commands, please refer to Document [1].
2. “*” means under development.

3.2 Power on/Power off/Reset Function

3.2.1 Power on

Module can be powered on by pulling the PWRKEY pin down to ground.

The PWRKEY pin has been pulled up with a diode to 1.8 V internally, so it does not need to be pulled up externally. It is strongly recommended to put an ESD protection diode, close to the PWRKEY pin as it would strongly enhance the ESD performance of PWRKEY pin. Please refer to the following figure for the recommended reference circuit.

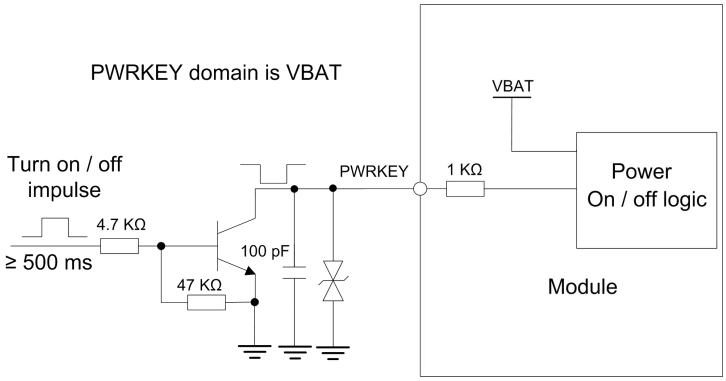

Figure 9: Reference Power On/off Circuit

NOTE

Module could be automatically power on by connecting PWRKEY pin to ground via 0 Ωresistor directly.

The power-on scenarios are illustrated in the following figure.

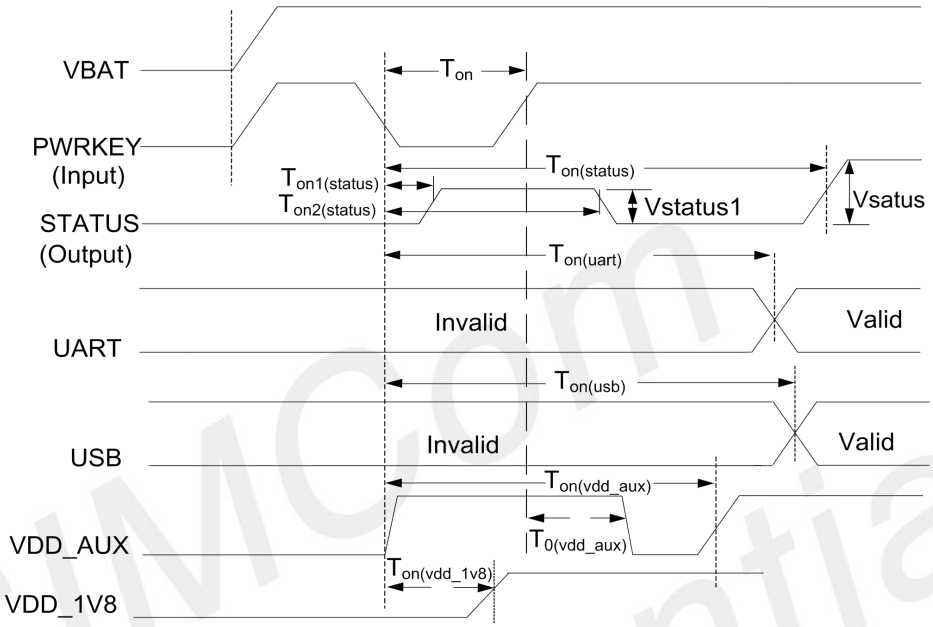

Figure 10: Power On Timing Sequence

Table 10: Power On Timing and Electronic Characteristic

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{on}	The time of active low level impulse of PWRKEY pin to power on module	500	1000	2000	ms
$T_{on(status)}$	The time from power-on issue to STATUS pin output high level(indicating power up ready)	20	-	-	s
$T_{on1(status)}$	The time from power-on issue to STATUS pin output the fisrt rising edge(indicating power up ready)	-	9.6	-	ms
$T_{on2(status)}$	The time from power-on issue to STATUS pin output the fisrt falling edge(indicating power up ready)		5.9		s
$T_{on(uart)}$	The time from power-on issue to UART port ready	15	-	-	s
$T_{on(vdd\_aux)}$	The time from power-on issue to VDD_AUX ready	20	-	-	s
$T_{0(vdd\_aux)}$	The VDD_AUX is on before the software ready	3	-	-	s
$T_{on(vdd\_1V8)}$	The time from power-on issue to VDD_1V8 ready	100	-	-	ms
$T_{on(usb)}$	The time from power-on issue to USB port ready	20	25	-	s
V_{IH}	Input high level voltage on PWRKEY pin	0.7*VBAT	VBAT	VBAT +0.3	V
V_{IL}	Input low level voltage on PWRKEY pin	-0.3	0	0.5	V
Vstatus	Input second hight voltage on STATUS pin	-	0.8		V
Vstatus1	Input first hight voltage on STATUS pin		1.8		V

NOTE

1. When the Ton time less than 500ms, the module might power on, but only the Ton time more than 500 ms, the module will power on is reliably guaranteed.
2. After power-on, STATUS shows a Vstatus1 level for a period of time, which is determined by the module itself, you can ignore it.

3.2.2 Power Off

The following methods can be used to power off module.

- Method 1: Power off module by pulling the PWRKEY pin down to ground.
- Method 2: Power off module by AT command “AT+CPOF”.
- Method 3: over-voltage or under-voltage automatic power off. The voltage range can be set by AT command “AT+CPMVT”.
- Method 4: over-temperature or under-temperature automatic power off.

NOTE

If the temperature is outside the range of -30~+80 ℃, some warning will be reported via AT port. If the temperature is outside the range of -40~+85 ℃, module will be powered off automatically.
For details about “AT+CPOF” and “AT+CPMVT”, please refer to Document [1].

These procedures will make module disconnect from the network and allow the software to enter a safe state, and save data before module be powered off completely.

The power off scenario by pulling down the PWRKEY pin is illustrated in the following figure.

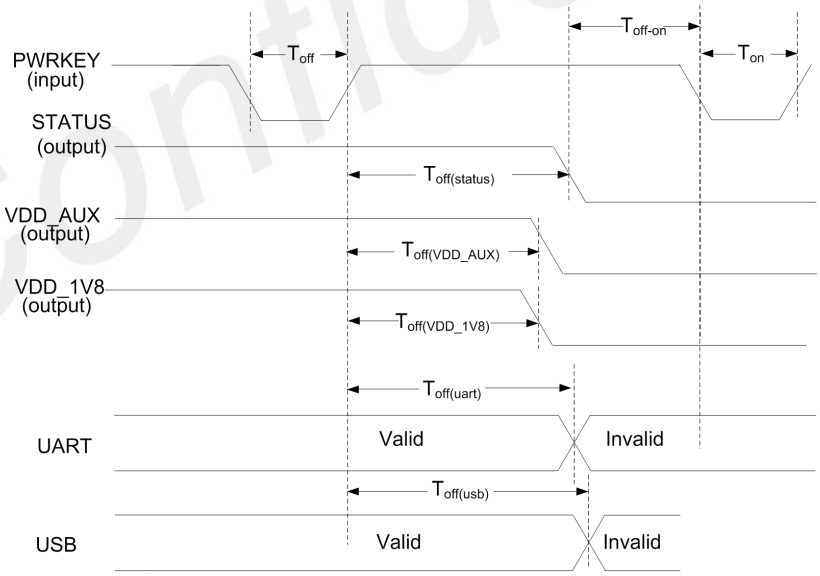

Figure 11: Power Off Timing Sequence

Table 11: Power Off Timing and Electronic Characteristic

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{off}	The active low level time pulse on PWRKEY pin to power off module	2.5	--	5.0	s
$T_{off(status)}$	The time from power-off issue to STATUS pin output low level(indicating power off)*	TBD	TBD	-	s
$T_{off(uart)}$	The time from power-off issue to UART port off	TBD	TBD	-	s
$T_{off(usb)}$	The time from power-off issue to USB port off	TBD	TBD	-	s
$T_{off(VDD\_AUX)}$	The time from power-off issue to vdd_aux off	TBD	-	-	s
$T_{off(VDD\_1V8)}$	The time from power-off issue to vdd_1V8f	TBD	-	-	s
T_{off-on}	The buffer time from power-off issue to power-on issue	3	-	-	s

NOTE

1. The STATUS pin can be used to detect whether module is powered on or not. When module has been powered on and firmware goes ready, STATUS will be high level, or else STATUS will still low level.
2. It is suggested that the host can cut off the power off the module, when the module could not switch off by PWRKEY of RESET interface, customer could cut off the power to restart the module.
3. If the PWERKY and RESET key works normally, it is not suggested to switch off module by remove the power supply for that might damage the flash.
4. The power off time may vary for the local net status.

3.2.3 Reset Function

Module can be reset by pulling the RESET pin down to ground.

NOTE

This function is only used as an emergency reset, when AT command “AT+CPOF” and the PWRKEY pin all have lost efficacy.

The RESET pin has been pulled up with a 40 KΩ resistor to 1.8 V internally, so it does not need to be pulled up externally. It is strongly recommended to put a100 nF capacitor and an ESD protection diode close to the RESET pin. Please refer to the following figure for the recommended reference circuit.

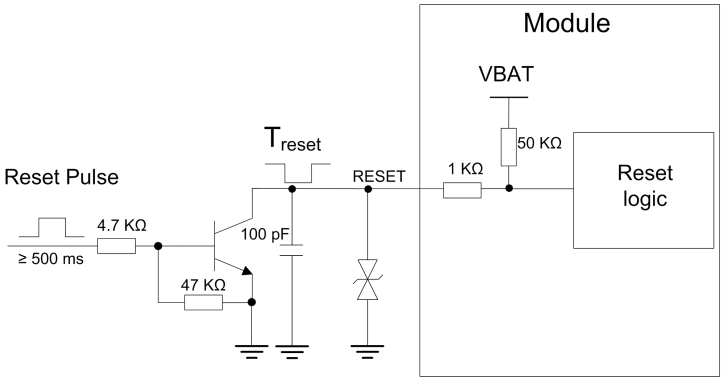

Figure 12: Reference Reset Circuit

Table 12: RESET Electronic Characteristic

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{reset}	The active low level time impulse on RESET pin to reset module	500	1000	2000	ms
V_{IH}	Input high level voltage	0.7*VBAT	VBAT	VBAT+ 0.3	V
V_{IL}	Input low level voltage	-0.3	0	0.5	V

NOTE

1. When the module could not switch off by PWRKEY of RESET interface, customer should cut off the power to restart the module.
2. If the PWERKY and RESET key works normally, it is not suggested to switch off module by remove the power supply for that might damage the flash.

3.3 UART Interfaces

The module provides three UART interfaces: one MAIN UART interface, one Debug UART interface, and one GNSS UART interface.

- **MAIN UART:** Module provides a 7-wire UART (universal asynchronous serial transmission) interface as DCE (Data Communication Equipment). AT commands and data transmission can be performed through UART interface.
- **Debug UART:** Used for Rtos console and log output.
  Default baud rate: 115200 bps
- **GNSS UART:** Used for GNSS communication.
  Default baud rate: 9600bps

3.3.1 MAIN UART Design Guide

The following figures show the reference design.

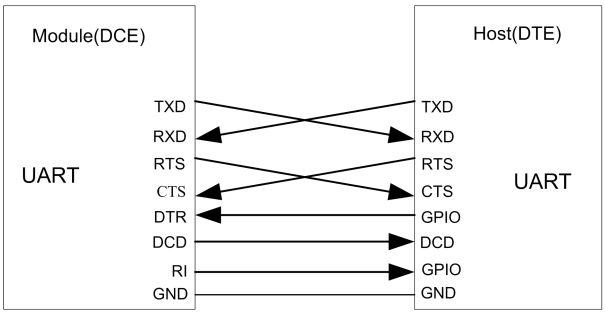

Figure 13: UART Full Modem

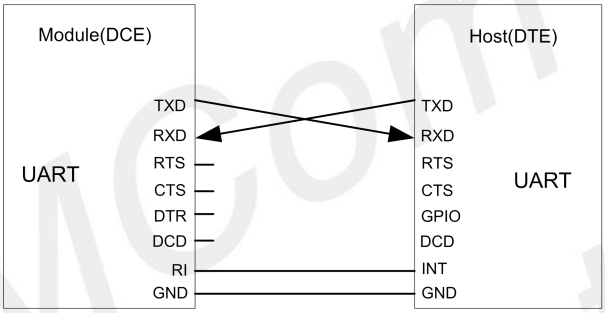

Figure 14: UART Null Modem

The module UART is 1.8 V voltage interface. If user's UART application circuit is 3.3 V voltage interface, the level shifter circuits should be used for voltage matching. The TXB0108RGYR provided by Texas Instruments is recommended. The following figure shows the voltage matching reference design.

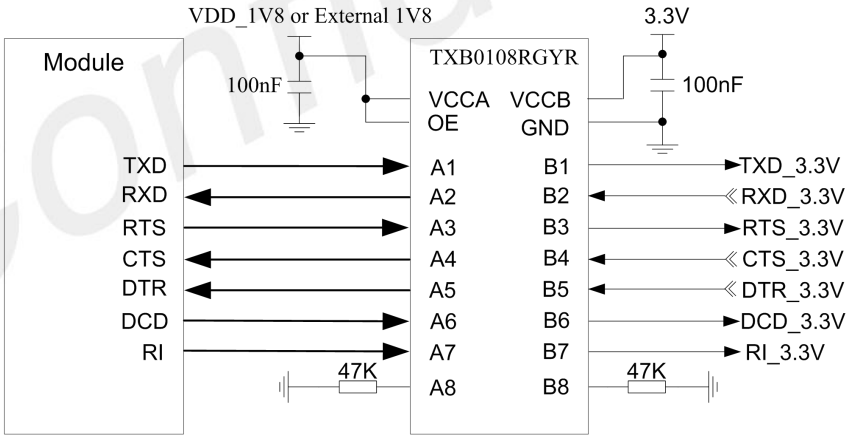

Figure 15: Reference Circuit of Level Shift

Customers can use another level shifter circuits as follow.

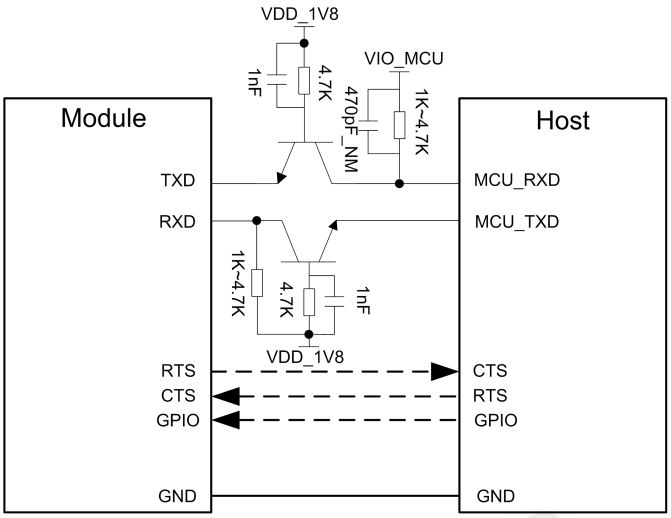

Figure 16: Level Matching Circuit With Triode

NOTE

1. User need to use high speed transistors such as MMBT3904.
2. MAIN UART supports the following baud rates: 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600, 1843200, 3686400 bps. The default band rate is 115200 bps.

3.3.2 RI and DTR Behavior

The RI pin can be used to interrupt output signal to inform the host controller such as application CPU.

Normally RI will keep high level until certain conditions such as receiving SMS, or a URC report coming, and then it will change to low level.

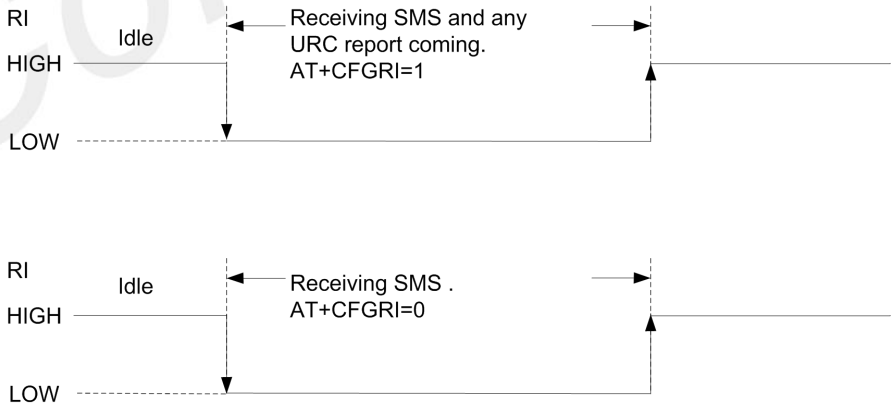

Figure 17: RI Behaviour（SMS and URC report）

Normally RI will be kept at a high level until a voice call, then it will output periodic rectangular wave with 5900 ms low level and 100ms high level. It will output this kind of periodic rectangular wave until the call is

answered or hung up.

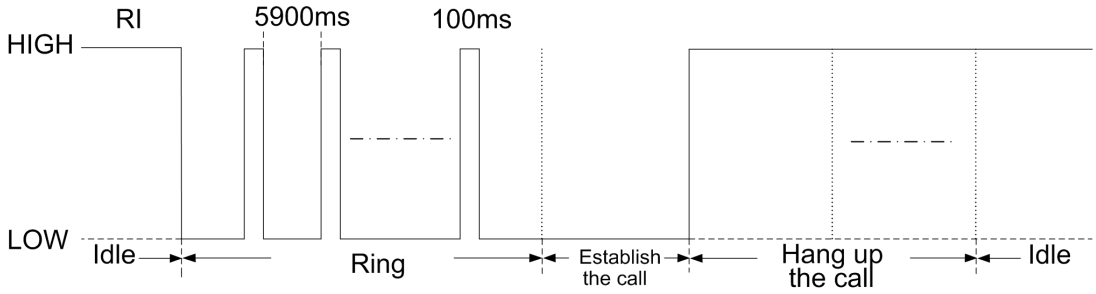

Figure 18: RI Behaviour（Voice Call）

NOTE

For more details of AT commands about UART, please refer to document [1] and [22].

DTR pin can be used to wake module from sleep. When module enters sleep mode, pulling down DTR can wake module.

3.4 USB Interface

The module contains a USB interface compliant with the USB2.0 specification as a peripheral, but the USB charging function is not supported.

3.4.1 USB Diagram

Module can be used as a USB device. module supports the USB suspend and resume mechanism which can reduce power consumption. If there is no data transmission on the USB bus, module will enter suspend mode automatically, and will be resumed by some events such as voice call, receiving SMS, etc. The USB interface is a frequency used debug port; it is suggested to reserved test point.

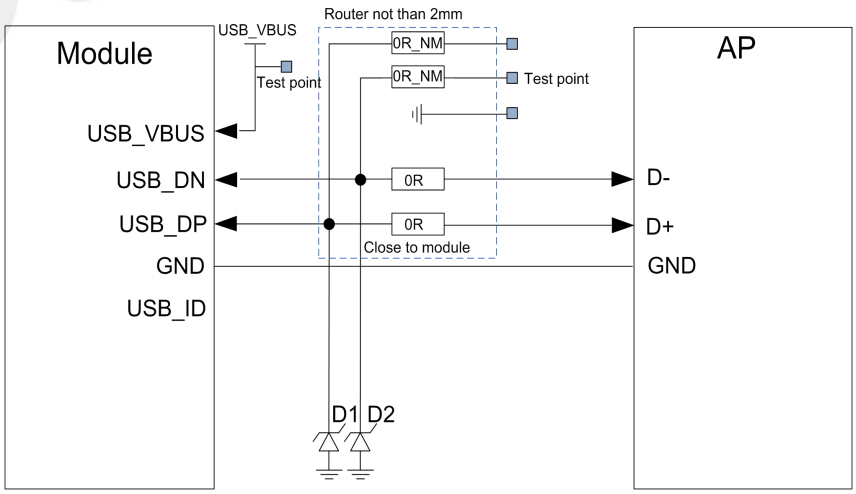

Figure 19: USB Reference Circuit

Because of the high bit rate on USB bus, more attention should be paid to the influence of the junction capacitance of the ESD component on USB data lines. Typically, the capacitance should be less than 1 pF. It is recommended to use an ESD protection component such as ESD9L5.0ST5G provided by On Semiconductor (www.onsemi.com).

NOTE

The USB_DN and USB_DP nets must be traced by 90 Ω+/-10% differential impedance.

3.4.2 USB_BOOT

Module can enter in download mode by USB_BOOT.

Table 13: USB_BOOT Description

PIN No	PIN Name	I/O	description	Power domain	Default status	Index
85	USB_BOOT	DI	USB boot	1.8 V	B-PU	

If the module download failed, then customer can make module enter download mode via this Pin. Before the module power on, pull the USB_BOOT to ground， then push the PWRKEY to power on module, when the module enter download mode, the pull down should be removed.

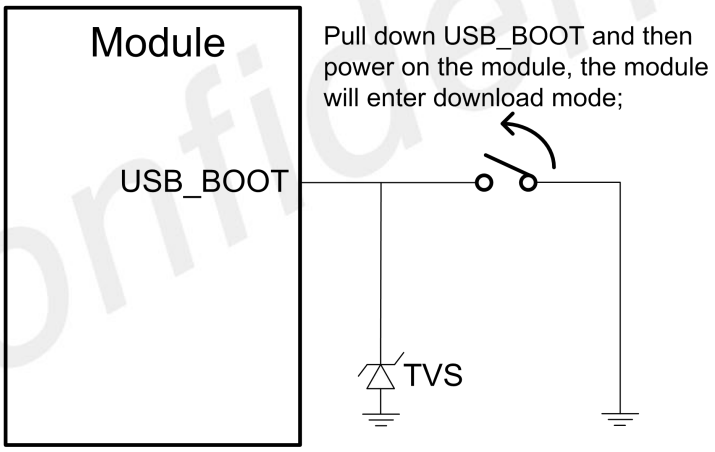

Figure 20: USB_BOOT Circuit

Customer can check the download port in the device management.

Figure 21: USB Download Port

3.4.3 USB_ID

Module support OTG function， but the USB_VBUS(PIN 11) cannot supply device with 5 V, so customer should design the circuit to power the USB device.

Table 14: USB_ID Description

PIN No	PIN Name	I/O	Function description	Domain	Default Status	index
16	USB_ID	DI	High level: module in USB device mode. Low level: module in USB host mode.	1.8 V	DI-PH	

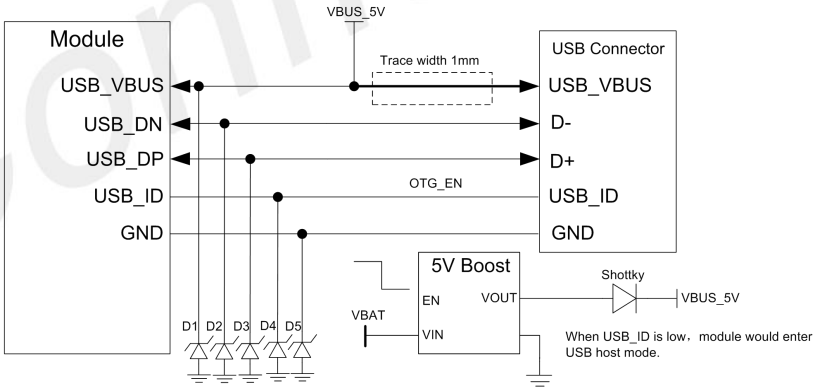

Figure 22: USB_OTG Diagram

3.5 Analog Audio

The module support 1 pair of audio input(MIC_P，MIC_N) for microphone, and support 1 pair of audio output for earphone.

Table 15: Audio Interface Definition

PIN No	PIN Name	I/O	Function description	Power domain	Default	Index
150	MIC_P	AI	Mic input positive	-	-	
151	MIC_N	AI	Mic input negative	-	-	
152	EAR_P	AO	Earphone output positive	-	-	
153	EAR_N	AO	Earphone output negative	-	-	
154	MIC_BIAS	PO	Mic bias voltage	-	-	
110,111	AGND	-	Analog ground	-	-	

Customer could use “AT+CMIC” to tune the gain of microphone input signal, “AT+CLVL” could used to tune the gain of output gain.

The following figure shows the reference circuit.

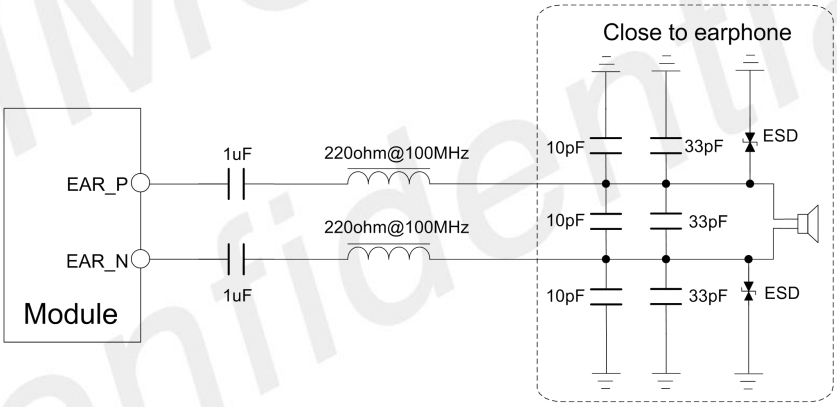

Figure 23: Receiver Circuit

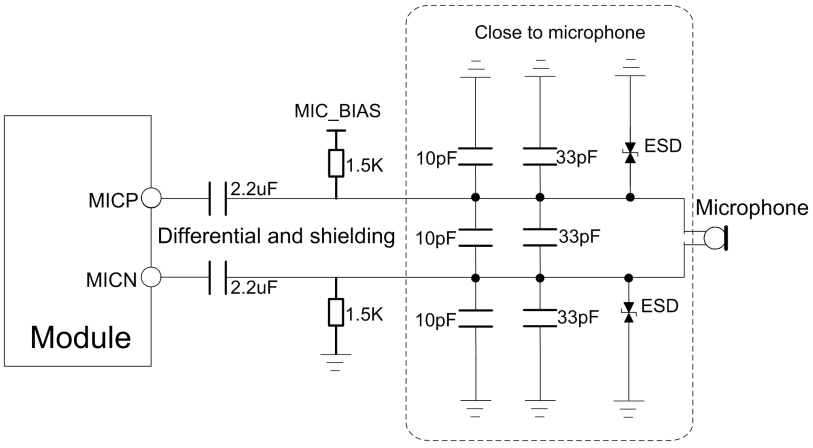

Figure 24: Microphone Circuit

Table 16: Audio Input Parameter

Parameter	Test condition	Min	Typ	Max	Unit
Mic bias voltage		-	1.8	-	V
Working current		-	-	2.0	mA
Dynamic Range	Measured as THD+N at 60dB below full scale, 0dB PGA gain,20~20KHz	-	91	-	dB
Peak-SNDR	-4dBFS output, at 0dB gain	-	86	-	
THD	-1dBFS output, at 0dB gain	-	80	-	dB
PGA+ADC gain options	GAIN= (0dB,6dB,12dB,18dB,24dB)	-	12	-	dB

Table 17: Audio Output Parameter

Parameter	Test condition	Dynamic Range（Typ）	THD+N(Typ)	Power（1% THD）
Output	RL=32 Ω eraphone	-	15	90
DAC	RL=10K Ω	101 dBA	-96 dB(@vout - 2 dBv)	1.59 Vp
Class-AB	Mono,32 Ω, differential	100 dBA	-90 dB(0.00316%) (@20 mW output)	37 mW

GSM signal can interfere with audio through coupling and conduction. Users can filter out coupling interference by adding 33 pF and 10 pF capacitors to the audio path. The 33 pF capacitor mainly filters out the interference in the GSM900 frequency band, and the 10 pF capacitor mainly filters out the interference in the DCS1800 frequency band. The coupling interference of TDD has a lot to do with the user's PCB design. In some cases, TDD in the 900 frequency band is more serious, and in some cases, the TDD interference in the 1800 frequency band is more serious.Therefore, the user can select the required filter capacitor according to the actual test results, and sometimes it is not necessary to paste the filter capacitor.

The antenna of GSM is the main source of coupling interference for TDD, so users should pay attention to keeping the audio trace away from the RF antenna and VBAT during PCB layout and wiring. It is best to place a set of audio filter capacitors close to the module end and another set close to the interface end. The audio output should be routed in accordance with the differential signal rules.

The conduction interference is mainly caused by the voltage drop of VBAT. If Audio PA is directly powered by VBAT, it is easier to hear a "squeak" sound at the output of SPK. Therefore, it is best to connect the input of Audio PA in parallel when designing the schematic. Some large value capacitors and series magnetic beads.

TDD and GND are also closely related. If GND is not handled well, many high-frequency interference signals will interfere with MIC and Speaker through bypass capacitors and other components. Therefore, it is important for users to ensure good GND performance during the PCB design stage.

3.6 USIM Interface

Module supports both 1.8 V and 3.0 V USIM Cards.

Table 18: USIM Electronic Characteristic in 1.8 V Mode (USIM_VDD=1.8 V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
USIM_VDD	LDO power output voltage	1.75	1.8	1.95	V
V_{IH}	High-level input voltage	0.65*USIM_VDD	-	USIM_VDD +0.3	V
V_{IL}	Low-level input voltage	-0.3	0	0.35*USIM_VDD	V
V_{OH}	High-level output voltage	USIM_VDD -0.45	-	USIM_VDD	V
V_{OL}	Low-level output voltage	0	0	0.45	V

Table 19: USIM Electronic Characteristic 3.0V Mode (USIM_VDD=2.95V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
USIM_VDD	LDO power output voltage	2.75	2.95	3.05	V
V_{IH}	High-level input voltage	0.65*USIM_VDD	-	USIM_VDD +0.3	V
V_{IL}	Low-level input voltage	-0.3	0	0.25*USIM_VDD	V
V_{OH}	High-level output voltage	USIM_VDD -0.45	-	USIM_VDD	V
V_{OL}	Low-level output voltage	0	0	0.45	V

3.6.1 USIM Application Guide

It is recommended to use an ESD protection component such as ESDA6V1W5 produced by ST (www.st.com) or SMF15C produced by ON SEMI (www.onsemi.com). Note that the USIM peripheral circuit should be close to the USIM card socket. The following figure shows the 6-pin SIM card holder reference circuit.

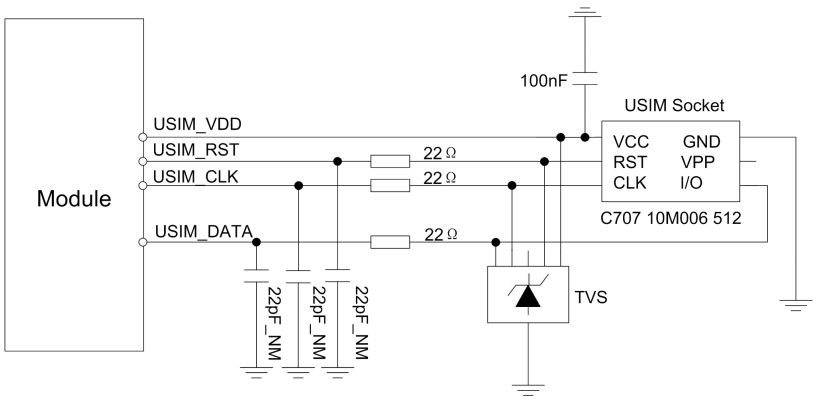

Figure 25: USIM Interface Reference Circuit

NOTE

1. USIM_DATA has been pulled up with a 10 KΩ resistor to USIM_VDD in module. A 100 nF capacitor on USIM_VDD is used to reduce interference.
2. For more details of AT commands about USIM, please refer to document [1]. USIM_CLK is very important signal, the rise time and fall time of USIM_CLK should be less than 40ns, otherwise the USIM card might not be initialized correctly.

The USIM_DET pin is used for detection of the USIM card hot plug in. User can select the 8-pin USIM card holder to implement USIM card detection function.

The following figure shows the 8-pin SIM card holder reference circuit.

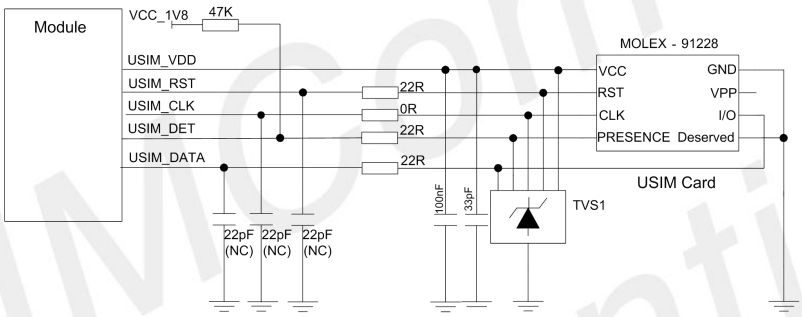

Figure 26: USIM Interface Reference Circuit with USIM_DET

If the USIM card detection function is not used, user can keep the USIM_DET pin open.

3.6.2 USIM Design Notice

USIM card circuit is susceptible; the interference may cause the SIM card failures or some other situations, so it is strongly recommended to follow these guidelines while designing:

- Make sure that the SIM card holder should be far away from the antenna while in PCB layout.
- SIM traces should keep away from RF lines, VBAT and high-speed signal lines.
- The traces should be as short as possible.
- Keep SIM holder's GND connect to main ground directly.
- Shielding the SIM card signal by ground.
- Recommended to place a 0.1～1 uF capacitor on USIM_VDD line and keep close to the holder.
- The rise/fall time of USIM_CLK should not be more than 40ns.
- Add some TVS and the parasitic capacitance should not exceed 60pF.

3.6.3 Recommended USIM Card Holder

It is recommended to use the 6-pin USIM socket such as C707 10M006 512 produced by Amphenol. User can visit http://www.amphenol.com for more information about the holder.

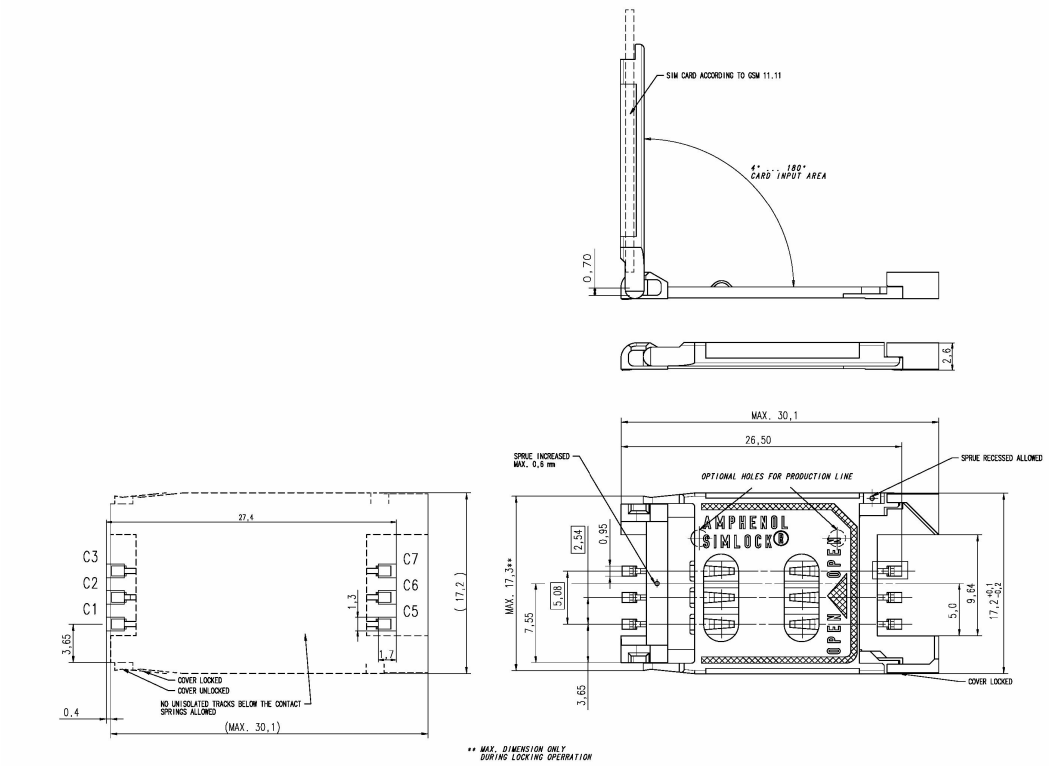

Figure 27: Amphenol SIM Card Socket

Table 20: Amphenol USIM Socket Pin Description

Pin	Signal	Description
C1	USIM_VDD	USIM Card Power supply.
C2	USIM_RST	USIM Card Reset.
C3	USIM_CLK	USIM Card Clock.
C5	GND	Connect to GND.
C6	VPP	
C7	USIM_DATA	USIM Card data I/O.

3.7 PCM Interface

Module provides a PCM interface for external codec, which can be used in master mode with short sync and 16 bits linear format.

Table 21: PCM Format

Characteristics	Specification
Line Interface Format	Linear(Fixed)
Data length	16bits(Fixed)
PCM Clock/Sync Source	Master Mode(Fixed)

PCM Clock Rate	2048kHz（2G/3G），4096Khz (4G)
PCM Sync Format	Short sync(Fixed)
Data Ordering	MSB

NOTE

For more details about PCM AT commands, please refer to document [1].

3.7.1 PCM Timing

Module supports 2.048 MHz PCM data and sync timing for 16 bits linear format codec.

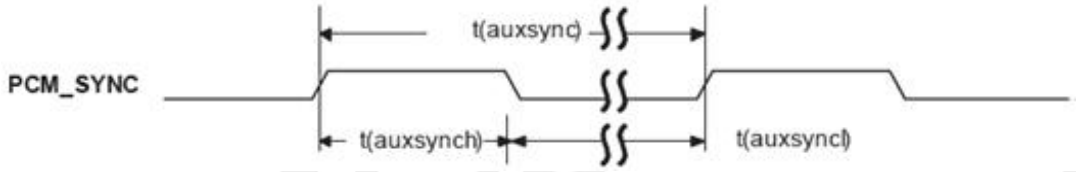

Figure 28: PCM_SYNC Timing

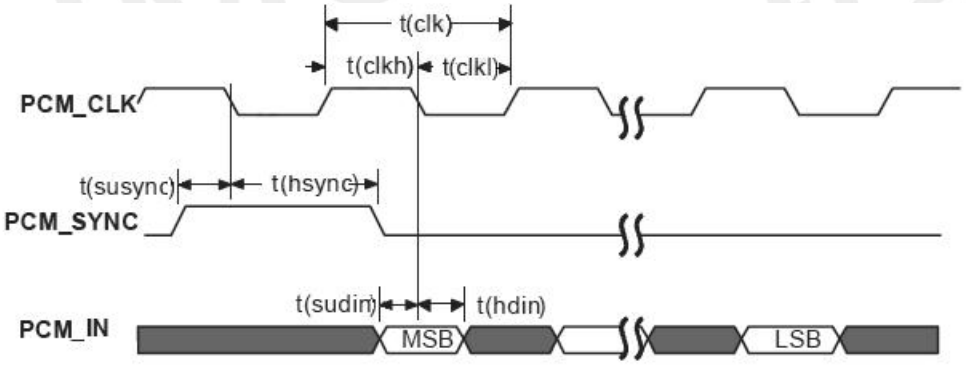

Figure 29: EXT Codec to Module Timing

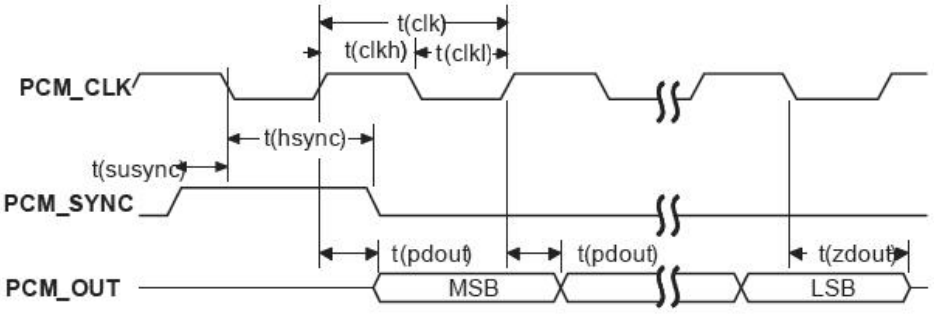

Figure 30: Module to Codec Timing

Table 22: PCM Timing Parameters (2G/3G mode)

Symbol	Parameter	Min.	Typ.	Max.	Unit
T(sync)	PCM_SYNC cycle time	–	125	–	μs
T(synch)	PCM_SYNC high level time	–	488	–	ns
T(syncl)	PCM_SYNC low level time	–	124.5	–	μs
T(clk)	PCM_CLK cycle time	–	488	–	ns
T(clkh)	PCM_CLK high level time	–	244	–	ns
T(clkl)	PCM_CLK low level time	–	244	–	ns
T(susync)	PCM_SYNC setup time high before falling edge of PCM_CLK	–	244	–	ns
T(hsync)	PCM_SYNC hold time after falling edge of PCM_CLK	–	244	–	ns
T(sudin)	PCM_IN setup time before falling edge of PCM_CLK	60	–	–	ns
T(hdin)	PCM_IN hold time after falling edge of PCM_CLK	10	–	–	ns
T(pdout)	Delay from PCM_CLK rising to PCM_OUT valid	–	–	60	ns
T(zdout)	Delay from PCM_CLK falling to PCM_OUT HIGH-Z	–	160	-	ns

Table 23: PCM Timing Parameters (4G mode)

Symbol	Parameter	Min.	Typ.	Max.	Unit
T(sync)	PCM_SYNC cycle time	–	62.5	–	μs
T(synch)	PCM_SYNC high level time	–	244	–	ns
T(syncl)	PCM_SYNC low level time	–	62.256	–	μs
T(clk)	PCM_CLK cycle time	–	244	–	ns
T(clkh)	PCM_CLK high level time	–	122	–	ns
T(clkl)	PCM_CLK low level time	–	122	–	ns
T(susync)	PCM_SYNC setup time high before falling edge of PCM_CLK	–	122	–	ns
T(hsync)	PCM_SYNC hold time after falling edge of PCM_CLK	–	122	–	ns
T(sudin)	PCM_IN setup time before falling edge of PCM_CLK	122	–	–	ns
T(hdin)	PCM_IN hold time after falling edge of PCM_CLK	122	–	–	ns
T(pdout)	Delay from PCM_CLK rising to PCM_OUT valid	–	–	122	ns
T(zdout)	Delay from PCM_CLK falling to PCM_OUT HIGH-Z	–	–	122	ns

3.7.2 PCM Application Guide

The following figure shows the external codec reference design.

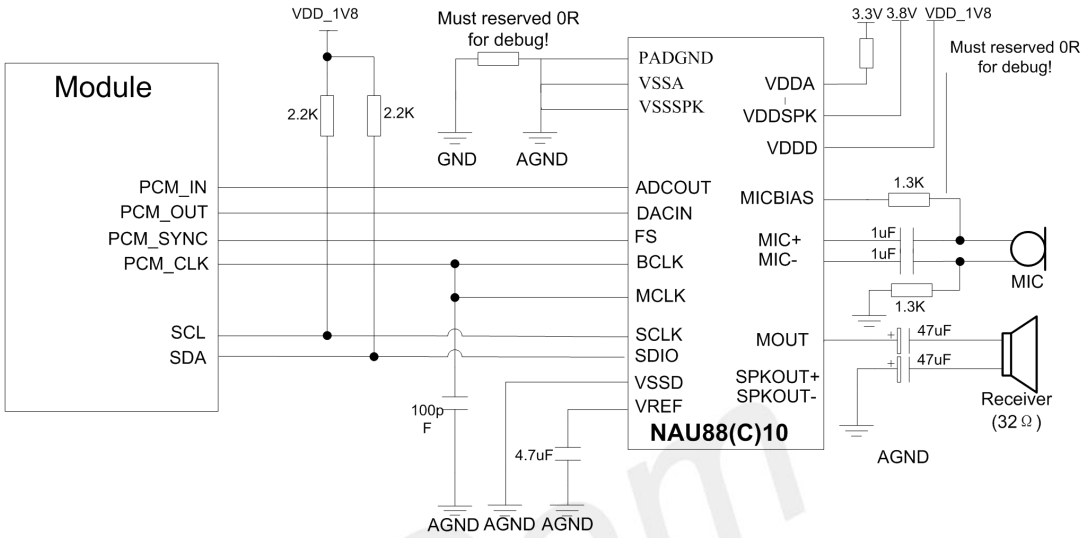

Figure 31: Audio Codec Reference Circuit

NOTE

This function is still in developing.

3.8 GPIO Interfaces

Table 24: GPIO Resources

PIN No	PIN Name	Int	Power Domain	Default Status
27	GPIO5	√	P3	PU
28	GPIO6	√	P3	PU
29	GPIO7	√	P3	PU
30	GPIO8	√	P3	PU
31	GPIO9	√	P3	PU
32	GPIO10	√	P3	PU
33	GPIO11	√	P3	PD
34	GPIO12	√	P3	PD
45	GPIO13	√	P3	PU
73	GPIO24	√	P3	PD
74	GPIO25	√	P3	PD
75	GPIO26	√	P3	PD
76	GPIO27	√	P3	PD

3.9 SD Interface

Module provides a 4-bit SD/MMC interface with clock rate up to 200 MHz, The voltage of MMC/SD interface is 3.0 V, which is compatible with SDIO Card Specification (version 3.0) and Secure Digital (Physical Layer Specification, version 3.0). It supports up to 32GB SD cards.

Table 25: 3.0V IO MMC/SD Electronic Characteristic (SD_DATA0-SD_DATA3，SD_CLK and SD_CMD) *

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage	2	-	3.6	V
V_{IL}	Low-level input voltage	-0.3	0	0.8	V
V_{OH}	High-level output voltage	2.4	-	-	V
V_{OL}	Low-level output voltage	0	-	0.4	V

Table 26: 1.8V IO MMC/SD Electronic Characteristic (SD_DATA0-SD_DATA3，SD_CLK and SD_CMD) *

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage	1.26	1.8	2.0	V
V_{IL}	Low-level input voltage	-0.3	0	0.8	V
V_{OH}	High-level output voltage	2.4	-	-	V
V_{OL}	Low-level output voltage	0	-	0.4	V

NOTE

SD_DET is 1.8 V operation voltage ,which is different from SD_DATA0-SD_DATA3，SD_CLK and SD_CMD.

Users should provide 2.85 V to power SD card system and the current should more than 500 mA, which is showed below as VDD_SD. ESD/EMI components should be arranged beside SD card socket. Refer to the following application circuit.

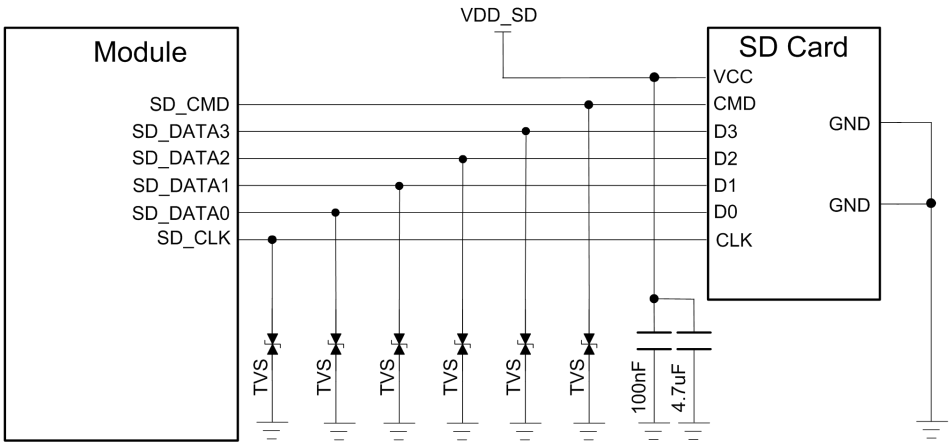

Figure 32: SD Reference Circuit

SD card layout guide lines:

- Protect other sensitive signals/circuits from SD card signals
- Protect SD card signals from noisy signals (clocks, SMPS, etc.)
- Up to 200 MHz clock rate, 50 Ω nominal, ±10% trace impedance
- CLK to DATA/CMD length matching < 1 mm
- 15–24 Ω termination resistor on clock lines near module
- Total routing length < 50 mm recommended
- Routing distance from module clock pin to termination resistor < 5 mm
- Spacing to all other signals = 2x line width
- Bus capacitance < 15 pF

3.10 I2C Interface

Module provides a I2C interface compatible with I2C specification, version 5.0, with clock rate up to 400 kbps. Its operation voltage is 1.8 V.

The following figure shows the I2C bus reference design.

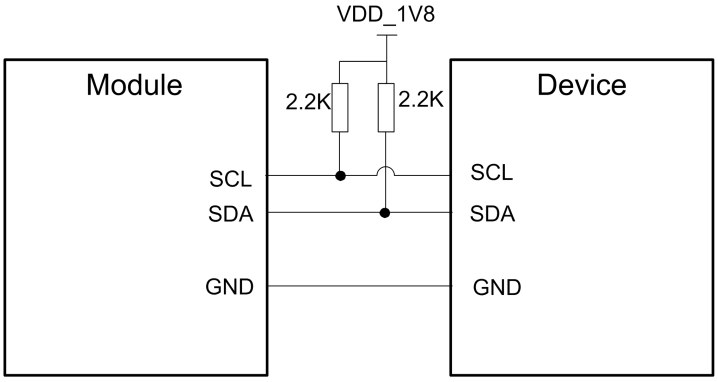

Figure 33: I2C Reference Circuit

NOTE

SDA and SCL do not have pull-up resistors in module. So, 2 externals pull up resistors are needed in application circuit.

3.11 SDIO Interface

Module provides a 4 bit 1.8 V SDIO interface for WLAN solution.

Table 27: WIFI Interface

PIN No	PIN Name	I/O	Power Domain	Function Description	Index
27	SDIO_DATA1	IO	P3	SDIO data bus bit1	
28	SDIO_DATA2	IO	P3	SDIO data bus bit2	
29	SDIO_CMD	IO	P3	SDIO bus command	
30	SDIO_DATA0	IO	P3	SDIO data bus bit0	
31	SDIO_DATA3	IO	P3	SDIO data bus bit3	
32	SDIO_CLK	DO	P3	SDIO bus clock	
49	WL_PDN	DO	P3	WIFI enable signal	
33	WL_PWR_EN	DO	P3	WIFI power enable	

3.12 SPI Interface

Module provides a SPI interface as a master only. Its operation voltage is 1.8 V, and its clock rate is up to 50 MHz.

3.13 Network Status

The NETLIGHT pin is used to control Network Status LED, its reference circuit is shown in the following figure.

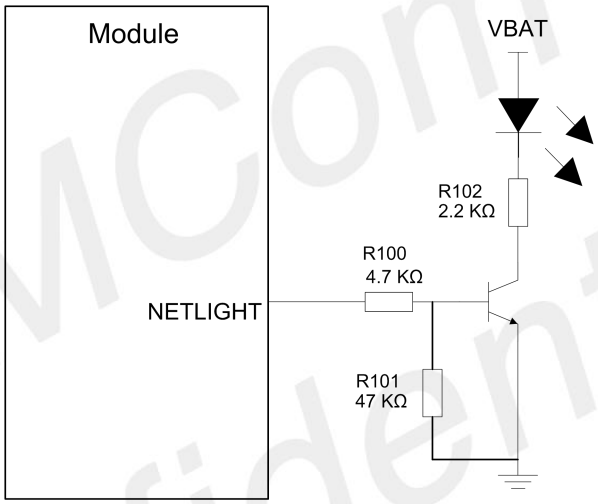

Figure 34: NETLIGHT Reference Circuit

NOTE

The value of the resistor named “R” depends on the LED characteristic.

Table 28: NETLIGHT Status

NETLIGHT pin status	Module status
Always On	Searching Network; Call Connect (include VOLTE,SRLTE)
200 ms ON, 200 ms OFF	Data Transmit; 4G registered;
800 ms ON, 800 ms OFF	2G/3G registered network
OFF	Power off; Sleep

NOTE

NETLIGHT output low level as “OFF”, and high level as “ON”.

3.14 Flight Mode Control

The FLIGHTMODE pin can be used to control module to enter or exit the Flight mode. In Flight mode, the RF circuit is closed to prevent interference with other equipment and minimize current consumption. Bidirectional ESD protection component is suggested to add on FLIGHTMODE pin, its reference circuit is shown in the following figure.

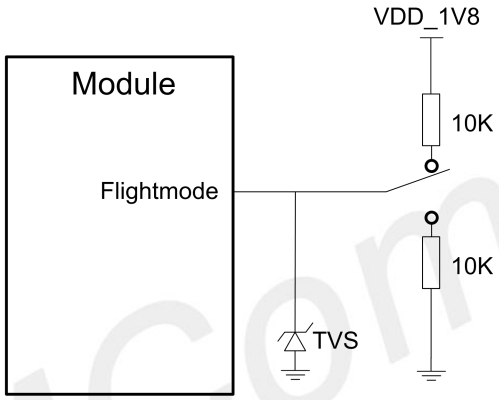

Figure 35: Flight Mode Switch Reference Circuit

Table 29: FLIGHTMODE Status

FLIGHTMODE pin status	Module operation
Input Low Level	Flight Mode: RF is closed
Input High Level	AT+CFUN=4: RF is closed AT+CFUN=1: RF is working

3.15 RMII Interface

Module support RMII nterface for 100Mbps LAN application.
The PHY' s IO voltage can be configured through PIN 159 VDDMAC_VIO, it can be configured to 1.8 V or 3.3 V.

Customer could refer to reference design for detail.

3.16 PCIe Interface*

Module provides 1 lane PCIe Gen1 interface, Only support host mode (RC mode)，the maximum data rate could up to 2.5 Gbps.

Feature：
- PCI Express® Base Specification Revision 3.1 compliant
- 32-bit PIPE interface, PIPE3.0 compliant
- Support 100 MHz differential reference clock, either with SSC or not
- SRIS (separate reference independent SSC) support

- Advanced Error Reporting (AER) support
- ECRC generation and check support
- Legacy PCI Power Management support
- Native Active State Power Management L0s and L1 state support
- Both WAKE# and beacon detection are supported
- MSI (up to 32) and INT message support
- Four reconfigurable DMA channels: 2 write and 2 read channels
- Up to 8 reconfigurable address translation tables for PCIe interface

3.17 GNSS Control Interface

The GNSS function is optional.
The GNSS is a stand-along function, the module integrated GNSS chip, and module provide VGNSS pin, customer provide a 1.8 V voltage for VGNSS and the GNSS function is started, the GNSS_TXD and GNSS_RXD will provide NMEA sentences, customer could connect GNSS_UART to UART2 to module, so the GNSS NMEA information could be handled by module, the GNSS_UART also could connect to host side for other usage.

If customer need the GNSS in low power mode, customer could cut off the VGNSS power.

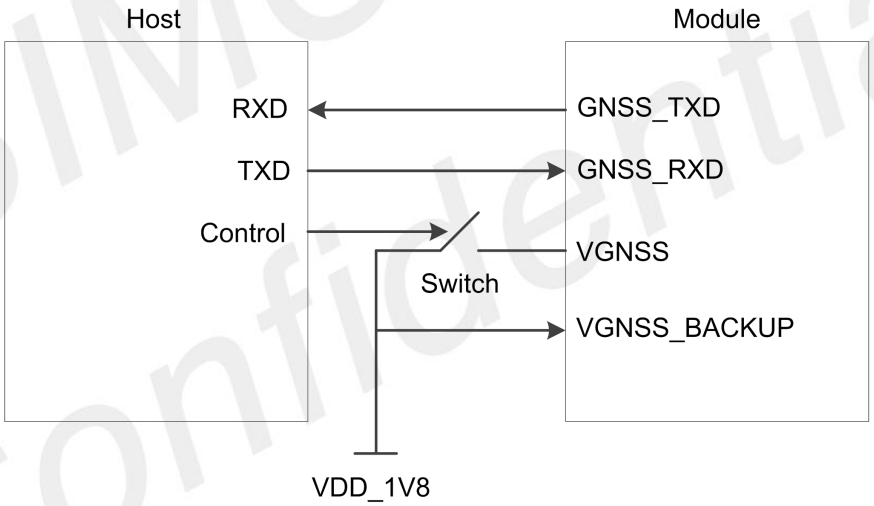

Figure 36: GNSS Circuit Diagram (NMEA to host UART)

3.18 Other Interface

3.18.1 ADC

The module has a dedicated ADC named ADC1.It is available for digitizing analog signals such as battery voltage and so on. These electronic specifications are shown in the following table.

Table 30: ADC1 Electronic Characteristics

Characteristics	Min.	Typ.	Max.	Unit
Resolution	–	15	–	Bits
Conversion time	–	442	–	us
Input Range	0.1		1.8	V
Input serial resistance	1	–	–	MΩ

NOTE

"AT+CADC=2" can be used to read the voltage, for more details, please refer to document [1].

3.18.2 LDO

Module has a LDO power output, named VDD_AUX. its output voltage is 2.8 V by default, Users can switch the LDO on or off by the AT command "AT+CVAUXS".

Table 31: LDO Electronic Characteristic

Symbol	Description	Min.	Typ.	Max.	Unit
V_{VDD_AUX}	Output voltage	-	2.80	-	V
I_O	Output current	-	-	150	mA

NOTE

For more details of AT commands about VDD_AUX, please refer to document [1].

4 RF Specifications

4.1 GSM/UMTS/LTE RF Specifications

Table 32: GSM/UMTS/LTE Conducted Transmission Power

Frequency	Power	Min
GSM850	33dBm ±2 dB	5dBm ± 5 dB
EGSM900	33dBm ±2 dB	5dBm ± 5 dB
DCS1800	30dBm ±2 dB	0dBm ± 5 dB
PCS1900	30dBm ±2 dB	0dBm ± 5 dB
GSM850 (8-PSK)	27dBm ±3 dB	5dBm ± 5 dB
EGSM900 (8-PSK)	27dBm ±3 dB	5dBm ± 5 dB
DCS1800 (8-PSK)	26dBm +3/-4 dB	0dBm ±5 dB
PCS1900 (8-PSK)	26dBm +3/-4 dB	0dBm ±5 dB
WCDMA B1	24dBm +1/-3 dB	<-50 dBm
WCDMA B2	24dBm +1/-3 dB	<-50 dBm
WCDMA B5	24dBm +1/-3 dB	<-50 dBm
WCDMA B8	24dBm + 1/-3 dB	<-50 dBm
LTE-FDD B1	23dBm +/-2.7 dB	<-40 dBm
LTE-FDD B3	23dBm +/-2.7 dB	<-40 dBm
LTE-FDD B4	23dBm +/-2.7 dB	<-40 dBm
LTE-FDD B5	23dBm +/-2.7 dB	<-40 dBm
LTE-FDD B7	23dBm +/-2.7 dB	<-40 dBm
LTE-FDD B8	23dBm +/-2.7 dB	<-40 dBm
LTE-FDD B12	23dBm +/-2.7 dB	<-40 dBm
LTE-FDD B13	23dBm +/-2.7 dB	<-40 dBm
LTE-FDD B18	23dBm +/-2.7 dB	<-40 dBm
LTE-FDD B19	23dBm +/-2.7 dB	<-40 dBm
LTE-FDD B20	23dBm +/-2.7 dB	<-40 dBm
LTE-FDD B26	23dBm +/-2.7 dB	<-40 dBm
LTE-FDD B28	23dBm +/-2.7 dB	<-40 dBm
LTE-TDD B38	23dBm +/-2.7 dB	<-40 dBm
LTE-TDD B40	23dBm +/-2.7 dB	<-40 dBm
LTE-TDD B41	23dBm +/-2.7 dB	<-40 dBm

Table 33: Operating Frequencies

Frequency	Receiving	Transmission
GSM850	869 ~ 894 MHz	824 ~ 849 MHz
EGSM900	925 ~ 960 MHz	880 ~ 915 MHz
DCS1800	1805 ~ 1880 MHz	1710 ~ 1785 MHz
PCS1900	1930~1990 MHz	1850~1910 MHz
WCDMA B1	2110 ~ 2170 MHz	1920 ~ 1980 MHz
WCDMA B2	1930~1990 MHz	1850~1910 MHz
WCDMA B5	869 ~ 894 MHz	824 ~ 849 MHz
WCDMA B8	925 ~ 960 MHz	880 ~ 915 MHz
The LTE Operating frequencies are shown in the following table 24. Note: Operating frequencies of LTE TDD B41 for the module is 100MHz BW, 2555 ~ 2655 MHz		
GPS	1574.4 ~ 1576.44 MHz	-
GLONASS	1598 ~ 1606 MHz	-
BD	1559 ~ 1563 MHz	

Table 34: E-UTRA Operating Bands

E-UTRA Band	Uplink (UL)	Downlink (DL)
LTE-FDD B1	1920 ~1980 MHz	2110 ~2170 MHz
LTE-FDD B2	1850~1910 MHz	1930~1990 MHz
LTE-FDD B3	1710 ~1785 MHz	1805 ~1880 MHz
LTE-FDD B4	1710~1755 MHz	2110~2155 MHz
LTE-FDD B5	824 ~ 849 MHz	869 ~ 894 MHz
LTE-FDD B7	2500~2570 MHz	2620~2690 MHz
LTE-FDD B8	880 ~915 MHz	925 ~960 MHz
LTE-FDD B12	699~716 MHz	728~746 MHz
LTE-FDD B13	777~787 MHz	746~757 MHz
LTE-FDD B18	815~830 MHz	860~875 MHz
LTE-FDD B19	830~845 MHz	875~890 MHz
LTE-FDD B20	832~862 MHz	791~ 821 MHz
LTE-FDD B26	814~849 MHz	859~894 MHz
LTE-FDD B28	703~748 MHz	758~803 MHz
LTE-TDD B38	2570 ~2620 MHz	2570 ~2620 MHz
LTE-TDD B40	2300 ~2400 MHz	2300 ~2400 MHz
LTE-TDD B41	2496 ~2690 MHz	2496 ~2690 MHz

Table 35: Conducted Receive Sensitivity

Frequency	Receive sensitivity (Typical)	Receive sensitivity (MAX)
GSM850	< -109 dBm	3GPP
EGSM900	< -109 dBm	3GPP
DCS1800	< -108 dBm	3GPP
PCS1900	< -108 dBm	3GPP
WCDMA B1	< -110 dBm	3GPP
WCDMA B2	< -110 dBm	3GPP
WCDMA B5	< -110 dBm	3GPP
WCDMA B8	< -110 dBm	3GPP
LTE FDD/TDD	See table 26.	3GPP

Table 36: Reference Sensitivity (QPSK)

E-UTRA band	Standard						Test Value @10 MHz
	1.4 MHz	3 MHz	5 MHz	10 MHz	15 MHz	20 MHz	
LTE-FDD B1	-	-	-100	-97	-95.2	-94	-101
LTE-FDD B2	-102.7	-99.7	-98	-95	-93.2	-92	-99
LTE-FDD B3	-101.7	-98.7	-97	-94	-92.2	-91	-99
LTE-FDD B4	-104.7	-101.7	-100	-97	-95.2	-94	-101
LTE-FDD B5	-103.2	-100.2	-98	-95			-99
LTE-FDD B7			-98	-95	-93.2	-92	-97
LTE-FDD B8	-102.2	-99.2	-97	-94			-102
LTE-FDD B12	-101.7	-98.7	-97	-94			-99
LTE-FDD B13			-97	-94			-99
LTE-FDD B18			-100	-97	-95.2		-101
LTE-FDD B19			-100	-97	-95.2		-101
LTE-FDD B20			-97	-94	-91.2	-90	-98
LTE-FDD B26	-102.7	-99.7	-97.5	-94.5	-92.7		-99
LTE-FDD B28		-100.2	-98.5	-95.5	-93.7	-91	-99
LTE-TDD B38	-	-	-100	-97	-95.2	-94	-101
LTE-TDD B40	-	-	-100	-97	-95.2	-94	-101
LTE-TDD B41	-	-	-99	-96	-94.2	-93	-101

4.2 GSM /UMTS/LTE Antenna Design Guide

Users should connect antennas to module's antenna pads through micro-strip line or other types of RF trace and the trace impedance must be controlled in 50 Ω. SIMCom recommends that the total insertion loss between the antenna pads and antennas should meet the following requirements:

Table 37: Trace Loss

Frequency	Loss
700 MHz-960 MHz	<0.5 dB
1710 MHz-2170 MHz	<0.9 dB
2300 MHz-2650 MHz	<1.2 dB

To facilitate the antenna tuning and certification test, a RF connector and an antenna matching circuit should be added. The following figure is the recommended circuit.

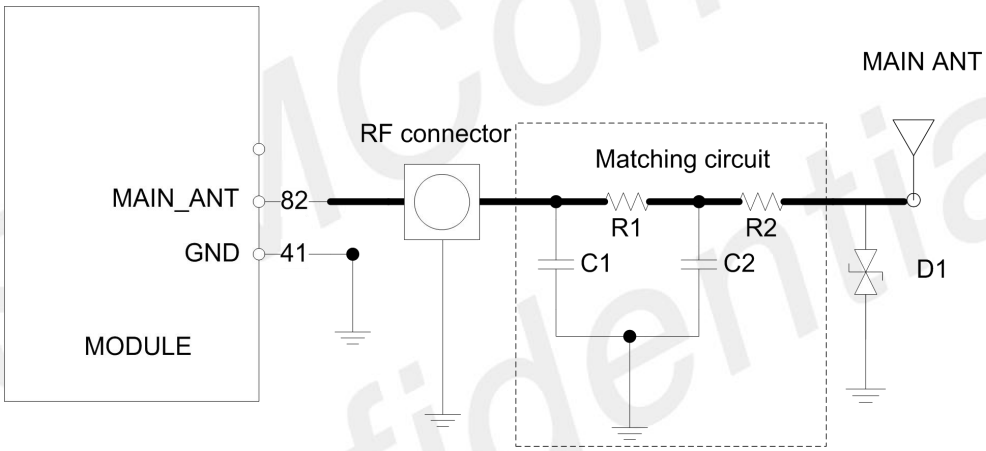

Figure 37: Antenna Matching Circuit (MAIN_ANT)

In above figure, the components R1, C1, C2 and R2 are used for antenna matching, the values of components can only be achieved after the antenna tuning and usually provided by antenna vendor. By default, the R1, R2 are 0 Ω resistors, and the C1, C2 are reserved for tuning. The component D1 is a TVS for ESD protection, and it is optional for users according to application environment.

The RF test connector is used for the conducted RF performance test, and should be placed as close as to the module's MAIN_ANT pin. The traces impedance between module and antenna must be controlled in 50 Ω.

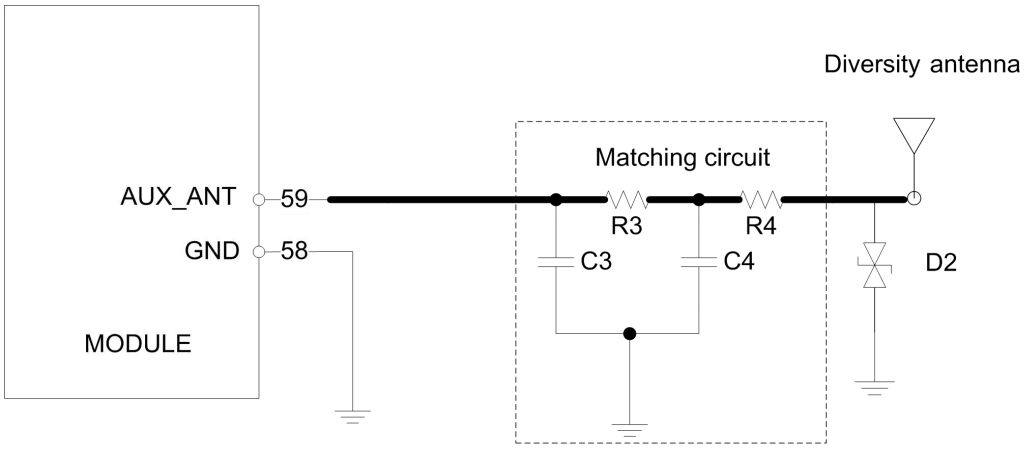

Figure 38: Antenna Matching Circuit (AUX_ANT)

In above figure, R3, C3, C4 and R4 are used for auxiliary antenna matching. By default, the R3, R4 are 0Ωresistors, and the C3, C4 are reserved for tuning. D2 is a TVS for ESD protection, and it is optional for users according to application environment.

Two TVS are recommended in the table below.

Table 38: Recommended TVS

Package	Part Number	Vender
0201	WE05DGCMS-BH	CYGWAYON
0402	PESD0402-03	PRISEMI
0402	PESD0402-12	PRISEMI

NOTE

SIMCom suggests the LTE auxiliary antenna to be kept on, since there are many high bands in the designing of LTE-TDD, such as band38, band40 and band41. Because of the high insert loss of the RF cable and layout lines, the receiver sensitivity of these bands above will have risk to meet the authentication without the diversity antenna. For more details about auxiliary antenna design notice, please refer to document [25].

4.3 GNSS

Module merges GNSS (GPS/GLONASS/BD/QZSS GALILEO) satellite and network information to provide a high-availability solution that offers industry-leading accuracy and performance. This solution performs well, even in very challenging environmental conditions where conventional GNSS receivers fail, and provides a platform to enable wireless operators to address both location-based services and emergency mandates.

4.3.1 GNSS Technical Specification

- Tracking sensitivity: -159 dBm (GPS) /-158 dBm (GLONASS) /-159 dBm (BD) /-159 dBm (GALILEO)
- Cold-start sensitivity: -148 dBm
- Accuracy (Open Sky): 2.5 m (CEP50)
- TTFF (Open Sky): Hot start <1 s, Cold start<35 s
- Receiver Type: 16-channel, C/A Code
- GPS L1 Frequency: 1575.42±1.023 MHz
- GLONASS: 1597.5~1605.8 MHz
- BD: 1559.05~1563.14 MHz
- GALILEO: 1575.42±1.023 MHz
- Update rate: Default 1 Hz
- GNSS data format: NMEA-0183
- GNSS Current consumption: 100mA (GSM/UMTS/LTE Sleep ,in total on VBAT pins)
- GNSS antenna: Passive/Active antenna

Table 39: Recommended Passive Antenna Characteristics

Passive	Recommended standard
Direction	Omnidirectional
Gain	>-3 dBi (Avg)
Input impedance	50 Ω
Efficiency	>50%
VSWR	<2

NOTE

If the antenna is active type, the power should be given by main board because there is no power supply on the GPS antenna pad. If the antenna is passive, it is suggested that the external LNA should be used.

4.3.2 GNSS Application Guide

Users can adopt an active antenna or a passive antenna to module. If using a passive antenna, an external LNA is a must to get better performance.
The following figures are the reference circuits.

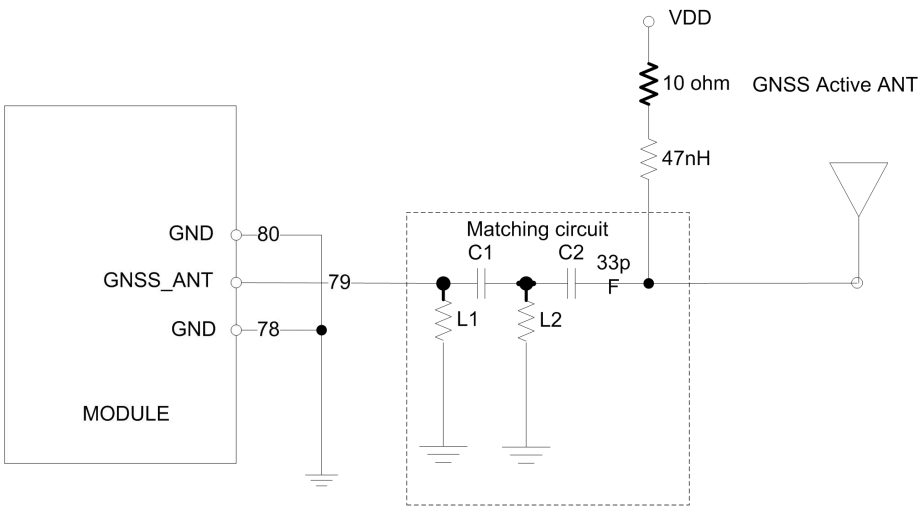

Figure 39: Active Antenna Circuit

NOTE

If customer need save the power when the GNSS function is disabled, then customer should design a switch circuit to cut off the active antenna power to get a lower power consumption.

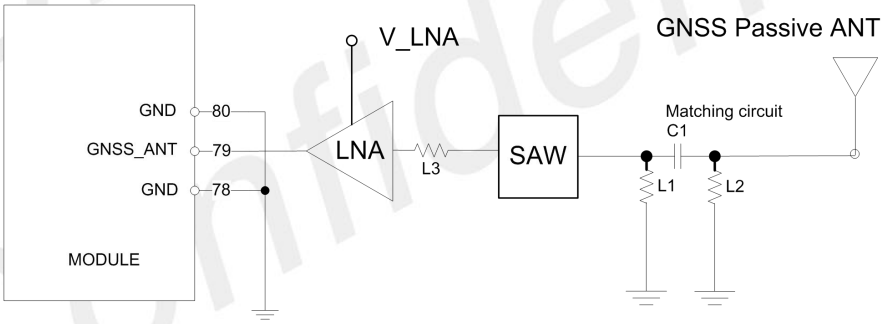

Figure 40: Passive Antenna Circuit (Default)

In above figures, the components C1, L1 and L2 are used for antenna matching. Usually, the values of the components can only be achieved after antenna tuning and usually provided by antenna vendor. C2 is used for DC blocking. L3 is the matching component of the external LNA, and the value of L3 is determined by the LNA characteristic and PCB layout. Both VDD of active antenna and V_LNA need external power supplies which should be considered according to active antenna and LNA characteristic. LDO/DCDC is recommended to get lower current consuming by shutting down active antennas and LNA when GNSS is not working.

Table 40: Recommended LNA and SAW Filter

Material	Part Number	Vendor
GPS LNA	MXDLN16TP	MAXSCEND
GPS LNA	BGA725L6	Infineon
GPS LNA	BGA824N6	Infineon
GPS SAW FILTER	HDF1588E-B5	SHOULDER
GPS SAW FILTER	SAFFB1G56KB0F0A	murata

GNSS can be tested by NMEA port. NMEA sentences can be obtained through UART or USB automatically. NMEA sentences include GSV, GGA, RMC, GSA, and VTG. Before using GNSS, user should configure module in proper operating mode by AT command. Please refer to related documents for details. module can also get position location information through AT directly.

NOTE

GNSS is closed by default and can be started by AT+CGPS. The AT command has two parameters, the first is on/off, and the second is GNSS mode. Default mode is standalone mode.
AGPS mode needs more support from the mobile telecommunication network. Please refer to document [24] for more details.

5 Electrical Specifications

5.1 Absolute Maximum Ratings

Absolute maximum ratings for digital and analog pins of module are listed in the following table.

Table 41: Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Unit
Voltage at VBAT	-0.3	-	6	V
Voltage at USB_VBUS	-0.5	-	5.5	V
Voltage at digital pins (RESET, SPI, Keypad, GPIO, I2C, UART, PCM)	-0.3	-	2.1	V
Voltage at digital pins (SD, USIM)	-0.3	-	3.3	V
Voltage at PWRKEY	-0.3	-	6	V

5.2 Operating Conditions

Table 42: Recommended Operating Ratings

Parameter	Min.	Typ.	Max.	Unit
Voltage at VBAT	3.4	3.8	4.2	V
Voltage at USB_VBUS	3.6	5.0	5.25	V

Table 43: 1.8V Digital I/O Characteristics*

Parameter	Description	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage	1.26	1.8	2	V
V_{IL}	Low-level input voltage	-0.3	0	0.54	V
V_{OH}	High-level output voltage	1.6	-	-	V
V_{OL}	Low-level output voltage	0	-	0.2	V
I_{OH}	High-level output current (no pull-down resistor)	-	2	-	mA
I_{OL}	Low-level output current (no pull up resistor)	-	-2	-	mA
I_{IH}	Input high leakage current (no pull-down resistor)	-	-	1	uA
I_{IL}	Input low leakage current (no pull up resistor)	-1	-	-	uA

NOTE

These parameters are for digital interface pins, such as SPI, GPIO (NETLIGHT, FLIGHTMODE, STATUS, USIM_DET, SD_DET), I2C, UART, PCM, and USB_BOOT.

The operating temperature of module is listed in the following table.

Table 44: Operating Temperature

Parameter	Min.	Typ.	Max.	Unit
Normal operation temperature	-30	25	80	℃
Extended operation temperature*	-40	25	85	℃
Storage temperature	-45	25	+90	℃

NOTE

Module is able to make and receive voice calls, data calls, SMS and make GSM/ UMTX/LTE traffic in -40 ℃ ~ +85 ℃. The performance will be reduced slightly from the 3GPP specifications if the temperature is outside the normal operating temperature range and still within the extreme operating temperature range.

5.3 Operating Mode

5.3.1 Operating Mode Definition

The table below summarizes the various operating modes of module product.

Table 45: Operating Mode Definition

Mode		Function
Normal operation	GSM /UMTS/LTE Sleep	In this case, the current consumption of module will be reduced to the minimal level and the module can still receive paging message, call, SMS and TCP/UDP.
	GSM/UMTS/LTE Idle	Software is active. Module is registered to the network, and the module is ready to communicate.
	GSM/UMTS/LTE Talk	Connection between two subscribers is in progress. In this case, the power consumption depends on network settings such as DTX off/on, FR/EFR/HR, hopping sequences, and antenna.
	GPRS/EDGE/ UMTS/LTE Standby	Module is ready for data transmission, but no data is currently sent or received. In this case, power consumption depends on network settings.
	GPRS/EDGE/ UMTS/LTE Data transmission	There is data transmission in progress. In this case, power consumption is related to network settings (e.g. power control level);

	uplink/downlink data rates, etc.
Minimum functionality mode	AT command “AT+CFUN=0” AT+CSCLK=1 can be used to set the module to a minimum functionality mode without removing the power supply. In this mode, the RF part of the module will not work and the USIM card will not be accessible, but the serial port and USB port are still accessible. The power consumption in this mode is lower than normal mode.
Flight mode	AT command “AT+CFUN=4” or pulling down the FLIGHTMODE pin can be used to set the module to flight mode without removing the power supply. In this mode, the RF part of the module will not work, but the serial port and USB port are still accessible. The power consumption in this mode is lower than normal mode.
Power off	Module will go into power off mode by sending the AT command “AT+CPOF” or pull down the PWRKEY pin, normally. In this mode the power management unit shuts down the power supply, and software is not active. The serial port and USB are is not accessible.

5.3.2 Sleep Mode

In sleep mode, the current consumption of module will be reduced to the minimal level, and module can still receive paging message and SMS and TCP/UDP.
Several hardware and software conditions must be satisfied together in order to let module enter into sleep mode:

- UART condition
- USB condition
- Software condition

NOTE

Before designing, pay attention to how to realize sleeping/waking function and refer to Document [26] for more details.

5.3.3 Minimum Functionality Mode and Flight Mode

Minimum functionality mode ceases a majority function of module, thus minimizing the power consumption. This mode is set by the AT command which provides a choice of the functionality levels.

- AT+CFUN=0: Minimum functionality
- AT+CFUN=1: Full functionality (Default)
- AT+CFUN=4: Flight mode

If module has been set to minimum functionality mode, the RF function and USIM card function will be closed. In this case, the serial port and USB are still accessible, but RF function and USIM card will be unavailable.
If module has been set to flight mode, the RF function will be closed. In this case, the serial port and USB

are still accessible, but RF function will be unavailable.
When module is in minimum functionality or flight mode, it can return to full functionality by the AT command “AT+CFUN=1”.

5.4 Current Consumption

The current consumption is listed in the table below.

Table 46: Current Consumption on VBAT Pins (VBAT=3.8V)

GNSS	
GNSS supply current (AT+CFUN=0,without USB connection)	@ -140 dBm，Tracking Typical:35 mA
GSM sleep/idle mode	
GSM/GPRS supply current (GNSS off，without USB connection)	Sleep mode@ BS_PA_MFRMS=2 Typical: 2.8 mA Idle mode@ BS_PA_MFRMS=2 Typical: 18 mA
UMTS sleep/idle mode	
WCDMA supply current (GNSS off，without USB connection)	Sleep mode @DRX=9 Typical: 3.3 mA Idle mode @DRX=9 Typical: 17.5 mA
LTE sleep/idle mode	
LTE supply current (GNSS off，without USB connection)	Sleep mode Typical: 2.3 mA Idle mode Typical: 17.5 mA
EVDO supply current (GNSS off，without USB connection)	Sleep mode Typical: 2.0 mA Idle mode Typical: 17.8 mA
GSM Talk	
GSM850	@power level #5 Typical: 220 mA
EGSM900	@ power level #5 Typical: 230 mA
DCS1800	@power level #5 Typical: 16 2mA
PCS1900	@power level #5 Typical: 190 mA
UMTS Talk	
WCDMA B1	@Power 24 dBm Typical: 540 mA
WCDMA B2	@Power 24 dBm Typical: 470 mA
WCDMA B5	@Power 24 dBm Typical: 530 mA
WCDMA B8	@Power 24 dBm Typical: 385 mA
GPRS	
GSM850(1 Rx,4 Tx)	@power level #5 Typical: 480 mA
EGSM900(1 Rx,4 Tx)	@power level #5 Typical: 230 mA
DCS1800(1 Rx,4 Tx)	@power level #0 Typical: 195 mA
PCS1900(1 Rx,4 Tx)	@power level #0 Typical: 390 mA
GSM850(3Rx, 2 Tx)	@power level #5 Typical: 330 mA
EGSM900(3Rx, 2 Tx)	@power level #5 Typical: 370 mA
DCS1800(3Rx, 2 Tx)	@power level #0 Typical: 275 mA
PCS1900(3Rx, 2 Tx)	@power level #0 Typical: 245 mA

EDGE	
GSM850(1 Rx,4 Tx)	@power level #8 Typical: 340 mA
EGSM900(1 Rx,4 Tx)	@power level #8 Typical: 400 mA
DCS1800(1 Rx,4 Tx)	@power level #2 Typical: 300 mA
PCS1900(1 Rx,4 Tx)	@power level #2 Typical: 330 mA
GSM850(3Rx, 2 Tx)	@power level #8 Typical: 280 mA
EGSM900(3Rx, 2 Tx)	@power level #8 Typical: 320 mA
DCS1800(3Rx, 2 Tx)	@power level #2 Typical: 230 mA
PCS1900(3Rx, 2 Tx)	@power level #2 Typical: 268 mA
GSM850(1 Rx,4 Tx)	
EGSM900(1 Rx,4 Tx)	@power level #8 Typical: 400 mA
DCS1800(1 Rx,4 Tx)	@power level #2 Typical: 300 mA
HSDPA data	
WCDMA B1	@Power 24 dBm Typical: 478 mA
WCDMA B2	@Power 23 dBm Typical: 475 mA
WCDMA B5	@Power 24 dBm Typical: 480 mA
WCDMA B8	@Power 24 dBm Typical: 430 mA
LTE data	
LTE-FDD B1	@5MHz 22.3 dBm Typical: 577 mA @10MHz 22.4 dBm Typical: 590 mA @20MHz 22.4 dBm Typical: 630 mA
LTE-FDD B2	@5MHz 22.1 dBm Typical: 515 mA @10MHz 22.4 dBm Typical: 544 mA @20MHz 22.3 dBm Typical:575 mA
LTE-FDD B3	@5MHz 22.2 dBm Typical: 479 mA @10MHz 22.1 dBm Typical: 498 mA @20MHz 22.1 dBm Typical: 530 mA
LTE-FDD B4	@5MHz 22.0 dBm Typical: 527 mA @10MHz 22.1 dBm Typical: 559 mA @20MHz 22.6 dBm Typical: 555 mA
LTE-FDD B5	@5MHz 22.2 dBm Typical: 610 mA @10MHz 22.1 dBm Typical: 600 mA @20MHz 22.1 dBm Typical: 630 mA
LTE-FDD B7	@5MHz 22.2 dBm Typical: 650 mA @10MHz 22.1 dBm Typical: 650 mA @20MHz 22.1 dBm Typical: 630 mA
LTE-FDD B8	@5MHz 22.8 dBm Typical: 644 mA @10MHz 22.8 dBm Typical: 646 mA
LTE-FDD B12	@5MHz 22.7 dBm Typical: 493 mA @10MHz 22.7 dBm Typical: 510 mA
LTE-FDD B13	@5MHz 21.9 dBm Typical: 505 mA @10MHz 22.0 dBm Typical: 497 mA
LTE-FDD B18	@5MHz 21.3 dBm Typical: 531 mA @10MHz 22.5 dBm Typical: 523 mA @15MHz 22.6 dBm Typical: 570 mA
LTE-FDD B19	@5MHz 22.4 dBm Typical: 532 mA @10MHz 22.3 dBm Typical: 541 mA @15MHz 22.5 dBm Typical: 590 mA
LTE-FDD B20	@5MHz 21.8 dBm Typical: 579 mA @10MHz 21.8 dBm Typical: 590 mA @20MHz 21.8 dBm Typical: 600 mA

LTE-FDD B26	@5MHz 22.4 dBm Typical: 525 mA @10MHz 22.7 dBm Typical: 570 mA @15MHz 22.3 dBm Typical: 580 mA
LTE-FDD B28	@5MHz 22.4 dBm Typical: 612 mA @10MHz 22.5 dBm Typical: 510mA @20MHz 22.4 dBm Typical: 670 mA
LTE-TDD B38	@5MHz 21.8 dBm Typical: 370 mA @10MHz 21.8 dBm Typical: 380 mA @20MHz 21.8 dBm Typical: 403 mA
LTE-TDD B40	@5MHz 21.5 dBm Typical: 407 mA @10MHz 21.7 dBm Typical: 416 mA @20MHz 21.7 dBm Typical: 444 mA
LTE-TDD B41	@5MHz 21.6 dBm Typical: 390 mA @10MHz 21.7 dBm Typical: 396 mA @20MHz 21.7 dBm Typical: 420 mA

5.5 ESD Notes

Module is sensitive to ESD in the process of storage, transporting, and assembling. When module is mounted on the users' mother board, the ESD components should be placed beside the connectors which human body may touch, such as USIM card holder, audio jacks, switches, keys, etc. The following table shows the module ESD measurement performance without any external ESD component.

Table 47: The ESD Performance Measurement Table (Temperature: 25 ℃, Humidity: 45%)

Part	Contact discharge	Air discharge	Part
VBAT, GND	+/-4 *KV*	+/-8 KV	VBAT, GND
Antenna port	+/-4 KV	+/-8 KV	Antenna port
USB	+/-1 KV	+/-2 KV	USB
UART	+/-1 KV	+/-2 KV	UART
Other PADs	+/-1 KV	+/-2 KV	Other PADs

6 SMT Production Guide

6.1 Top and Bottom View of Module

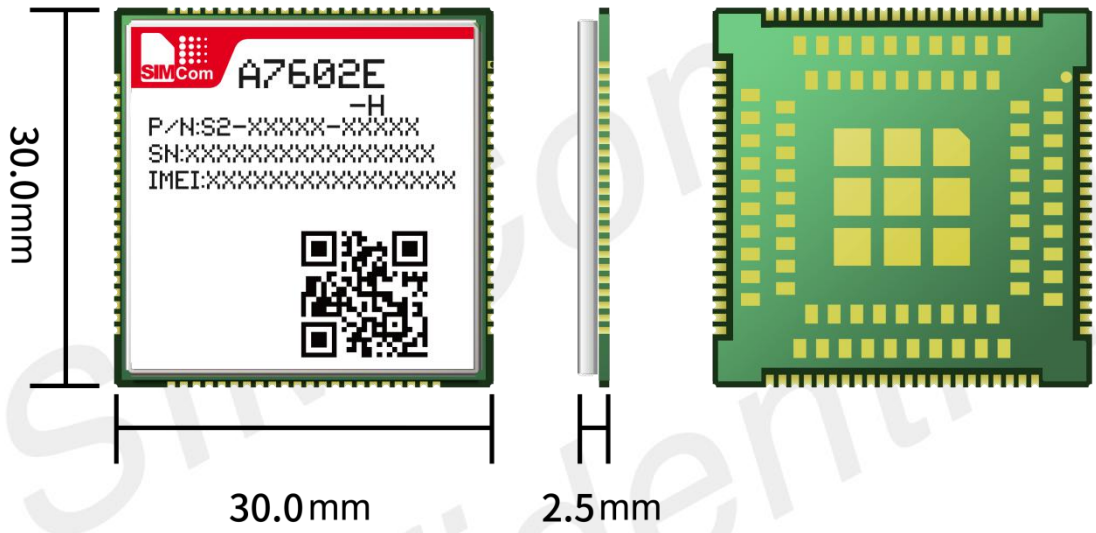

Figure 41: Top and Bottom View of Module

6.2 Label Information

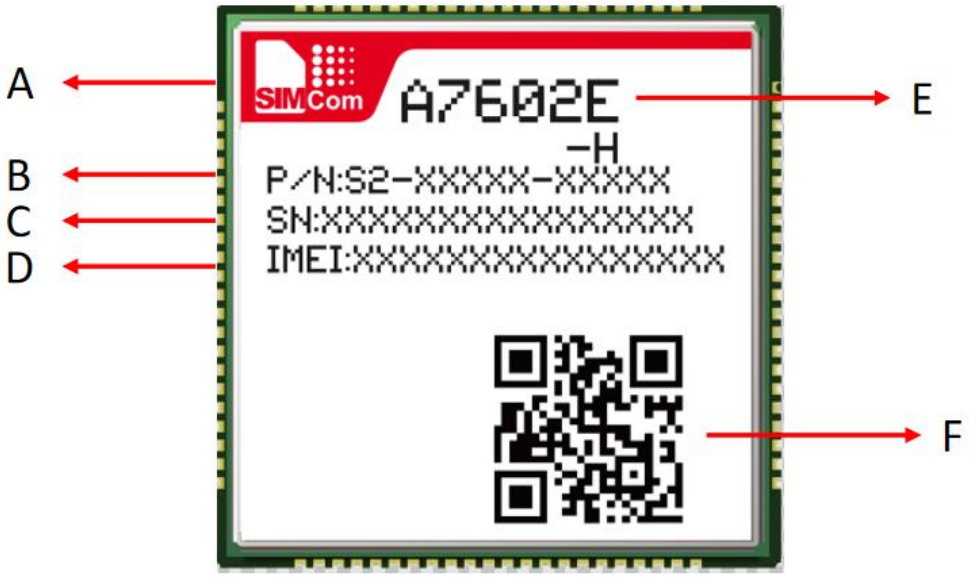

Figure 42: Label Information

Table 48: The Description of Label Information

No.	Description
A	LOGO
B	Module part number
C	Project name
D	Serial number
E	International mobile equipment identity
F	QR code

6.3 Typical SMT Reflow Profile

SIMCom provides a typical soldering profile. Therefore, the soldering profile shown below is only a generic recommendation and should be adjusted to the specific application and manufacturing constraints.

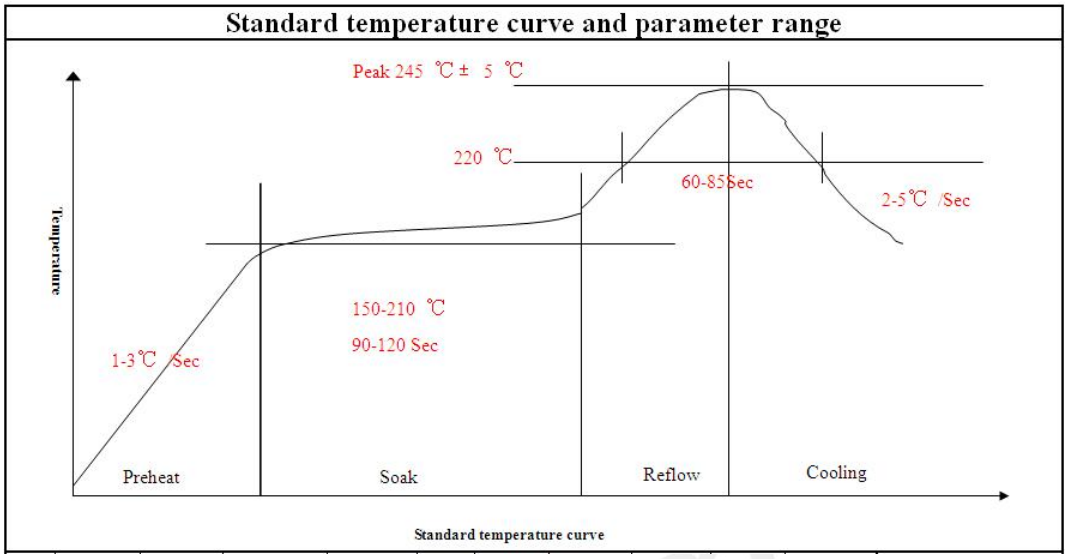

Figure 43: The Ramp-soak-spike Reflow Profile of Module

NOTE

For more details about secondary SMT, please refer to the document [21].

6.4 Moisture Sensitivity Level (MSL)

Module is qualified to Moisture Sensitivity Level (MSL) 3 in accordance with JEDEC J-STD-033. If the prescribed time limit is exceeded, users should bake module for 192 hours in drying equipment (<5% RH) at 40+5/-0 °C, or 8 hours at 120+5/-5 °C. Note that plastic tray is not heat-resistant, and only can be baked at 45° C.

Table 49: Moisture Sensitivity Level and Floor Life

Moisture Sensitivity Level (MSL)	Floor Life (out of bag) at factory ambient≤30°C/60% RH or as stated
1	Unlimited at ≦30℃/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, it must be reflowed within the time limit specified on the label.

NOTE

IPC / JEDEC J-STD-033 standard must be followed for production and storage.

6.5 Recommend Dimensions of SMT Stencil

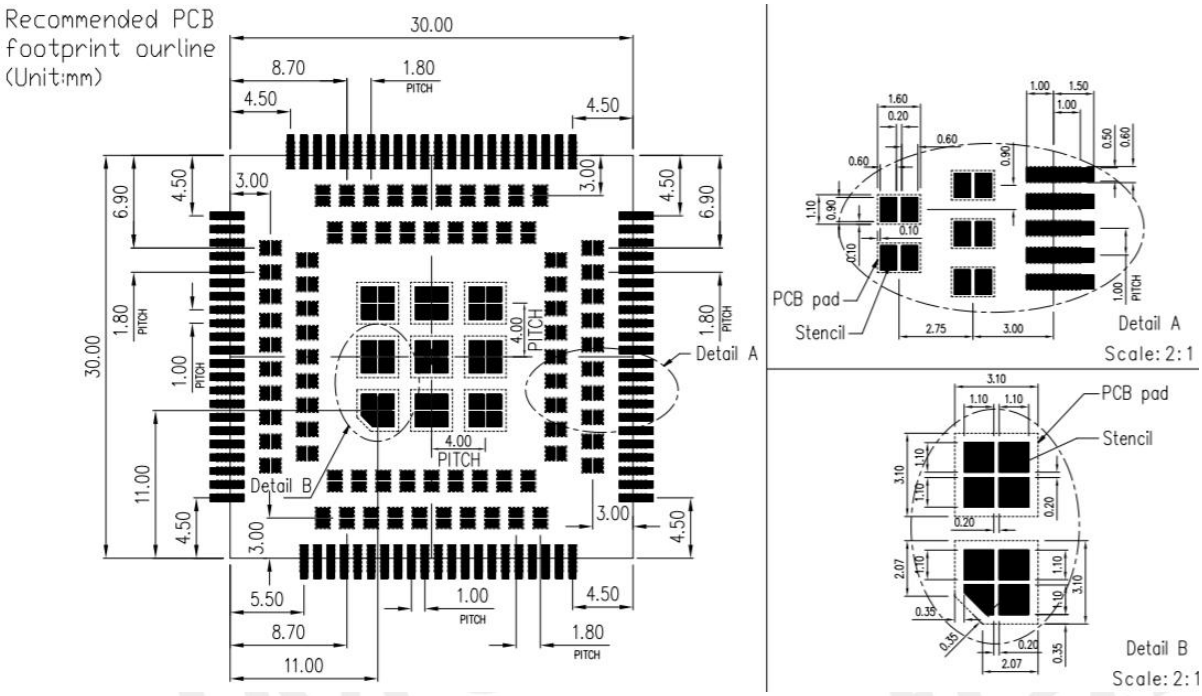

Figure 44: Recommend SMT Stencil

6.6 Stencil Foil Design Recommendation

The recommended thickness of stencil foil is more than 0.13mm.

7 Packaging

Module support tray packaging.

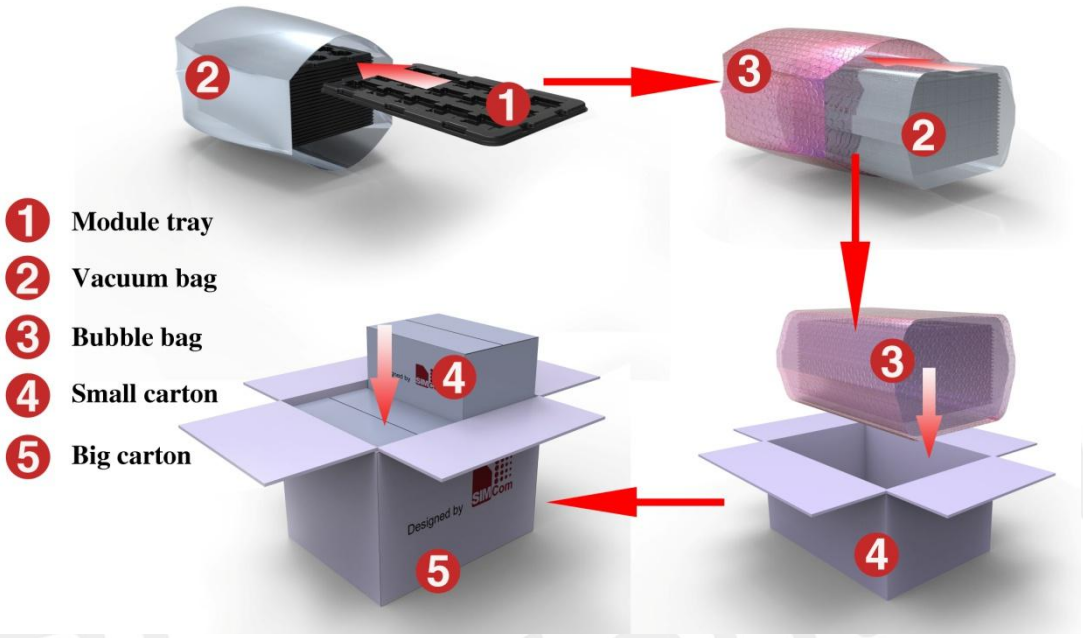

Figure 45: Packaging Diagram

Module tray drawing：

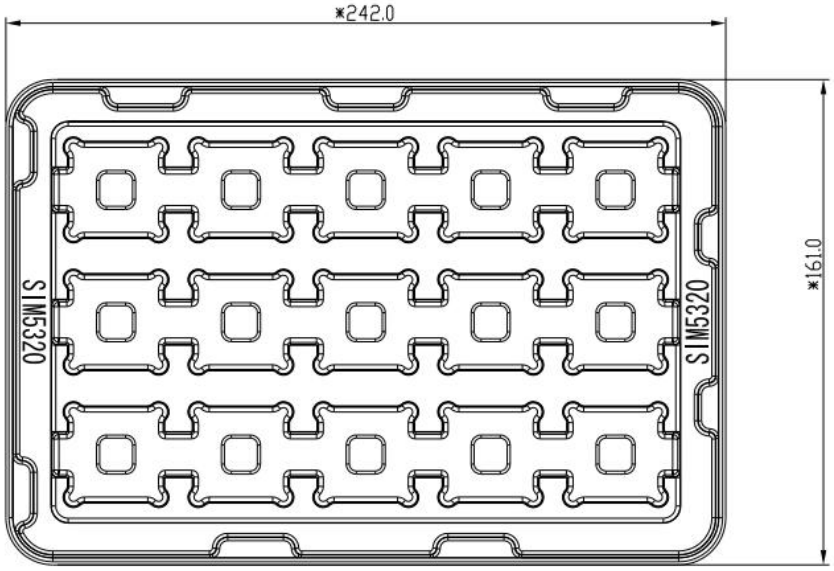

Figure 46: Tray Drawing

Table 50: Tray Size

Length (±3mm)	Width (±3mm)	Number
242.0	161.0	15

Small carton drawing：

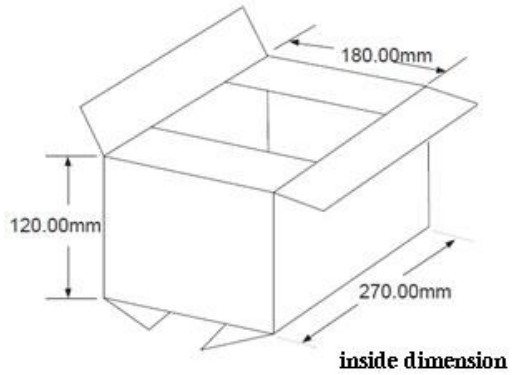

Figure 47: Small Carton Drawing

Table 51: Small Carton Size

Length (±10mm)	Width (±10mm)	Height (±10mm)	Number
270	180	120	15*20=300

Big carton drawing：

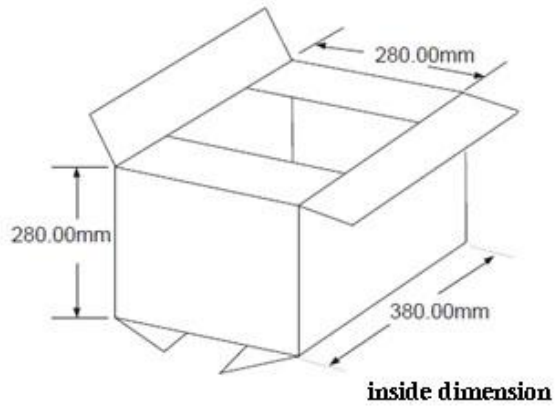

Figure 48: Big Carton Drawing

Table 52: Big Carton Size

Length (±10mm)	Width (±10mm)	Height (±10mm)	Number
380	280	280	300*4=1200

8 Appendix

8.1 Coding Schemes and Maximum Net Data Rates over Air Interface

Table 53: Coding Schemes and Maximum Net Data Rates over Air Interface

Multislot definition(GPRS/EDGE)			
Slot class	DL slot number	UL slot number	Active slot number
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
GPRS coding scheme	**Max data rata (4 slots)**		**Modulation type**
CS 1 = 9.05 kb/s / time slot	36.2 kb/s		GMSK
CS 2 = 13.4 kb/s / time slot	53.6 kb/s		GMSK
CS 3 = 15.6 kb/s / time slot	62.4 kb/s		GMSK
CS 4 = 21.4 kb/s / time slot	85.6 kb/s		GMSK
MCS 1 = 8.8 kb/s/ time slot	35.2 kb/s		GMSK
MCS 2 = 11.2 kb/s/ time slot	44.8 kb/s		GMSK
MCS 3 = 14.8 kb/s/ time slot	59.2 kb/s		GMSK
MCS 4 = 17.6 kb/s/ time slot	70.4 kb/s		GMSK
MCS 5 = 22.4 kb/s/ time slot	89.6 kb/s		8PSK
MCS 6 = 29.6 kb/s/ time slot	118.4 kb/s		8PSK
MCS 7 = 44.8 kb/s/ time slot	179.2 kb/s		8PSK
MCS 8 = 54.4 kb/s/ time slot	217.6 kb/s		8PSK
MCS 9 = 59.2 kb/s/ time slot	236.8 kb/s		8PSK
HSDPA device category	**Max data rate (peak)**		**Modulation type**
Category 1	1.2M bps		16QAM,QPSK
Category 2	1.2M bps		16QAM,QPSK
Category 3	1.8M bps		16QAM,QPSK

Category 4	1.8 Mbps	16QAM,QPSK
Category 5	3.6 Mbps	16QAM,QPSK
Category 6	3.6 Mbps	16QAM,QPSK
Category 7	7.2 Mbps	16QAM,QPSK
Category 8	7.2 Mbps	16QAM,QPSK
Category 9	10.2 Mbps	16QAM,QPSK
Category 10	14.4 Mbps	16QAM,QPSK
Category 11	0.9 Mbps	QPSK
Category 12	1.8 Mbps	QPSK
Category 13	17.6 Mbps	64QAM
Category 14	21.1 Mbps	64QAM
Category 15	23.4 Mbps	16QAM
Category 16	28 Mbps	16QAM
Category 17	23.4 Mbps	64QAM
Category 18	28 Mbps	64QAM
Category 19	35.5 Mbps	64QAM
Category 20	42 Mbps	64QAM
Category 21	23.4 Mbps	16QAM
Category 22	28 Mbps	16QAM
Category 23	35.5 Mbps	64QAM
Category 24	42.2 Mbps	64QAM
HSUPA device category	**Max data rate (peak)**	**Modulation type**
Category 1	0.96 Mbps	QPSK
Category 2	1.92 Mbps	QPSK
Category 3	1.92 Mbps	QPSK
Category 4	3.84 Mbps	QPSK
Category 5	3.84 Mbps	QPSK
Category 6	5.76 Mbps	QPSK
LTE-FDD device category (Downlink)	**Max data rate (peak)**	**Modulation type**
Category 1	10 Mbps	QPSK/16QAM/64QAM
Category 2	50 Mbps	QPSK/16QAM/64QAM
Category 3	100 Mbps	QPSK/16QAM/64QAM
Category 4	150 Mbps	QPSK/16QAM/64QAM
LTE-FDD device category (Uplink)	**Max data rate (peak)**	**Modulation type**
Category 1	5 Mbps	QPSK/16QAM
Category 2	25 Mbps	QPSK/16QAM
Category 3	50 Mbps	QPSK/16QAM
Category 4	50 Mbps	QPSK/16QAM

8.2 Related Documents

Table 54: Related Documents

NO	Title	Description
[1]	SIM7500_SIM7600 Series_AT Command Manual_V1.xx	AT Command Manual
[2]	ITU-T Draft new recommendationV.25ter	Serial asynchronous automatic dialing and control
[3]	GSM 07.07	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[4]	GSM 07.10	Support GSM 07.10 multiplexing protocol
[5]	GSM 07.05	Digital cellular telecommunications (Phase 2+); Use of Data Terminal Equipment – Data Circuit terminating Equipment (DTE – DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
[6]	GSM 11.14	Digital cellular telecommunications system (Phase 2+); Specification of the SIM Application Toolkit for the Subscriber Identity Module – Mobile Equipment (SIM – ME) interface
[7]	GSM 11.11	Digital cellular telecommunications system (Phase 2+); Specification of the Subscriber Identity Module – Mobile Equipment (SIM – ME) interface
[8]	GSM 03.38	Digital cellular telecommunications system (Phase 2+); Alphabets and language-specific information
[9]	GSM 11.10	Digital cellular telecommunications system (Phase 2)； Mobile Station (MS) conformance specification； Part 1: Conformance specification
[10]	3GPP TS 51.010-1	Digital cellular telecommunications system (Release 5); Mobile Station (MS) conformance specification
[11]	3GPP TS 34.124	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[12]	3GPP TS 34.121	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[13]	3GPP TS 34.123-1	Technical Specification Group Radio Access Network; Terminal conformance specification; Radio transmission and reception (FDD)
[14]	3GPP TS 34.123-3	User Equipment (UE) conformance specification; Part 3: Abstract Test Suites.
[15]	EN 301 908-02 V2.2.1	Electromagnetic compatibility and Radio spectrum Matters (ERM); Base Stations (BS) and User Equipment (UE) for IMT-2000. Third Generation cellular networks; Part 2: Harmonized EN for IMT-2000, CDMA Direct Spread (UTRA FDD) (UE) covering essential requirements of article 3.2 of the R&TTE Directive
[16]	EN 301 489-24 V1.2.1	Electromagnetic compatibility and Radio Spectrum Matters (ERM); Electromagnetic Compatibility (EMC) standard for

		radio equipment and services; Part 24: Specific conditions for IMT-2000 CDMA Direct Spread (UTRA) for Mobile and portable (UE) radio and ancillary equipment
[17]	IEC/EN60950-1(2001)	Safety of information technology equipment (2000)
[18]	3GPP TS 51.010-1	Digital cellular telecommunications system (Release 5); Mobile Station (MS) conformance specification
[19]	GCF-CC V3.23.1	Global Certification Forum - Certification Criteria
[20]	2002/95/EC	Directive of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS)
[21]	Module secondary-SMT-UGD-V1.xx	Module secondary SMT Guidelines
[22]	SIM7X00 Series_UART_Application Note_V1.xx	This document describes how to use UART interface of SIMCom modules.
[23]	SIM7100_SIM7500_SIM7600 Series_USB AUDIO_Application Note_V1.xx	USB AUDIO Application Note
[24]	SIM7X00 Series_GPS_Application Note_V1.xx	GPS Application Note
[25]	Antenna design guidelines for diversity receiver system	Antenna design guidelines for diversity receiver system
[26]	SIM7100_SIM7500_SIM7600_ Sleep Mode_Application Note_V1.xx	Sleep Mode Application Note
[27]	7600CE-LAN-Reference Design V1.0	HSIC Application Note

8.3 Terms and Abbreviations

Table 55: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
ARP	Antenna Reference Point
BER	Bit Error Rate
BTS	Base Transceiver Station
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DAC	Digital-to-Analog Converter
DRX	Discontinuous Reception
DSP	Digital Signal Processor
DTE	Data Terminal Equipment (typically computer, terminal, printer)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
ETS	European Telecommunication Standard
EVDO	Evolution Data Only
FCC	Federal Communications Commission (U.S.)
FD	SIM fix dialing phonebook
FDMA	Frequency Division Multiple Access
FR	Full Rate
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global Standard for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
I2C	Inter-Integrated Circuit
IMEI	International Mobile Equipment Identity
LTE	Long Term Evolution
MO	Mobile Originated
MS	Mobile Station (GSM engine), also referred to as TE
MT	Mobile Terminated
NMEA	National Marine Electronics Association

PAP	Password Authentication Protocol
PBCCH	Packet Switched Broadcast Control Channel
PCB	Printed Circuit Board
PCS	Personal Communication System, also referred to as GSM 1900
RF	Radio Frequency
RMS	Root Mean Square (value)
RTC	Real Time Clock
SIM	Subscriber Identification Module
SMS	Short Message Service
SPI	serial peripheral interface
SMPS	Switched-mode power supply
TDMA	Time Division Multiple Access
TE	Terminal Equipment, also referred to as DTE
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
VSWR	Voltage Standing Wave Ratio
SM	SIM phonebook
NC	Not connect
EDGE	Enhanced data rates for GSM evolution
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
ZIF	Zero intermediate frequency
WCDMA	Wideband Code Division Multiple Access
VCTCXO	Voltage control temperature-compensated crystal oscillator
USIM	Universal subscriber identity module
UMTS	Universal mobile telecommunications system

8.4 Safety Caution

Table 56: Safety Caution

Marks	Requirements
	When in a hospital or other health care facility, observe the restrictions about the use of mobiles. Switch the cellular terminal or mobile off, medical equipment may be sensitive and not operate normally due to RF energy interference.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it is switched off. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. Forgetting to think much of these instructions may impact the flight safety, or offend local legal action, or both.
	Do not operate the cellular terminal or mobile in the presence of flammable gases or fumes. Switch off the cellular terminal when you are near petrol stations, fuel depots, chemical plants or where blasting operations are in progress. Operation of any electrical equipment in potentially explosive atmospheres can constitute a safety hazard.
	Your cellular terminal or mobile receives and transmits radio frequency energy while switched on. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	Road safety comes first! Do not use a hand-held cellular terminal or mobile when driving a vehicle, unless it is securely mounted in a holder for hands free operation. Before making a call with a hand-held terminal or mobile, park the vehicle.
	GSM cellular terminals or mobiles operate over radio frequency signals and cellular networks and cannot be guaranteed to connect in all conditions, especially with a mobile fee or an invalid SIM card. While you are in this condition and need emergent help, please remember to use emergency calls. In order to make or receive calls, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength. Some networks do not allow for emergency call if certain network services or phone features are in use (e.g. lock functions, fixed dialing etc.). You may have to deactivate those features before you can make an emergency call. Also, some networks require that a valid SIM card be properly inserted in the cellular terminal or mobile.