

M52778SP

VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

DESCRIPTION

The M52778SP is a single-chip semiconductor integrated circuit to process signals of a color TV. Circuits to process video IF, sound IF, video, color, and deflection signals, a I²C bus control circuit, and D/ A are build in this device.

This IC can be used not only for popular-type TV sets but also for middle-class TV sets. Combined with a SECAM chroma decoder, the M52325AP, this device can process signals of every type of TVs in the world by discriminating them fully automatically.

FEATURES

- A built-in I²C bus control circuit makes it possible to reduce the number of peripheral parts and rationalize production lines.
- Various filters (TRAP, BPF, Y-DL, RGB clamp) are built in this IC.
- PLL detection system is introduced to process video IF and voice IF. Furthermore, AFT coil is not necessary.
- DL aperture control
- Color signal frequency and vertical frequency of TVs of every type can be discriminated fully automatically.
- Horizontal/vertical countdown system
- V-Ramp output
- RGB output

APPLICATION

PAL/NTSC CTV

RECOMMENDED OPERATING CONDITION

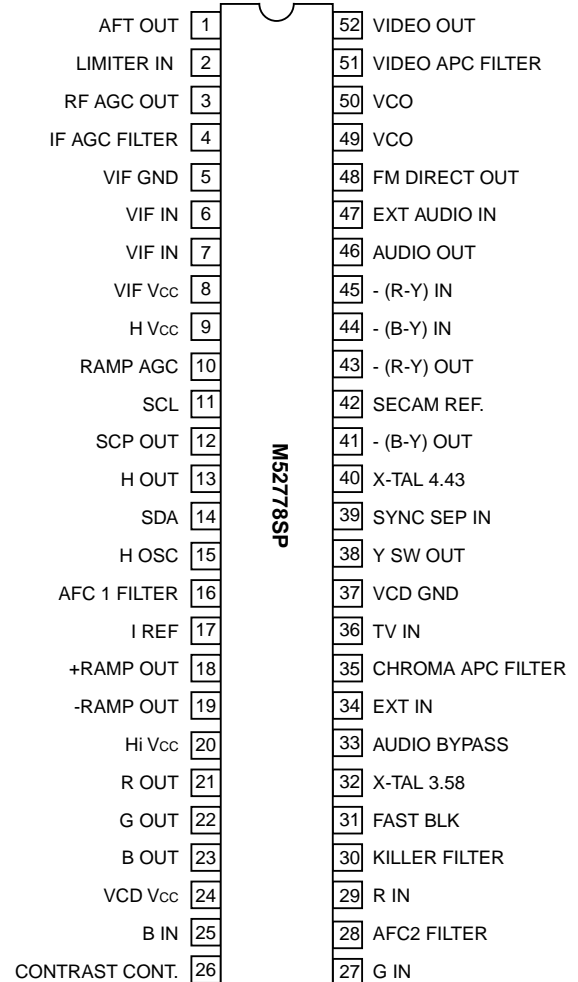
Supply voltage.....V8, 24=5V, V9, 20=8V

Rated supply voltage.....V8, 24=4.75 to 5.25V

V9, 20 =7.6 to 8.4V

Maximum output current.....5.0mA (pin13)

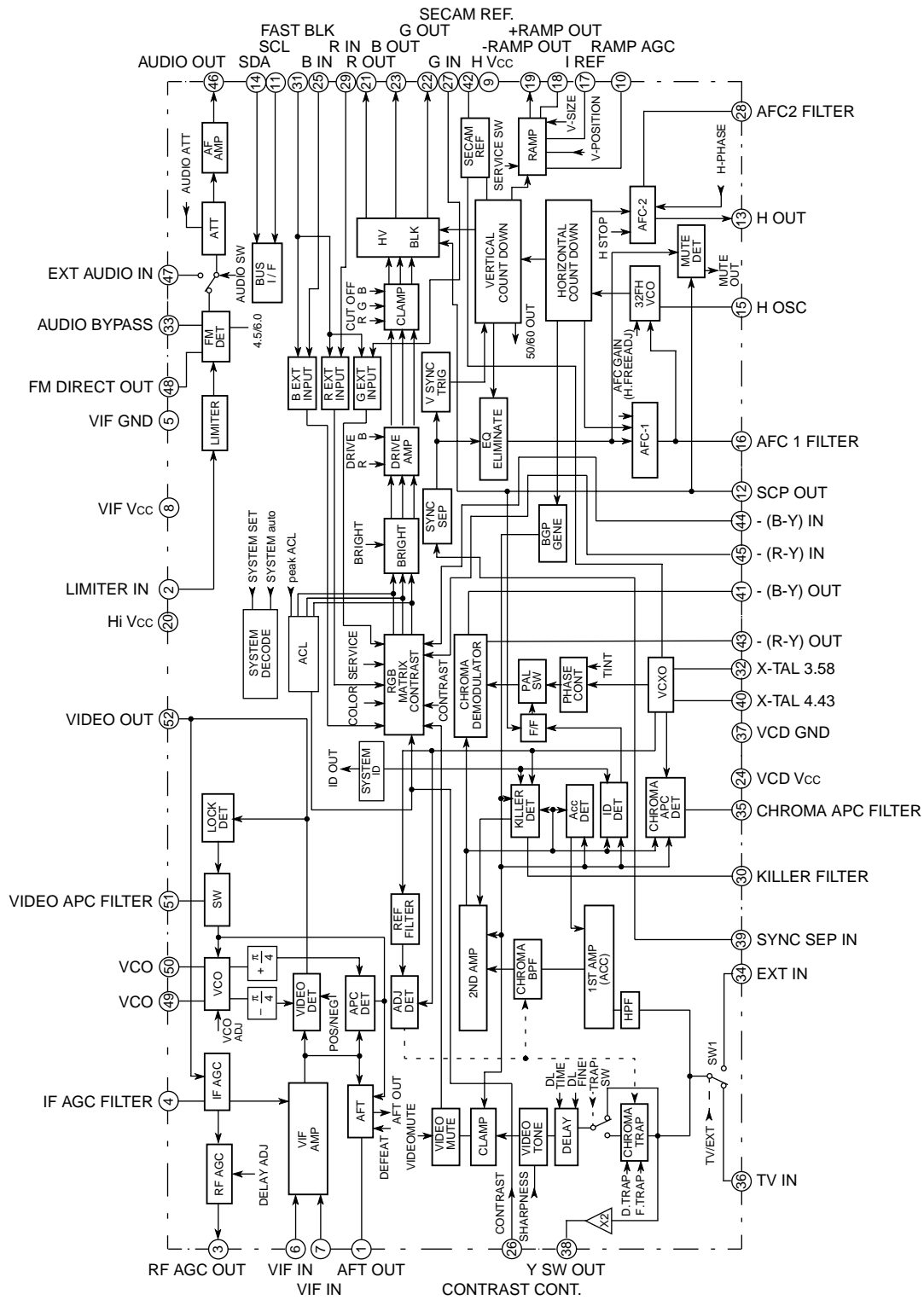
PIN CONFIGURATION (TOP VIEW)



Outline 52P4B

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BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V _{cc}	Supply voltage	6.0, 9.0	V
P _d	Power dissipation	1.69	W
T _{opr}	Operating temperature	-20 to +65	°C
T _{stg}	Storage temperature	-40 to +150	°C
Surge	Electrostatic discharge	-200 to +200	V

I²C BUS DEFAULT CONDITION OF ALL BLOCKS IN M52778SP

	sub address	00H		01H		02H						03H	04H		05H	06H			07H
	function	DLA	P/N	VCOA	AVSW	4.5/6.0	DFA	TRF2	DBF	TRAP	VidG	ATT	SHARP	DEFE	CONT	DLTA	TV/EXT	AUTO	TINT
All Blocks	DATA	20H		20H		00H						40H	00H		20H	02H			40H
	function	32	0	32	0	0	0	0	0	0	0	64	0	0	32	2	0	0	64

	sub address	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H			12H	13H						
	function	COLOR	SET	HP	BRI	DR	MUTE	DB	CR	CG	CB	V-PO	TRF	HA	SUBPO	ACL	SER	HST	AFCG	ACL
All Blocks	DATA	20H	40H	20H	20H	20H	10H	10H	10H	60H			00H	40H						
	function	32	0	8	32	32	0	32	16	16	16	0	1	1	0	1	0	0	0	0

* Please refer to the following sub-address data for each parameter you measure.

ELECTRICAL CHARACTERISTICS (Ta=25°C, pin8 and pin24:5V supply/pin9 and pin20:8V supply unless otherwise noted.)

Symbol	Parameter	Input signal		SW	Test conditions																Limits			Unit	Note														
					Sub address function																V _{cc}																		
		Input	SG	PIN	P1	P3	P4	P12	P13	P16	P18	P19	P46	P48	P52	DLA	P/N	VCOA	AVSW	ATT	00H	01H	03H	P8	P9	P20	P24	Min.	Typ.	Max.									
Supply current																																							
-	Default conditions of supply current	-	-	SW	1	1			0	0									20H	20H	40H																		
				PIN															32	0	32	0	64				5V	8V	8V	5V	-	-	-						
I _{cc8} I _{cc24}	Pin8, 24 supply current	-	-	SW																																			
				PIN																																			
I _{cc9}	Pin9 supply current	-	-	SW																																			
				PIN																																			
I _{cc20}	Pin20 supply current	-	-	SW																																			
				PIN																																			
VIF block																																							
-	Default conditions of VIF	-	-	SW	1	1			0	0									20H	20H	00H																		
				PIN															32	0	32	0	0				5V	8V	8V	5V	-	-	-	-					
V _{dc} NEG	Video detector output DC voltage (NEG)	-	-	SW																																			
				PIN																																			
V _{dc} POS	Video detector output DC voltage (POS)	-	-	SW																																			
				PIN																																			
V _o NEG	Video detector output AC voltage (NEG)	V	SG1	SW	0																																		
				PIN																																			
V _o POS	Video detector output AC voltage (POS)	V	SG2	SW	0																																		
				PIN																																			
P/N	Video S/N	V	SG3	SW	0																																		
				PIN																																			
V _f	Video frequency characteristics	V	SG4	SW	0																																		
				PIN																																			

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ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Input signal		SW	Test conditions																								Limits			Unit	Note
					Input	SG	P1	P3	P4	P12	P13	P16	P18	P19	P46	P48	P52	Sub address function						Vcc				Min.	Typ.	Max.			
															00H	01H	03H					P8	P9	P20	P24								
V _{in min}	Input sensitivity	V	SG5	SW PIN		0																								-	47	52	dBμ
V _{in max}	Maximum permissible input	V	SG6	SW PIN		0																							102	107	-	dBμ	
GR	AGC control range	-	-	SW PIN																								50	60	-	dBμ	calcu- late	
V4H	Maximum IF AGC voltage	-	-	SW PIN		0																							4.0	4.4	4.8	V	
V4T	IF AGC voltage (80dBu)	V	SG7	SW PIN		0		M																					2.2	2.6	3.0	V	
V4L	Minimum IF AGC voltage	V	SG8	SW PIN		0		M																					1.5	1.9	2.3	V	
V1	AFT defeat voltage	-	-	SW PIN			M																						3.7	4.0	4.3	V	
μAFT N	AFT detector sensitivity (NEG)	V	SG9	SW PIN		0	M																						43	61	79	mV/ kHz	
V1H N	Maximum AFT voltage (NEG)	V	SG10	SW PIN			M																						7.2	7.7	-	V	
V1L N	Minimum AFT voltage (NEG)	V	SG11	SW PIN			M																						-	0.3	0.8	V	
V3H	Maximum RF AGC voltage	V	SG3	SW PIN			M																						7.2	7.7	-	V	
V3L	Minimum RF AGC voltage	V	SG8	SW PIN			M																						-	0.3	0.8	V	
CRU	Capture range (upper)	V	SG9	SW PIN												M													0.8	1.2	-	MHz	
CRL	Capture range (lower)	V	SG9	SW PIN												M													2.2	2.6	-	MHz	
CRT	Capture range (total)	-	-	SW PIN																									3.0	3.8	-	MHz	calcu- late
IM	Intermodulation	V	SG12	SW PIN											M														31	36	-	dB	
DG	DG	V	SG13	SW PIN											M														-	3	7	%	
DP	DP	V	SG13	SW PIN											M														-	3	7	deg	
SPN	Sync ratio (NEG)	V	SG13	SW PIN											M														25.0	28.5	32.0	%	
DLPH	Maximum delay point (NEG/POS)	V	SG14	SW PIN			M										00/40H												90	96	-	dBμ	
DLPL	Minimum delay point (NEG/POS)	V	SG15	SW PIN			M										3F/7FH												-	70	76	dBμ	
SIF block																																	
-	Default conditions of SIF	-	-	SW PIN		1	1			0	0						20H	20H	40H														
VAF	AF output (DC)	S	SG21	SW PIN											M														2.0	2.4	2.8	V	
V _{oAF N}	AF direct output (4.5M)	S	SG16	SW PIN											M														400	570	740	mVrms	
V _{oAF P}	AF direct output (5.5M)	S	SG17	SW PIN											M														430	570	710	mVrms	
V _{oAF S}	AF direct output (6.0M)	S	SG18	SW PIN											M														440	590	740	mVrms	

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ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Input signal		SW	Test conditions																									Limits			Unit	Note																
		Input	SG		PIN	S	S		S	S													Sub address function					VCC				Min.			Typ.	Max.														
				P1		P3	P4	P12	P13	P16	P18	P23	P41	P42	P43	DL TA	TV/ EX T	AU TO	TINT	SE T	H P						P8	P9	P20	P24																				
chroma block (NTSC)																																																		
Cn3	Output signal amplitude 3:- (B-Y)	VI	SS3N	SW PIN																																46H					5V	8V	8V	5V	470	670	870	mV _{P-P}		
Cn4	Output signal amplitude 4:- (R-Y)	VI	SS3N	SW PIN												M																				46H									320	480	620	mV _{P-P}		
VkN	Threshold color killer on	VI	VS3N	SW v=variable PIN												M																				46H									-	-46	-38	dB		
killN	Residual color leakage at killer on	VI	VS3N	SW eb=0mV PIN												M																				46H									0	30	60	mV _{P-P}		
APC2	APC pull in range 2	VI	VS3N	SW f=variable PIN													M																			46H									+350	+870	-	Hz	eb=ec+50kHz	
R/BN	Ratio of (R-Y/B-Y)	VI	VS3N	SW eb=monochroma PIN												M																				46H									0.4	0.6	0.8	-		
θR-Y N	Demoduration phase θR-Y	VI	VS3N	SW eb=monochroma PIN												M																				46H									80	95	110	deg		
TC1	Tint control 1	VI	VS3N	SW eb=monochroma PIN												M																				7FH	46H									25	45	60	deg	
TC2	Tint control 2	VI	VS3N	SW eb=monochroma PIN												M																				00H	46H									25	45	60	deg	
chroma block (others)																																																		
SRA	SECAM ref output amplitude	-	-	SW PIN												M																				41H					5V	8V	8V	5V	200	400	570	mV _{P-P}		
SRD	SECAM ref output DC voltage	-	-	SW PIN												M																				41H									3.8	4.3	4.8	V		
AUTO 1	System identification 1 4.43 PAL	VI	SS4P	SW PIN																																25H													bus data read mode	
AUTO 2	System identification 2 4.43 NTSC	VI	SS4N	SW PIN													M																			25H													bus data read mode	
AUTO 3	System identification 3 3.58 PAL	VI	SS3P	SW PIN													M																			25H													bus data read mode	
AUTO 4	System identification 4 3.58 NTSC	VI	SS3N	SW PIN													M																			25H													bus data read mode	
AUTO 5	System identification 5 SECAM	-	-	SW PIN													M																			25H													bus data read mode	
AUTO 6	System identification 6 black & white	-	-	SW PIN													M																			25H													bus data read mode	

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ELECTRICAL CHARACTERISTICS

Video & RGB I/F block (cont.)

Symbol	Parameter	Input signal		SW	Test conditions																								Limits			Unit	Note	
					Sub address function																													
					Input	SG	PIN	P21	P22	P23	P26	P38	P40	4.5/6.0	DF A	TR F2	DB F	TR AP	Vid G	SH AP	DE FP	CO NT	DL TA	TV/EXT	AU TO	0A H	09H	0C H	10H	Min.	Typ.			Max.
GT5M	Video tone 5	VI	SGB	SW														20H	32H												-4	-1.4	1.2	dB
				PIN	M	M	M													32	50													
GYnor	Contrast 1	VI	SGB	SW															40H												2.1	2.5	2.9	V _{P-P}
				PIN	M	M	M														64													
GYmin	Contrast 2	VI	SGB	SW															00H												-	-	50	mV
				PIN	M	M	M														0													
Lumnor	Bright 1	-	-	SW																					40H						1.1	1.4	1.8	V
				PIN	M	M	M																			64								
Lummax	Bright 2	-	-	SW																					7FH						0.6	1.0	1.4	V
				PIN	M	M	M																			127								
Lummin	Bright 3	-	-	SW																					00H						-1.4	-1.0	-0.6	V
				PIN	M	M	M																			0								
D (R)	Drive R	VI	SGA	SW																						00/3FH					2.9	5.5	7.1	dB
				PIN	M																						0/63							
D (B)	Drive B	VI	SGA	SW																						00/3FH					2.9	5.5	7.1	dB
				PIN		M																					0/63							
EX (R)	EXT (R) I/O	FB ER	SGD	SW																					7FH				00H	4.8	6.0	7.2	V _{P-P}	
				PIN	M																						127							0
EX (G)	EXT (G) I/O	FB EG	SGD	SW																					7FH				00H	4.8	6.0	7.2	V _{P-P}	
				PIN		M																					127							0
EX (B)	EXT (B) I/O	FB EB	SGD	SW																					7FH				00H	4.8	6.0	7.2	V _{P-P}	
				PIN	M		M																				127							0

Video & RGB I/F block (cont.)

Symbol	Parameter	Input signal		SW	Test conditions																								Limits			Unit	Note	
					Sub address function																													
					Input	SG	PIN	P21	P22	P23	P26	P38	P40	4.5/6.0	DF A	TR F2	DB F	TR AP	Vid G	CO NT	DL TA	TV/EXT	AU TO	CO LR	BR I	0A H	0D H	0E H	0F H	13H	Min.			Typ.
OFRG	Offset voltage R-G	-	-	SW																						40H					-160	0	160	mV
				PIN		M																					64							
OFBG	Offset voltage B-G	-	-	SW																						40H					-160	0	160	mV
				PIN		M	M																				64							
C (R)	Cut off R	-	-	SW																						40H	00/FFH				1.0	1.4	1.8	V
				PIN	M																						64	0/255						
C (G)	Cut off G	-	-	SW																							00/FFH				1.0	1.4	1.8	V
				PIN		M																						0/255						
C (B)	Cut off B	-	-	SW																							00/FFH				1.0	1.4	1.8	V
				PIN			M																					0/255						

ELECTRICAL CHARACTERISTICS

Video & RGB I/F block (cont.)

Symbol	Parameter	Input signal		SW	Test conditions																											Limits			Unit	Note																	
					Sub address function																																																
Input	SG	PIN	P	P	P	P	P	P	Sub address function																			Min.	Typ.	Max.																							
			21	22	23	26	38	40	4.5/6.0	DA	TRF	DBF	TRAP	VidG	CO NT	DL TA	TV/EXT	AU TO	CO LO R	BR I	CR	CG	CB	AC L	SE R	HS T	AF CG																										
									02H	05H	06H	08H	0AH	0DH	0EH	0FH	13H																																				
DLF	Y delay time (fine)	VI	SGA	SW					02H	03H																											9	45	65	nsec													
				PIN	M	M	M			1																																											
Ccon1	Color control 1	-R	SGE	SW			1	1													7F	48																															
				PIN	M																	127	72																														
Ccon2	Color control 2	-R	SGE	SW			1	1													00	48																															
				PIN	M																	0	72																														
VMF	Video mute	VI	SGB f=4.43M	SW																																																	
				PIN	M	M	M																																														
MTXB	Matrix 1	-B	SGE	SW			1	1		20H				32								40	7F																														
				PIN	M							1	50										64	127																													
MTXG	Matrix 2	-B	SGE	SW			1	1		20H				32								40	7F																														
				PIN		M						1	50										64	127																													
MTXR	Matrix 3	-R	SGE	SW			1	1		20H				32								40	7F																														
				PIN		M						1	50										64	127																													
MTXG1	Matrix 4	-R	SGE	SW			1	1		20H				32								40	7F																														
				PIN		M						1	50										64	127																													
OSD1	OSD speed 1	ER,EG EB,FB	SGD	SW																		00																															
				PIN	M	M	M																0																														
OSD2	OSD speed 2	ER,EG EB,FB	SGD	SW																			00																														
				PIN	M	M	M																0																														
GYmax1	Contrast 3	VI	SGA	SW										7F																																							
				PIN	M	M	M	2.9 V																																													
GYmin1	Contrast 4	VI	SGA	SW										7F																																							
				PIN	M	M	M	0V																																													
ABR	Bright control (Vcc=8.5V at pin20)	-	-	SW																		7F																															
				PIN		M																																															
PACL1	Peak ACL 1	VI	SGB	SW										7F	00H							20	20	20																													
				PIN		M																	32	32	32	0	0	0	0																								
PACL2	Peak ACL 2	VI	SGB	SW										7F	00H								20	20	20																												
				PIN		M																	32	32	32	8	0	0	0																								
PACL3	Peak ACL 3	VI	SGB	SW										7F	00H								20	20	20																												
				PIN		M																	32	32	32	15	0	0	0																								

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No.	Sub address	06H			08H
	function	DLTA	TV/EXT	AUTO	COLOR
D0	DATA	20H			00H
	function	0	0	1	0

ELECTRICAL CHARACTERISTICS

Deflection block

Symbol	Parameter	Input signal		SW	Test conditions																				Limits			Unit	Note
					S4	S16	S44	S45	Sub address function												Vcc				Min.	Typ.	Max.		
		Input	SG	PIN	P12	P13	P16	P18	P19	P21	P22	P23	P39	09H	10H	11H	12H	13H				P8	P9	P20	P24	Min.	Typ.	Max.	
-	Default conditions of deflection	-	-	SW	1	1			0	0			40H	60H	20H	00H	47H								-	-	-	-	
				PIN									0	8	0	1	1	32	0	15	0	0	0	5V	8V	8V	5V		
ISS	Sync. sep. input sensitivity; current	-	-	SW																				-	0.1	0.2	mA		
				PIN							M																		
BGP1	Burst gate pulse timing 1 (PAL)	SY	SGa	SW																				1.5	2.5	3.5	μsec		
				PIN	M						M																		
BGP2	Burst gate pulse timing 2 (NTSC)	SY	SGb	SW																				1.6	2.6	3.6	μsec		
				PIN	M						M																		
BGPW	Burst gate pulse width	SY	SGa	SW																				4.8	6.0	7.2	μsec		
				PIN	M																								
fH	Horizontal free-running frequency	-	-	SW																				15.3	15.7	16.1	kHz		
				PIN	M																								
FPH1	Horizontal pull-in range 1	SY	SGc f=variable	SW																				+580	+780	-	Hz		
				PIN	M						M																		
FPH2	Horizontal pull-in range 2	SY	SGc f=variable	SW																				-	-440	-220	Hz		
				PIN	M						M																		
HPT1	Horizontal pulse timing 1	SY	SGa	SW																				7.0	8.1	9.2	μsec		
				PIN	M						M																		
HPT2	Horizontal pulse timing 2	SY	SGa	SW									00H											-2.0	-1.4	-0.8	μsec		
				PIN	M						M	0																	
HPT3	Horizontal pulse timing 3	SY	SGa	SW									78H											0.8	1.4	2.0	μsec		
				PIN	M						M	15																	
TH	Horizontal pulse width	-	-	SW																				21	25	29	μsec		
				PIN	M																								
VH	Horizontal pulse amplitude	-	-	SW																				3	4	-	V		
				PIN	M																								
HSTO	Horizontal pulse stop function	-	-	SW																				3	4	-	V		
				PIN	M																								
AFCG	AFG gain	SY	SGa	SW			0																	2.0	4.0	10	dB		
				PIN	M																								
fV	Vertical free-running frequency	-	-	SW																				41	44	47	Hz		
				PIN			M																						
AVER5	50/60 identification 5	SY	SGd f70Hz	SW																									
				PIN																									
SW	Service switch	-	-	SW					M	M														3.5	4	4.5	V		
				PIN																									
FPV	Vertical pull-in range	SY	SGd f=variable	SW	1	1				0	0																		
				PIN			M																						
VW	Vertical pulse width	-	-	SW																				0.35	0.52	0.65	msec		
				PIN			M																						

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Deflection block (cont.)

Symbol	Parameter	Input signal		SW	Test conditions																			Limits			Unit	Note																						
		Input	SG		PIN	P12	P13	P16	P18	P19	P21	P22	P23	P39	Sub address function										Vcc																									
				09H											10H				11H	12H	13H				P8	P9			P20	P24	Min.	Typ.	Max.																	
VBKWW	Vertical blanking width (pin21, 22, 23)	–	–	SW																																		1.35	1.5	1.6	msec									
AVER1	50/60 identification 1	SY	SGd f63Hz	SW																																			–	63	–	Hz	w-D7=1							
AVER2	50/60 identification 2	SY	SGd f57Hz	SW																																			–	57	–	Hz	w-D7=1							
AVER3	50/60 identification 3	SY	SGd f53Hz	SW																																				–	53	–	Hz	w-D7=0						
AVER4	50/60 identification 4	SY	SGd f47Hz	SW																																				–	47	–	Hz	w-D7=0						
WVSS	Vertical sync. detection minimum width	SY	SGd f60Hz width variable	SW																																					9.5	–	–	µsec						
Rsi1	Vertical ramp size	SY	SGA	SW																																				900	1100	1300	mV _{P-P}							
RΔs1	Vertical ramp size control range	SY	SGA	SW														00/40H																								83	93	103	%					
Rpo1	Vertical ramp position control range	SY	SGA	SW														7F/60H	20H																										120	170	220	mV		
Rgc	Vertical position center adjustment	SY	SGA	SW															31/0																										4	–	27	data		
Rpr	Vertical ramp out pulse width (PAL)	SY	SGA	SW																																										520	545	570	µsec	

ELECTRICAL CHARACTERISTICS TEST METHOD

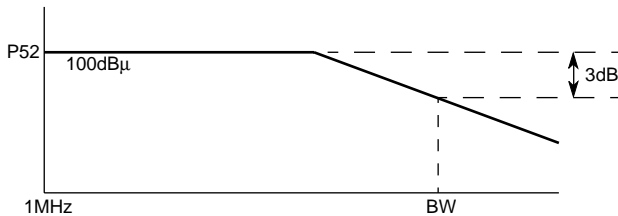
P/N Video S/N

1. Input SG3 and measure the rms value of output signal at pin 52.
2. P/N is defined as follows:

$$P/N=20\log \frac{V_{0NEG} \text{ measured value (VP-P)} \times 10^3 \times 0.7}{\text{Measured value (mVrms)}} \text{ (dB)}$$

BW Video frequency characteristics

1. Input SG4 and set the frequency f2 to 37.9MHz so that the beat element of 1MHz is output to pin 52.
2. Then set the applied voltage at pin 4 so that the beat element of 1MHz at pin 52 may be 100dBμ.
3. Decrease f2 to the level at which the beat element becomes 3dB smaller than the element of 1MHz, and read the value at that level.



Vin min. Input sensitivity

1. Decrease SG5 level until the video detector output is 3dB smaller than the measured value of Parameter V3 "Video detector output".

Vin max. Maximum permissible input

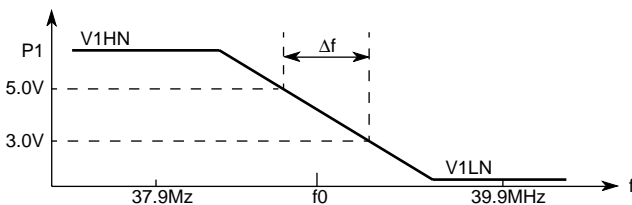
1. Input 90dBu SG6.
2. VA is the output level at pin 52. Increase SG6 voltage until the output at pin 52 becomes 3dB smaller than VA. The input level at that time is the maximum permissible input.

μAFTN AFT detector sensitivity (NEG)

V1HN Maximum AFT voltage (NEG)

V1LN Minimum AFT voltage (NEG)

See the following figure.



μAFTN is defined as follows:

$$\mu\text{AFTN} = \frac{(5.0-3.0) \times 10^3 \text{mV}}{\Delta f \text{ kHz}} \text{ (mV/kHz)}$$

IM Intermodulation

1. Adjust the applied voltage at pin 4 so that the lowest output signal voltage at pin 52 is 2.2V.



2. Measure elements of 1.07MHz and 4.43MHz of output at pin 52.
3. IM is defined as follows:

$$IM=20\log \frac{\text{Element of 1.07MHz}}{\text{Element of 4.43MHz}} \text{ (dB)}$$

ATT Maximum attenuation

1. Measure the element of 400Hz of output at pin 46.

$$ATT=20\log \frac{V_{0AFmax}}{\text{Measured value}} \text{ (dB)}$$

LIM Input limiting sensitivity

Decrease the input level of SG 18. Measure the input level when the element of 400Hz at pin 46 is 3dB smaller than V0AFM (S6: Maximum AF output (6.0M)).

AMR

1. Vam is the element of 400Hz at pin 46.
2. AMR is defined as follows:

$$AMR=20\log \frac{V_{0AFS} \text{ (mVrms)}}{V_{am} \text{ (mVrms)}} \text{ (dB)}$$

AF S/N

1. Measure the noise (20Hz to 100kHz) of output at pin 46.
2. AF S/N is defined as follows:

$$AF \text{ S/N}=20\log \frac{V_{0AFmax}}{\text{Measured value}} \text{ (dB)}$$

GEAu EXT Audio GAIN

Input SG22 at pin 47, and measure the output VP-P at pin 46.

$$GAIN=20\log \frac{\text{Input signal VP-P}}{\text{Output signal VP-P (pin46)}} \text{ (dB)}$$

Cn1 Output signal amplitude 1 (PAL)

Cn2 Output signal amplitude 2 (PAL)

1. Input SS4P to VI IN.
2. Measure output amplitude, Cn1 and Cn2, at pins 41 and 43 respectively.

VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

Acc1

1. Input VS4P (eb=570mV:level+6dB) to VI IN.
2. Measure the output amplitude at pin 43.
3. Acc1 is defined as follows:

$$Acc1=20\log \frac{\text{Measured value (V}_{P-P})}{Cn1 (V_{P-P})} \text{ (dB)}$$

Acc2

1. Input VS4P (input level:20dB) to VI IN.
2. Measure the output amplitude at pin 41.
3. Acc2 is defined as follows:

$$Acc2=20\log \frac{\text{Measured value (V}_{P-P})}{Cn1 (V_{P-P})} \text{ (dB)}$$

OL Chroma overload

1. Input VS4P (ec=800mV:P-P:chroma+3dB) to VI IN.
2. Measure the output amplitude at pin 41.
3. OL is defined as follows:

$$OL=20\log \frac{\text{Measured value (V}_{P-P})}{Cn1 (V_{P-P})} \text{ (dB)}$$

VikP Threshold color killer on (PAL)

1. Input VS4P (level:variable) to VI IN at input level 0dB.
2. Lower the input level whth monitoring the output amplitude at pin 41 and measure the input level when output amplitude isnot found.

KilIP Residual color leakage at killer on (PAL)

1. Input VS4P (level:40dB) to VI IN.
2. Measure the output amplitude at pin 41.

APC1 APC pull-in range 1

1. Input VS4P (f=eb=ec=variable) to VI IN.
2. Change the input signal frequency and measure the frequency range from the point at which signal is output to pin 41 and to the point that no signal is output to the pin. The reference value is 4.433619MHz.

R/B P Ratio of (R-Y/B-Y)

1. Input VS4P (eb=single chroma=ec+50kHz) to VI IN.
2. V41 is the output amplitude at pin 41.
3. V43 is the output amplitude at pin 43.
4. R /B P is defined as follows:

$$R/B P=20\log \frac{V43 (V_{P-P})}{V41 (V_{P-P})} \text{ (dB)}$$

θR-Y P Demodulation phase

1. Input VS4P (ed=single chroma=ec+50kNz) to VI IN.
2. V41 is the output amplitude at pin 41.
3. V43 is the output amplitude at pin 43.

4. R-Y P is defined as follows:

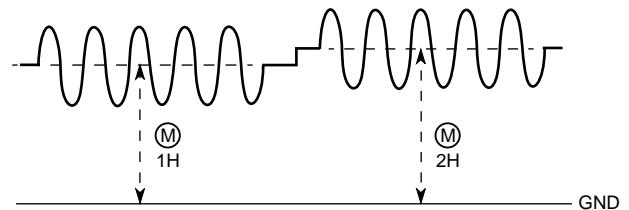
$$\theta R-Y P=\tan^{-1} \frac{V43 \times 3.8}{V41 \times 1.9} +45 \text{ (deg)}$$

CC Residual carrier leakage

Measure the element of 4.43MHz of the demodulated output in no-input state.

DDH Offset of demodulated output by line

1. Input 4.2MHz CW (Vi=575mV:P-P) to VI IN.
2. Measure the center DC voltage of output beat amplitude for two lines at pins 41 and 43. The absolute value of the difference in DC voltage is the difference of demodulated output on line.



Cn3, Cn4 Output signal amplitude3, 4 (NTSC)

1. Input SS3N to VI IN.
2. Cn3 and Cn4 are output amplitude measured at pins 41 and 43 respectively.

VikN Threshold color killer on (NTSC)

1. Input VS3N (level:variable) to VI IN at input level 0dB.
2. Lower the input level with monitoring the output amplitude at pins 41 and measure the input level when output amplitude is not found.

KilIN Residual color leakage at killer on (NTSC)

1. Input VS3N (level:-40dB) to VI IN.
2. Measure the output amplitude at pin 41.

APC2 APC Pull-in range 2

1. Input VS3N (f=eb=ec=variable) to VI IN.
2. Change the input signal frequency and measure the frequency range from the point at which no signal is output to 41 pin and to the point at which signal is output to the pin. (Pull-in state) The reference value is 3.579545MHz.

R/B N Ratio of (R-Y/B-Y)

1. Input VS3N (eb=signal chroma=ec+50kHz) to VI IN.
2. V41 is the output amplitude at pin 41.
3. V43 is the output amplitude at pin 43.
4. R/B N is defined as follows:

$$R/B N=20\log \frac{V43 (V_{P-P})}{V41 (V_{P-P})} \text{ (dB)}$$

VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

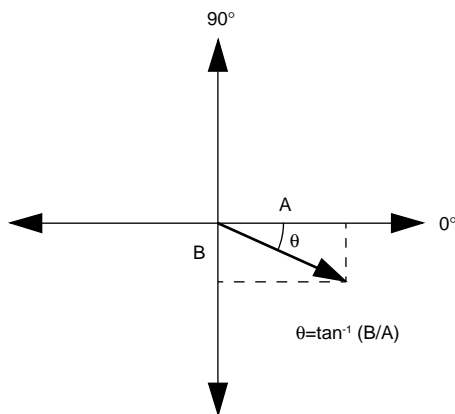
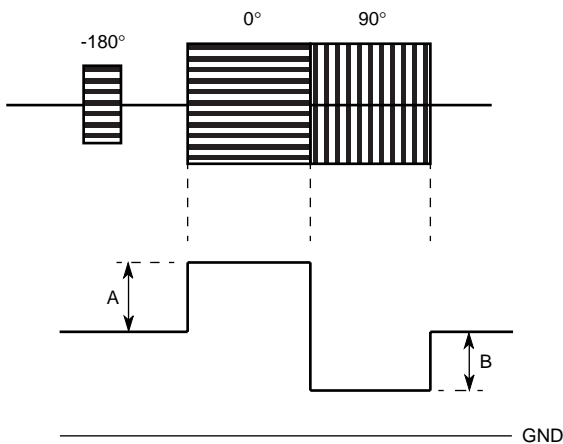
θR-Y N Demodulation phase

1. Input VS3N (eb=single chroma=ec+50kHz) to VI IN.
2. V41 is the output amplitude at pin 41.
3. V43 is the output amplitude at pin 43.
4. R-YN is defined as follows:

$$\theta_{R-YN} = \tan^{-1} \frac{V_{43} \times 3.8}{V_{41} \times 1.9} + 45 \text{ (deg)}$$

TC1 Tint control 1, TC2 Tint control 2

1. Input VS3N (see the following figure) to VI IN. Based on the output voltage at pin 41, find the absolute angle as shown in the following figure.



2. TC is defined as the angle when tint data is center (63).
TCmax is the angle when tint data is max, and TCmin is the angle when tint data is min.
TC1=TCMAX-TC (deg)
TC2=TC-TCMIN (deg)

SRA SECAM REF output amplitude

SRD SECAM REF output DC voltage

Measure the amplitude (SRA) and DC voltage (SRD) of the element of 4.43MHz of output at pin 42.

AUTO1 to 6 System identification 1 to 6

Set to AUTO mode and confirm that bus for each output signal is read correctly.

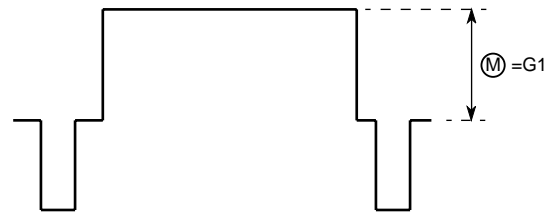
Ymax Maximum video output

1. Input SGA to VI IN
2. Measure the amplitude (P-P) except that at blanking part of output at pins 21, 22 and 23.



GY Video gain

1. Input SGA to VI IN
2. Measure the amplitude (P-P) except that at blanking part of output at pins 21, 22 and 23. This amplitude is defined as G1.



3. GY is defined as follows:

$$GY = 20 \log (G1 V_{P-P} / 0.714 V_{P-P}) \text{ (dB)}$$

BW Video frequency characteristics

1. Input SGB (5MHz, 0.4VP-P) to VI IN.
2. Measure the amplitude (P-P) except that at blanking part of the output at pin 22. The amplitude is defined as YB.
3. BW is defined as follow:

$$BW = 20 \log (YB V_{P-P} / GY V_{P-P}) \text{ (dB)}$$

2AGY Pin38 output amplitude

1. Input SGA to VI IN.
2. Measure the amplitude (P-P) at pin 38 output.

CTR1 Chroma trap attenuation 1 (common to R/G/B output)

1. Input SS3N to VI IN. Measure the frequency level of 3.58MHz at trap data 0. The level is defined as No.
2. Then, measure the level at trap data 1.
3. CTR1 is defined as follows.

$$CTR1 = 20 \log \frac{\text{Measured value (mVP-P)}}{N_0 \text{ (mVP-P)}} \text{ (dB)}$$

VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

**TRF1 Chroma trap fine adj. attenuation 1
(common to R/G/B output)**

1. Input SS3N to VI IN.
2. Measure the output amplitude of the element of 3.58MHz when trap fine adj. switch is on. (TRFon)
3. TRF1 is defined as follows.

$$TRF1=20\log \frac{TRFon (mVP-P)}{No (mVP-P)} (dB)$$

Measure the most attenuation part in three condition of (2), and the most attenuation part is defined as Y6.

The three condition of (2) is shown below.

	TRAP FINE ADT SW	FINE 2
condition 1	ON	OFF
condition 2	OFF	ON
condition 3	ON	ON

**DTR1 Chroma double trap attenuation 1
(common to R/G/B output)**

1. Input SS3N to VI IN.
2. Measure the output amplitude of the element of 3.58MHz when D.trap switch is on. (DTR on)
3. DTR1 is defined as follows.

$$DTR1=20\log \frac{DTRon (mVP-P)}{No (mVP-P)} (dB)$$

CTR2 Chroma trap attenuation 2 (common to R/G/B output)

1. Input SS4P to VI IN and measure the frequency level of 4.43MHz at trap data 0. The level is defined as Po.
2. Then, measure the level at trap data 1.
3. CTR2 is defined as follows.

$$CTR2=20\log \frac{\text{Measured value (mVP-P)}}{Po (mVP-P)} (dB)$$

TRF2 Chroma trap fine adj. attenuation 2

1. Input SS4P to VI IN.
2. Measure the output amplitude of the element of 4.43MHz when trap fine adj. switch is on. (TRFon)
3. TRF2 is defined as follows.

$$TRF2=20\log \frac{TRFon (mVP-P)}{Po (mVP-P)} (dB)$$

Measure the most attenuation part in three condition of (2), and the most attenuation part is defined as Y9.

The three condition of (2) is shown below.

	TRAP FINE ADT SW	FINE 2
condition 1	ON	OFF
condition 2	OFF	ON
condition 3	ON	ON

DTR2 Chroma double trap attenuation 2

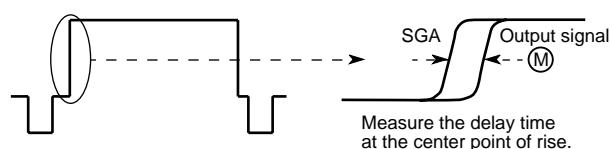
1. Input SS4P to VI IN.
2. Measure the output amplitude of the element of 4.43MHz when D.trap switch is on. (DTR on)
3. DTR2 is defined as follows.

$$DTR2=20\log \frac{DTRon (mVP-P)}{Po (mVP-P)} (dB)$$

Note: In parameters Y5,Y6,Y8 and Y9, limits are defined based on the maximum attenuation by comparing each one.

YDL1 Y delay time1

1. Input SGA to VI IN.
2. Measure the delay time from signal input to output at pins 21, 22 and 23.



YDL2 to 4 Y delay time2 to 4

1. Input SGA to VI IN.
2. Measure the delay time from signal output at pins 21, 22 and 23 to Y11, YDL1.

GTnor Video tone 1

1. Input SGB (f=3MHz) to VI IN.
2. Measure output amplitude at pins 21, 22 and 23.

GTmax Video tone 2

1. Input SGB (f=3MHz) to VI IN.
2. Measure output amplitude at pins 21, 22 and 23.
3. GTmax is defined as follows:

$$GTmax=20\log \frac{\text{Measured value (VP-P)}}{GTnor (VP-P)} (dB)$$

GTmin Video tone 3

1. Input SGB (f=3MHz) to VI IN.
2. Measure output amplitude at pins 21, 22 and 23.
3. GTmin is defined as follows:

$$GTmin=20\log \frac{\text{Measured value (VP-P)}}{GTnor (VP-P)} (dB)$$

GT2M Video tone 4

1. Input SGB (f=2MHz) to VI IN.
2. Measure output amplitude at pins 21, 22 and 23.
3. GT2M is defined as follows:

$$GT2M=20\log \frac{\text{Measured value (VP-P)}}{GTnor (VP-P)} (dB)$$

VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

GT5M Video tone 5

1. Input SGB (f=5MHz) to VI IN.
2. Measure output amplitude at pins 21, 22 and 23.
3. GT5M is defined as follows:

$$GT5M=20\log \frac{\text{Measured value (V}_{P-P})}{GYnor (V_{P-P})} \text{ (dB)}$$

GYnor Contrast 1

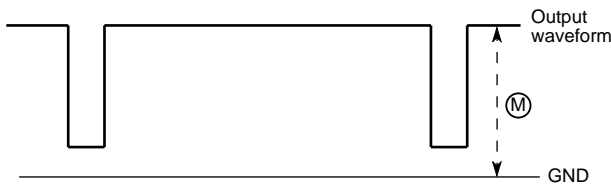
1. Input SGB (f=100kHz) to VI IN.
2. Measure output amplitude at pins 21, 22 and 23.

GYmin Contrast 2

1. Input SGB (f=100kHz) to VI IN.
2. Measure output amplitude at pins 21, 22 and 23.

Lum nor Brightness control 1, Lum max Brightness control 2, Lum min Brightness control 3

1. No signal is input. (Only SG50 is input to SY IN.)
2. Measure DC voltage of output at pins 21, 22 and 23 except that at blanking part.



3. Y23=(Lum max)-(Lum nor), Y24=(Lum min)-(Lum nor)

D (R) Drive R

1. Input SGA to VI IN.
2. Measure DRmin and DRmax which are output amplitude at pins 21 at D (R) data min and D (R) data max respectively.
3. G (R) is defined as follows:

$$G (R)=20\log \frac{DRmax (V_{P-P})}{DRmin (V_{P-P})} \text{ (dB)}$$

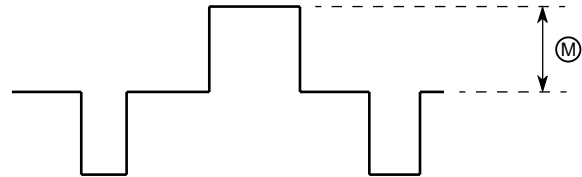
D (B) Drive B

1. Input SGA to VI IN.
2. Measure DBmin and DBmax which are output amplitude at pin 23 at D (B) data min and D (B) data max respectively.
3. D (B) is defined as follows:

$$D (B)=20\log \frac{DBmax (V_{P-P})}{DBmin (V_{P-P})} \text{ (dB)}$$

EXR EXT (R) I/O, EXG EXT (G) I/O, EXB EXT (B) I/O

1. Input SGD to FB, ER, EG and EB.
2. Measure output amplitude which is higher than the pedestal level at pins 21, 22 and 23. The amplitude at blanking part should not be measured.



OFRG Offset voltage R-G, OFBG Offset voltage B-G

1. Measure DC voltage of output at pin 21, 22 and 23 except that at blanking part .

2. OFRG and OFRB are defines as follows:

OFRG=

(pin 21 Measured voltage)-(pin 22 Measured voltage) (mV)

OFBB=

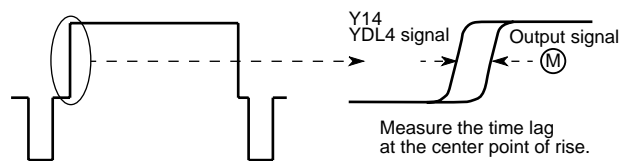
(pin 23 Measured voltage)-(pin 22 Measured voltage) (mV)

R (C) Cutoff R, G (C) Cutoff G, B (C) Cutoff B

1. Measure DC voltage of output at pin 21, 22 and 23 when R (C), G (C) and B (C) data are maximum and minimum respectively. The DC voltage at blanking part should not be measured.
2. R (C), G (C) and B (C) are defined as follows:
R (C), G (C) and B (C)=
(Voltage at data max.)-(Voltage at data min.) (V)

DLFY delay time (fine)

1. Input SGA to VI IN.
2. Measure the time lag (absolute value) between signal YDL4 and output signal at pins 21, 22 and 23.



Ccon1 Color control 1, Ccon2 Color control 2

1. Input SGE to -RIN (pin 45).
2. Measure output amplitude at pins 21 under each condition.

VMF Video mute

1. Input SGB to VI IN.
2. Measure output amplitude of the element of 4.43MHz when the mute switch is on and off. (VMFon, VMFoff)
3. VMF is defined as follows:

$$VMF=20\log \frac{TRFon (V_{P-P})}{TRFoff (V_{P-P})} \text{ (dB)}$$

VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

MTXB Matrix 1, MTXG Matrix 2

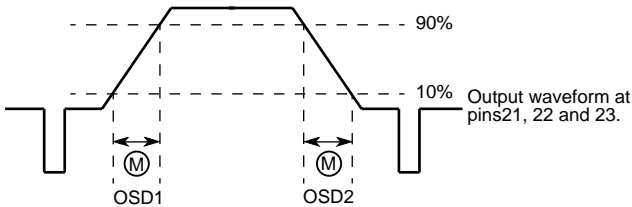
1. Input SGE to-B IN (pin 44).
2. Measure output amplitude at pins 22 and 23.
(P23=MTXB, P22=MTXG)

MTXR Matrix 3, MTXG1 Matrix 4

1. Input SGE to-R IN (pin 45).
2. Measure output amplitude at pins 21 and 22.
(P21=MTXR, P22=MTXG1)

OSD1 OSD speed 1, OSD2 OSD speed 2

1. Input SGD to FB, ER, EG and EB.
2. Measure rise time and fall time of the signal of output at pins 21, 22 and 23. Measurement points should be higher than the pedestal level and blanking part should not be measured.



GYmax1 Contrast 3, GYmin1 Contrast 4

1. Input SGA to VI IN.
2. Measure output amplitude at pins 21, 22 and 23 when 2.9V and 0V are externally applied to pin 26.

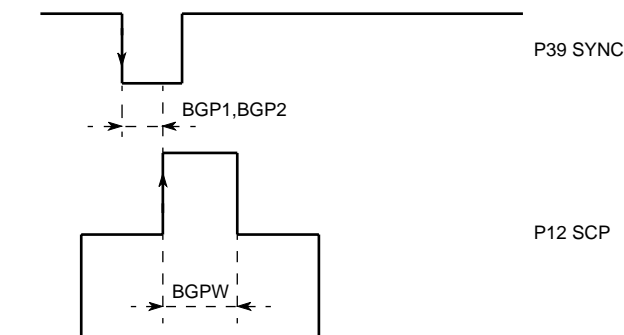
ISS Sync separation input sensitivity current

Make current flow out from pin 39 and measure the flow current when the free running frequency (=45Hz) changed at pin 18.

BGP1 Burst gate pulse timing 1 (PAL)

BGP2 Burst gate pulse timing 2 (NTSC)

BGPW Burst gate pulse width



FH Horizontal free running frequency

Measure the output frequency at pin 13 when no signal is input.

FPH1 Horizontal pull-in range 1

FPH2 Horizontal pull-in range 2

Change the frequency of SGc and measure the frequency at the moment when the output signal at pin 13 and the input signal at pin 39 are pulled in. The horizontal pull-in range is measured by comparing with 15.625kHz.

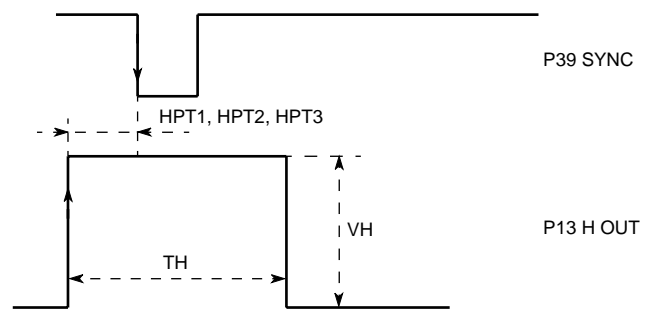
HPT1 Horizontal pulse timing 1

HPT2 Horizontal pulse timing 2

HPT3 Horizontal pulse timing 3

$$HPT2 = \text{Hphase data (0)} - HPT1$$

$$HPT3 = \text{Hphase data (15)} - HPT1$$



TH Horizontal pulse width, VH Horizontal pulse amplitude

HSTO Horizontal pulse stop function

Confirm that the horizontal output is high when the horizontal stop switch is on.

AFCG AFC gain

1. Measure AFC on which is the output amplitude of pin 16 when AFC switch is on and AFC off which is that when the switch is off.
2. AFCG is defined as follows:

$$AFCG = 20 \log \frac{AFC_{on} (V_{P-P})}{AFC_{off} (V_{P-P})} \text{ (dB)}$$

FV Vertical free running frequency

Measure the output frequency at pin 18 when no signal is input.

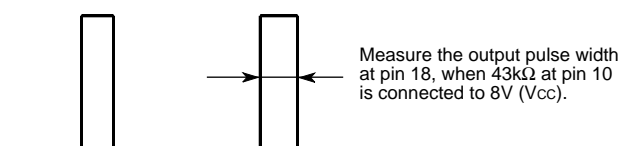
SW Service SW operation

Measure the output DC voltage at pin 18 when the service switch is on.

FPV Vertical pull-in range

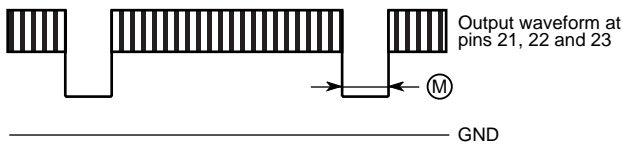
Decrease the frequency of SGd and measure the frequency when output waveform at pin 18 is pulled in.

VW Vertical pulse width (free running)



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VBLKW Vertical blanking width



**AVER5 50/60 identification 5, AVER1 50/60 identification 1
 AVER2 50/60 identification 2, AVER3 50/60 identification 3,
 AVER4 50/60 identification 4**

Confirm that the frequency of output at pin 18 is the same at each input frequency (pull-in state). Also, confirm the state of the bus read mode (D7).

WVSS Vertical sync.detection minimum width

Change the input pulse width of SGd and measure the input pulse width at the moment when the output signal at pin 18 and the input signal at pin 39 are pulled in.

Rsi1 Vertical ramp size

Measure the pin18 amplitude.

Rs1 Vertical ramp size control range

1. Measure the pin 18 amplitude. (size data : max and min)
2. $Rs1 = \frac{\text{Pin18 size max} - \text{pin18 size min}}{Rs1} \times 100(\%)$

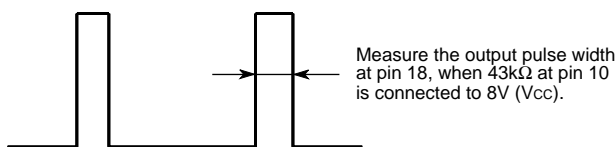
Rpo1 Vertical ramp position control range

1. Measure the pin 18 top voltage. (position data : max and min)
2. $Rpo1 = \text{pin 18 posi max} - \text{pin 18 posi min} \text{ (mv)}$

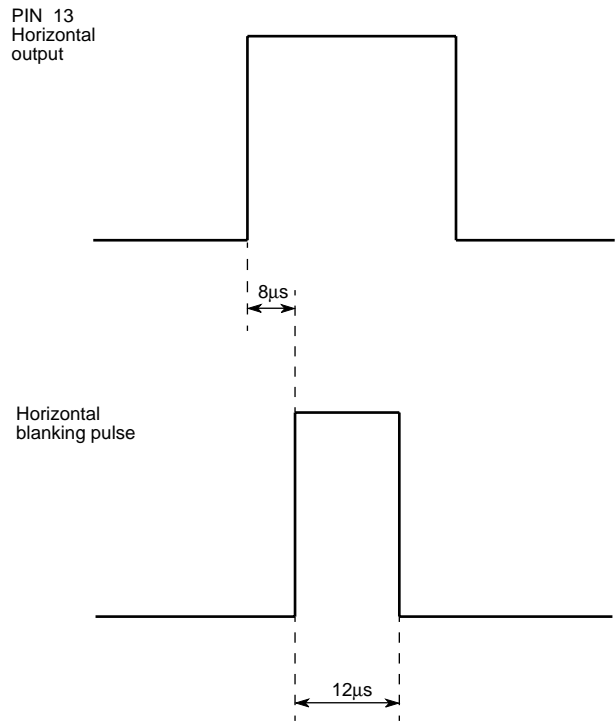
Rgc Vertical position center adjustment

1. Adjust the position bus data so that the output DC bias current at pin18 and pin 19 should be equal.
2. Specify this position bus data adjusted above.

Rgr Vertical ramp out pulse width (PAL)



Note: The timing and pulse width of the horizontal blanking pulse should be as shown in the following figure by adjusting the variable resistor of the single shot multi vibrator.

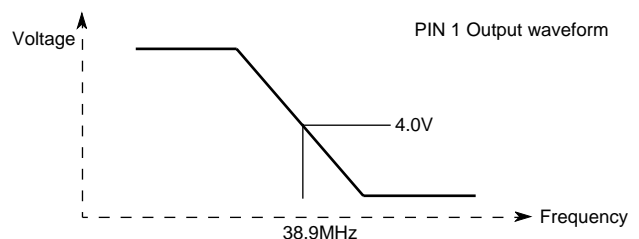


The variable resistor at pin 15 of the TTL IC, M74LS221P, is used to fix the timing at 8μs and that at pin 7 is used to fix the pulse width at 12μs.

*Coil adjustment

VCO COIL

1. Set the test conditions as shown in the parameter V14.
2. Input CW (fo=38.9MHz, Vi=90dBμ) to input pin A.
3. Set the DC voltage at pin 1 (AFT OUT) to 1/2Vcc (4.0V) by adjusting VCO coil.



Note: VCO coil should always be adjusted as above before using this IC.

M52778SP

VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

(The binary, Decimal and hexadecimal number table)

Hexadecimal number	Binary number				Decimal
	D3	D2	D1	D0	
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	2
3	0	0	1	1	3
4	0	1	0	0	4
5	0	1	0	1	5
6	0	1	1	0	6
7	0	1	1	1	7
8	1	0	0	0	8
9	1	0	0	1	9
A	1	0	1	0	10
B	1	0	1	1	11
C	1	1	0	0	12
D	1	1	0	1	13
E	1	1	1	0	14
F	1	1	1	1	15

(Note)	Hexadecimal number	Decimal	Hexadecimal number	Decimal
	10H	= 16	90H	= 144
	20H	= 32	A0H	= 160
	30H	= 48	B0H	= 176
	40H	= 64	C0H	= 192
	50H	= 80	D0H	= 208
	60H	= 96	E0H	= 224
	70H	= 112	F0H	= 240
	80H	= 128		

INITIAL CONDITION

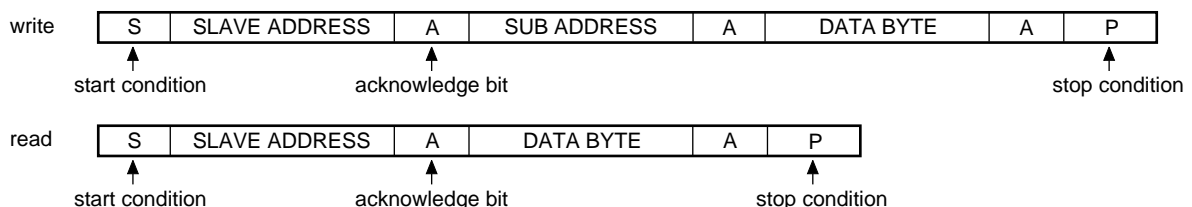
NO

	D7	D6	D5	D4	D3	D2	D1	D0	Data
00H		POS/NEG	DELAY ADJ						00H
	0	0	0	0	0	0	0	0	
01H		AVSW	VCO ADJ						20H
	0	0	1	0	0	0	0	0	
02H		VideoG	TRAP	DBF	FTRAP2		DFA	4.5/6.0	06H
	0	0	0	0	0	1	1	0	
03H		AUDIO ATT						00H	
	0	0	0	0	0	0	0		0
04H		DEFEAT	SHARPNESS						20H
	0	0	1	0	0	0	0	0	
05H		CONTRAST						20H	
	0	0	1	0	0	0	0		0
06H			AUTO			TV/EXT	DL TIME	02H	
	0	0	0	0	0	0	1		0
07H		TINT						40H	
	0	1	0	0	0	0	0		0
08H		COLOR						20H	
	0	0	1	0	0	0	0		0
09H		HPHASE			3.58	NTSC	SECAM	40H	
	0	1	0	0	0	0	0		
0AH		BRIGHT						20H	
	0	0	1	0	0	0	0		0
0BH		MUTE	DRIVE R						20H
	0	0	1	0	0	0	0	0	
0CH			DRIVE B						20H
	0	0	1	0	0	0	0	0	
0DH		CUT OFF R						10H	
	0	0	0	1	0	0	0		0
0EH		CUT OFF G						10H	
	0	0	0	1	0	0	0		0
0FH		CUT OFF B						10H	
	0	0	0	1	0	0	0		0
10H		HADJ	FTRAP	V-POSI				38H	
	0	0	1	1	1	0	0		0
11H			V-SIZE				20H		
	0	0	1	0	0	0		0	0
12H							SUB-POSI	00H	
	0	0	0	0	0	0	0		0
13H		ACL	AFCG	HST	SERSW	ACL		40H	
	0	1	0	0	0	0	0		0

I²C BUS FORMATS

(1) Slave address: A6 A5 A4 A3 A2 A1 A0 R/W
 1 0 1 1 1 0 1 0 (=BAH)

(2) Slave address format:



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VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

(3) Sub address byte and data byte format:

write

*SW

	No.	Functions	BIT	SUB ADD	Data byte							
					D7	D6	D5	D4	D3	D2	D1	D0
IF	1	DELAY ADJ	6	00H	0	–	A05	A04	A03	A02	A01	A00
	2	POS/NEG	1	00H		POS/NEG						
	3	VCO ADJ	6	01H	0	–	A15	A14	A13	A12	A11	A10
	4	AUDIO SW*	1	01H		AUDIO SW						
	5	4.5/6.0*	1	02H								4.5/6.0
	6	DEFEAT*	1	04H		DEFEAT						
	7	AUDIO ATT	7	03H	0	A36	A35	A34	A33	A32	A31	A30
VIDEO	36	VIDEO OUT GAIN*	1	02H		VIDEO OUT GAIN						
	8	sharpness	6	04H	0	–	A45	A44	A43	A42	A41	A40
	9	contrast cont	7	05H	0	A56	A55	A54	A53	A52	A51	A50
	10	DL time ADJ*	2	06H	0	0	0	–	–	–	A61	A60
	25	DL fine ADJ.	1	02H							0	
		+50nsec +0nsec									1	
	11	TV/EXT*	1	06H						TV/EXT		
	14	TRAP on/off*	1	02H			TRAP					
	37	DOUBLE TRAP*	1	02H				DTRAP				
38	TRAP fine adj. 1*	1	10H			FTRAP1						
40	TRAP fine adj. 2*	1	02H					FTRAP2				
36	VIDEO MUTE*	1	0BH		VIDEO MUTE							
CHROMA	15	tint cont	7	07H	0	A76	A75	A74	A73	A72	A71	A70
	16	color cont	7	08H	0	A86	A85	A84	A83	A82	A81	A80
	17	SYSTEM auto*	1	06H			auto					
	18	SYSTEM SET*	3	09H	0	–	–	–	–	3.58	NTSC	SECAM
INTER-FACE	19	bright cont	7	0AH	0	AA6	AA5	AA4	AA3	AA2	AA1	AA0
	20	drive (R)	6	0BH	0	0	AB5	AB4	AB3	AB2	AB1	AB0
	21	drive (B)	6	0CH	0	0	AC5	AC4	AC3	AC2	AC1	AC0
	22	cut off (R)	8	0DH	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
	23	cut off (G)	8	0EH	AE7	AE6	AE5	AE4	AE3	AE2	AE1	AE0
	24	cut off (B)	8	0FH	AF7	AF6	AF5	AF4	AF3	AF2	AF1	AF0
	31	PEAK ACL	4	13H	0	A136	–	–	–	A132	A131	A130
DEFLECTION	27	AFC-2 H phase	4	09H	0	A96	A95	A94	A93	–	–	–
	29	V-SIZE	6	11H	0	0	A115	A114	A113	A112	A111	A110
	28	V-POSITION	5	10H	0	–	–	A104	A103	A102	A101	A100
	30	SUB-POSITION*	2	12H	0	–	–	–	–	–	A121	A120
	33	Service SW*	1	13H					Service SW			
	34	H STOP*	1	13H				H STOP				
	35	AFC GAIN*	1	13H			AFC GAIN					
	41	H fo ADJ*	1	10H		HADJ						

read

Data byte							
D7	D6	D5	D4	D3	D2	D1	D0
50/60	COINCIDENCE	AFT1	AFT0	3.58	NTSC	SECAM	CONDITION/ killer out

VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

DATA BYTE CONDITIONS AT SW

	Functions	Data	Condition	Initial condition		
IF	POS/NEG	POS/NEG	0	NEG	NEG	
			1	POS		
	AUDIO SW	AUDIO SW	0	OFF	OFF	
			1	ON		
	DEFEAT	DEFEAT	0	OFF	OFF	
			1	ON		
	4.5/6.0	4.5/6.0	0	6.0	6.0	
			1	4.5		
	VIDEO OUT GAIN	VIDEO OUT GAIN	0	Normal	Normal	
			1	gain down		
VIDEO	DL time ADJ	A71, A70	0 0	120nsec	360nsec	
			0 1	280nsec		
			1 0	360nsec		
			1 1	440nsec		
	TV/EXT	TV/EXT	0	TV	TV	
			1	EXT		
	VIDEO MUTE	MUTE	0	VIDEO OUT	VIDEO OUT	
			1	VIDEO MUTE		
	TRAP on/off	TRAP	0	TRAO OFF	TRAP OFF	
			1	TRAP ON		
	DOUBLE TRAP	DTRAP	0	SINGLE TRAP	SINGLE TRAP	
			1	DOUBLE TRAP		
	INTERFACE	TRAP fine adj. 1	FTRAP1	0	fo down	fo up
				1	fo up	
TRAP fine adj. 2		FTRAP2	0	fo down	fo down	
			1	fo up		
CHROMA	SYSTEM auto	auto	0	manual	manual	
			1	auto		
	SYSTEM SET	3.58, NTSC, SECAM	0 0 0	4.43 PAL	4.43 PAL	
			1 0 0	3.58 PAL		
			1 1 0	3.58 NTSC		
			0 1 0	4.43 NTSC		
0 0 1	SECAM					
DEFLECTION	Service SW	Service SW	0	Normal mode	normal mode	
			1	Service mode		
	H STOP	H STOP	0	H OUT	H OUT	
			1	H STOP		
	AFC GAIN	AFC GAIN	0	NORMAL	NORMAL	
			1	HIGH		
	H fo ADJ	H to ADJ	0	Normal	Normal	
			1	fo down		
	SUB-POSITION	SUB-POSITION	0 0	normal mode	normal mode	
			0 1	upside mode		
1 0			downside mode			
1 1			normal mode			

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VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

DATA BYTE CONDITIONS AT D/A

	Functions	BIT	Data	Condition (change DATA 0-->MAX.)	Initial condition
IF	DELAY ADJ	6	0 to 63		0
	VCO ADJ	6	0 to 63		32
	AUDIO ATT	7	0 to 127	gain min.-->max	0
VIDEO	sharpness	6	0 to 63	soft-->sharp	32
	contrast cont	7	0 to 127	min.-->max	32
CHROMA	tint cont	7	0 to 127	-45deg-->+45deg	64
	color cont	7	0 to 127	gain min.-->max	32
INTERFACE	bright cont	7	0 to 127	dark-->bright	32
	drive (R)	6	0 to 63	gain min.-->max	32
	drive (B)	6	0 to 63	gain min.-->max	32
	cut off (R)	8	0 to 255	low-->high	0
	cut off (G)	8	0 to 255	low-->high	0
	cut off (B)	8	0 to 255	low-->high	0
	peak ACL ADJ.	4	0 to 15	low-->high	8
DEFLECTION	AFC-2 H phase	4	0 to 15	left-->right	8
	V-SIZE	6	0 to 63	min.-->max	32
	V-POSITION	5	0 to 31	low.-->high	24

DATA BYTE CONDITIONS AT READ MODE

	Function name	0	1
D7	Field frequency	50Hz	60Hz
D6	COINCIDENCE	unlocked	locked
D5	AFT1	see Fig. 1	
D4	AFT0		
D3	chroma fsc	4.43MHz	3.58MHz
D2	System1 (PAL/NTSC)	PAL	NTSC
D1	System0 (SECAM/Not SECAM)	not SECAM	SECAM
D0	SYSTEM auto: condition	undistin- guished	distinguished
	SYSTEM set: killer out	killer on	killer off

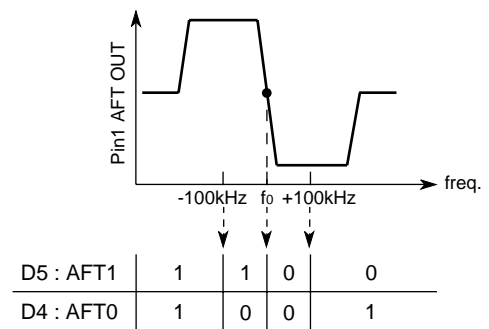
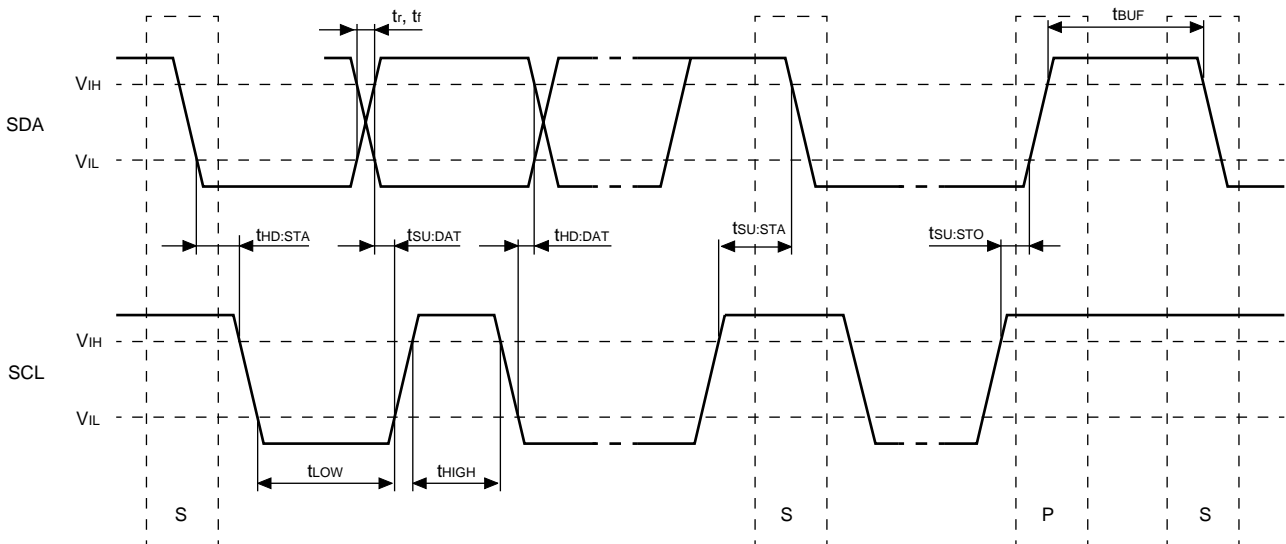


Fig.1

I²C BUS CONTROL SECTION SDA, SCL CHARACTERISTICS

Symbol	Parameter	Limits		Unit
		Min.	Max.	
V _{IL}	Min. input low voltage	-0.5	1.5	V
V _{IH}	Max. input high voltage	3.0	5.5	V
f _{SCL}	SCL clock frequency	0.0	100	kHz
t _{BUF}	Time the bus must be free before a new transmission can start	4.7	-	μs
t _{HD:STA}	Hold time start condition. After this period the first clock pulse is generated	4.0	-	μs
t _{LOW}	The low period of the clock	4.7	-	μs
t _{HIGH}	The high period of the clock	4.0	-	μs
t _{SU:STA}	Setup time for start condition (Only relevant for a repeated start condition)	4.7	-	μs
t _{HD:DAT}	Hold time DATA	0.0	-	μs
t _{SU:DAT}	Set-up time DATA	250	-	ns
t _r	Rise time of both SDA and SCL lines	-	1000	ns
t _f	Fall time of both SDA and SCL lines	-	300	ns
t _{SU:STO}	Set-up time for stop condition	4.0	-	μs

TIMING DIAGRAM



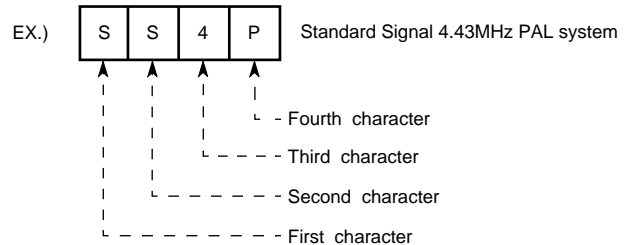
VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

**INPUT SIGNAL
VIF/SIF**

SG No.	Signals (50Ω termination)
1	f ₀ =38.9MHz 90dB _μ fm=20kHz AM77.8%
2	f ₀ =38.9MHz 90dB _μ fm=50kHz AM77.8%
3	f ₀ =38.9MHz 80dB _μ CW
4	f ₁ =38.9MHz 90dB _μ CW (Mixed signal) f ₂ =37±5MHz 70dB _μ CW (Mixed signal)
5	f ₀ =38.9MHz variable fm=20kHz AM77.8%
6	f ₀ =38.9MHz fm=20kHz AM16% level variable
7	f ₀ =38.9MHz 80dB _μ CW
8	f ₀ =38.9MHz 110dB _μ CW
9	f ₀ =38.9±5MHz 90dB _μ CW
10	f ₀ =37.9MHz 90dB _μ CW
11	f ₀ =39.9MHz 90dB _μ CW
12	f ₁ =38.9MHz 90dB _μ CW (Mixed signal) f ₂ =34.47MHz 80dB _μ CW (Mixed signal) f ₃ =33.4MHz 80dB _μ CW (Mixed signal)
13	f ₀ =38.9MHz standard 10-step modulation Sync ratio 28.6% AM=87.5%video modulation Sync chip level 90dB _μ
14	f ₀ =38.9MHz 93dB _μ CW
15	f ₀ =38.9MHz 73dB _μ CW
16	f ₀ =4.5MHz 100dB _μ fm=400Hz FM±25kHz dev
17	f ₀ =5.5MHz 100dB _μ fm=400Hz FM±50kHz dev
18	f ₀ =6.0MHz 100dB _μ fm=400Hz FM±50kHz dev
19	f ₀ =6.5MHz 100dB _μ fm=400Hz FM±50kHz dev
20	f ₀ =6.0MHz 100dB _μ fm=400Hz AM30%
21	f ₀ =6.0MHz 100dB _μ CW
22	f=1kHz 1V _{P-P} CW

**INPUT SIGNAL PARAMETERS INCLUDING
INPUT SIGNALS**

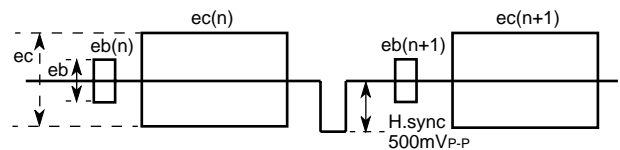
1. Input signal name is four alphanumeric characters.



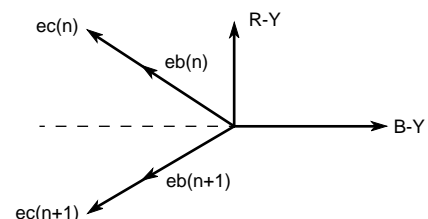
- First character: Standard=S, Nonstandard=V
(Modified parts should be specified.)
- Second character: Meaning of signal
- Third character: Frequency of burst and chroma.
4 (4.433619MHz), 3 (3.579545MHz)
(In case of "S", SECAM standard signal is applied.)
- Fourth character: Color system
N (NTSC), P (PAL)

2. Structure of input color signal

The following figure shows the structure of color signal.

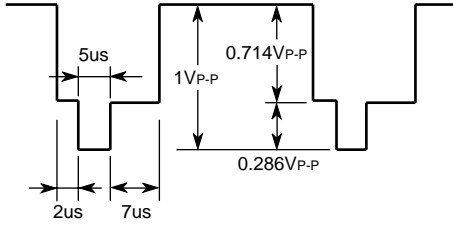
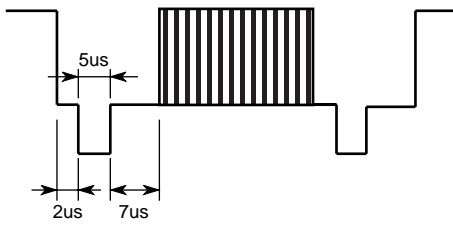
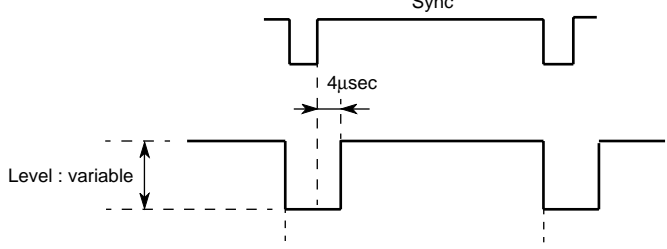
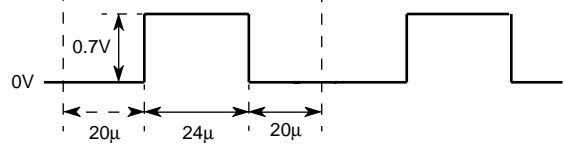
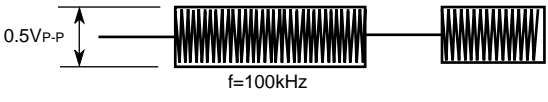

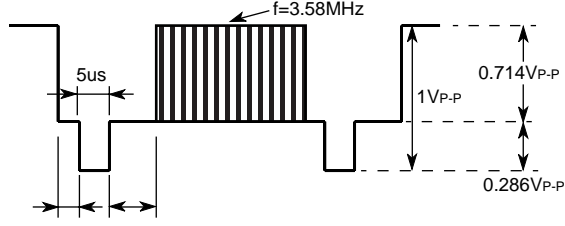
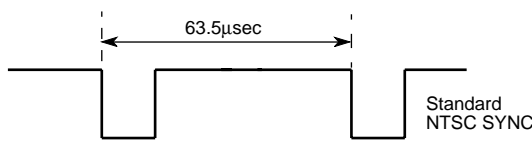


- 1) When S (standard) is used as the first character, the standard color bar signal of each system is applied. H.sync should be added for input clamp. (The frequency of H.sync is fixed according to the fourth character. P:50Hz, N:60Hz)
- 2) Amplitude and frequency of burst are represented as eb. In case of standard signal, the amplitude is 285mV_{P-P} and the frequency is shown by the third character.
- 3) Amplitude and frequency of chroma are represented as ec. In case of standard signal, the amplitude is 570mV_{P-P} and the frequency is shown by the third character.
- 4) The following figure shows the phase of a PAL system signal.



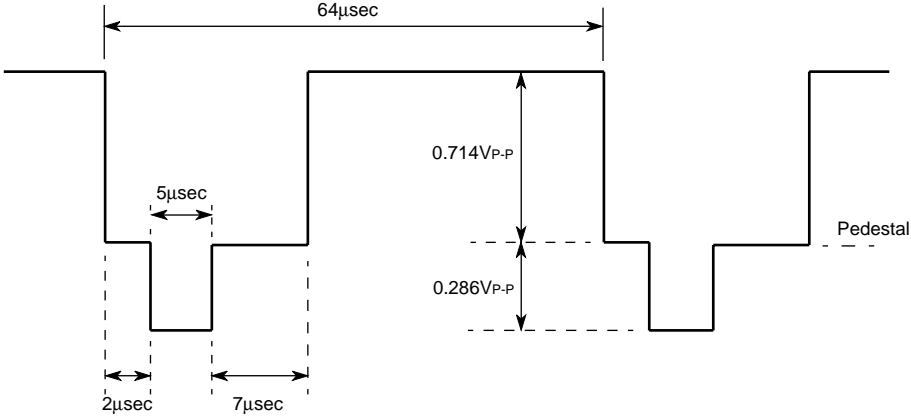
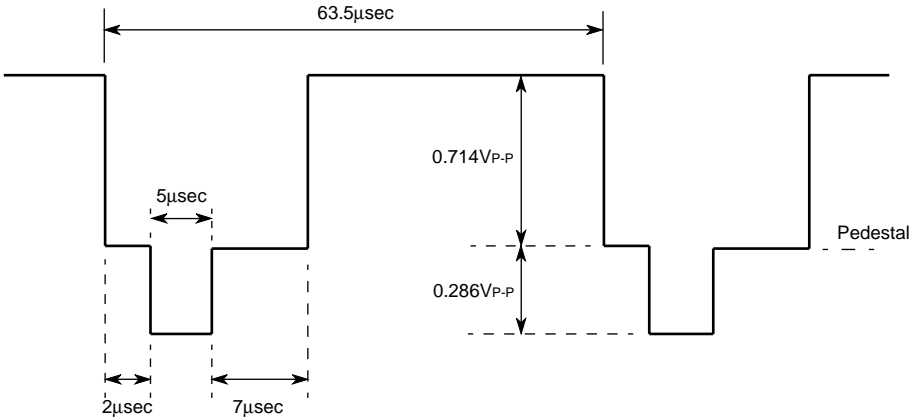

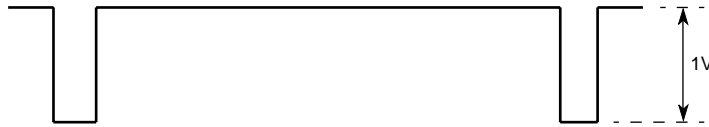
VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

VIDEO/INTERFACE

SG No.	Signal (50Ω termination)
SGA	<p>PAL system PAL system APL100% standard video signal should be input as sync separation input as shown in the figure. The vertical signal should be interlaced at 50Hz.</p> 
SGB	<p>The frequency and amplitude of signal Lumi can be changed by signal SGA. The typical amplitude is 0.714mVp-p.</p> 
SGC	
SGD	
SGE	
SG50	<p>Level : variable typ=0.3Vp-p H=15.625kHz, V=50Hz</p>  <p>Standard PAL SYNC</p>
SGF	
SG60	<p>NTSC System Level : variable typ=0.3Vp-p H=15.734kHz, V=60Hz</p>  <p>Standard NTSC SYNC</p>

VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

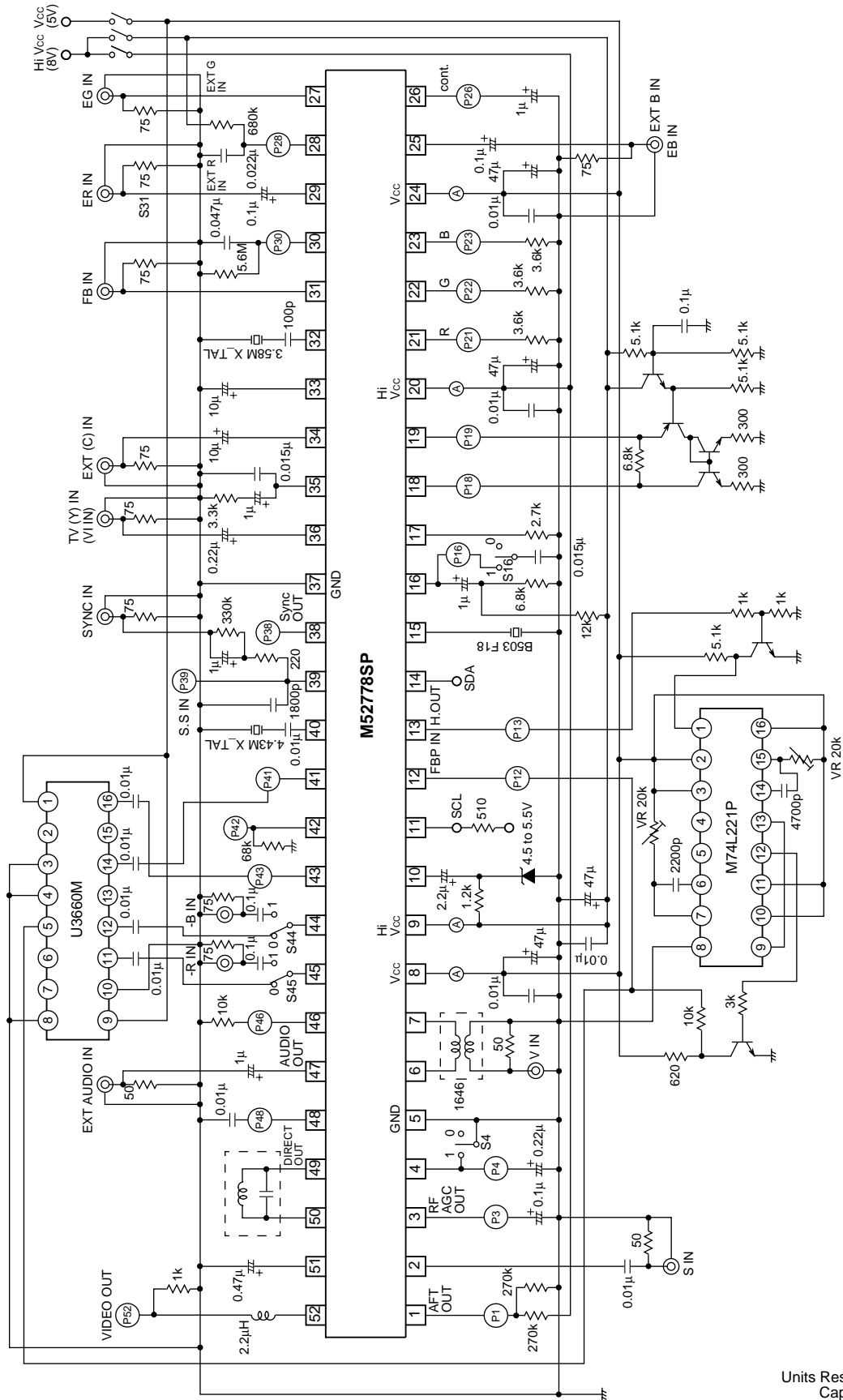
DEFLECTION

SG No.	Signal (50Ω termination)
SGa	<p>The input signal should be PAL system APL-variable video signal. Vertical should be interlaced at 50Hz.</p> 
SGb	<p>The input signal should be NTSC APL-variable video signal. Vertical should be interlaced at 60Hz.</p> 
SGc	<p>Duty90% Frequency:variable Level:variable (Typ. :1VP-P)</p> 
SGd	<p>Duty95% Frequency:variable Level:variable (Typ. :1VP-P) Duty: variable (95%)</p> 

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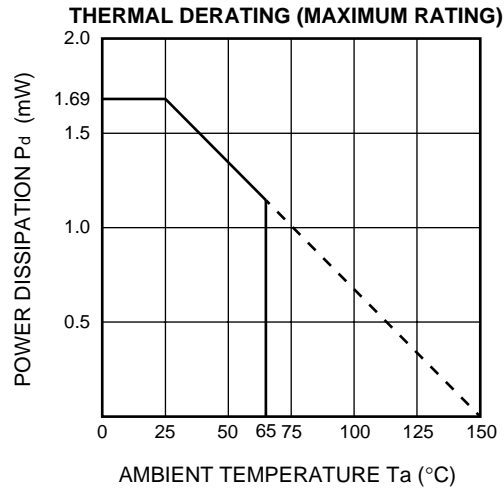
VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

TEST CIRCUIT



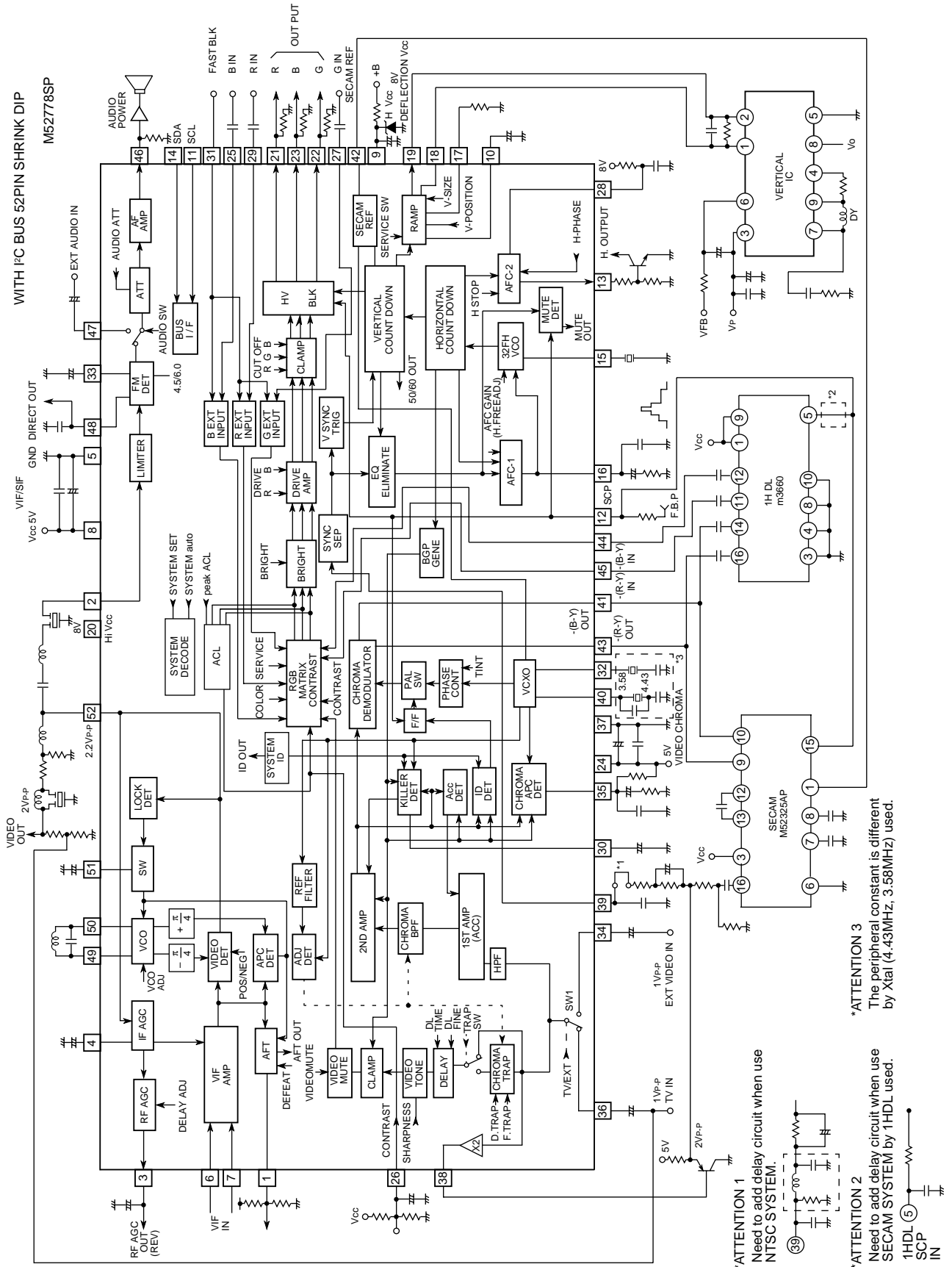
Units Resistance : Ω
Capacitance : F

TYPICAL CHARACTERISTICS

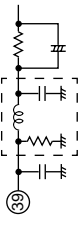


APPLICATION EXAMPLE

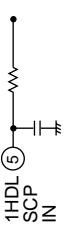
PAL/NTSC SYSTEM SINGLE-CHIP COLOR TV SIGNAL PROCESSOR



*ATTENTION 1
Need to add delay circuit when use NTSC SYSTEM.



*ATTENTION 2
Need to add delay circuit when use SECAM SYSTEM by 1HDL used.



*ATTENTION 3
The peripheral constant is different by Xtal(4.43MHz, 3.58MHz) used.

VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

DESCRIPTION OF PIN

Pin No.	Name	DC voltage and wave information	Peripheral circuit of pins	Description of function
1	AFT OUT	DC 0.2 to 7.7V (Charge and discharge current is 0.25mA max.)		<p>⟨AFT output pin⟩ This pin is current output. μ of PLL loop is adjustable by external resistor. External resistor value is 270k/270kΩ typ.</p>
2	LIMITER IN	FM signal input (AC coupled)		<p>⟨SIF detector input pin⟩ Standard input level is 100dBμ typ. input impedance is 4.7kΩ typ.</p>
3	RE AGC OUT	DC 0.1 to 7.8V		<p>⟨RF AGC output pin⟩ current output type. Charge and discharge current is 0.4mA max.</p>
4	IF AGC filter	DC 1.9 to 4.6V		<p>⟨IF AGC filter pin⟩ charge current POS : 1μA NEG : 10μA discharge current POS : 4mA NEG : 400μA</p>
5	GND	-	-	⟨ground pin of VIF block⟩

VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

DESCRIPTION OF PIN (cont.)

Pin No.	Name	DC voltage and wave information	Peripheral circuit of pins	Description of function
6 7	VIF IN	1.4V		<p>⟨VIF detector input pin⟩ input impedance is 900Ω, 5pF typ. pay attention to matching with SAW filter.</p>
8	VIF Vcc (5V)	5.0V	-	<p>⟨power supply for VIF block⟩ 5.0V typ.</p>
9	H Vcc (8V)	8.0V	-	<p>⟨power supply for DEFLECTION and VIF/ SIF output stage⟩ 8.0V typ.</p>
10	RAMP AGC	DC 3.4V typ (charge current is 9μA and discharge current is 170μA typ.)		<p>⟨vertical ramp AGC filter pin⟩ this pin is sensitive to current leakage. Pay attention to PCB layout and external components. Pulling up this pin to Vcc (8V) with R=47kΩ, pin 18 output is "V pulse" type.</p>
11	SCL	-		<p>⟨SCL pin for I²C BUS⟩ Vth=3V approx.</p>
12	SCP OUT			<p>⟨Sand castle pulse output pin⟩ four-level pulse output</p>

VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

DESCRIPTION OF PIN (cont.)

Pin No.	Name	DC voltage and wave information	Peripheral circuit of pins	Description of function
13	H OUT	<p>pin 12 $\approx 8\mu\text{s}$ 4.0V $25\mu\text{s}$</p>		<p>⟨Horizontal pre-drive output pin⟩ this pin is open emitter type. (output resistor is 200Ω) maximum drive current is 4mA typ.</p>
14	SDA	-		<p>⟨SDA pin of I²C BUS⟩</p>
15	H OSC	<p>DC2.45V</p> <p>0.3V_{P-P}</p>		<p>⟨horizontal oscillator pin⟩ connect with ceramic resonator for 32fH VCO. recommended resonator is " MURATA CSB503F18.</p>
16	AFC 1 FILTER	<p>0.3V_{P-P} $DC 5.3\text{V}$ during sync.</p>	<p>AFC gain H: 900µA AFC gain L: 500µA</p>	<p>⟨AFC-1 filter pin of 32fH VCO⟩ μ is 1.2kHz / V typ. charge and discharge current is; AFC gain H: 900µA AFC gain L : 500µA</p>

VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

DESCRIPTION OF PIN (cont.)

Pin No.	Name	DC voltage and wave information	Peripheral circuit of pins	Description of function
17	I REF	DC 2.5V		<p><Band gap reference output> this pin generates reference current for vertical ramp. external resistor needs tolerance within 1%, and is stable for temperature. resistor value is 2.7kΩ typ.</p>
18 19	+RAMP OUT -RAMP OUT	<p>bias current : 460uA current amplitude: 180uA P-P pin19 upside down (when BUS DATA of V size is 41.)</p>		<p><vertical ramp output pin> connects with vertical IC. external resistor needs tolerance within 1%, and is stable for temperature. resistor value is 6.8kΩ typ.</p>
20	H:Vcc (8V)	8.0V	-	<p><power supply for RGB interface output stage> 8.0V typ.</p>
21 22 23	R OUT G OUT B OUT			<p><RGB output pin> these pins are open emitter type. maximum output current is 4mA typ.</p>
24	VCD Vcc (5V)	5.0V	-	<p><power supply for VCD block> 5.0V typ.</p>
25 27 29	B IN G IN R IN	DC 2.5V		<p><external RGB input pin> input RGB signals with clamp capacitor. capacitor value is 0.1μF typ. charge and discharge current is 150μA typ.</p>

VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

DESCRIPTION OF PIN (cont.)

Pin No.	Name	DC voltage and wave information	Peripheral circuit of pins	Description of function
26	CONTRAST CONT	-		<p>⟨filter pin for PEAK ACL detection⟩ value of R1, R2, R3 set average ACL. the ratio of R1:R2=3:7 time constant is given by $(R1 \cdot R2)/(R1+R2)$ and C.</p>
28	AFC2 FILTER	DC 4.5V		<p>⟨AFC2 filter pin⟩ connect with hold capacitor, and can control the horizontal sync. signal phase. hold capacitor value can change the response speed of horizontal phase shift.</p>
30	KILLER FILTER	DC		3.7V
31	FAST BLK			0
32	X-TAL 3.58	<p>DC 3.2V</p>		
33	AUDIO BYPASS	<p>DC</p> <p>4.5MHz:2.3V 5.5MHz:2.3V 6.0MHz:2.6V 6.5MHz:3.0V</p>		


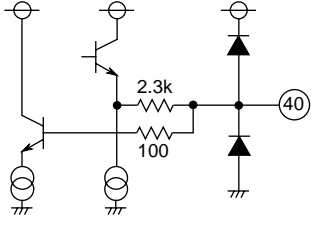
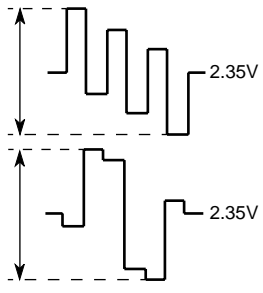
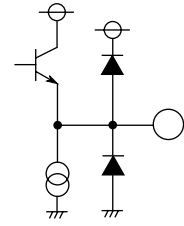
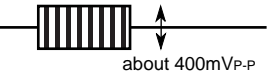
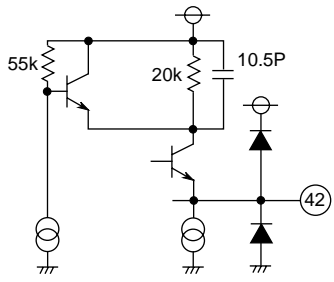
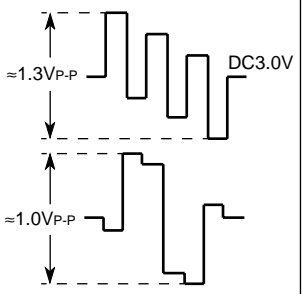
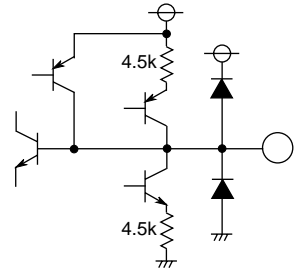
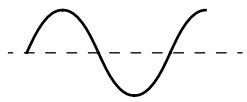
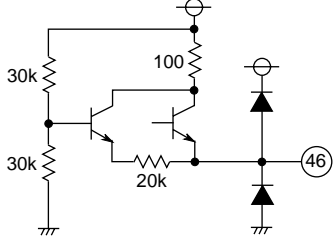
VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

DESCRIPTION OF PIN (cont.)

Pin No.	Name	DC voltage and wave information	Peripheral circuit of pins	Description of function
34	EXT IN	DC 1.95V composite video 1V _{P-P} typ.		
35	CHROMA APC FILTER	DC 3V typ.		
36	TV IN	DC 1.95V composite video 1V _{P-P} typ.		
37	VCD GND		-	
38	Y SW OUT	sync tip: 1.3V composite video: 2V _{P-P}		
39	SYNC SEP IN			

VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

DESCRIPTION OF PIN (cont.)

Pin No.	Name	DC voltage and wave information	Peripheral circuit of pins	Description of function
40	X-TAL 4.43	DC 3.3V  70mVp-P		
41 43	- (B-Y) OUT - (R-Y) OUT	 2.35V 2.35V		
42	SECAM REF	PAL/NTSC:1.4V SECAM:4V  about 400mVp-P		
44 45	- (B-Y) IN - (R-Y) IN	 ≈1.3Vp-P DC3.0V ≈1.0Vp-P		3.0V
46	AUDIO OUT	DC:2.8V MAX 4.1Vp-P  DC:2.8V MAX 4.1Vp-P		

VIF, SIF, VIDEO, CHROMA, DEFLECTION FOR PAL/NTSC

DESCRIPTION OF PIN (cont.)

Pin No.	Name	DC voltage and wave information	Peripheral circuit of pins	Description of function
47	EXT AUDIO IN	-		
48	FM DIRECT OUT	DC:2.4V NTSC:740Vrms PAL:690Vrms 		
49 50	VCO	DC:4.2V 38.9MHz 0.285V _{P-P} or 100dB _μ 		
51	VIDEO APC FILTER	DC:3.0V at VCO free-run		
52	VIDEO OUT	NEG --- 4.5V --- 2.3V POS --- 4.4V --- 2.6V 		

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