ST7FLITE1B 8-bit MCU

By P. Oteri
ST7 Microcontrollers

COST EFFECTIVE MICROCONTROLLER SERIES FOR ROBUST DESIGN IN SMALL APPLIANCES

The general purpose ST7FLITE1B microcontrollers, available with 2kB /4kB flash memory and 128 byte data EEPROM, are top runners of the ST7FLITE family. They are already in production in SO-20 / DIP-20 and SO-16 / DIP-16 and 20 lead QFN5x5.

The ST7FLITE1B introduce a fast analog comparator and an enhanced 12-bit auto-reload timer, marking a significant step forward in lighting and control functionality for real-time embedded system and motor control applications.

What's New in the ST7FLITE1B

The analog comparator with 16 internal or external voltage references has been added to enlarge the rich set of peripherals already available in the LITE family. This flexible embedded comparator allows an increase in system integration, design cost and control or protection algorithms. In fact, in power applications it is common to provide system protection through an external comparator.

The 12-bit timer offers four independent PWM (Pulse Width Modulated) output channels with programmable dead time generation, intended for use in half-bridge driving mode especially for lighting applications, where PWM signals must not overlap. To better address these applications, two new features have been added: 32MHz PLL and the enhanced one-pulse mode functionality, providing more flexibility to peripheral usage.

Development Tools

The ST7FLIT1B series is supported by a complete set of hardware and software development aids from ST. These include low cost programming tools, realtime emulators and a free of charge IDE (STVD7). Low cost third party development kits such as ST7FLITE-SK/RAIS from Raisonance® are also available. These tools easily integrate the free of charge 16k ANSI-C compiler from Cosmic® (http://www.comicsoftware.com) and are compatible with ST7 Software Library.

Part number	Flash	EEPROM	Package
ST7FLIT10BF0M6	2k		SO-20
ST7FLIT10BF0B6	2k		DIP-20
ST7FLIT15BF0M6	2k		SO-20
ST7FLIT15BF0B6	2k		DIP-20
ST7FLIT19BF0M6	2k	128	SO-20
ST7FLIT19BF0B6	2k	128	DIP-20
ST7FLIT10BY0M6	2k		SO-16
ST7FLIT10BY0B6	2k		DIP-16
ST7FLIT15BY0M6	2k		SO-16
ST7FLIT15BY0B6	2k		DIP-16
ST7FLIT19BY0M6	2k	128	SO-16
ST7FLIT19BY0B6	2k	128	DIP-16
ST7FLIT10BF1M6	4k		SO-20
ST7FLIT10BF1B6	4k		DIP-20
ST7FLIT15BF1M6	4k		SO-20
ST7FLIT15BF1B6	4k		DIP-20
ST7FLIT19BF1M6	4k	128	SO-20
ST7FLIT19BF1B6	4k	128	DIP-20
ST7FLIT10BY1M6	4k		SO-16
ST7FLIT10BY1B6	4k		DIP-16
ST7FLIT15BY1M6	4k		SO-16
ST7FLIT15BY1B6	4k		DIP-16
ST7FLIT19BY1M6	4k	128	SO-16
ST7FLIT19BY1B6	4k	128	DIP-16

ST7FLITE1B commercial products

Typical Applications

The rich set of peripherals cover several power applications such as: high intensity discharge lamps used for street lighting and shops, and digital ballasts for fluorescent tubes where electrical stress to the cathode during the startup phase is avoided. Thanks to the availability of multiple PWM outputs and fast analog to digital converter, also multicolor LED driving or LCD backlight display driver applications are addressable.

ST7SCR Series

By L. Rabiej
8-bit Microcontrollers Marketing

SINGLE CHIP SOLUTION FOR ALL TYPES OF SMART CARD READERS

The ST7SCR series is part of ST's Application Specific Standard Microcontrollers (ASSMs) product portfolio. They target PC-linked readers and terminal applications of the smart card reader market.

ST7SCR Block Functionalities

ST has developed a single-chip solution embedding all the necessary functional blocks in typical readers and terminal architectures. Based on industry standard ST7 core with either ROM or FLASH 16K bytes memory, interrupt function and LED drivers are also integrated. A full speed USB interface allows communication with a host computer. EMV certification blocks, i.e. IS07816 UART interface and power supply unit, control the communication with the smart card.

Key Features

- USB 2.0 12Mbps full speed CCID (chip card interface device) compliance
- EMV compliant 1.8/3/5V selectable power supply unit
- ISO7816 compliant UART serial bus
- Fully integrated LED drivers
- 4kV on-chip ESD protection on smartcard I/Os
- Packaged in TQFP, SO, QFN or die form

24 lead SO and QFN versions offer small footprints whereas the TQFP64 lead version provides more I/Os and functionalities for full keyboard management.

ST7SCR Commercial Products

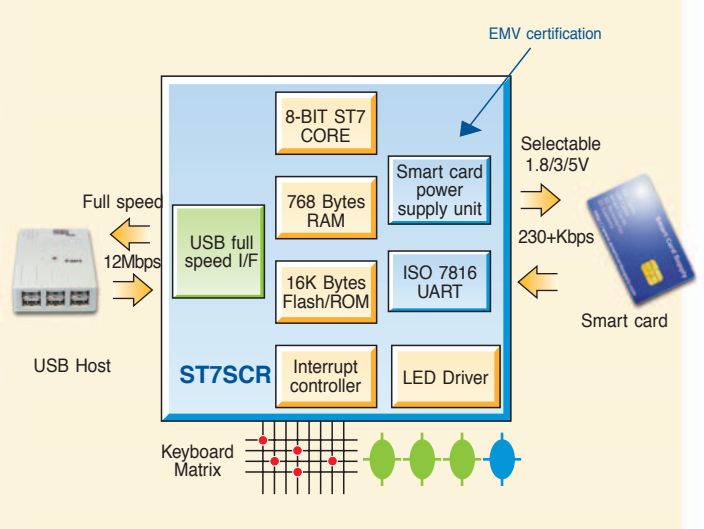
Part number	Memory	I/O	Package
ST7SCR1E4	16K Flash	4	SO-24
ST7SCR1R4	16K Flash	35	TQFP64
ST7SCR/XXX	16K ROM	4 or 35	SO-24 TQFP64 QFN24*

* under qualification

Target Applications

The ST7SCR series has been initially specified and developed for PC-linked reader applications and industry leaders like Gemplus, and others have selected ST solutions for stand-alone and keyboard-integrated

readers. However, smart cards technology proliferation and standardization now offer new target markets. Among the most promising are the emergence of USB pocket readers for e-banking, security tokens and personal secure data.



ST7SCR internal block diagram

ROM vs FLASH Memory

Flash memory architecture offers flexibility during the development phase. A Flash version is usually the customers' choice until production phase and/or pre-series volumes. ROM memory architecture offers die size optimization once customer codes are frozen and ready for full production volumes. A customer specific commercial product (…/XXX) is codified and adequate masks sets are used during manufacturing.

µPSD3400 8-bit MCU

By B. Hahn
Advanced MCUs

HIGH PERFORMANCE 32KB SRAM, 8-BIT MCU PROVIDES USB 2.0 FULL-SPEED, PLD AND JTAG DEBUG

The new µPSD3454 8051-based MCU integrates a market-leading 32KB of SRAM and 256KB of Flash memory, together with USB 2.0 full-speed and a range of other interfaces and peripherals. The µPSD family now offers the same memory densities across all three series, providing a performance upgrade path for existing users, as well as one of the most competitive and versatile 8051-based solutions for new embedded control applications.

The 32KB of on-chip SRAM provides ample storage space for data buffering, or to handle the extra stacks required by a Real Time Operating System (RTOS).

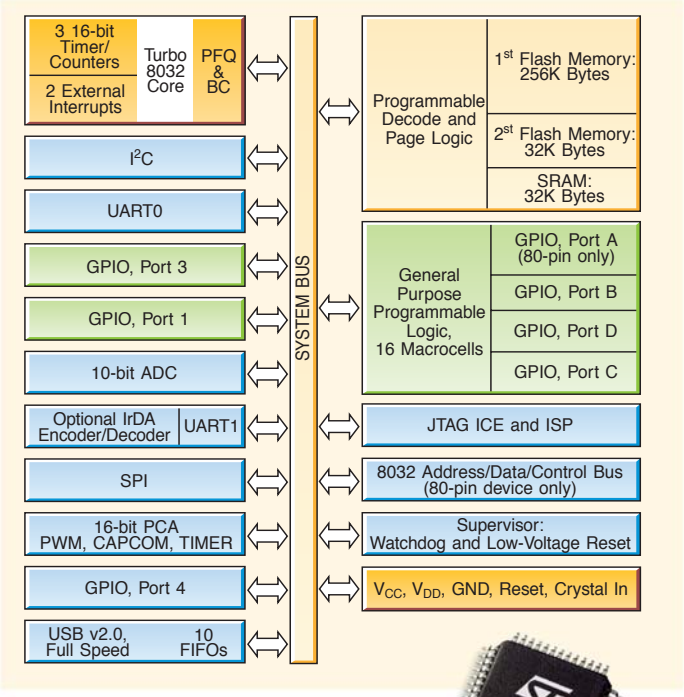
µPSD3400 Turbo Plus Overview

The core of the µPSD3400 Turbo Plus series is a 4-cycle-per-instruction 40-MHz 8032 MCU. The high-performance core is further enhanced by the addition of an internal 16-bit path that allows 2-byte instructions to be fetched in a single memory cycle. The wider path coupled with a pre-fetch queue and branch cache brings average performance to 9 MIPS, with peak performance at 10 MIPS.

A JTAG interface supports in-system programming and MCU core debug with high speed instruction tracing capability, eliminating the need for a hardware In-Circuit Emulator (ICE). Inexpensive and easy-to-use development tools from both ST and from third parties make it easy to implement new projects.

Typical Applications

The µPSD3400 Turbo Plus series is suitable for a wide range of embedded applications, such as Point Of Sale (POS) peripherals, vending machines, security and building controls, RFID readers, data acquisition systems and telecommunication products.



µPSD3400 series block diagram

Key Features

- USB 2.0 full-speed (12Mbps)
- Up to 288KB dual-bank flash memory for in-application programming and EEPROM emulation
- Up to 32KB SRAM with battery backup
- On-chip JTAG debug eliminates the need for a separate hardware in-circuit emulator
- Fast 16-bit wide internal instruction path
- On-chip programmable logic
- JTAG ISP eliminates the need for sockets and pre-programmed memory and logic devices
- Enhanced programmable counter array
- I²C, UART (x2), SPI and IrDA interfaces
- 8-ch, 10-bit ADC
- Supervisory functions

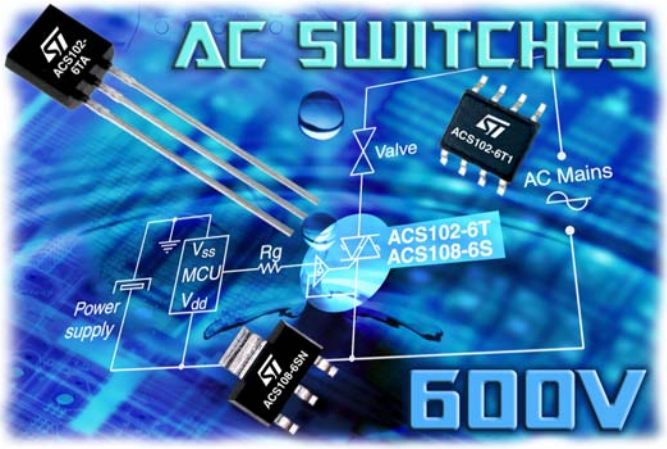
µPSD3400 Series Product Matrix

Part number	Main Flash	2nd Flash	SRAM	GPIO	Voltage	Package
UPSD3422EV	64KB	32KB	4KB	36 / 45	3.0 to 3.6	TQFP52 / TQFP80
UPSD3422E					4.5 to 5.5	
UPSD3433EV	128KB	32KB	8KB	36 / 45	3.0 to 3.6	TQFP52 / TQFP80
UPSD3433E					4.5 to 5.5	
UPSD3434EV	256KB	32KB	8KB	36 / 45	3.0 to 3.6	TQFP52 / TQFP80
UPSD3434E					4.5 to 5.5	
UPSD3454EV	256KB	32KB	32KB	36 / 45	3.0 to 3.6	TQFP52 / TQFP80
UPSD3454E					4.5 to 5.5	

ACS102-6Tx & ACS108-6Sx

By B. Cheron
ASD & IPAD Product Marketing

NEW 600V AC SWITCHES FOR HIGHER CAPABILITY



The home appliance industry is shifting to electronic control on a worldwide basis. Along with this trend, electronics can now handle the AC mains constraints where high voltage robustness and transient voltage compatibility are the key challenges. ACSs have been designed to control the numerous AC loads necessary for the appliance process. These ACSs meet the requirements for reliability, compactness, and mass production capability. The new generation of 600V rated ACSs ensure overall system reliability and efficiency, and can be directly controlled by a microcontroller.

ACS108-6Sx and ACS102-6Tx Profile

ACS and ACST devices are now well known in the appliance world. The development of new products dedicated to specific loads provides global kits to the designer who wants to provide robustness, immunity and new functions in systems. In parallel with the new device developments, the current versions of ACSs are re-designed to benefit from the continuous improvements in the technology.

The well known ACS102-5Tx and ACS108-5Sx have been re-designed to improve the overall electrical performance of these high reliability switches. The new versions are ACS102-6Tx and ACS108-6Sx. The voltage capability (V_{DRM}/V_{RRM}) has been increased from 500V to 600V. Therefore the crowbar structure starts to protect the system at a higher voltage level than the previous version, and the robustness has been re-qualified because the higher crowbar threshold voltage causes a higher energy than the switch must sustain.

The static characteristics have also been improved. The latching and holding levels have been drastically reduced (50% of the previous version), allowing a more optimized gate pulse control mode, especially in case of lower power rated loads, thus helping to save energy. The dynamic characteristics also show enhanced performance. The switching capabilities and the electrical noise immunity have been improved by about 15%. This new performance gives a higher guard margin in case of specific load control.

1A Sensitive Standard Triac

Symbol	Test conditions	Quadrant		Sensitivity 03	07	09	10	Unit
I_{GT}(1)	V_D=12V R_L=30Ω	I-II-III-IV	Max.	3 5	5 7	10 10	25 25	mA
dV/dt(2)	V_D=67% V_{DRM} gate open	T_J = 110°C	Min.	10	20	50	100	V/µs

Old ACS108 500V version (I_{GT} = 10mA)

Symbol	Test conditions			Values	Unit
I_{GT}	V_{OUT}= 12V R_L=140Ω	T_J = 25°C	Max.	10	mA
dV/dt	V_{OUT} = 400V gate open	T_J = 110°C	Min.	500	V/µs

New ACS108 600V version (I_{GT} = 10mA)

Symbol	Test conditions	Quadrant		Values	Unit
I_{GT}(1)	V_{OUT}= 12V R_L= 33Ω	II - III	Max.	10	mA
dV/dt(2)	V_{OUT} = 67% V_{DRM} gate open	T_J = 125°C	Min.	500	V/µs

10 times better

+15% higher capability

New ACS 600V Benefits

- Required external protection snubber or varistor
- Overvoltage crowbar technology
- Enables equipment to meet IEC 61000-4-5
- Reduces component count by up to 80%
- Interfaces directly with the microcontroller
- Common package tab connection allows connection of several ACSs on the same cooling pad

New ACS 600V Main Features

Parameters	ACS102-6Tx	ACS108-6Sx
Current capability $I_{T(RMS)}$	0.2A	0.8A
Voltage capability V_{DRM}/V_{RRM}	600	600
Holding current	20mA	25mA
Latching level	25mA	30mA
High sensitivity (I_{GT} max.)	5mA	10mA
High noise immunity	300V/µs	500V/µs

PCLT-2A Sensor Termination

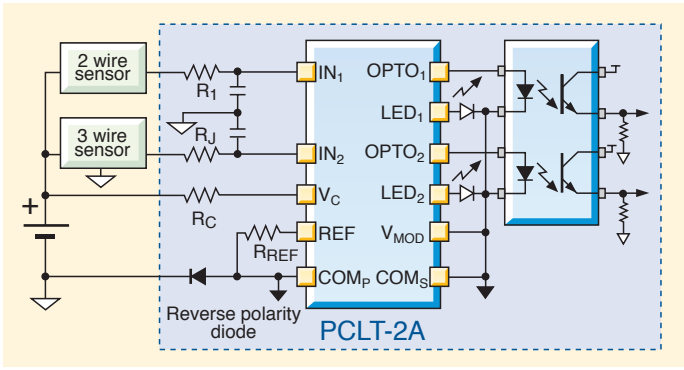
By T. Castagnet and M. Boulin
ASD & IPAD

SENSOR INPUT TERMINATION FOR INDUSTRIAL AUTOMATION I/O MODULES

Industrial automation is demanding more computing power, smaller size and less consumption. In distributed and PLC I/O modules this has led to the emergence of low dissipative and EMI proof input terminations. ST is responding to this demand by extending its CLT family with a new device, the PCLT.

PCLT Main Features

- Dual input channel
- Robust and EMC
  - IEC61000-4-4: 4kV fast transient burst
  - IEC61000-4-5: 0.5 to 1kV surge voltage
  - IEC61000-4-2: 15kV air ESD
- Wide range of operation
  - -30V to 35V input voltage (R_I = 750Ω)
  - -0.3V to 35V supply voltage (R_C = 2.2kΩ)
  - -25 to 85°C ambient temperature
- Exposed pad TSSOP14
  - $R_{TH\ JA}$ < 120°C/W
- Flexible current limiter
  - Programmable input current limiter from 3mA to 7.5mA
  - Narrow spread of limitation < 18%
- Output drive
  - Outputs disabled for I_{IN} < 2mA
  - Visual sensor status by LED
  - 3.3V to 12V CMOS compatible output option



Isolated PCLT in a PLC application

Flexible Solution for IEC61131-2 Digital Input

The PCLT-2A is a dual termination device for the front-end of a 24V DC digital input module.

Made up of an input voltage protection, a serial current limiter circuit and an output driver, each channel circuit

terminates the connection between a high-side proximity sensor and the I/O module.

The input clamping device protects the module against electromagnetic interference as described in the IEC61000-4-x standard: ESD, fast transient bursts and voltage surges.

An external resistance R_{REF} allows the current limiter to be programmed for the type 2 (7.5mA), type 3 and 1 (2.5mA) characteristic as described in the IEC61131-2 standard.

The output circuit transfers the input sensor logic state to the output and a light emitting diode. In ON state (V_I > 11V), both output and LED drivers share the input current, respectively 30% and 60%.

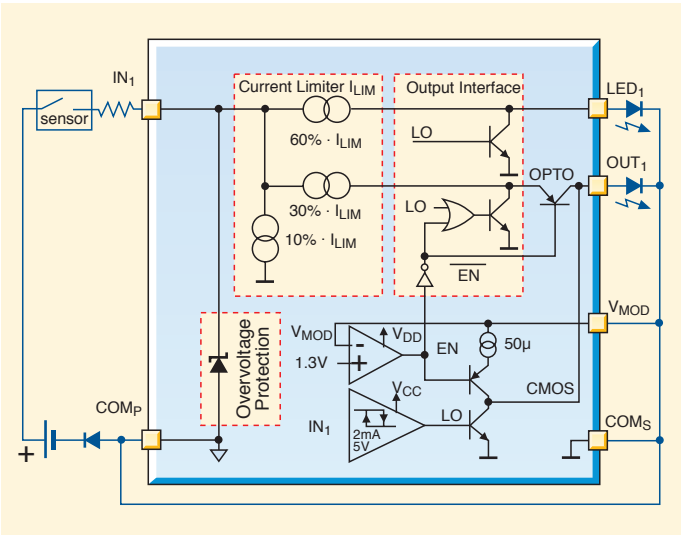


Diagram of one PCLT-2A channel with its over voltage and current limiter

Thanks to its pin MOD, the PCLT output can run either as an opto-coupler driver or as a CMOS driving buffer for 3.3V to 12V non-isolated designs. When the input current is less than 2mA, the output circuits shunt all current and maintain both LED and output in OFF state.

Benefits

- Reduced dissipation
  - 45% to 60% in the whole chain
  - 36% to 67% in the CLT module
- Compact SMD module
- Flexible logic input solution
  - Selectable input type 1, 2, 3
  - CMOS or photo-transistor output drive
- Higher reliability
  - Over-voltage and EMI robust
  - Limitation of current and dissipation
  - Reverse input polarity
- Enhanced operation
  - LED gives true logic sensors state
- Insensitive to load and power supply

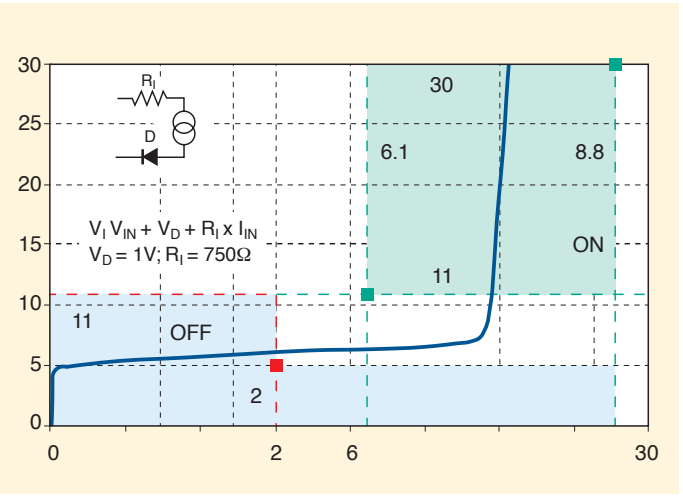
IEC 61131-2		Input type		
Setting	Unit	1	3	2
R_{REF}	kΩ	22	22	10
R_I	kΩ	2.2	1.2	0.75
Performance				
I_{IN} Min	mA	3	3	6.1
I_{IN}	mA	3.6	3.6	7.5
I_{IN} Max	mA	4.2	4.2	8.8
I_{LED}	mA	1.9	1.9	4
Application Surge	kV	1.5	1	0.5
Application ESD	kV	15 air; 8 contact (class 4)		

PCLT-2A resistance setting

Robust, Low Dissipation Type 2 Digital Input

Because of its IEC type programmability and the isolated/non-isolated output options, the PCLT offers a flexible and easy to design solution for highly integrated I/O modules.

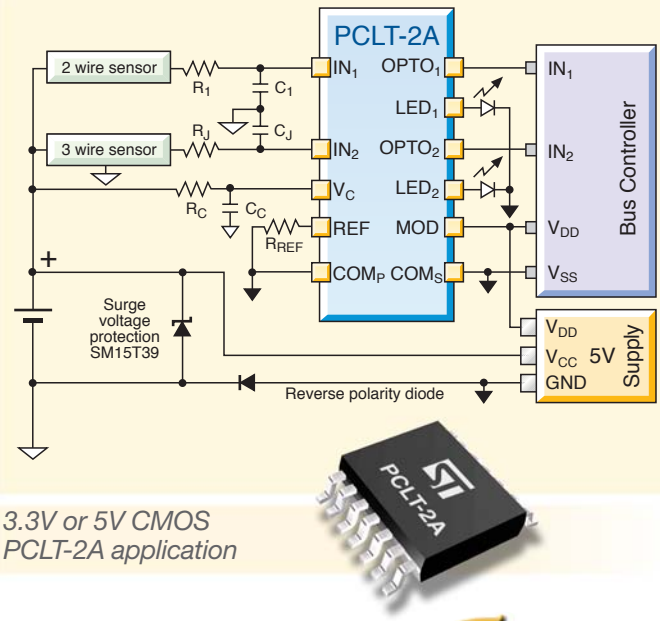
Type 2 digital inputs were not popular due to their high losses and their poor EMI robustness. The PCLT addresses this challenge successfully because it divides the input losses by three (~0.2W per channel), while improving its EMI robustness levels up to 15kV ESD and 4kV fast transient bursts.



PCLT-2A based IEC61131-2 type 2 input

Conclusion

The PCLT sensor termination has been designed for I/O modules in factory automation. Its flexibility allows designers to develop a large variety of input types in isolated and non-isolated versions. With its robust protection and its current limiter, it is a low-loss EMI-proof solution for highly integrated module interfacing with proximity sensors.



3.3V or 5V CMOS PCLT-2A application

DVIULC6-4SC6

By S. Caron
ASD & IPAD Product Marketing

DVI PORT PROTECTION AGAINST ESD STRIKES FOR COMPUTER & CONSUMER ELECTRONIC DEVICES

With data serialization and higher bit rates, the next computer and consumer generations require new features like high levels of protection from electrostatic discharge (ESD) and consistently ultra low line capacitance. The Digital Video Interface (DVI) uses small CMOS transmitters and receivers susceptible to ESD. The integrity of the high speed digital signals presents a significant challenge when selecting the appropriate protection device.

ST is expanding its protection diode array portfolio with DVIULC6-4SC6, its first ultra low capacitance ESD protection device. This product completes the low capacitance USBLC product family.

What is DVI?

DVI stands for Digital Video Interface. It is the means of connecting a display and computer system using a serial data link with speeds up to 1.65Gb/s.

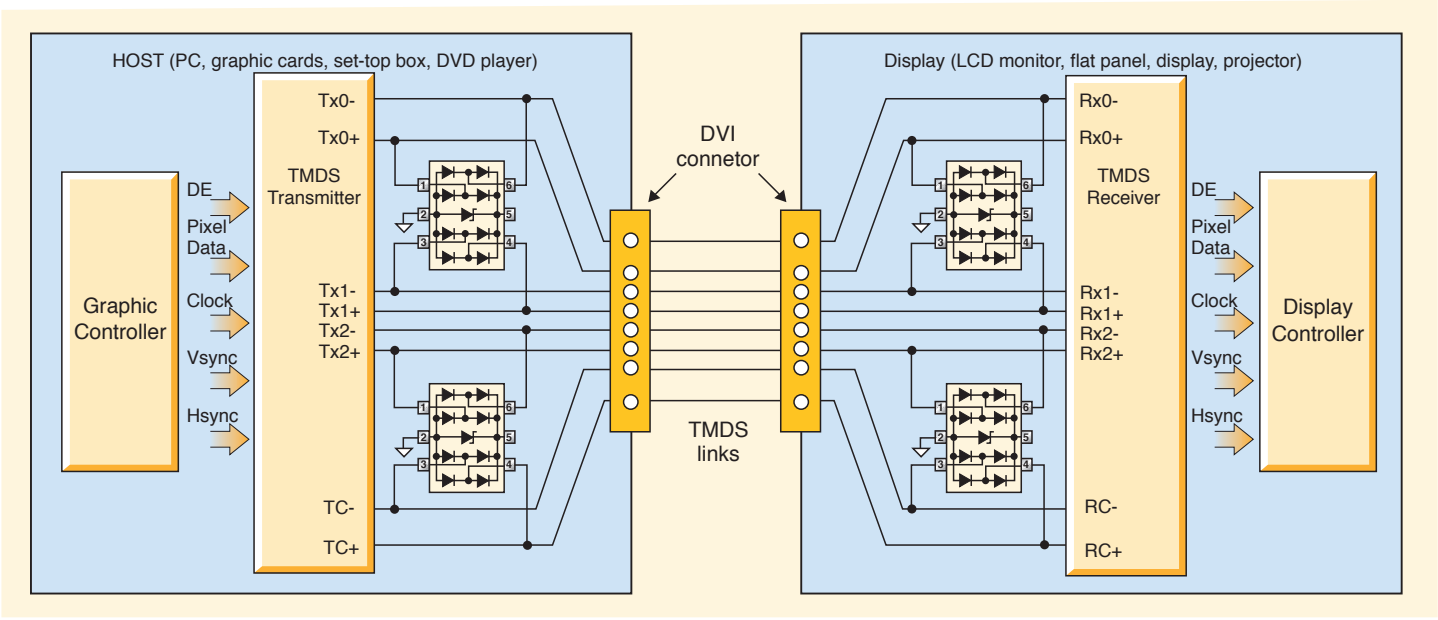
DVIULC6-4SC6 Technical Details

Parameters	Value	Unit
Transil breakdown voltage @ 1mA	> 6	V
Capacitance I/O to GND	0.6	pF
Capacitance variation I/O to GND	0.015	pF
Capacitance I/O to I/O	0.3	pF
Capacitance variation I/O to I/O	0.07	pF
Leakage current @ 5V	< 0.5	µA

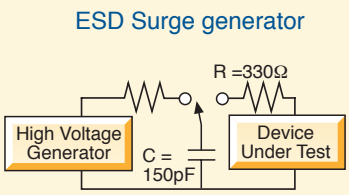
DVI Application Requirements

All pins of the DVIULC6-4SC6 comply with the most stringent ESD standards, 330Ω resistor IEC61000-4-2 level 4.

This means the device must withstand over 15kV when discharging a 150pF capacitor through a 330Ω resistor. Rigorous testing of the DVIULC6-4SC6 has shown that the device withstands considerably higher levels of discharge than that required by the standard.



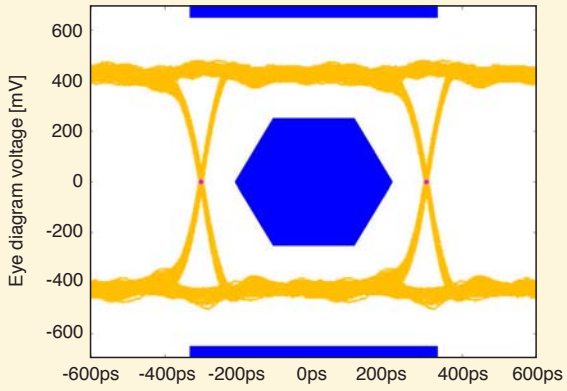
Topology of DVI protection against ESD



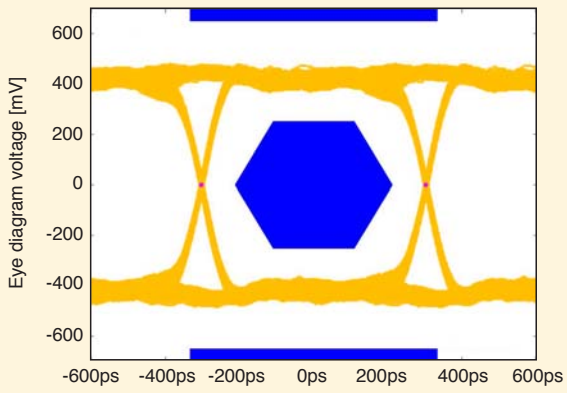
Contact discharge		Air discharge	
Level	Test voltage kV	Level	Test voltage kV
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15

IEC 61000-4-2 standard class 4

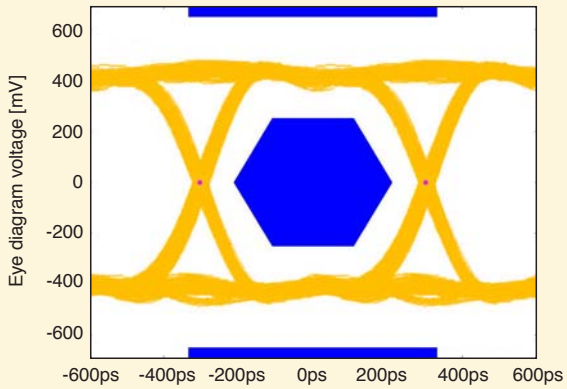
The DVIULC6-4SC6 provides a 5.5GHz cut-off frequency and a 0.6pF line capacitance, fulfilling all DVI port design requirements, such as rise time, as well as differential capacitance balance and data signal integrity. The device provides the security of protection transparent to the performance of the link. With such an ultra-low line capacitance, the DVIULC6-4SC6 is ready for the next generation of high speed digital signals supporting rates of up to 3.2Gb/s.



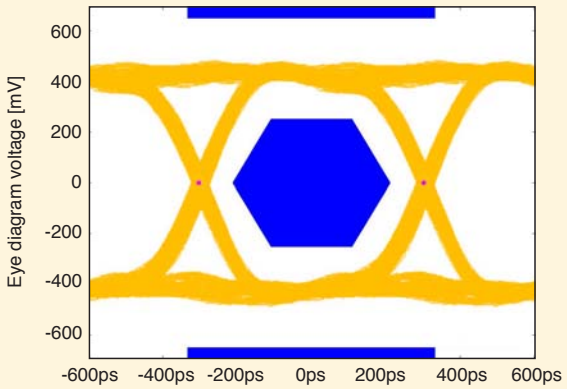
1.65Gb/s standalone board



1.65Gb/s with DVIULC6-4SC6 15kV ESD protection



3.2Gb/s standalone board



3.2Gb/s with DVIULC6-4SC6 15kV ESD protection

DVIULC6-4SC6 Key Benefits and Advantages

- The DVIULC6-4SC6 provides the best trade-off in protection/performance for high speed series data lines of up to 3.2Gb/s. It offers data integrity, balanced signal, low leakage current with unbeatable protection from the most stringent electrostatic discharges.
- The standard SOT-23 package offers simplicity in design and implementation of DVI circuits.

The DVIULC6-4SC6 is released as a market pioneer in ESD protection.
With the proliferation of data serialization and higher and higher bit rates, ST is expanding its innovative "Ultra Low Capacitance" ESD protection portfolio in addressing emerging sockets as HDMI and eSATA.

SMP100MC HV & ESDALC-2BP5

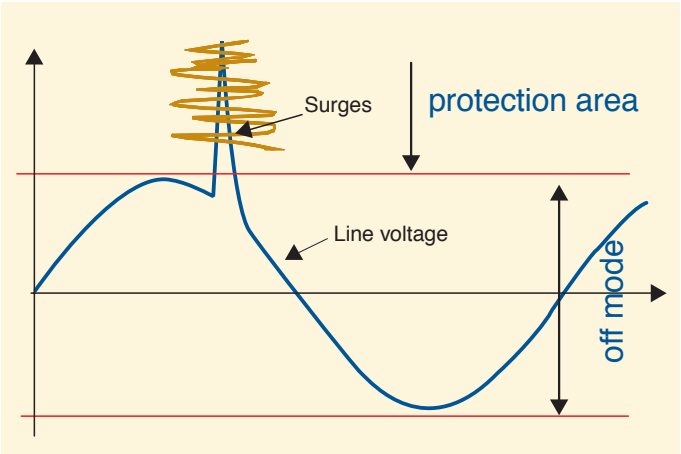
By P. Rabier
ASD & IPAD Product Marketing

ADSL2+ AND VDSL MODEM PROTECTION COMBINATION

ADSL baud rate is increasing and imposing shorter and shorter telecommunication lines to avoid distorsion and errors due to parastic elements such as line resistances and capacitances.
This requires more remote central offices (RCO) nearer customer premises instead of single large central offices. Reliability is becoming a critical issue to avoid sending technical staff to fix RCOs. In the mean-time the race to lower capacitances is far from over.

Basic Protection Requirements

Protection devices must comply with various surge standards that simulate lightning and power faults. Compliance with standards such as ITU-T-K20/21, TIA/EIA-IS-968 or UL6095 is essential, but fully protected error-free data transmission is the real objective.



Protection area in case of surges on the line

High Voltage Trisil Advantage

In the field the risk of power faults with 120V, 220V or 240V is much higher than 600V (requested by some standards). The use of Trisils having breakdown voltages higher than peak line voltages avoids blown fuses if the surge duration is too long. In this case the primary of the line transformer and the capacitance must withstand over-current for long periods.

Micro Capacitance Advantage

When transmitting data at 25Mb/s, minimized capacitance is critical to avoid bit error rate (BER). The MC technology provides a 33% capacitance reduction (typically 40pF instead of 60pF for a 270V Trisil). The combination of the high voltage technology with the micro-capacitance one is another step towards lowering capacitance values.

Capacitance Comparison With SMP100LC-270

Parameters	Capacitance	
	C @ 2V	C @ 50V
SMP100LC-270	**60**	**30**
SMP100MC-270	40	20
SMP100MC-320	35	15
SMP100MC-360	35	15
SMP100MC-400	**30**	**15**

Using a 400V device allows the capacitance to be divided by two. SMP100MC-360 and 400 have the lowest capacitance in the market. These Trisil devices located before the transformer are generally the first step in the protection design.

Protection on 2ndry Side of the Transformer

Whatever the protection before the transformer, silicon device or gas tube discharge, spikes appear after the transformer. The reason is easy to understand: when the Trisil is fired with a high di/dt through the primary winding of the transformer and the capacitance, the secondary winding generates a spike which must be clamped to avoid problems on DSL line drivers. Furthermore the faster the transmission, the more sensitive the line drivers are.

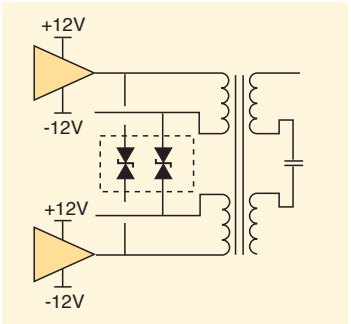
Up to now this protection used a discrete Transil (SMAJ type) but the high capacitance of such a diode makes it unsuitable for high bandwidth applications. Another possibility was the use of small Metal Oxide Varistors (MOV) which provide lower capacitances (around 50pF). This is close to the maximum limit but may be problematic in some topologies. An advantage of the MOV is the surge capability, but its capacitance reduction also reduces that capability, and the clamping voltage is quite often too high to safely protect the line drivers.
Some basic bipolar diodes like BAV99 have been tested but, as these devices were not designed to withstand surges, forward voltage peak may be too high and then voltage on the line will be equal to V_{DD} +V_{fp}. Sensitive line drivers will be damaged. Furthermore, with rail to rail protection topology, surges will be re-injected in the power supply and can damage the driver through these pins.

New ESDALCxx-2BP5 for Line Drivers

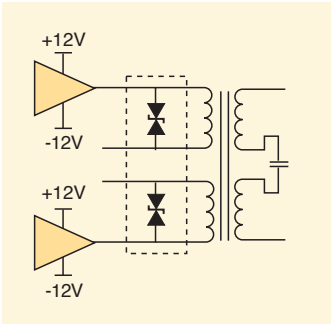
The ESDALCxx-2PB5 has been developed according to the following requirements:

- Line driver power supply voltages
- Compliance with telecommunication standards like ITU-T K20/21 and GR1089 Core which are the most stressfull when using protection on the primary winding
- Compatibility with high DSL debit rate for the capacitance to avoid BER or oscillation problems
- Integration of 2 separate Transils in a small SOT-665 package.

Choice of either a 14.2V or a 25V Transil gives the possibility of using both topologies:



Topology 1: ESDALC25-2BP5 protection on tx and rx



Topology 2: ESDALC14V2-2BP5 on secondary winding

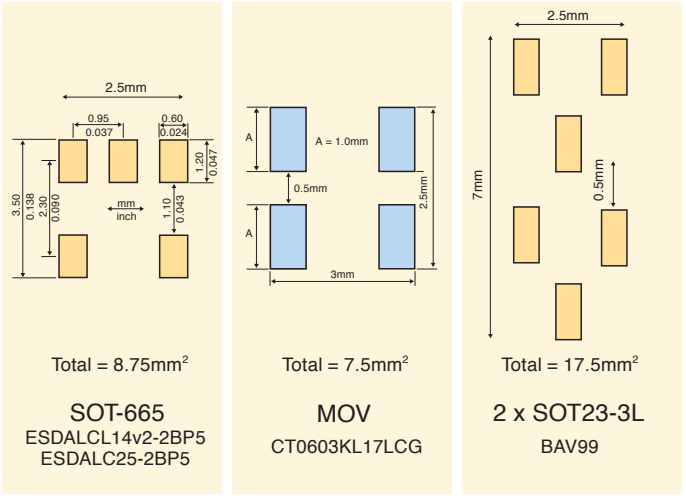
In this case, one Transil is used to protect Tx while the second one is used to protect Rx.

In this case, each secondary winding of the transformer is protected. For both topologies, the SOT-665 must be implemented as close as possible to the transformer to avoid disturbances on the board.

Parameters	Key Parameters	
	Capacitance	Surge
BAV99	1.5pF	2.6 A @ 2.5 µs non repetitive
CT0603KL17LCG	50pF	10 A 8/20 µs @ 75V 6 A 8/20 µs @ 65V
ESDALC14V2-2BP5	8pF at 3V	6 A 2.5 µs @ 25V
ESDALC25-2BP5	14pF at 3V	6 A 2.5 µs @ 35V

Comparison between ESDALC and non-silicon devices like Metal Oxide Varistors (MOV)

If the MOV in CT0603KL17LCG is the smallest package solution, the high voltage during clamping makes it unsuitable for this kind of protection. BAV99 uses two packages so PCB consumption is twice that of the SOT-665.



Footprint comparison between SOT-665, MOV and SOT23-3L

Conclusion

SMP100MC-xxx with ESDALCxx-2BP5 offers the best trade-off between surge, clamping voltage, capacitance and package for DSL protection after the transformer to comply with telecommunication standards.

STD65N55 & STD60N55

By R. Gulino
Power MOSFET Technical Marketing

LOW $R_{DS(on)}$ POWER MOSFETs FOR INDUSTRIAL AND AUTOMOTIVE APPLICATIONS

Following the recent introduction of the STB180N55 and STB185N55, ST has enlarged its range of devices designed in the new low voltage MDmesh technology. The new STD65N55 and STD60N55 compete well against the best industry technologies to achieve one of the lowest $R_{DS(on)}$ values in DPAK.

Custom Made Devices

Instead of generating multi-application devices, the individual requirements of the automotive and industrial segments are met in separate components. Consequently the industrial market is the main target for the STD60N55, while the STD65N55 has been developed for harsh automotive applications, and is fully compliant to all of ST's strict automotive rules.

Applications

- High current switching applications
- DC / DC converters
- Wiping systems
- PWM motion control
- PWM FAN control
- Diesel glow plug

"N" Series Power MOSFETs

The 55V "N" series Power MOSFET comes from the Multi-Drain approach now applied to low voltage technology in order to significantly reduce the $R_{DS(on)}$ per area.
The $R_{DS(on)}$ per area for these new "N" series Power MOSFETs is about 40% lower than that of the previous "NF" series, as already seen for the first devices housed in D^2PAK, and TO-220. In fact, the 'N' series provides the same $R_{DS(on)}$ value with about 40% less silicon area.

Features

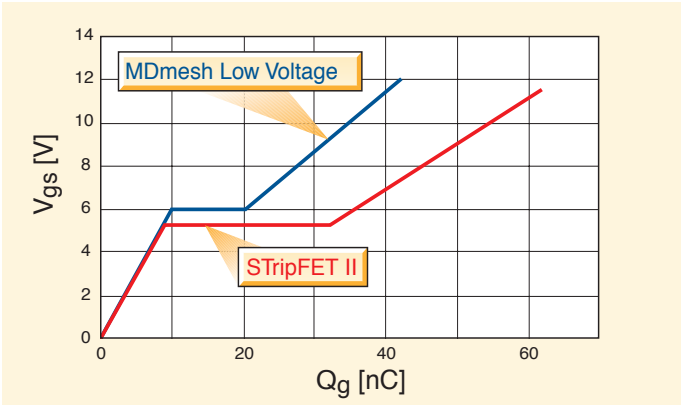
- 175°C operating temperature
- Standard threshold drive
- Typical $R_{DS(on)}$ in the range of 8.0mΩ.
- 100% avalanche rated tested, either at wafer level or finished parts
- P.A.T. (Part Average Testing) applied during wafer probing for the STD65N55.

Electrical Characteristics

Part number	$V_{(BR)DSS}$ [V]	$R_{DS(on)}$ Max @ 10V [mΩ]	R_{THJ-C} [°C/W]	I_D [A]
STD65N55 STD60N55	55	10.5	1.36	65

Lower Gate Charge

Both STD65N55 and STD60N55 have a lower gate charge value compared to STD60NF06, the equivalent device made with standard STripFET II technology.



Gate charge improvement of the new MDmesh low voltage technology compared to the previous STripFET II technology

The new devices also have a Q_{GD} / Q_{GS} ratio about three times lower than that of the "NF" series. This is important for minimizing cross-conduction power losses due to shoot-through, mainly in DC-DC converters and in full-bridge motion control applications.

SuperFREDMesh™

By Andrea Tranchida
Power MOSFET Product Marketing

OUTSTANDING DV/DT CAPABILITY FOR LIGHTING APPLICATIONS

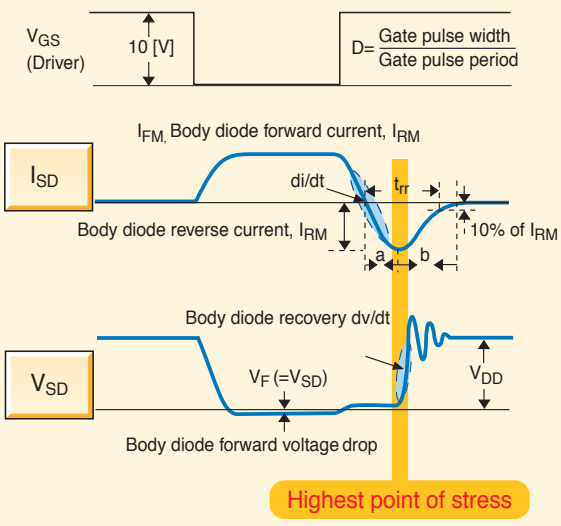
The most typical block diagram of tubular fluorescent ballasts includes a bridge rectifier, a power factor correction circuit and a Power MOSFET half-bridge stage with a driver. When designing a ballast, one of the most important parameters to take into account is the diode recovery dv/dt of the half bridge Power MOSFETs.

A 'Dangerous' Stress Condition

If the Power MOSFET driving is not properly arranged, diode recovery dv/dt is very often the reason for ballast failures, especially during sudden frequency changes in the bridge caused by:

- Start-up of the tube
- Tube removal
- End of life

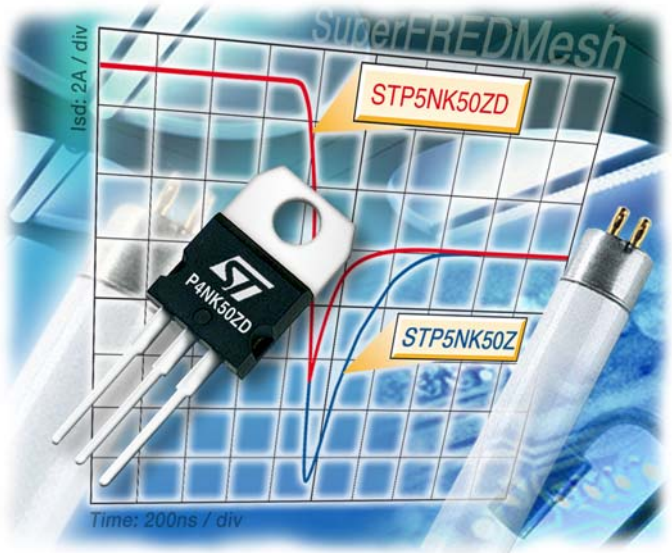
The Power MOSFET may be destroyed by simultaneous stresses such as high drain current, high drain source voltage during the diode recovery.



Body diode dv/dt and di/dt crossing during recovery phase

SuperFREDmesh Product Family

For those cases where it is not possible to maintain low rates of dv/dt, the choice for Power MOSFETs with higher capability is mandatory.



ST has recently enhanced its standard SuperMESH product family by adding a new series that includes a fast recovery body diode: SuperFREDMesh. This product series, obtained with a new carrier lifetime control technique, besides the well known low Qrr and trr, offers an outstanding dv/dt capability of 15V/ns.

All the features mentioned are the exact requirements of lighting applications such as electronic ballasts and High Intensity Discharge Lamps, without renouncing to the traditional cost competitiveness of the SuperMESH family.

Features

- DV/DT immunity up to 15V/ns
- Extremely low trr
- Ideal for ZVS resonant topologies
- Cost effective technology

New SuperFREDmesh Devices

Part number	B_{VDSS} [V]	$R_{DS(on)}$ [Ω]	dv/dt [ns]	Package
STP4NK50ZD	500	2.7	15	TO-220
STP5NK52ZD	520	1.5	15	TO-220
STP9NK60ZD	600	0.95	15	TO-220

ESBT® in QR-ZVS Fly-Back

By Reddiconto / Buonomo
Bipolar Market & Application Development

STC08DE150HV: THE COOLEST SOLUTION FOR YOUR ADAPTER

Following the success of ESBTs in high-end industrial applications, attention is now being shifted towards lower-end applications such as adapters for notebooks, printers and SMPS for TVs. One of the most popular and simplest ways to increase efficiency is to operate in QR (quasi resonant mode) with a flyback converter.

Quasi Resonant ZVS Fly-Back Using ESBTs

QR flyback converters are variable frequency versions of standard fly-back converters. Several advantages exist by using this topology:

- QR approach makes use of the otherwise undesirable parasitic drain capacitance to generate a zero-voltage condition that minimizes turn-on losses of the power switch.
- Variable frequency operation is inherent in such functionality. The main benefit concerns conducted EMI.

Basically the QR fly-back operates to get the so called valley switching, where the turn on occurs at the minimum voltage during the resonance occurring after the core demagnetization.

The turn on losses are given by the formula: $E_{on}=1/2CV^2$, where V is the turn on voltage and C is the parasitic capacitance.

It can be easily understood that it is preferable to turn on the switch at zero voltage.

This can be obtained choosing a fly-back voltage equal to the input voltage. However this will lead to a very high voltage stress on the device. In a typical off-line converter this voltage reaches, with typical transformer leakage inductance, at least 1200V (without any clamp).

Thanks to ESBT's very low voltage drop, regardless of the high switching capability and the voltage and current rating, it offers the most effective solution.

Experimental Results in a 180W Adapter

An 180W single 19V output adapter using a 600V Power MOSFET (and a large clamping network to allow 600V switch to be used) as the main switch has been modified to use a 1200V ESBT, removing the clamping newtork

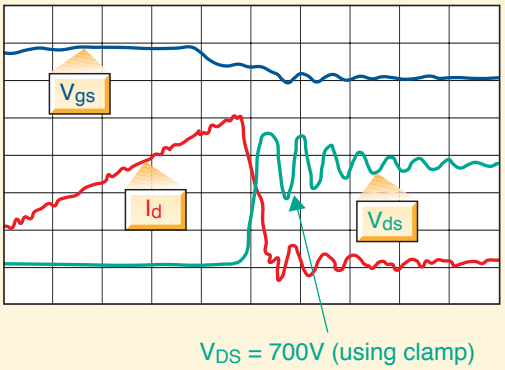
Original Adapter Characteristics

Input Voltage [VAC]	Input Power [W]	Output Current [A]	Freq. [kHz]	Efficiency [%]	Std-by [W]
110	201	9	70	85	0.49
220	194.7	9	70	87.8	0.75
Power MOSFET case temperature: 75°C					

- Fly-back voltage: 130V (limited by Power MOSFET $BV_{(BR)DSS}$
- Transformer turn ratio: 20/3
- Output voltage: 19V

The voltage stress on the Power MOSFET is well above its rated breakdown voltage with consequent possible avalanche and unsafe working conditions. The choice of a 600V breakdown voltage is dictated by the need for a very low $R_{DS(on)}$ (high efficiency).

In order to show the higher performance and the safety achievable using the ESBT technology, the clamp network was removed and the base driving network added. In this case a 1200V ESBT, the STC15DE120HV, is necessary, since the peak voltage reaches 900V.

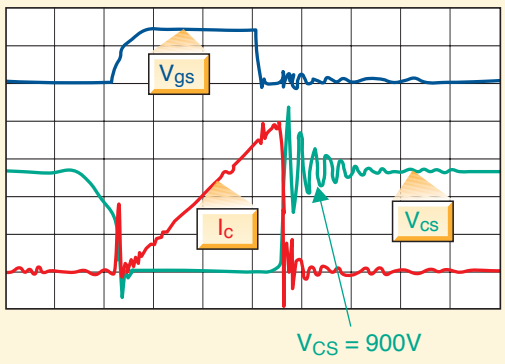


QR waveform with Power MOSFET showing turn-off

STC15DE120HV + Removed Clamp

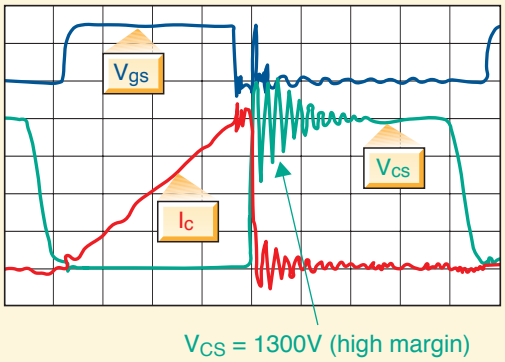
Input Voltage [VAC]	Input Power [W]	Output Current [A]	Freq. [kHz]	Efficiency [%]	Std-by [W]
110	194.6	9	70	87.88	0.44
220	189.2	9	70	90.38	0.57
ESBT case temperature: 48°C					

By removing the clamping network the maximum voltage across the ESBT reaches 900V making the use of a 1200V device unavoidable.
The ESBT working case temperature is 48°C. The results show how the low Vcesat and the fast switching capability of the ESBT reduce the power dissipation of 6W, increasing the overall efficiency by 3%.



QR waveform with STC15DE120HV

Further improvement could be achieved redesigning the transformer in order to increase the fly-back voltage and have a real zero-voltage condition at turn-on. The turn ratio of the main transformer has been modified in order to achieve a fly-back voltage of 400V.



QR-ZVS waveform with ESBT

In this case the STC08DE150HV has been used to withstand the very high voltage stress of 1300V across the power switch.
In this last analysis the ESBT works cooler than in any other condition (42°C) using the same heat sink.

Monolithic ESBT Development for Adapter Market

Thanks to the Power MOSFET integration inside the bipolar structure, the ESBT monolithic technology is being implemented in adapter platforms with a power range from 90W to 180W. The monolithic structure allows the device to be housed in the small TO-2204L package, making ST's devices both performance and price competitive. The new target is to offer STP12IE904F in a power range from 90W to 180W, giving a 100V higher safety margin when compared to a 800V CoolMOS, the standard market solution.

ESBT Product Range for Adapters

Part number	B_{VDSS} [V]	I_C [V]	Flyback voltage* [V]	Package
STP12IE904F	900	12	150	TO-220-4LFP
STC15DE120HV	1200	15	300	TO-247-4LHV
STC08DE150HV	1500	8	400	TO-247-4LHV

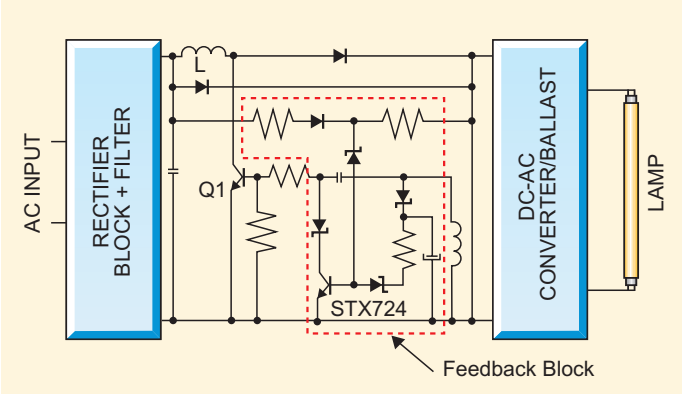
* Recommended

BULx04 & BULx05 in PFCs

By B. Rubino
Power Bipolar Transistor Product Marketing

NEW BIPOLAR TRANSISTORS SERIES IN LOW COST ACTIVE PFCs FOR LIGHTING

The low-cost lighting market requires PFC converters to provide simple, cost-effective solutions without sacrificing PF and THD levels.
Passive solutions assure neither V_{out} regulation against supply voltage variations nor protection on the DC/AC converter during start up and overload conditions. ST is now offering an easy to implement solution which guarantees the previous performance and also targets the low-cost HF Ballast market up to 80W, making the PF correction without using any IC to generate the PWM signal.



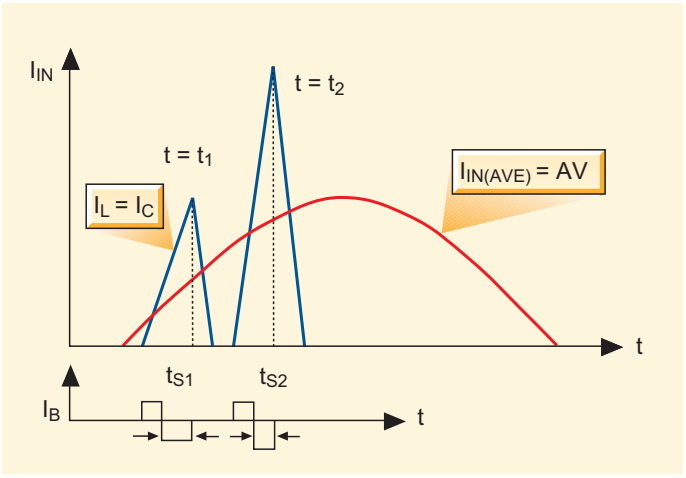
Bipolar PFC in HF ballast

Simple Cost Effective Solution

The proposed active PFC with Bipolar transistors adopts the Boost topology working in discontinuous conduction mode. This is the most simple and cost effective solution for 220V and 120V mains at low to medium power levels. In this case no IC is used to generate a PWM signal, but the physical relation (t_S, I_C) of any power bipolar transistor is exploited when the base current I_B value is kept constant.

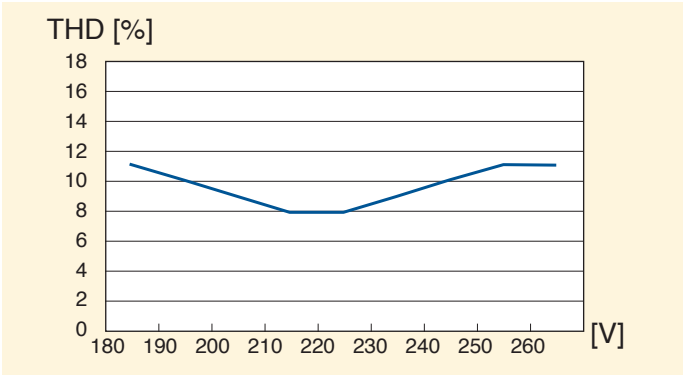
PWM by Storage Time Modulation

The following graph shows two different storage time values at two different input Vac values: at $t = t_1$ the bipolar reaches a higher saturation level than that at $t = t_2$, and this means $t_{s1} > t_{s2}$. The overall switch on time is given by the sum of "I_{BON} time" plus the storage time, therefore keeping the "I_{BON} time" constant, the duty cycle changes according to the t_S modulation.



Storage time modulation effect

This natural duty cycle variation generates an appropriate PWM signal used to control the PFC stage and reduces the I_{main} distortion.
The negative feedback network further controls the duty cycle modulation by modifying the total charge injected into the base of the main transistor.
This duty is accomplished through the low voltage/high h_{FE} STX724 which reduces the Q_1 I_{Bon} amplitude and duration, mainly close to the peak value of the V_{AC} wave .
The solution proposed achieves satisfactory THD values, (about 10%) inside the range ±20% Vmains.



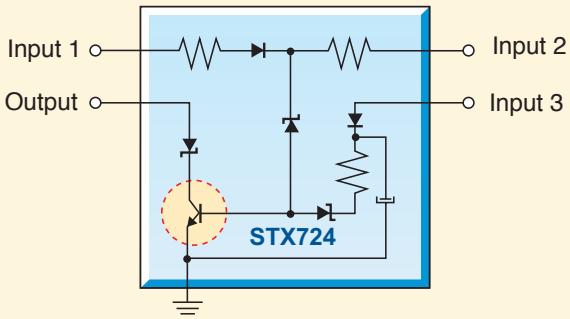
THD versus AC mains variation

Start Up and Overload Protection

The feedback block also performs the lamp power regulation and the system protection phase thanks to a smart combination of three inputs:

- A voltage signal coming from the line (Input 1).
- A voltage signal coming from PFC V_{out} (Input 2).
- A voltage signal proportional to lamp current (Input 3).

The Output signal drives the Q_1 main switch.



Feedback block

Input 1 is used to reduce the THD by improving the storage time modulation.
Input 2 helps to regulate the PFC Vout against supply voltage variations.
Input 3 is useful as start up/overload protection

Application Features

- Compliant to IEC6100-3-2 class C
- THD ≈10%
- PF ≥ 0.98
- Optimized for half bridge voltage fed topologies and for dedicated voltage mains.
- 40W demoboard and application note available: AN2349 Simple cost effective PFC using bipolar transistors for low-to-medium power HF ballasts.

40W PFC With DC/AC Converter Demoboard

ST offers a complete solution including the PFC stage and the DC/AC converter realized with a complementary pair of power bipolar transistors with a high gain characteristic. However, the PFC stage works correctly no matter what type of DC/AC converter is used. A 40W demoboard is already available while the higher power version (up to 80W) will be available soon.

Dedicated BULx0x for PFC

- Low spread of h_{FE} and t_S parameters
- Large RBSOA
- High BV_{ceo}

As a main characteristic, these devices show a hFE curve optimized to perform the proper modulation of the duty cycle necessary to achieve the sinusoidal input current.
In addition, since the BUL804 and BUL805 are designed for a 220V mains, they guarantee high breakdown voltage (BV_{ceo} = 450V) and large RBSOA to sustain high energy levels in turn-off during lamp start-up at high Vac values.

V_{mains} Power	120 [V]	220 [V]
Up to 40W	BUL704	BUL804
Up to 80W	BUL705	BUL805

BULx0x series

Plasma Display Panels

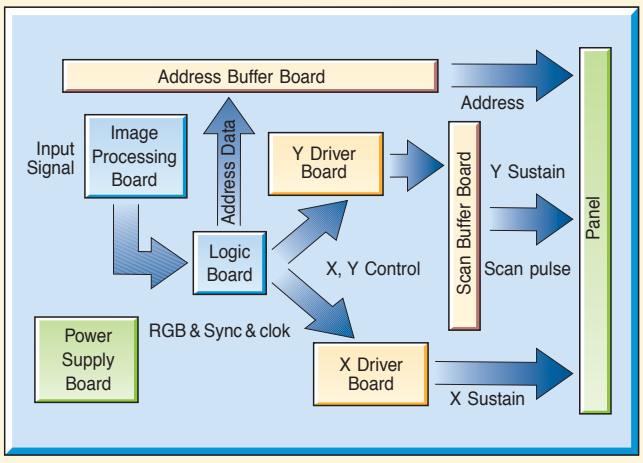
By S. Russo
Systems Lab.

A COMPREHENSIVE APPROACH TO ENERGY SAVING

Plasma Display Panels (PDP) are emerging as the leading candidate for large-area wall-hanging color TVs and HDTVs. Its large screen, wide viewing angle, and thinness have given it the edge over conventional displays. Scan, energy recovery (ERC) and sustain circuits are important blocks that fulfill the important energy saving requirements.

PDP Module Structure

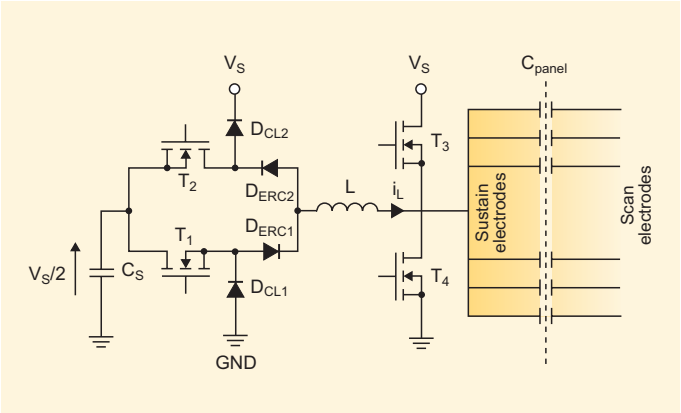
Power supply, address buffer, logic and scan buffer boards are the fundamental blocks of a PDP. In particular, the energy recovery and sustain function are performed by the Y and X drive boards. Power MOSFETs and IGBTs are key products for ERC and sustain both in X and in Y drive board, as well as they are for the path, reset and erase function in the Y drive board only. Path switches are mandatory to isolate ERC and Sustain switches from the negative voltage applied to the display during the scan phase. While, reset switches set identical initial condition of the plasma cells before each address cycle.



Signal flow in PDP module structure

ERC Architecture Review

The aim of the ERC is to reduce the power losses in the sustain transistors during the sustain phase. In fact, this resonant circuit recovers the energy trapped by the intrinsic plasma panel capacitance (Cpanel) and stores it in the storage capacitance



Sustain bridge (half section) and sustain energy recovery circuit

(Cs). The stored energy is reused during each sustain cycle instead of being dissipated in the sustain switches.

ERC is carried out with an inductor L, a capacitor Cs, two sustain switches (T3 and T4), two energy recovery switches (T1 and T2), and two energy recovery diodes (D_{CL1} and D_{CL2}).

The sustain voltage V_S is close to 200V and depends on the gas mixture inside the panel.

During the ERC operation, a high-value sine wave current flows through both the ERC diodes and Power MOSFET for a short time with a peak current of 60A. During sustain operation a panel current discharge flows through the sustain Power MOSFET for a short time, with a peak current of 200A in the worst case.

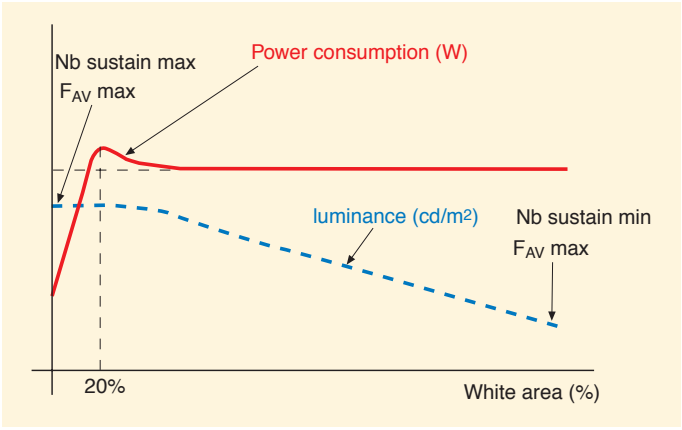
ST's Solution for ERC

ST's extensive portfolio covers the whole solution for an energy recovery circuit (ERC) and a sustain and scan circuit, taking into account all fundamental requirements like cost, component count, reliability and power consumption.

Reduced power losses and higher switching frequency are the main benefits of ST's advanced technology.

It allows an important power consumption reduction increasing luminous efficiency (lm/W).

ST has an extensive product coverage of both the switching and driving sections.



Power consumption and luminance versus white area

Switching Section

- STTH60P03SW, STTH40P03 ERC diodes
  - I_{RM}: peak reverse recovery during turn OFF
  - V_{FP}: peak forward voltage at turn ON
- STTH2003CG clamping diodes:
  - V_F: forward drop
- STW75N20 ERC Power MOSFET:
  - $R_{DS(on)}$: low $R_{DS(on)}$ is required to reduce power losses.
  - Q_g: low total gate charge to allow high frequencies.
- STW52NK25Z sustain Power MOSFET:
  - $R_{DS(on)}$: low $R_{DS(on)}$ is required to reduce power losses and avoid pixel turn OFF.
  - Q_g: low total gate charge to allow high frequencies

Driving Section

- STS01DTP06 push-pull Power MOSFET and IGBT gate driving
  - Reduced board space and component count
  - High efficiency
- 74VHCT541 input signal buffer
  - High speed and low power dissipation
  - Enhanced PCB layout due to single side output
- L6385 high voltage, high and low side driver
  - dV/dT immunity
  - No interlocking function
  - Space saving and single voltage supply

ST's product coverage map for PDPs

New Dedicated Products

New high performance IGBTs tailored to the latest PDP application will be available shortly:

- STGW100N30 high frequency-low drop IGBT for sustain and ERC, this device is suitable also for low frequency low-drop Path function.
  The devices will be offered both with or without diode.

The Complete System Solution

ST offers its customers a complete product portfolio covering the whole PDP. ST's system approach helps customers design effective energy recover (ERC) and sustain circuits, improving their time to market. PDP power consumption is greatly reduced using ST's dedicated products.

	Part number	Description	Package
Switching section	**STTH60P03SW**	Energy Recovery Diode	TO-247 / Dice
	STTH2003CG	Clamping Diode	D^2PAK / Dice
	STW75N20	Energy Recovery Power MOSFET	TO-247 / Dice
	STW52NK25Z	Sustain and Path Power MOSFET	TO-247 / Dice
Driving section	**74VHCT541**	High Speed Input signal buffer	SOP20 / TSSOP20
	L6385	High voltage, high and low side driver	SO-8 / DIP-8
	STS01DTP06	Push-pull Power MOSFET and IGBT gate driving	SO-8

Express provides up-to-date information about MICROS - POWER - ANALOG

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