



SANYO Semiconductors

# DATA SHEET

## LA6574H — Monolithic Linear IC Five-Channel Driver (four BTL channels plus one H bridge channel) for MD and CD Player

### Overview

The LA6574H is a motor driver IC for MD and CD players with four BTL channels and one H bridge channel. The LA6574H features a separate power supply for the H bridge block, an output adjustment pin, and a 3.3 V regulator to support a wide range of applications.

### Functions and Features

- Four power amplifier channels plus one H bridge channel
- $I_O$  max: 700 mA (each channel)
- Built-in level shifting circuits for the BLT amplifiers
- Thermal protection circuit (Thermal shutdown circuit)
- Separate loading block power supply
- Built-in 3.3 V regulator
- Provides a dedicated pin for adjusting the loading block output.

### Specifications

Maximum Ratings at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}$ max		14	V
Allowable power dissipation	$P_{dmax}$	Independent IC	0.82	W
		* Mounted on a board.	2.0	W
Maximum output current	$I_O$ max	Each channel for CH1 to CH5	0.7	A
Maximum input voltage	$V_{INB}$		13	V
MUTE pin voltage	$V_{MUTE}$		13	V
Operating temperature	$T_{opr}$		-30 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

Note \*: Mounted on a board (76.1 × 114.3 × 1.6 mm) Material: glass epoxy

Recommended Operating Conditions at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}$		5.6 to 13	V

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## LA6574H

**Electrical Characteristics** at  $T_a = 25^\circ\text{C}$ ,  $V_{CC1} = V_{CC2} = 8\text{ V}$ ,  $V_{REF} = 1.65\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Overall Characteristics]						
No load current drain - ICC on	$I_{CC-ON}$	All outputs on, FWD = REV = 0 V *1		30	50	mA
VREF input voltage range	VREF-IN		1		$V_{CC}-1.5$	V
[BTL Amplifier Block]						
Output offset voltage	V <sub>OFF</sub>	BTL amplifiers, the voltage difference across each channel's output	-50		+50	mV
Input voltage range	V <sub>IN</sub>	Input resistance: 11 k $\Omega$	0		$V_{CC}$	V
Output voltage	V <sub>O</sub>	The voltage between each of the V <sub>O+</sub> /V <sub>O-</sub> pairs when R <sub>L</sub> is 8 $\Omega$ . *2	4	5		V
Closed loop voltage gain	VG	Gain from input to output		4		Multi-plier
Slew rate	SR	With the amplifier operating independently, twice the value measured between outputs *4		0.5		V/ $\mu$ s
[H Bridge Block]						
Output voltage	V <sub>O-LOAD</sub>	The voltage between each of the V <sub>O+</sub> /V <sub>O-</sub> pairs when R <sub>L</sub> is 8 $\Omega$ . *2		6		V
Low-level input voltage	V <sub>IN-L</sub>				1	V
High-level input voltage	V <sub>IN-H</sub>		2			V
Output control voltage	V <sub>CONT</sub>	V <sub>CONT</sub> = 3 V *2		3.5		V
[Regulator Block]						
Output voltage	V <sub>reg</sub>	I <sub>L</sub> = 100 mA	3.05	3.3	3.55	V
Load regulation	$\Delta V_{RL}$	I <sub>L</sub> = 0 to 200 mA	-50	0	+10	mV
Line regulation	$\Delta V_{VCC}$	$V_{CC} = 6$ to 12 V, I <sub>L</sub> = 100 mA	-15	+21	+60	mV

Note \*1: The total current drain for  $V_{CC1}$  and  $V_{CC2}$  with no load.

\*2: Voltage difference across the load (8  $\Omega$ ). With the outputs in the saturated state.

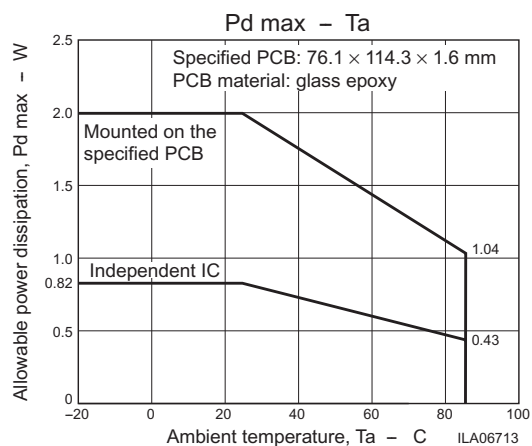
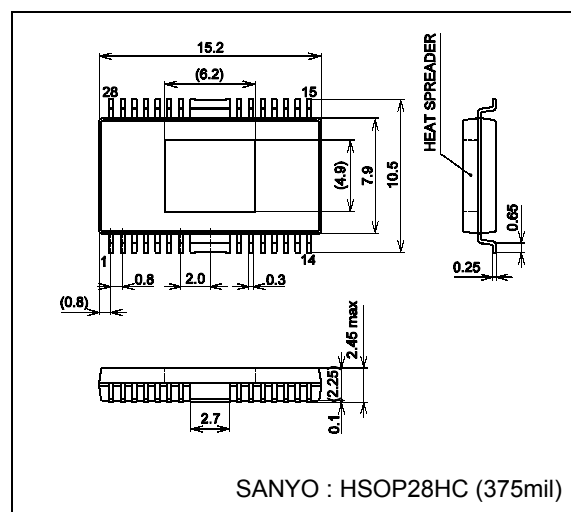
\*3: When the MUTE pin is high, the outputs will be on, and when low, the outputs will be off (high-impedance state).

\*4: Design guarantee value

### Package Dimensions

unit: mm

3234B



## LA6574H

### Pin Functions

Pin No.	Symbol	Pin descriptions
1	V <sub>CC2</sub>	Channels 3, 4, and 5 power supply (This pin must be shorted to V <sub>CC1</sub> and V <sub>CC-S</sub> .)
2	V <sub>O5-</sub>	Loading output (-)
3	V <sub>O5+</sub>	Loading output (+)
4	V <sub>O4+</sub>	Channel 4 output (+)
5	V <sub>O4-</sub>	Channel 4 output (-)
6	V <sub>O3+</sub>	Channel 3 output (+)
7	V <sub>O3-</sub>	Channel 3 output (-)
8	V <sub>O2+</sub>	Channel 2 output (+)
9	V <sub>O2-</sub>	Channel 2 output (-)
10	V <sub>O1+</sub>	Channel 1 output (+)
11	V <sub>O1-</sub>	Channel 1 output (-)
12	V <sub>CC1</sub>	Channels 1 and 2 (BTL) power supply (This pin must be shorted to V <sub>CC-S</sub> and V <sub>CC2</sub> .)
13	V <sub>IN1</sub>	Channel 1 input
14	V <sub>IN1G</sub>	Channel 1 input (gain adjustment input)
15	V <sub>IN2</sub>	Channel 2 input
16	V <sub>IN2G</sub>	Channel 2 input (gain adjustment input)
17	V <sub>IN3</sub>	Channel 3 input
18	V <sub>IN3G</sub>	Channel 3 input (gain adjustment input)
19	REG-IN	Regulator input (external pnp transistor base)
20	REG-OUT	Regulator output (external pnp transistor collector)
21	VREF-IN	Reference voltage input
22	V <sub>CC-S</sub>	Signal system power supply (This pin must be shorted to V <sub>CC1</sub> and V <sub>CC2</sub> .)
23	V <sub>IN4G</sub>	Channel 4 input (gain adjustment input)
24	V <sub>IN4</sub>	Channel 4 input
25	VCONT	Channel 5 (VLO) output voltage control
26	S-GND	Signal system ground
27	FWD	Channel 5 (VLO) output switching (FWD); loading block logic input
28	REV	Channel 5 (VLO) output switching (REV); loading block logic input

- Note:
- The center frame (FR) is used as the power system ground. Along with the signal system ground (S-GND), this level must be the lowest potential in the system.
  - The three power supply pins V<sub>CC-S</sub>, V<sub>CC1</sub>, and V<sub>CC2</sub> must be shorted together externally.

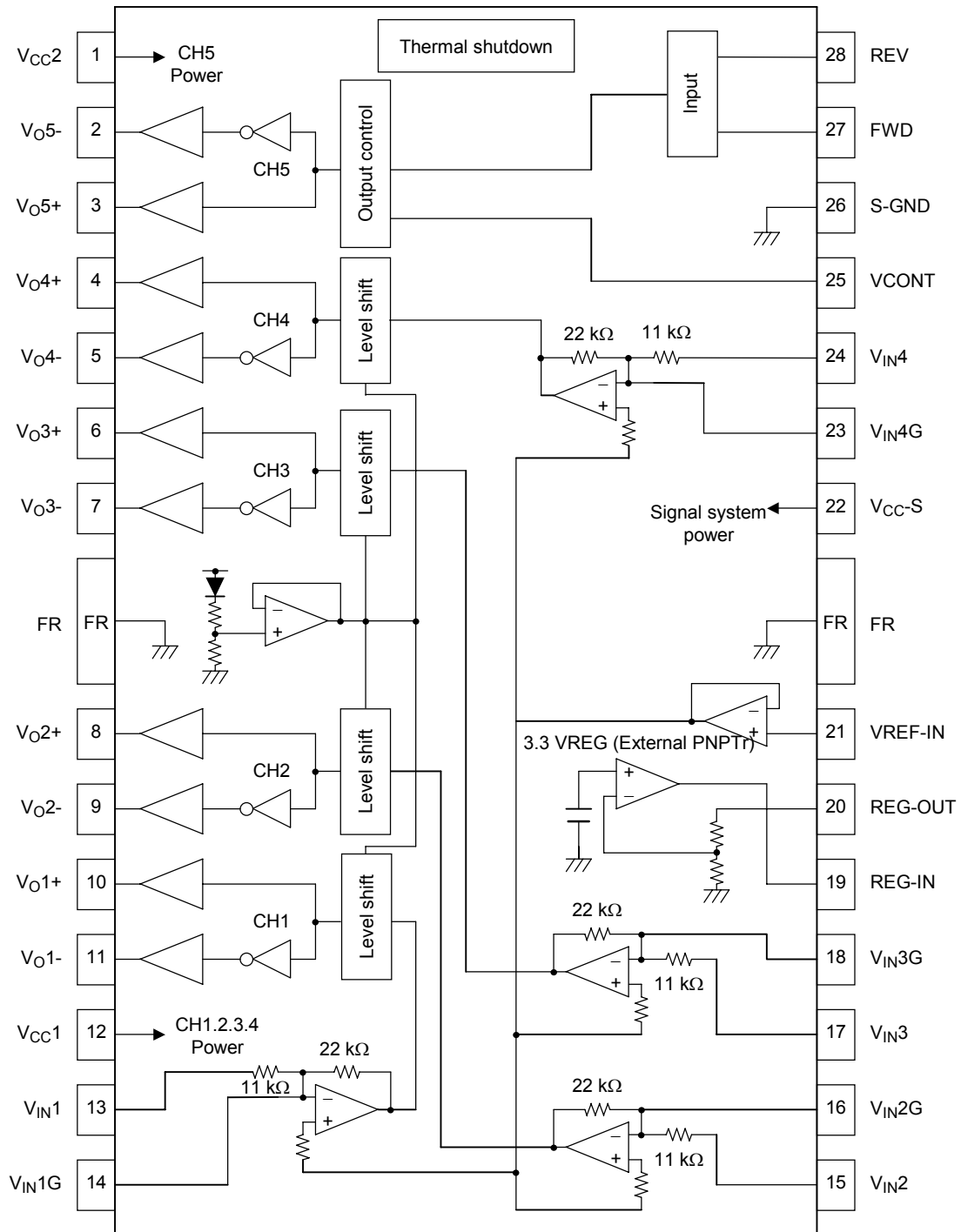
# LA6574H

## Pin Functions

Pin No.	Symbol	Pin name	Pin description	Equivalent circuit
13 14 15 16 17 18 23 24	$V_{IN}$	Inputs	Inputs	
4 5 6 7 8 9 10 11	$V_O$	Outputs	Outputs	
2 3 25	$V_{O5+}$ $V_{O5-}$ VCONT	$V_{O5}$	H bridge outputs	
27 28	FWD REV	FWD REV	H bridge inputs	

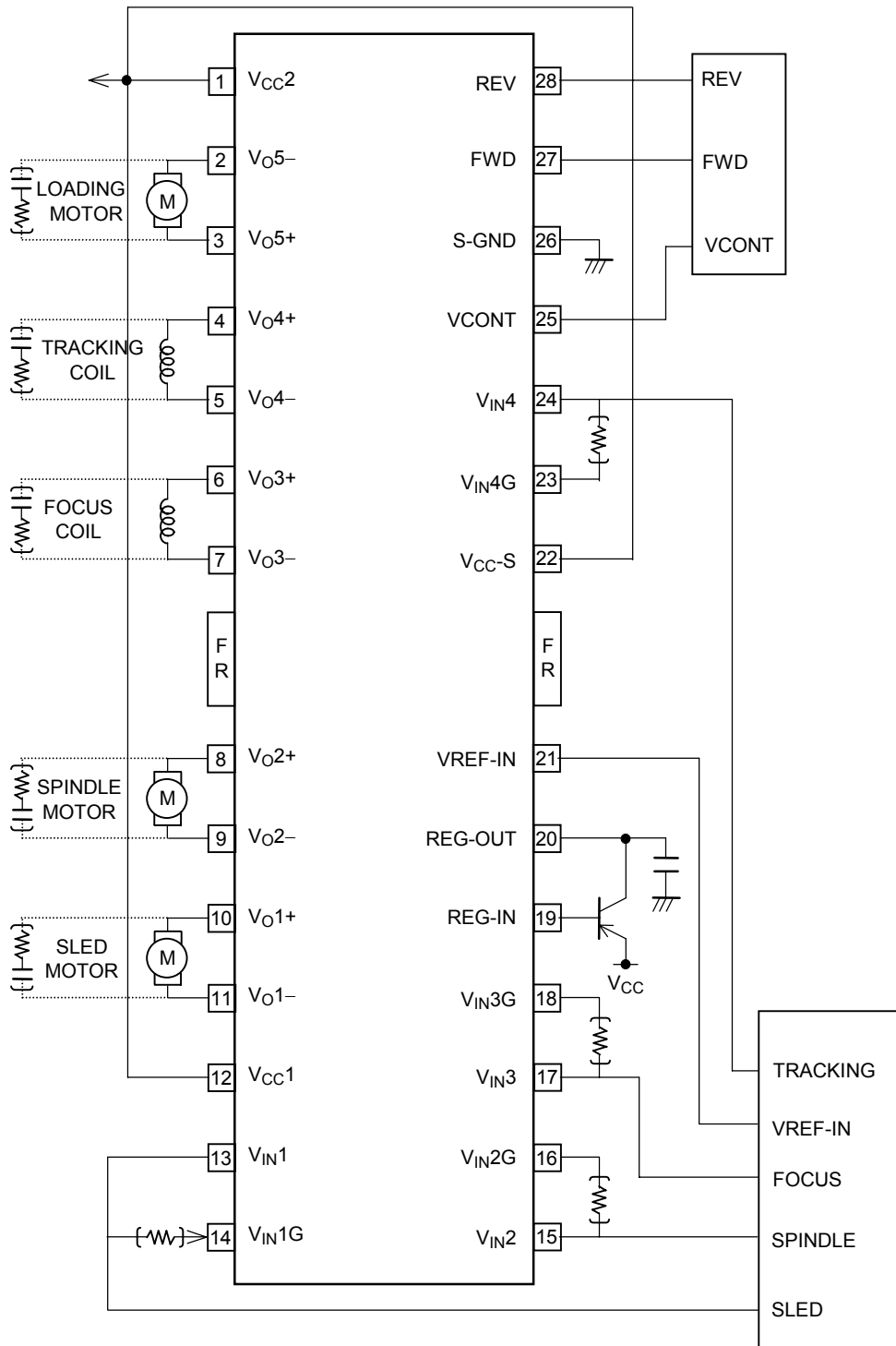
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## Block Diagram



# LA6574H

## Sample Application Circuit



## LA6574H

### H Bridge Block

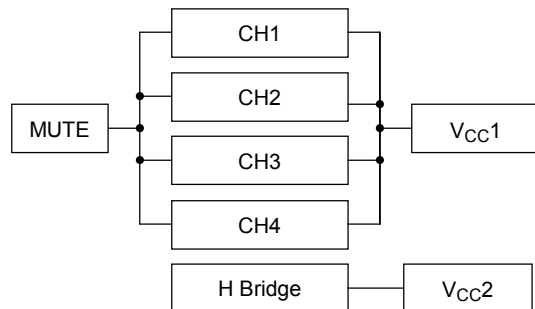
FWD	REV	V <sub>O5+</sub>	V <sub>O5-</sub>	Mode
L	L	OFF	OFF	Open *1
L	H	H	L	Forward
H	L	L	H	Reverse
H	H	L	L	Brake *2

Note \*1: The output are in the high-impedance state in this mode

\*2: In brake mode, the sink side transistors are on (short-circuit braking). The V<sub>LO+</sub> and V<sub>LO-</sub> levels go to a level essentially the same as the ground level.

\*3: V<sub>CONT</sub> (output voltage setting pin) and V<sub>LO</sub> have the following relationship:  $V_{LO} = V_{CONT} - 1\text{ V}$  (typical)

### Relationship between the MUTE pin and the power supplies (V<sub>CC</sub>\*)



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