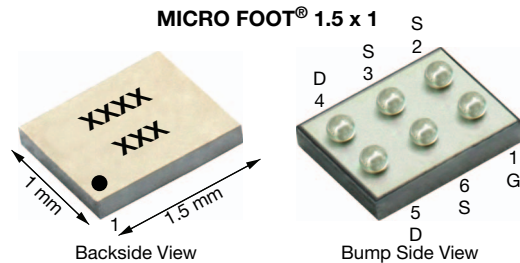


N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A)	Q _g (TYP.)
20	0.033 at V _{GS} = 4.5 V	16 ^e	7.5 nC
	0.037 at V _{GS} = 2.5 V	16 ^e	
	0.042 at V _{GS} = 1.8 V	15	



Marking Code: xxxx = 8406

xxx = Date / lot traceability code

Ordering Information:

Si8406DB-T2-E1 (Lead (Pb)-free and halogen-free)

FEATURES

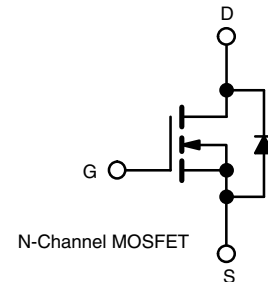
- TrenchFET® power MOSFET
- Ultra-small 1.5 mm x 1 mm maximum outline
- Ultra-thin 0.59 mm maximum height
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS COMPLIANT
HALOGEN FREE
 Available

APPLICATIONS

- Load switch
- Battery management
- Boost converter



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	± 8	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	16 ^e
		T _C = 70 °C	13.5
		T _A = 25 °C	7.8 ^{a,b}
		T _A = 70 °C	6.2 ^{a,b}
Pulsed Drain Current (t = 300 μs)	I _{DM}	30	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	2.3 ^{a,b}
Maximum Power Dissipation	P _D	T _C = 25 °C	13
		T _C = 70 °C	8.4
		T _A = 25 °C	2.77 ^{a,b}
		T _A = 70 °C	1.77 ^{a,b}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C
Package Reflow Conditions ^c	IR/Convection	260	

Notes

- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Refer to IPC/JEDEC® (J-STD-020), no manual or hand soldering.
- Case in defined as the top surface of the package.
- T_C = 25 °C package limited.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient ^{a,b}	R _{thJA}	37	45	°C/W
Maximum Junction-to-Case (Drain) ^c	R _{thJC}	7	9.5	

Notes

- Surface mounted on 1" x 1" FR4 board.
- Maximum under steady state conditions is 85 °C/W.
- Case is defined as top surface of the package.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA	20	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	18	-	mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J		-	-3	-	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.4	-	0.85	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 70 °C	-	-	10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	5	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 1 A	-	0.026	0.033	Ω
		V _{GS} = 2.5 V, I _D = 1 A	-	0.028	0.037	
		V _{GS} = 1.8 V, I _D = 1 A	-	0.030	0.042	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 1 A	-	20	-	S
Dynamic ^b						
Input Capacitance	C _{ISS}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	-	830	-	pF
Output Capacitance	C _{OSS}		-	146	-	
Reverse Transfer Capacitance	C _{RSS}		-	61	-	
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 8 V, I _D = 1 A	-	13	20	nC
		V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 1 A	-	7.5	12	
Gate-Source Charge	Q _{gs}	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 1 A	-	1.1	-	nC
Gate-Drain Charge	Q _{gd}		-	0.8	-	
Gate Resistance	R _g		V _{GS} = 0.1 V, f = 1 MHz	-	3.6	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	7	15	ns
Rise Time	t _r		-	18	40	
Turn-Off Delay Time	t _{d(off)}		-	30	60	
Fall Time	t _f		-	10	20	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 10 Ω I _D = 1 A, V _{GEN} = 8 V, R _g = 1 Ω	-	5	10	ns
Rise Time	t _r		-	17	35	
Turn-Off Delay Time	t _{d(off)}		-	25	50	
Fall Time	t _f		-	10	20	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	-	-	20	A
Pulse Diode Forward Current	I _{SM}		-	-	30	
Body Diode Voltage	V _{SD}	I _S = 1 A, V _{GS} = 0	-	0.7	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 1 A, di/dt = 100 A/μs, T _J = 25 °C	-	15	30	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	5	10	nC
Reverse Recovery Fall Time	t _a		-	8	-	ns
Reverse Recovery Rise Time	t _b		-	7	-	

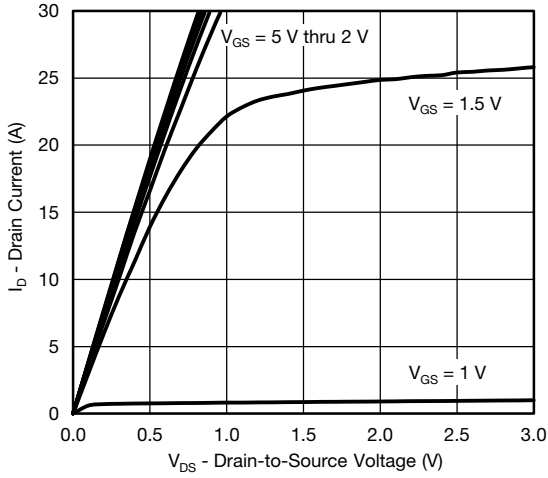
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.

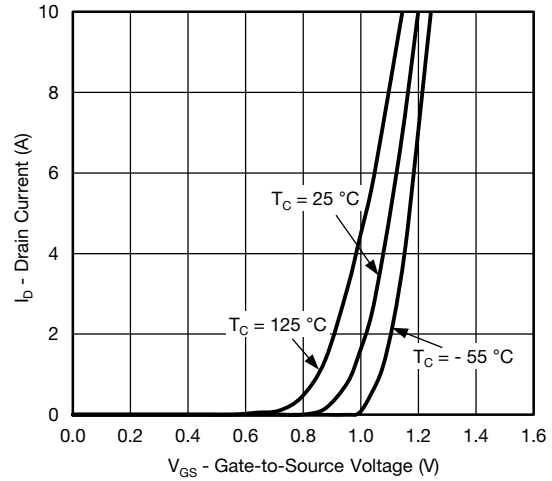
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



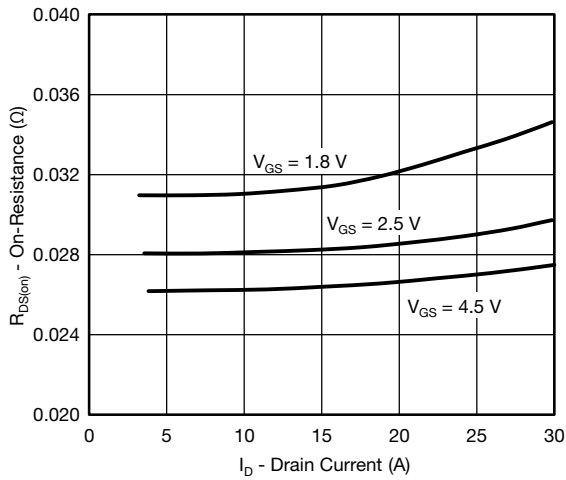
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



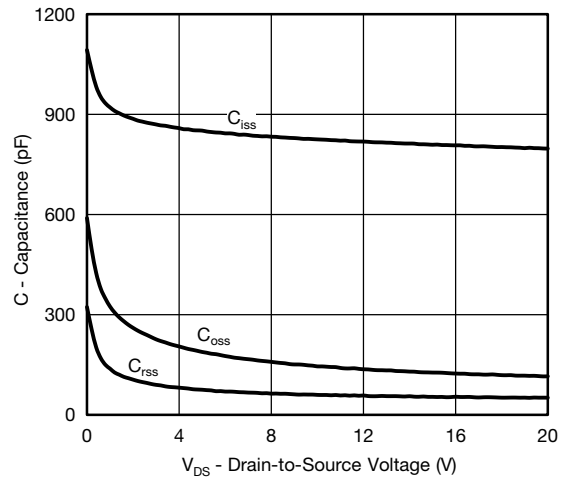
Output Characteristics



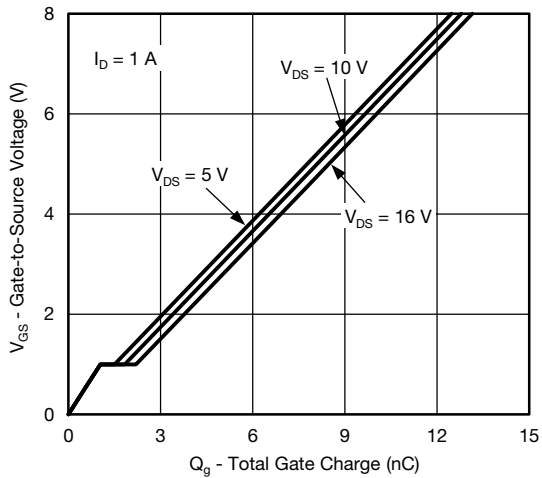
Transfer Characteristics



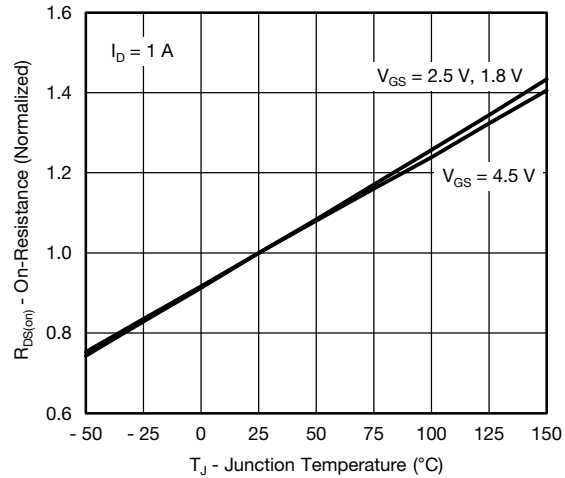
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



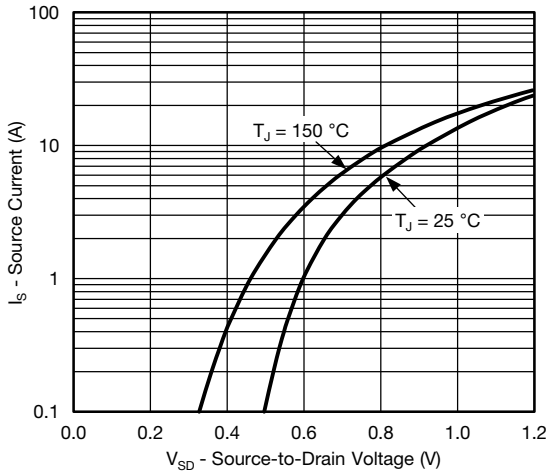
Gate Charge



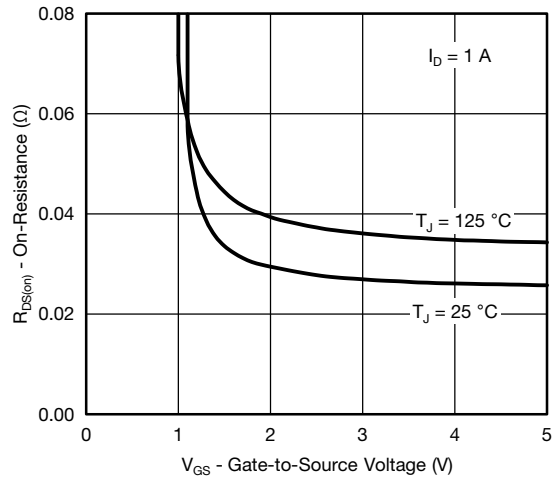
On-Resistance vs. Junction Temperature



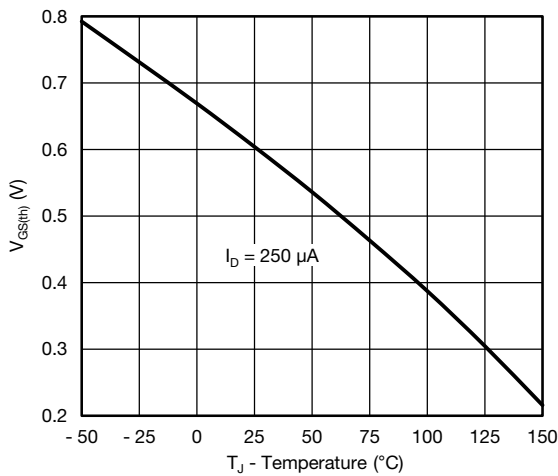
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



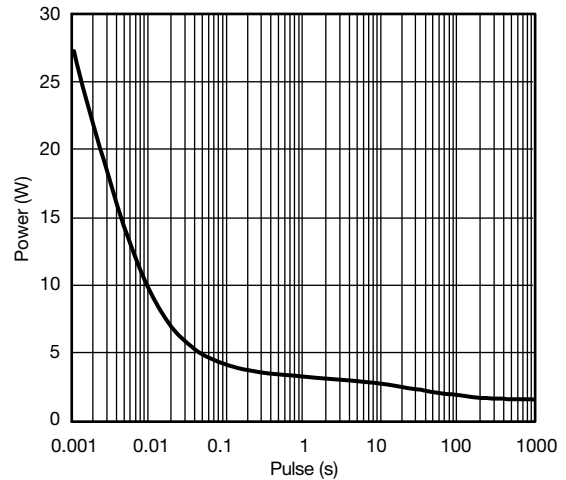
Source-Drain Diode Forward Voltage



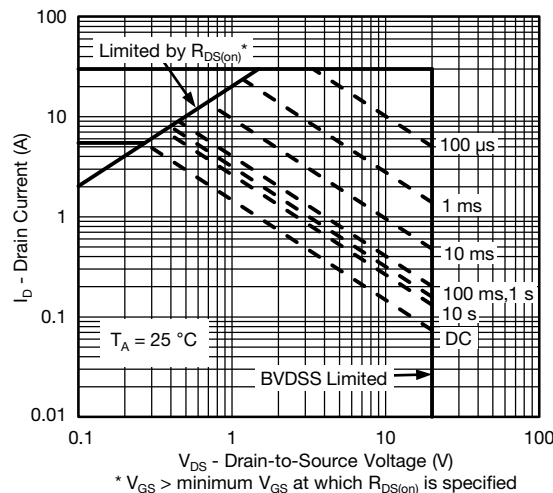
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



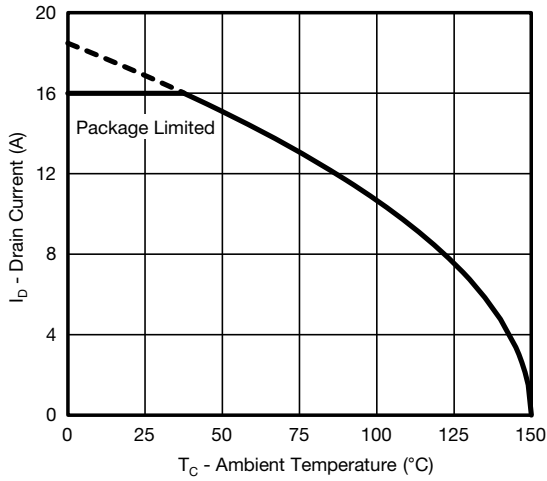
Single Pulse Power, Junction-to-Ambient



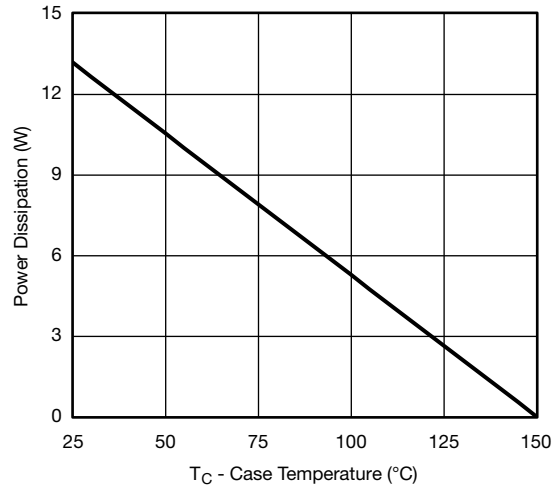
Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*

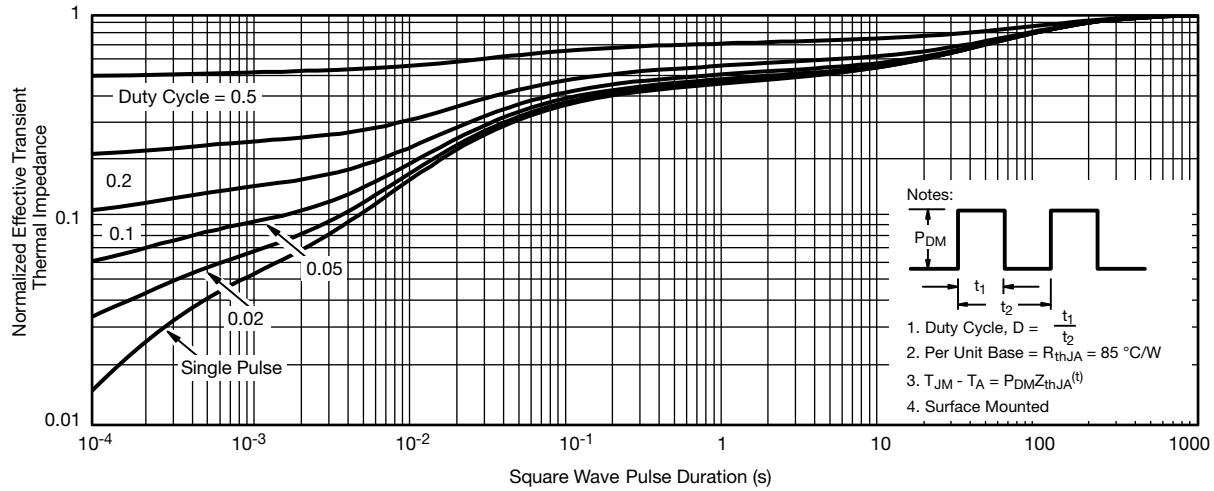


Power Derating

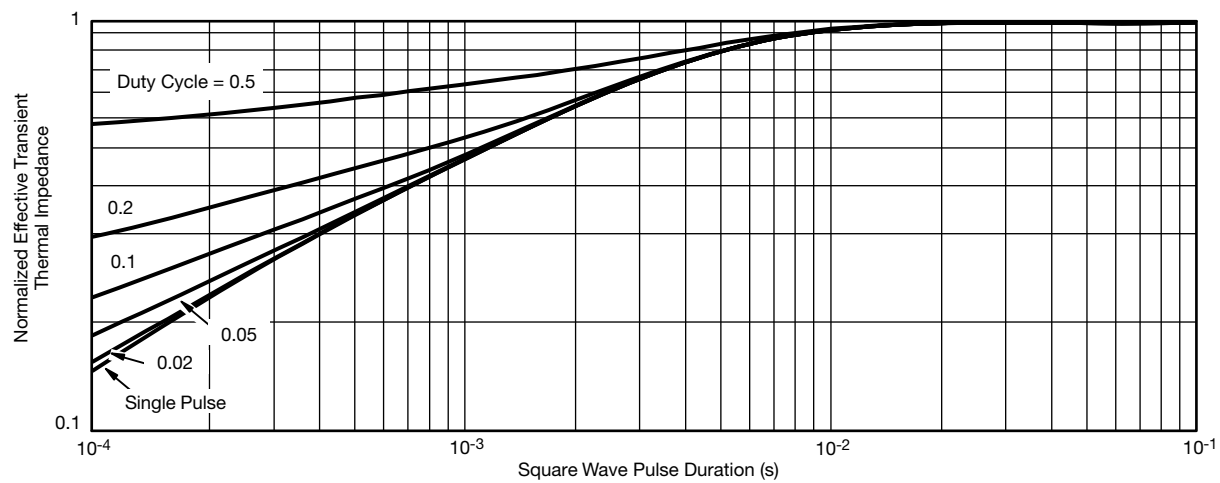
* The power dissipation P_D is based on T_{J (max.)} = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



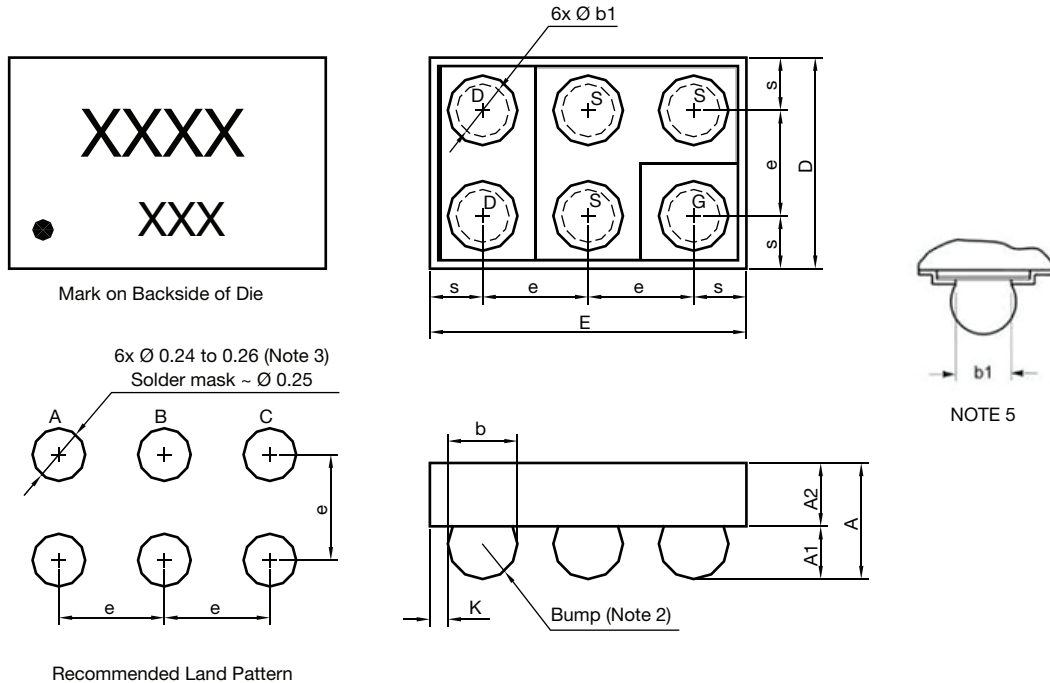
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62530.

MICRO FOOT[®]: 6-Bump (1.5 mm x 1 mm, 0.5 mm Pitch, 0.250 mm Bump Height)


Notes

(unless otherwise specified)

1. Six (6) solder bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
2. Backside surface is coated with a Ti/Ni/Ag layer.
3. Non-solder mask defined copper landing pad.
4. Laser marks on the silicon die back.
5. "b1" is the diameter of the solderable substrate surface, defined by an opening in the solder resist layer solder mask defined.
6. • is the location of pin 1

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.510	0.575	0.590	0.0201	0.0226	0.0232
A ₁	0.220	0.250	0.280	0.0087	0.0098	0.0110
A ₂	0.290	0.300	0.310	0.0114	0.0118	0.0122
b	0.297	0.330	0.363	0.0116	0.0129	0.0143
b1		0.250			0.0098	
e		0.500			0.0197	
s	0.210	0.230	0.250	0.0082	0.0090	0.0098
D	0.920	0.960	1.000	0.0362	0.0378	0.0394
E	1.420	1.460	1.500	0.0559	0.0575	0.0591
K	0.028	0.065	0.102	0.0011	0.0025	0.0040

Note

- Use millimeters as the primary measurement.

 ECN: T15-0140-Rev. A, 20-Apr-15
 DWG: 6035



Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.