SONY

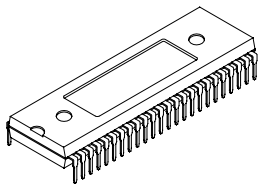
CXA2060BS

Y/C/RGB/D for PAL/NTSC/SECAM Color TVs

Description

The CXA2060BS is a bipolar IC which integrates the luminance signal processing, chroma signal processing, RGB signal processing, and sync and deflection signal processing functions for PAL/NTSC/SECAM system color TVs onto a single chip. This IC includes deflection processing functions for wide-screen TVs. With a SECAM decoder and 1H delay line built in for PAL/SECAM, this IC can be used in configuring multi-color system TV set.

48 pin SDIP (Plastic)



Features

- Supports the I^2C bus
- 1H delay line and SECAM decoder
- Supports NTSC/PAL-N/PAL-M systems with three crystal pins
- Deflection compensation circuit for support of various wide modes
- Count down system eliminates need for V oscillation frequency adjustment
- Automatic identification of 50/60Hz vertical frequency (forced control possible)
- Supports non-interlace display (even/odd selectable)
- Automatic identification of PAL, NTSC and SECAM color systems (forced control possible)
- Automatic identification of 4.43MHz/3.58MHz for crystal (forced control possible)
- No adjustment of Y/C filter required
- Three CV inputs, two Y/C inputs (Y/C input shared with CV input), one Y/C input supporting external comb filter, two RGB inputs
- Dynamic picture/dynamic color circuit
- AKB and gamma correction circuits
- YS1 can be forcibly turned OFF
- FSC output (shared with PAL-N crystal pin)

Applications

Color TVs (4:3, 16:9)

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C, GND1, 2 = 0V)

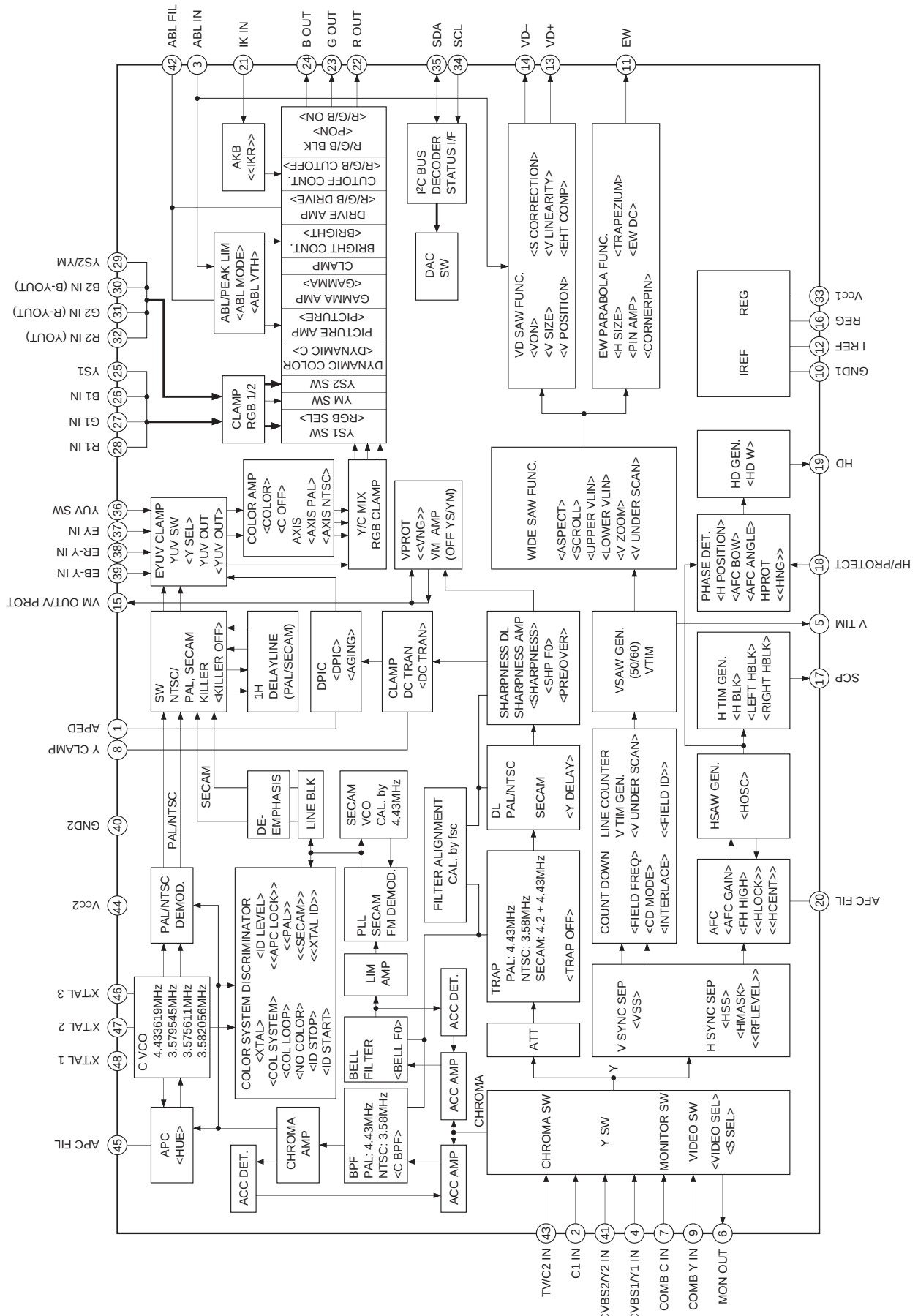
• Supply voltage	$V_{CC}1, 2$	–0.3 to +12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1.5	W
(When mounted on a 50mm × 50mm board)			
• Voltage at each pin		–0.3 to $V_{CC}1, 2$ + 0.3	V

Operating Conditions

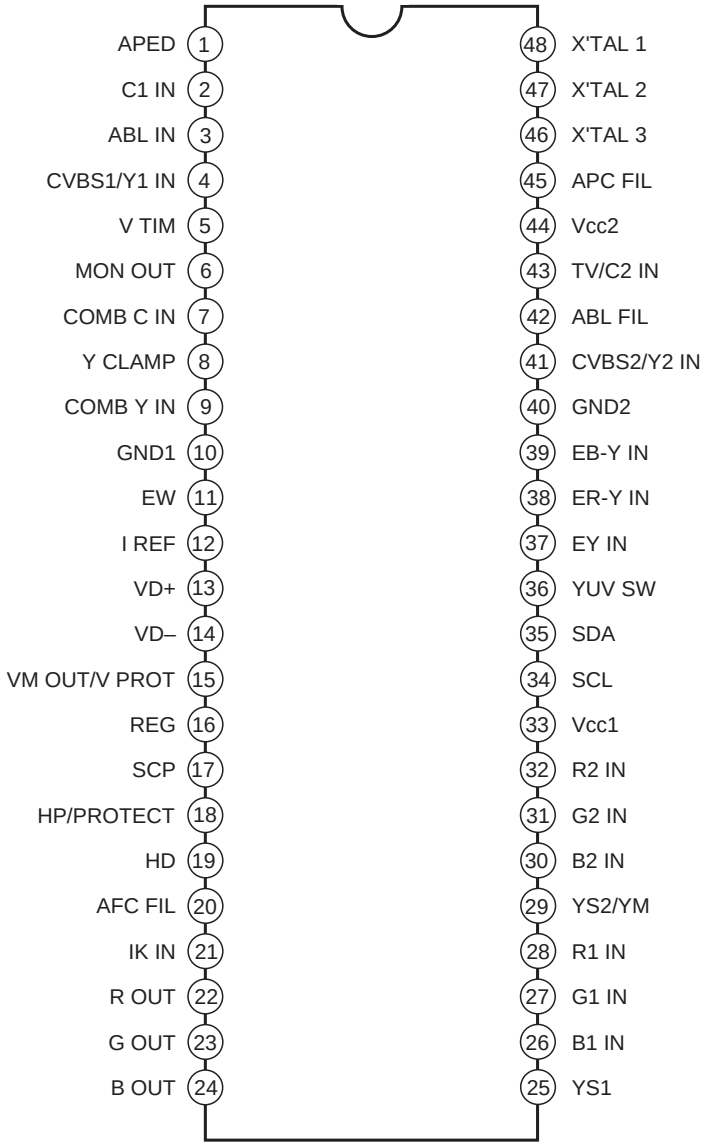
Supply voltage	$V_{CC}1, 2$	9 ± 0.5	V

E98631-PS

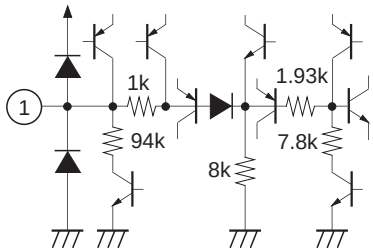
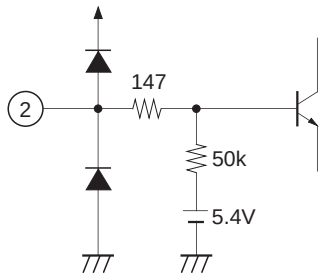
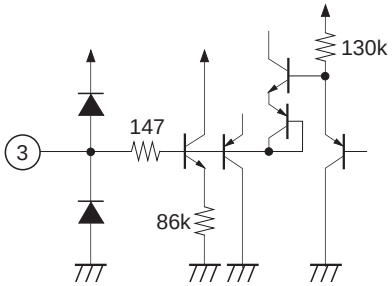
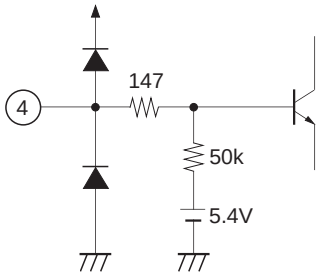
Block Diagram

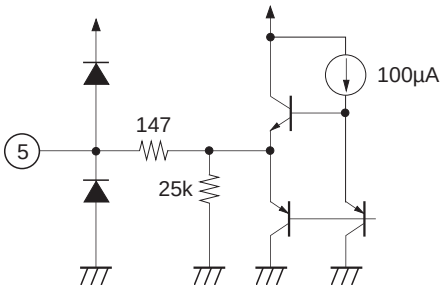
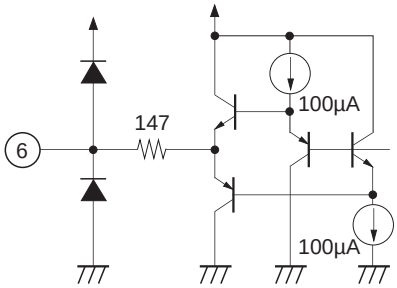
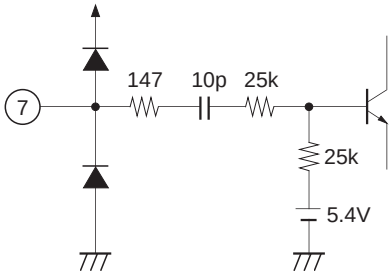
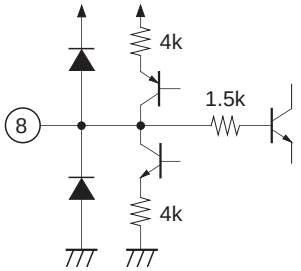
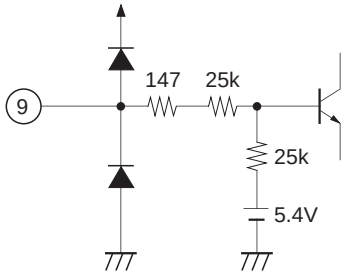


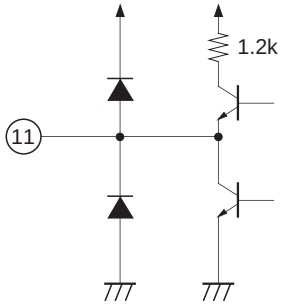
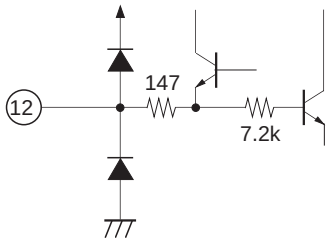
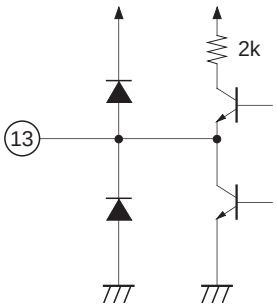
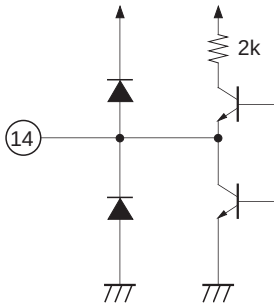
Pin Configuration

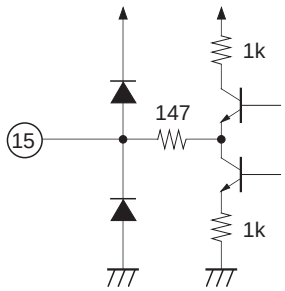
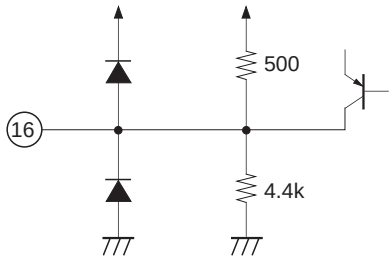
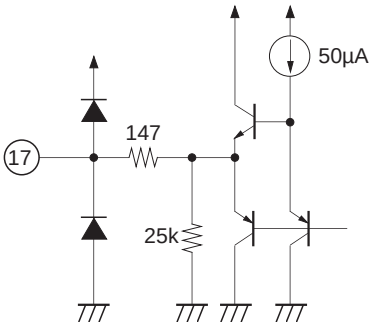
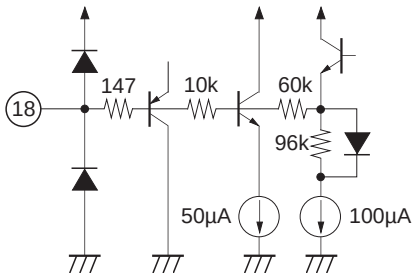


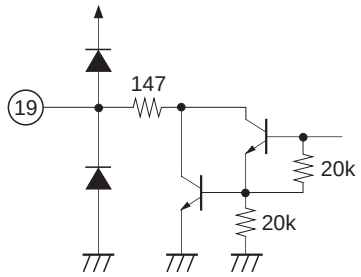
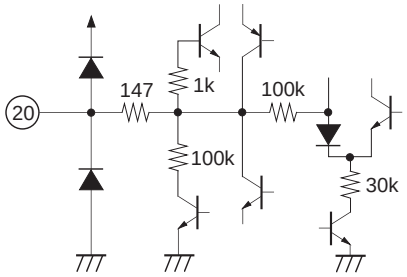
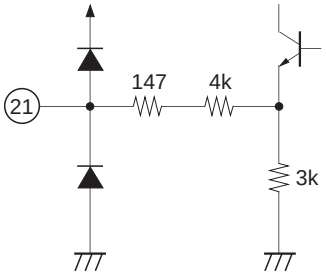
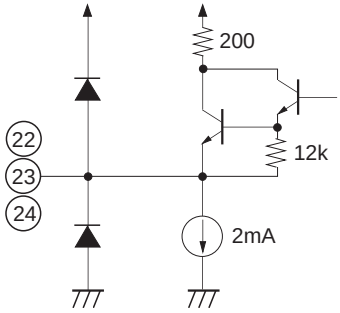
Pin Description

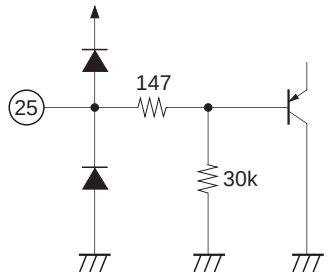
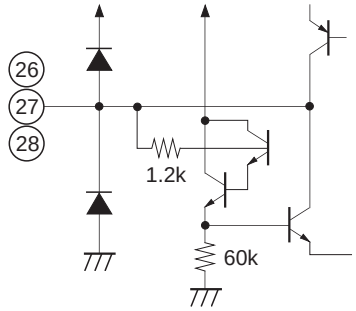
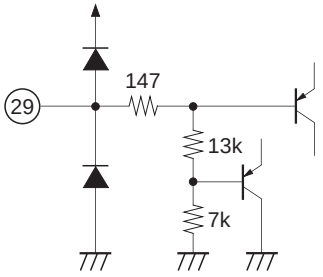
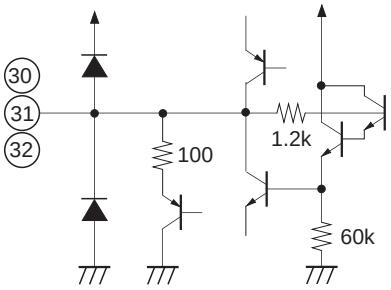
Pin No.	Symbol	Equivalent circuit	Description
1	APED		Connects a capacitor for black peak hold of the dynamic picture feature (black extension). The 4.7µF capacitor is connected to GND.
2	C1 IN		Chroma signal input. Input a chroma signal having a burst level of 300mVp-p via a 0.01µF capacitor. Normally the S pin signal is input.
3	ABL IN		This pin is for both ABL control signal input and VD high-voltage correction signal input. High-voltage correction has linear control characteristics when this pin's voltage is in the approximate range of 1V and 8V. Control characteristics can be varied using the EHT_COMP control of the bus. ABL functions as a PIC/BRT-ABL (average value type). The threshold voltage at which ABL activates can be switched to either 3V or 1V depending on the bus.
4	CVBS1/Y1 IN		CVBS signal/luminance signal input. Input a 1Vp-p (100% white including sync) CVBS signal via a 1µF capacitor. Input the Y signal when a separated Y/C signal is input.

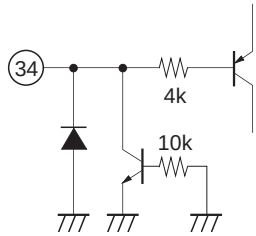
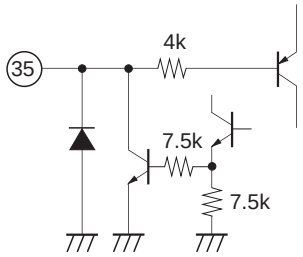
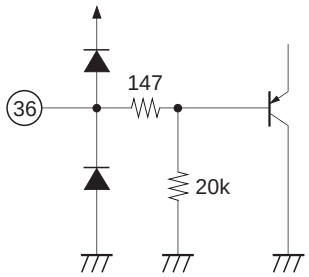
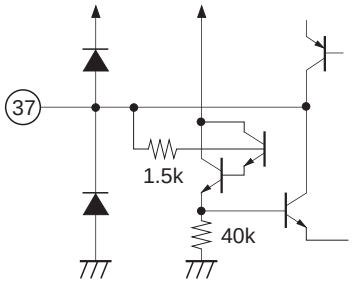
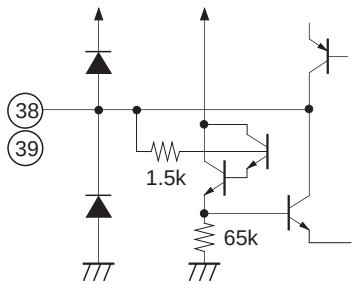
Pin No.	Symbol	Equivalent circuit	Description
5	V TIM		V timing pulse output. This is a 0/5V negative polarity pulse. HSS/VSS can be monitored using the V TIM SEL register.
6	MON OUT		Output of the signal input from TV, CVBS1 or CVBS2 as selected by VIDEO SEL and S SEL of the bus. In the case of S pin input, a luminance signal and chroma signal are mixed and output. Output level is 2Vp-p including sync.
7	COMB C IN		Chroma signal input from a comb filter. The input chroma signal is a 0.6Vp-p burst signal.
8	Y CLAMP		Connects a capacitor for luminance signal clamp. The 0.1µF capacitor is connected to GND.
9	COMB Y IN		Luminance signal input from a comb filter. The signal is input via a 1µF capacitor and has a level of 2Vp-p. (100% white including sync)

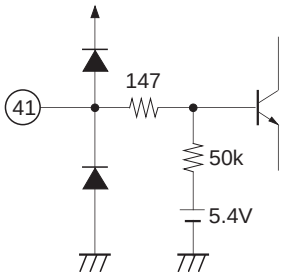
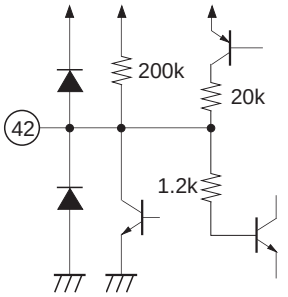
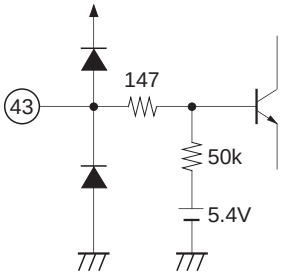
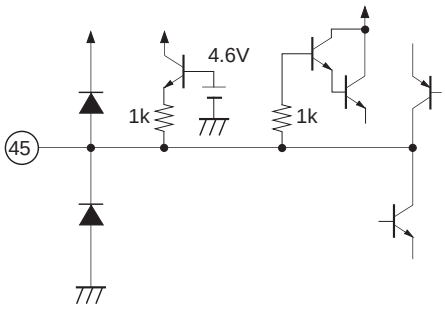
Pin No.	Symbol	Equivalent circuit	Description
10	GND1		GND for 1HDL and deflection system circuit.
11	EW		V parabola wave output.
12	I REF		This pin is used to set the reference current within the IC. A 10kΩ resistor (metallic film resistor) having an error less than 1% is connected to GND.
13	VD+		V sawtooth wave output. The polarity of Pin 13 output and Pin 14 output are reversed.
14	VD–		

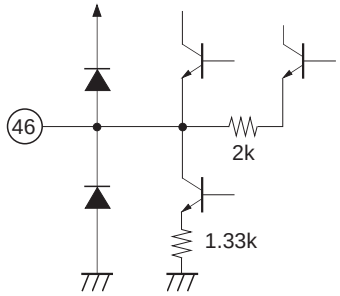
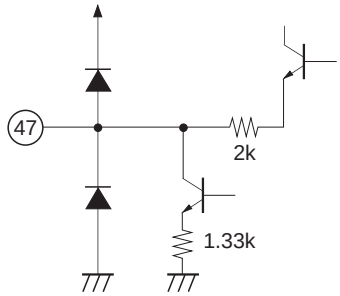
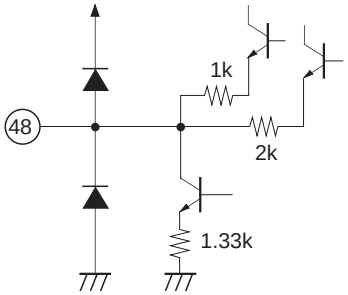
Pin No.	Symbol	Equivalent circuit	Description
15	VM OUT/ V PROT		Output of luminance signal differential waveform for VM (Velocity Modulation). The phase of VM output is synchronized to the phase of RGB output. It is approximately 250ns ahead of RGB output. This pin is also used for V protect signal input. When the large current (4mA) is forcibly drawn through this pin, all RGB output is blanked, and 1 is output to the status register VNG.
16	REG		Decoupling capacitance for the regulator within the IC. The 47µF capacitor is connected to GND.
17	SCP		Sand castle pulse output. The sand castle pulse is a waveform superimposed with the burst gate pulse on the composite blanking pulse.
18	HP/PROTECT		H deflection pulse input for H AFC. The 5Vp-p pulse is input via a capacitor. Since this pin is also used to input an X-RAY protect signal, a hold down function activates if this pin's voltage goes above a "7V cycle" and below 1V. If this occurs, HD output goes high impedance, RGB output is blanked, and 1 is output to the status register HNG. It is necessary to turn the IC's power OFF then ON again to cancel this status.

Pin No.	Symbol	Equivalent circuit	Description
19	HD		H drive signal output. This is open collector output for the NPN transistor.
20	AFC FIL		Connects an AFC lag lead filter. CR is connected to GND.
21	IK IN		CRT beam current input (cathode current IK). This current is converted into voltage within the IC. In order to eliminate any adverse effects exercised by CRT leak current (max. 100µA) for AKB operation, it is clamped at the V blanking interval. The AKB loop is activated by comparing the reference pulse component of this signal to the reference voltage within the IC. The RGB output cutoff can be varied using CUTOFF of the bus. The IK reference signal current can be controlled ±50% around a 13µA center. Since the beam current of the video section is large, be sure to attach a zener diode of about 4V to the pin to protect the IC.
22 23 24	R OUT G OUT B OUT		RGB signal output. Outputs 3.0Vp-p during 100% white input. PICTURE: 3Fh DRIVE: 3Fh BRIGHT: 1Fh

Pin No.	Symbol	Equivalent circuit	Description
25	YS1		YS1 switch control pin. Selects RGB1 input. YS1 Vth: 0.7V This pin is also used as the slave address modification switch. If the voltage at this pin goes over 7V, the slave address is changed from 88h to 8Ah. SLAVE ADDRESS Vth: 7V
26 27 28	B1 IN G1 IN R1 IN		RGB1 signal input. A 0.7Vp-p (no-sync 100 IRE) signal is input via a 0.01µF capacitor. The input signal is clamped at the SCP burst timing.
29	YS2/YM		YS2/YM switch control pin. Selects RGB2 input. When operating at High level (YM Vth: 0.7V) as a YM switch the output signal undergoes 10dB attenuation. YS2 Vth: 2V
30 31 32	B2 IN G2 IN R2 IN		RGB2 signal input. A 0.7Vp-p (no-sync 100 IRE) signal is input via a 0.01µF capacitor. The input signal is clamped at the SCP burst timing just as RGB1 IN. This pin becomes the YUV output pin based on the YUV OUT register. Be sure to pull up this pin by 10kΩ when used for YUV output.
33	Vcc1		Power pin for the signal block and deflection block.

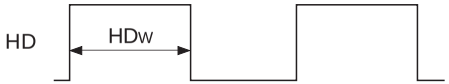
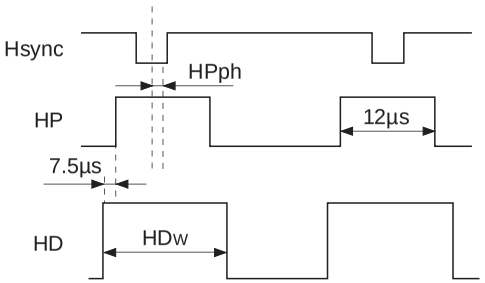
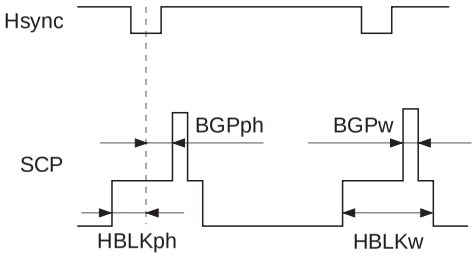
Pin No.	Symbol	Equivalent circuit	Description
34	SCL		I²C bus standard SCL (Serial Clock) input.
35	SDA		I²C bus standard SDA (Serial Data) input/output.
36	YUV SW		YUV SW control pin. Selects external YUV input. Vth: 0.7V This switch includes a function for forcibly turning OFF external Y input only using Y SEL of the bus.
37	EY IN		External Y/R-Y/B-Y signal input. Input is via a 0.01µF capacitor. EY IN: 0.7Vp-p (no sync) ER-Y IN: 0.735Vp-p (75% color bar) EB-Y IN: 0.931Vp-p (75% color bar)
38 39	ER-Y IN EB-Y IN		
40	GND2		GND pin for signal block circuits.

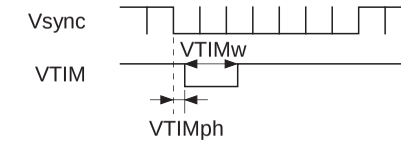
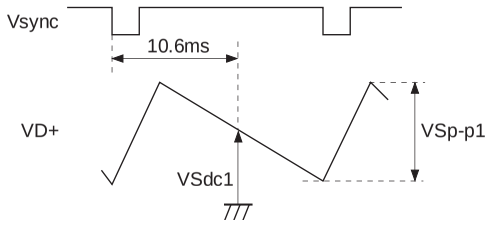
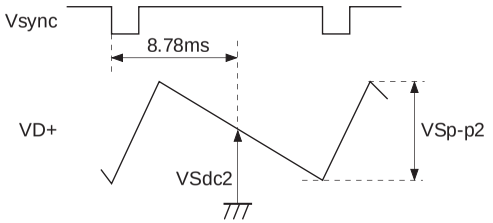
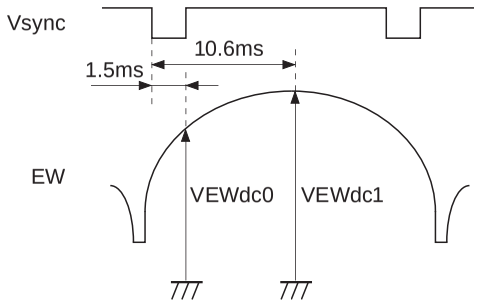
Pin No.	Symbol	Equivalent circuit	Description
41	CVBS2/Y2 IN		CVBS signal/luminance signal input. A 1Vp-p signal (including sync) is input via a 1µF capacitor. Input the Y signal when a separated Y/C signal is input.
42	ABL FIL		Connects the capacitor (4.7µF) forming the ABL control signal LPF to GND.
43	TV/C2 IN		Input of CVBS signal from a TV tuner or chroma signal. A 1Vp-p (including sync) CVBS signal or 300mVp-p burst chroma signal is input via a 1µF capacitor.
44	Vcc2		Power pin for the signal block.
45	APC FIL		Connects a chroma APC lag lead filter. CR is connected to GND.

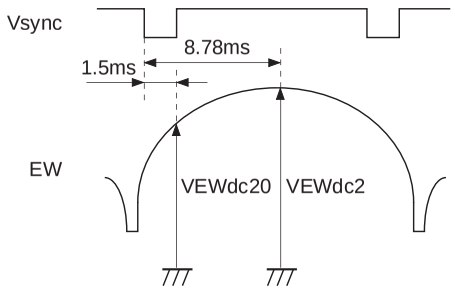
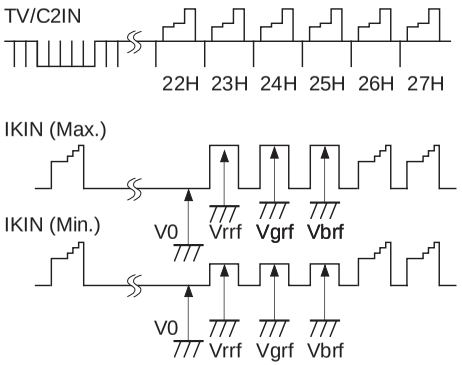
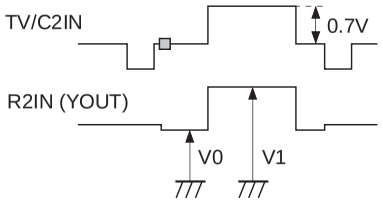
Pin No.	Symbol	Equivalent circuit	Description
46	X'tal 3		Connects an APC crystal. The crystals should be connected as follows. X'tal 3: PAL-N crystal (3.58205625MHz) X'tal 2: NTSC crystal (3.579545MHz) X'tal 1: PAL/SECAM crystal (4.43361875MHz) or PAL-M crystal (3.57561149MHz) Pin 46 can be switched for use as FSC output using the FSCSW register. 2V DC, 0.7Vp-p signal is output.
47	X'tal 2		
48	X'tal 1		

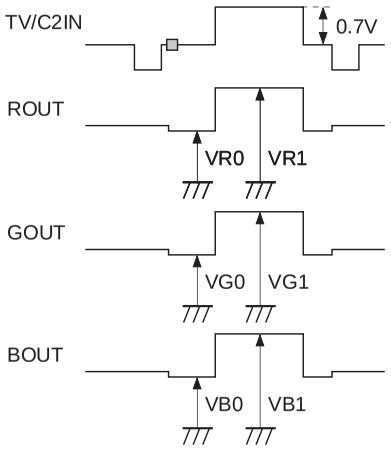
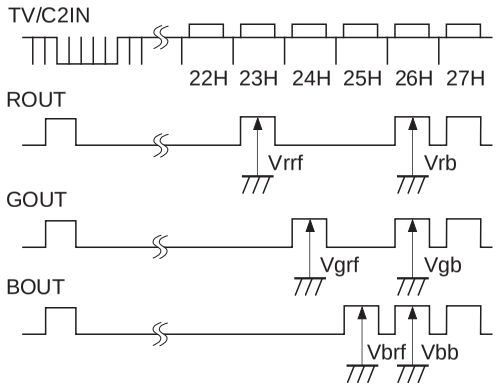
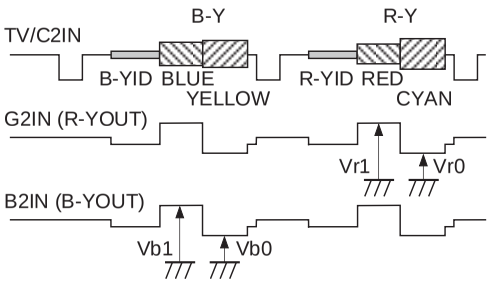
Electrical Characteristics Measurement Conditions

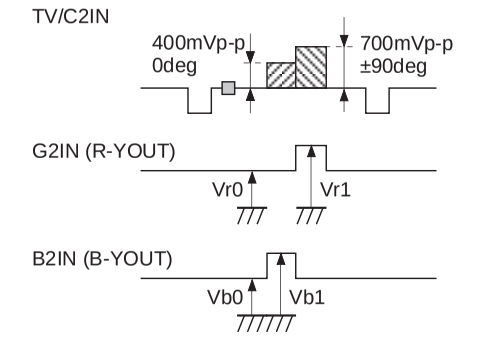
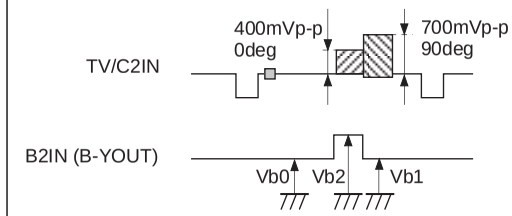
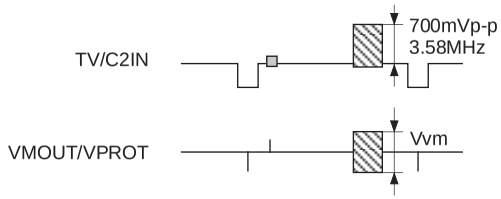
Set I^2C bus registers to I^2C Bus Register Initial Setting Values and measure them. Ta = 25°C, $V_{CC}1$, $V_{CC}2$ = 9V, GND1, GND2 = 0V

No.	Item	Symbol	Measurement conditions	Measure-ment pin	Measurement contents	Min.	Typ.	Max.	Unit
1	Current consumption	I_{CC}	$V_{CC}1$, $V_{CC}2$ = 9V Bus data: initial setting values	33, 44	Measure the current flowing into the pin.	80	125	170	mA
Sync deflection block items									
2	Horizontal free-running frequency	fHFR	HOSC = 7 (no input signal) FH HIGH = 1	19	H drive output frequency	15.5	15.7	15.9	kHz
3	Horizontal free-running frequency 2	fHHIFR	FH HIGH = 0			16.2	16.7	17.2	kHz
4	HD pulse width	HDw	HDW = 0			22.5	24	25.5	µs
5	HD pulse width 2	HDw	HDW = 1 tstr (HP) = 7.5µs, tHP = 12µs			19	20	21	µs
6	HP phase	HPph	HPph = HP (cent) – Hsync (cent)	18		3.0	3.7	4.4	µs
7	H BLK phase	HBLKph	HBLKph = SCP (HBLKrise) – Hsync (cent)	17		–2.5	–1.75	–1	µs
8	H BLK pulse width	HBLKw				9	10	11	µs
9	BGP phase	BGPph	BGPph = SCP (BGPrise) – Hsync (cent)			3.4	3.9	4.4	µs
10	BGP pulse width	BGPw				2.8	3.0	3.2	µs

No.	Item	Symbol	Measurement conditions	Measure-ment pin	Measurement contents	Min.	Typ.	Max.	Unit
11	VTIM phase	VTIMph	C/D non-standard mode VTIMph = VTIM (fall) – Vsync (fall)	5		10	20	30	µs
12	VTIM pulse width	VTIMw				45	60	75	µs
13	V drive output center voltage (50Hz)	VSdc1	50Hz	13		3.4	3.6	3.8	V
14	V drive output amplitude (50Hz)	VSp-p1	50Hz			1.2	1.35	1.5	V
15	V drive output center voltage (60Hz)	ΔVSdc	60Hz – 50Hz ΔVSdc = VSdc2 – VSdc1	13		–10	0	10	mV
16	V drive output amplitude (60Hz)	ΔVSp-p	60Hz/50Hz ΔVSp-p = VSp-p2/VSp-p1 × 100			99	100	101	%
17	EW drive output center voltage (50Hz)	VEWdc1	50Hz	11		3.9	4.1	4.3	V
18	EW drive output amplitude (50Hz)	VEWp-p	50Hz VEWp-p = VEWdc1 – VEWdc0			450	560	670	mV

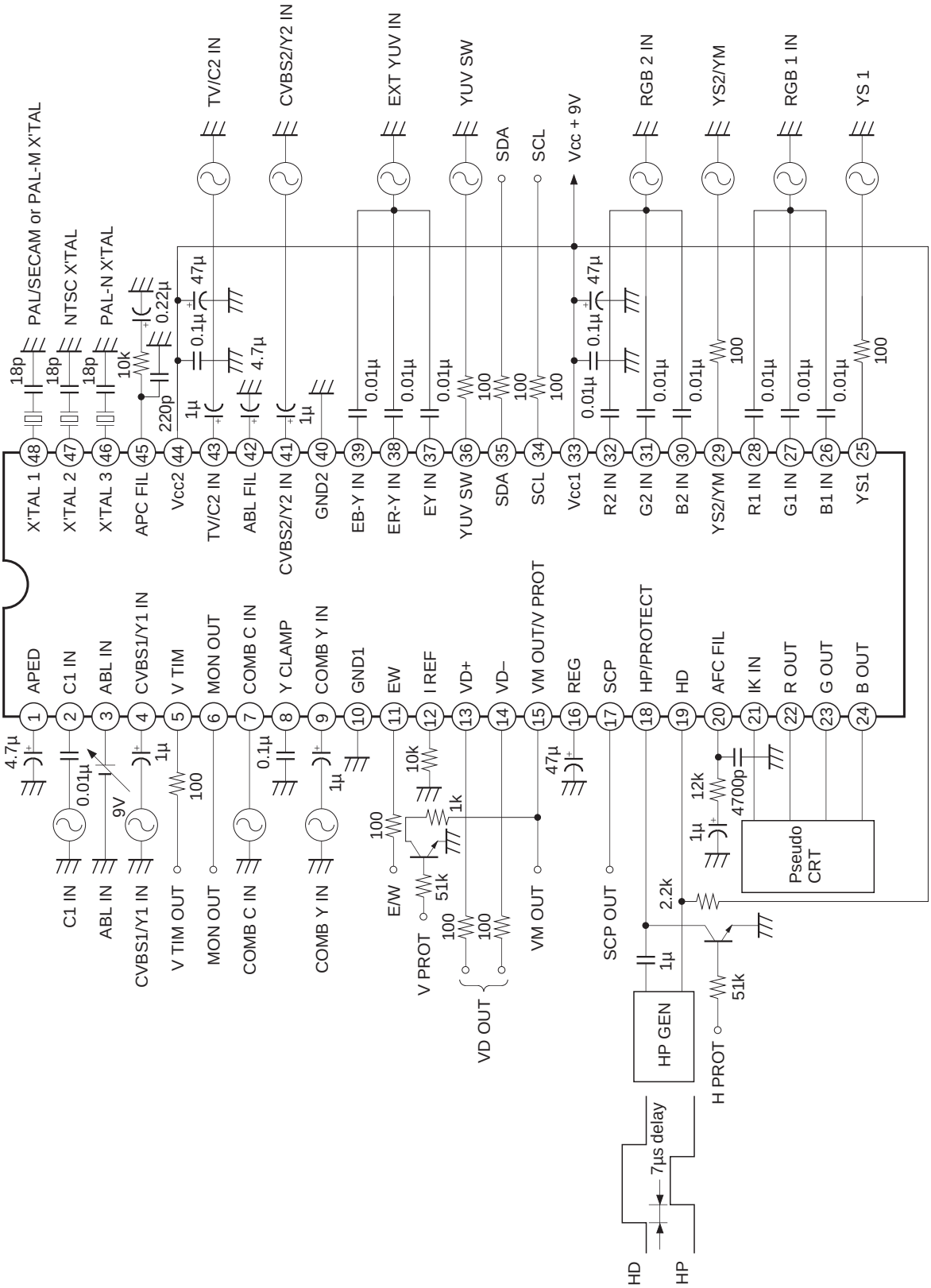
No.	Item	Symbol	Measurement conditions	Measure-ment pin	Measurement contents	Min.	Typ.	Max.	Unit
19	EW DRIVE output center voltage (60Hz)	ΔVEWdc	60Hz – 50Hz ΔVEWdc = VEWdc2 – VEWdc1	11		–10	0	10	mV
20	EW DRIVE output amplitude (60Hz)	ΔVEWp-p	60Hz/50Hz ΔVEWp-p = (VEWdc2 – VEWdc20)/ VEWp-p × 100			97	100	103	%
Signal block items									
21	R BLK voltage	VRBLK	P ON = 0	22	Measure the pin voltage.	0	0.15	0.3	V
22	G BLK voltage	VGBLK		23		0	0.15	0.3	V
23	B BLK voltage	VBBLK		24		0	0.15	0.3	V
24	IK current (Max.)	IIK	R CUTOFF = Fh G CUTOFF = Fh B CUTOFF = Fh IIK = (Vrrf – V0)/4k	21		15	22	29	μA
25	IK current (Min.)	ΔIIK	R CUTOFF = 0h G CUTOFF = 0h B CUTOFF = 0h IIKmin/IIKmax	21		27	32	37	%
26	Luminance (Y) output	Vy	YUV OUT = 1 Vy = V1 – V0	32		610	670	730	mV

No.	Item	Symbol	Measurement conditions	Measure-ment pin	Measurement contents	Min.	Typ.	Max.	Unit
27	RGB amplitude ratio	ΔG	$\Delta G_R = 20 \times \log ((VR1 - VR0)/Vy)$ $\Delta G_G = 20 \times \log ((VG1 - VG0)/Vy)$ $\Delta G_B = 20 \times \log ((VB1 - VB0)/Vy)$	22, 23, 24		12	13.5	15	dB
28	RGB BRIGHT voltage	Vbrt	Black level – Ref. P. level Rch: Vbrtr = Vrb – Vrrf Gch: Vbrtg = Vgb – Vgrf Bch: Vbrtb = Vbb – Vbrf	22, 23, 24		–450	–400	–350	mV
29	SECAM color difference (R-Y) output	Vr-y	SECAM signal (75%) Vr-y = Vr1 – Vr0	31		690	800	910	mV
30	SECAM color difference (B-Y) output	Vb-y	SECAM signal (75%) Vb-y = Vb1 – Vb0	30		880	1040	1200	mV

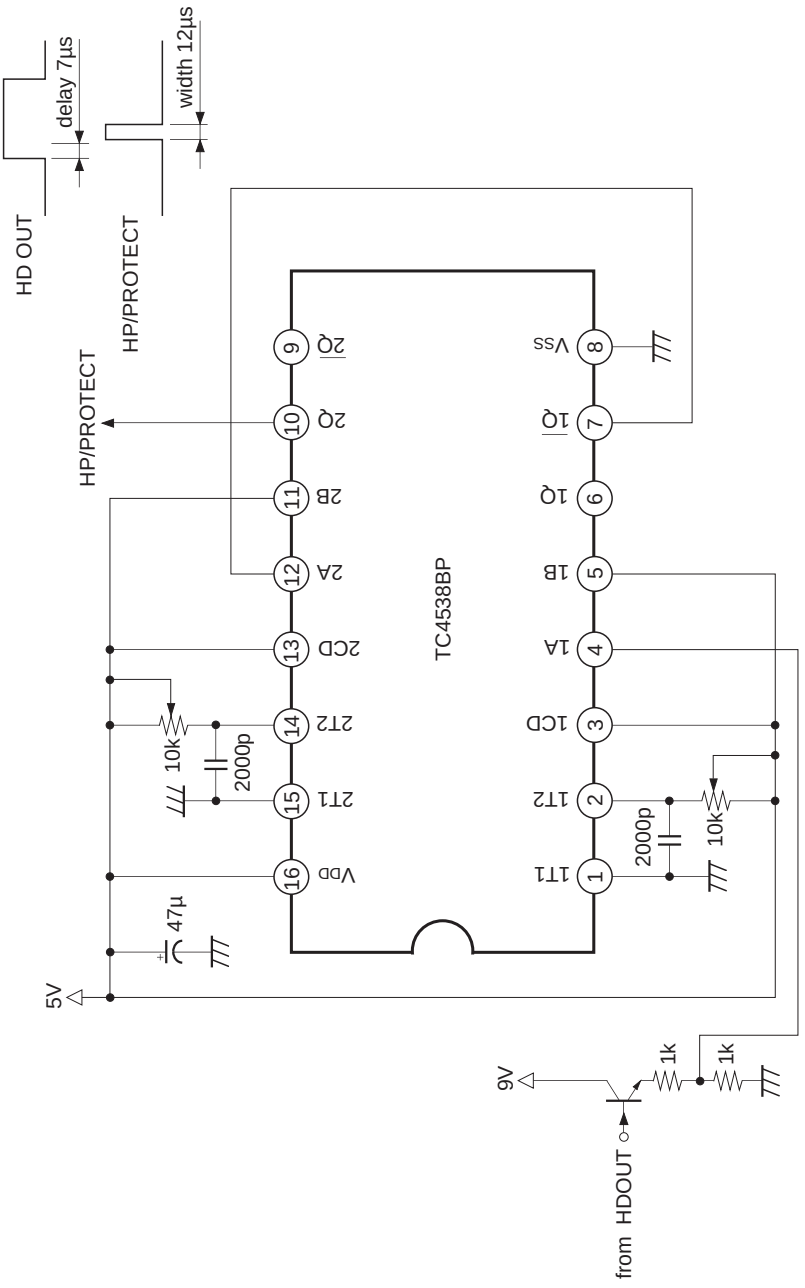
No.	Item	Symbol	Measurement conditions	Measure-ment pin	Measurement contents	Min.	Typ.	Max.	Unit
31	PAL color difference (R-Y) output	Vr-y	PAL signal Vr-y = Vr1 – Vr0	31		900	1000	1100	mV
32	PAL color difference (B-Y) output	Vb-y	PAL signal Vb-y = Vb1 – Vb0	30		430	500	570	mV
33	HUE center offset	ϕoffset	YUV OUT = 1, NTSC signal ϕoffset = $\tan^{-1}$ (4/7 × ((Vb1 – Vb0)/ (Vb2 – Vb0)))	30, 31		–6	0	6	Deg
34	VM output	Vvm	3.58MHz 700mVp-p	15		1.8	2.3	2.8	V
35	FSC output	Vfsc	FSC SW = 1	46		500	900	1300	mV

Electrical Characteristics Measurement Circuit

Signal sources ⏦ are all GND unless otherwise specified in the measurement column for Electrical Characteristics.



HP GEN Circuit



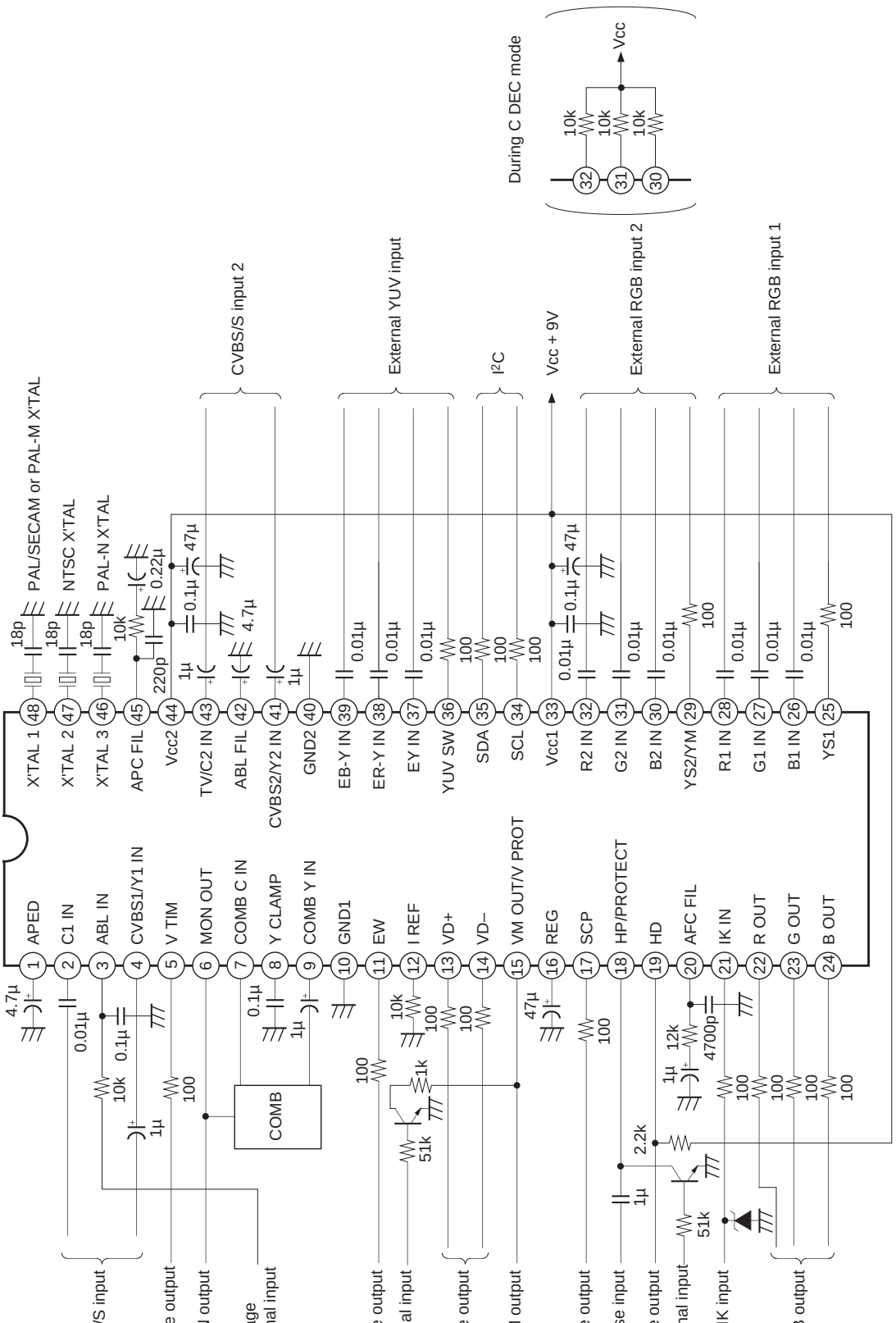
Electrical Characteristics Measurement Conditions (I^2C Bus Register Initial Settings)

Register name	Number of bits	Initial setting value	Description
P ON	1	1	RGB output ON
HD W	1	0	HD pulse width normal
AXIS PAL	1	0	PAL axis forced OFF
V ON	1	1	VD ON
FH HIGH	1	1	fH normal
YUV OUT	1	0	RGB2 IN input mode
AGING	1	0	AGING OFF
VIDEO SEL	2	0	Selects TV input
S SEL	2	0	Selects TV/CVBS/BLK
R ON	1	1	R output ON
G ON	1	1	G output ON
B ON	1	1	B output ON
Y SEL	1	0	Enables YUVSW switching
X'TAL	2	3	Automatically identified
COL SYSTEM	2	3	Automatically identified
COL LOOP	2	1	Automatically identified at 4STD
C BPF	1	1	BPF ON
C TRAP OFF	1	0	TRAP ON
PICTURE	6	3Fh	Max. value
NO COLOR	1	0	No signal = NTSC
FSC SW	1	0	FSC OFF
COLOR	6	1Fh	Center value
C OFF	1	0	C signal ON
KILLER OFF	1	0	Cancels KILLER OFF forced OFF mode
HUE	6	1Fh	Center value
SHP F0	1	0	F0 2.5MHz
AXIS NTSC	1	0	NTSC JAPAN axis
BRIGHT	6	1Fh	Center value
DC TRAN	1	0	100%
PRE/OVER	1	0	1:1
SHARPNESS	4	7h	Center value
R CUTOFF	4	7h	Center value
G CUTOFF	4	7h	Center value
B CUTOFF	4	7h	Center value

Register name	Number of bits	Initial setting value	Description
R DRIVE	6	3Fh	Max. value
ABL MODE	1	1	PICTURE/BRIGHT shared mode
ABL VTH	1	0	VTH = 3V
G DRIVE	6	3Fh	Max. value
DY COL	1	0	Dynamic color OFF
RGB SEL	1	0	Enables YS1 SW switching
B DRIVE	6	3Fh	Max. value
GAMMA	2	0	Gamma correction OFF
H OSC	4	7h	Center value
Y DELAY	4	7h	Center value
FIELD FREQ	2	0	Automatically identified (free-running 50Hz)
CD MODE	2	0	Standard mode
INTERLACE	2	0	Interlace mode
H SS	1	0	1/3 from sync tip
V SS	1	0	1/3 from sync tip
V SIZE	6	1Fh	Center value
H MASK	1	0	Macrovision countermeasure OFF
V POSITION	6	1Fh	Center value
AFC GAIN	2	1	Gain medium
SCORRECTION	4	0	No correction
V LINEARITY	4	7h	100%
H SIZE	6	1Fh	Center value
EW DC	1	0	DC level standard mode
H POSITION	6	1Fh	Center value
PIN AMP	6	1Fh	Center value
CORNER PIN	6	1Fh	Center value
TRAPEZIUM	4	7h	Center value
EHT COMP	4	Fh	Max. correction level
AFC BOW	4	7h	Center value
AFC ANGLE	4	7h	Center value
LEFT HBLK	4	7h	Center value
RIGHT HBLK	4	7h	Center value
ASPECT	6	2Fh	Center value
H BLK	1	0	H BLK width variability OFF
VUNDERSCAN	1	0	OFF

Register name	Number of bits	Initial setting value	Description
SCROLL	6	1Fh	Center value
V ZOOM	1	0	Zoom OFF
UPPER VLIN	4	0	Linearity 100%
LOWER VLIN	4	0	Linearity 100%
V TIM SEL	2	0	V timing pulse output
ID STOP	2	1	Center value
ID START	2	2	Center value
BELL F0	6	1Fh	Center value
ID LEVEL	2	1	Center value

Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Register Table

Sleve Address

Slave ADD pin = GND 88H: Slave Receiver 89H: Slave Transmitter
Slave ADD pin = V_{CC} 8AH: Slave Receiver 8BH: Slave Transmitter

Control Register (Sub Address 00000 results in Power-On-Reset)

Sub Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
x x x 0 0 0 0 0	P ON	HD W	AXIS PAL	V ON	FH HIGH	YUV OUT	AGING	0
x x x 0 0 0 0 1	VIDEO SEL		S SEL		R ON	G ON	B ON	Y SEL
x x x 0 0 0 1 0	X'TAL		COL SYSTEM		COL LOOP		C BPF	C TRAP OFF
x x x 0 0 0 1 1	PICTURE						NO COLOR	FSCSW
x x x 0 0 1 0 0	COLOR						C OFF	KILLER OFF
x x x 0 0 1 0 1	HUE						SHP F0	AXIS NTSC
x x x 0 0 1 1 0	BRIGHT						DC TRAN	PRE/OVER
x x x 0 0 1 1 1	SHARPNESS				R CUTOFF			
x x x 0 1 0 0 0	G CUTOFF				B CUTOFF			
x x x 0 1 0 0 1	R DRIVE						ABL MODE	ABL VTH
x x x 0 1 0 1 0	G DRIVE						DY COL	RGB SEL
x x x 0 1 0 1 1	B DRIVE						GAMMA	
x x x 0 1 1 0 0	H OSC				Y DELAY			
x x x 0 1 1 0 1	FIELD FREQ		CD MODE		INTERLACE		H SS	V SS
x x x 0 1 1 1 0	V SIZE						*	H MASK
x x x 0 1 1 1 1	V POSITION						AFC GAIN	
x x x 1 0 0 0 0	S CORRECTION				V LINEARITY			
x x x 1 0 0 0 1	H SIZE						*	EW DC
x x x 1 0 0 1 0	H POSITION						*	*
x x x 1 0 0 1 1	PIN AMP						*	*
x x x 1 0 1 0 0	CORNER PIN						*	*
x x x 1 0 1 0 1	TRAPEZIUM				EHT COMP			
x x x 1 0 1 1 0	AFC BOW				AFC ANGLE			
x x x 1 0 1 1 1	LEFT HBLK				RIGHT HBLK			
x x x 1 1 0 0 0	ASPECT						H BLK	V UNDER SCAN
x x x 1 1 0 0 1	SCROLL						V ZOOM	*
x x x 1 1 0 1 0	UPPER VLIN				LOWER VLIN			
x x x 1 1 0 1 1	0	0	VTIM SEL		ID STOP		ID START	
x x x 1 1 1 0 0	BELL F0						ID LEVEL	

Status Register

1st BYTE	H LOCK	IKR	V NG	H NG	APC LOCK	PAL	SECAM	FIELD ID
2nd BYTE	H CENT	X'TAL ID		NO VSYNC	RF LEVEL		0	1

Description of Registers

Register Name (Number of Bits) Description

1. Y Signal Block Registers

VIDEOSEL (2) Switches the VIDEO switch to select various input signals.
Enabled when S SEL = 0 or 3.
0 = Selects TV input signal
1 = Selects CVBS1 input signal
2 = Selects CVBS2 input signal
3 = Mute

S SEL (2) Selects Y/C input signals.
Set VIDEO SEL to 3 (Mute) when S SEL is set to 1 or 2.
0 = Selects one of TV, CVBS1 or CVBS2 input, or Mute
1 = Selects Y1/C1 input
2 = Selects Y2/C2 input
3 = Selects Y/C input from comb filter
(In this case, select one of TV, CVBS1 or CVBS2 input, or Mute for MON OUT.)

C TRAP OFF (1) ON/OFF switch for Y block chroma trap filter
Set the chroma trap filter to OFF (= 1) using microcomputer control as necessary when APC LOCK and SECAM status are 0.
0 = Trap filter ON
1 = Trap filter OFF

SHP F0 (1) Switches sharpness f0
0 = 2.5MHz
1 = 3.0MHz

SHARPNESS (4) Sharpness gain control
0h = –12dB
7h = +3.5dB
Fh = +9dB

DC TRAN (1) Switches the DC transmission rate
0 = 100%
1 = 85%

PRE/OVER (1) Sharpness preshoot/overshoot control
0 = 1:1
1 = 2:1

Y DELAY (4) Y signal delay control
0h = MIN
Fh = MAX

Y SEL (1) Internal Y signal fixed mode ON/OFF switch
0 = YUV SW (Pin 36) standard operation (When Pin 36 = high, selects EY IN, ER-Y IN, EB-Y IN input)
1 = EY IN (Pin 37) input only disabled (When Pin 36 = high, selects internal Y, ER-Y IN, EB-Y IN input)

AGING (1) White output aging mode ON/OFF switch (set to 0 at power ON)
0 = Aging mode OFF
1 = Aging mode ON
(The Y block outputs a 60 IRE flat signal when there is no input signal.)

2. Chroma Signal Block Registers

COLOR SYSTEM (2) Color system setting
0 = Forced PAL
1 = Forced SECAM
2 = Forced NTSC
3 = Automatic identification mode

X'TAL (2) Crystal setting
0 = Forced X'TAL1 (PAL/SECAM or PAL-M crystal)
1 = Forced X'TAL2 (NTSC crystal)
2 = Forced X'TAL3 (PAL-N crystal)
3 = Automatic identification mode

COLOR LOOP (2) Identification loop setting in color system automatic identification mode
0 = Automatically identifies the three systems PAL, SECAM and NTSC 4.43 (one crystal: 4.43 MHz)
1 = Automatically identifies the four systems PAL, SECAM, NTSC and NTSC 4.43 (two crystals: 4.43 and 3.58 MHz)
2 = Automatically identifies the three systems PAL-M, PAL-N, and NTSC (three crystals)
3 = Do not use

HUE (6) Hue control (Phase control for the chroma demodulation axis. Enabled for NTSC only.)
0h = –35°
3Fh = +35°

COLOR (6) Color gain control
0h = –30dB or less
1Fh = 0dB
3Fh = +6dB

C OFF (1) Chroma signal ON/OFF switch
0 = Chroma signal ON
1 = Chroma signal OFF

FSC SW (1) FSC signal ON/OFF switch
0 = FSC OFF: used as crystal pin
1 = FSC ON: outputs 700mVp-p FSC

C BPF (1) Chroma band pass filter ON/OFF switch
0 = Band pass filter OFF
1 = Band pass filter ON

AXIS NTSC (1) In NTSC mode, this switch selects Japan axis or US axis color detection axis.
This is valid when AXIS PAL = 0.
(This is automatically switched to PAL/SECAM detection axis in PAL/SECAM mode.)
0 = Set to Japan axis
B-Y: 0°/1, R-Y: 95°/0.78, G-Y: 236°/0.33
1 = Set to US axis
B-Y: 0°/1, R-Y: 102°/0.78, G-Y: 236°/0.3

AXIS PAL (1) Switch for forcing the color detection axis to an orthogonal axis (PAL axis)
0 = Forced OFF
1 = Orthogonal axis forced ON
B-Y: 0°/1, R-Y: 90°/0.57, G-Y: 227°/0.34

NO COLOR (1) This switch switches the no signal definition for the chroma signal in the PAL (/NTSC) status register.
0 = PAL status register is 1 when there is no signal
1 = PAL status register is 0 when there is no signal

YUV OUT (1) This switch switches the R2 IN, G2 IN and B2 IN input pins (Pins 32, 31 and 30) to the Y and color difference signal output pins.
0 = R2 IN, G2 IN and B2 IN signal input mode
1 = Pin 30: B-Y output
Pin 31: R-Y output
Pin 32: Y output (At this time, connect each pin to Vcc via a 10kΩ resistor.)

KILLER OFF (1) Color killer ON/OFF switch
0 = Color killer standard mode
1 = Color killer forced OFF mode

ID START (2) The position at which the SECAM identification pulse starts can be changed. (0.2µs/STEP)
0 = Delayed 0.4µs to center position.
2 = Center
3 = Advanced 0.2µs to center position.

ID STOP (2) The position at which the SECAM identification pulse stops can be changed. (0.2µs/STEP)
0 = Delayed 0.2µs to center position.
1 = Center
3 = Advanced 0.4µs to center position.
SECAM identification performance can be optimized by adjusting these together with the ID LEVEL register.
Color is more easily applied when the identification pulse width is wide and less easily applied when it is narrow.

BELL F0 (6) BELL Filter f0 adjustment (0.7%/STEP)
0h = f0 – 16%
1Fh = f0 center
3Fh = f0 + 16%

ID LEVEL (2) SECAM identification level setting
SECAM identification performance can be optimized by adjusting this together with ID START/STOP registers.
0 = Color is less easily applied
3 = Color is easily applied

3. RGB Signal Block Registers

PICTURE (6) Picture gain control
0h = –15dB
3Fh = 0dB (During 0.7Vp-p input: RGB output 3.0Vp-p, gamma OFF, DRIVE MAX)

BRIGHT (6) Brightness control (RGB DC bias control)
0h = –30 IRE to center
1Fh = –12 IRE to reference pulse
3Fh = +30 IRE to center (100 IRE = 2.4Vp-p)

R DRIVE (6) R output drive control
0h = 1.5Vp-p
3Fh = 3.0Vp-p (PICTURE: MAX)

G DRIVE (6) G output drive control
0h = 1.5Vp-p
3Fh = 3.0Vp-p (PICTURE: MAX)

B DRIVE (6) B output drive control
0h = 1.5Vp-p
3Fh = 3.0Vp-p (PICTURE: MAX)

R CUTOFF (4) RGB output cutoff control
G CUTOFF (4) (Input current of reference pulse excluding leak component)
B CUTOFF (4) 0h = 6.5µA
7h = 13µA
Fh = 19µA

GAMMA (2) RGB output gamma correction control
0 = Gamma correction OFF
3 = +12 IRE correction to 40 IRE input (PICTURE: MAX)

ABL MODE (1) Switches ABL mode
0 = Mode in which only picture ABL functions
1 = Mode for both picture ABL and bright ABL

ABL VTH (1) Switch for switching ABL control signal detection level (VTH)
0 = VTH: 3V
1 = VTH: 1V

DYNAMIC C (1) Dynamic color function ON/OFF switch
0 = Dynamic color OFF
1 = Dynamic color ON

RGB SEL (1) Disables switching of the YS1 switch and disallows input of external signals from RGB1.
0 = YS1 standard mode
1 = YS1 forced OFF mode

P ON (1) Switch for blanking all RGB output signals including the AKB reference pulse (set to 0 at power ON)
0 = RGB output blanking (AKB reference pulse is also not output)
1 = RGB output ON

R ON (1) Switch for blanking the R output signal not including the AKB reference pulse
0 = R output blanking
1 = R output ON

G ON (1) Switch for blanking the G output signal not including the AKB reference pulse
0 = G output blanking
1 = G output ON

B ON (1) Switch for blanking the B output signal not including the AKB reference pulse
0 = B output blanking
1 = B output ON

4. Deflection Block Registers

H OSC (4) H VCO oscillation frequency adjustment (40Hz/STEP)
0h = Low
Fh = High

V SS (1) Switches the slice level for vertical sync signal separation
0 = 1/3 (from sync tip)
1 = 1/4 (from sync tip)

H MASK (1) Macrovision countermeasure ON/OFF
0 = OFF
1 = ON

H SS (1) Switches the slice level for horizontal sync signal separation
0 = 1/3 (from sync tip)
1 = 1/4 (from sync tip)

VTIM SEL (2) Selects the signal output on the VTIM pin (Pin 5).
0 = V retrace timing pulse
1 = Horizontal sync signal
2 = Vertical sync separation signal
3 = Do not use

CD MODE (2) V countdown system mode switching
0 = Standard mode (used during RF signal input)
1 = Mode where time constant used during countdown mode switching has been lowered from standard mode (used during VCR signal input)
2 = Fixed wide window mode
This setting is recommended when shortening the lock time.
3 = Do not use

FIELD FREQ (2) Sets the V frequency mode
0 = Automatic identification mode (selects 50Hz when there is no signal)
1 = Automatic identification mode (selects 60Hz when there is no signal)
2 = Forced 50Hz
3 = Forced 60Hz

INTERLACE (2) Switches interlace/non-interlace mode
0, 1 = Interlace mode
2 = Non-interlace mode (even fields are shifted +1/2H)
3 = Non-interlace mode (odd fields are shifted +1/2H)

AFC GAIN (2) AFC loop gain control (PLL for H sync and H VCO)
0 = Gain high
1 = Gain medium
2 = Gain low
3 = Gain minimum

H POSITION (6) Horizontal picture position adjustment (HAFC phase control)
0h = 2µs delay (right picture position: picture delayed to HD)
3Fh = 2µs advance (left picture position: picture advanced to HD)

AFC BOW (4) Vertical line bow compensation amount adjustment
(phase control using HAFC parabola wave)
0h = Top and bottom of picture delayed 380ns to picture center
7h = Center
Fh = Top and bottom of picture advanced 380ns to picture center

AFC ANGLE (4) Vertical line slope compensation amount adjustment
(phase control using HAFC VSAW)
0h = Top of picture delayed 320ns and bottom of picture advanced 320ns to picture center
7h = Center
Fh = Top of picture advanced 320ns and bottom of picture delayed 320ns to picture center

LEFT HBLK (4) Controls the BLK width on the left side of the picture when HBLK = 1
0h = +1.2µs: HBLK max. width
7h = Center
Fh = –1.2µs: HBLK min. width

RIGHT HBLK (4) Controls the BLK width on the right side of the picture when HBLK = 1
0h = +1.2µs: HBLK max. width
7h = Center
Fh = –1.2µs: HBLK min. width

HBLK (1) HBLK width control switch when a 16:9 CRT is in 4:3 soft normal mode
0 = Control OFF
1 = Control ON

FH HI (1) Increases the free-running frequency of the H oscillation frequency 1kHz.
(ON mode set at power ON)
0 = Max. frequency mode ON
1 = Max. frequency mode OFF (standard free-running frequency)

HD W (1) HD pulse width switch (set to 0 at power ON)
0 = Standard mode (25µs pulse width)
1 = Narrow pulse width mode (use this mode when the time between the HD rising edge and FBP rising edge is short)

V SIZE (6) Vertical picture size adjustment (VD output gain control)
0h = –15% (min. size)
1Fh = 0%
3Fh = +15% (max. size)

V POSITION (6) Vertical picture position adjustment (DC bias control for VD output)
0h = –0.1V (lowers picture position)
1Fh = 0V (center 3V DC)
3Fh = +0.1V (raises picture position)

S CORRECTION (4) Vertical S distortion correction amount adjustment
(gain control for secondary component of VD)
0h = Secondary component amplitude added to the VD signal is 0mVp-p
Fh = Secondary component amplitude added to the VD signal is 100mVp-p

V LINEALITY (4) Vertical linearity adjustment (gain control for secondary component of VD)
0h = 85% (picture bottom/picture top) picture top enlarged
1Fh = 100% (picture bottom/picture top)
3Fh = 115% (picture bottom/picture top) picture top compressed

EHT COMP (4) High-voltage fluctuation compensation setting for vertical picture size
(gain control for VD output)
0h = 0%
Fh = –5% (max. compensation)

V ON (1) VD output ON/OFF switch (set to 0 at power ON)
0 = DC voltage
1 = Sawtooth wave

H SIZE (6) Horizontal picture size adjustment (DC bias control for EW output)
0Fh = –0.5V (small horizontal picture size)
1Fh = 0V (center 4V DC)
3Fh = +0.5V (large horizontal picture size)

PIN AMP (6) Horizontal pin distortion compensation amount adjustment
(gain control for V parabola wave)
0h = 0.15Vp-p (large horizontal size at picture top and bottom: min. compensation)
1Fh = 0.7Vp-p
3Fh = 1.3Vp-p (small horizontal size at picture top and bottom: max. compensation)

CORNER PIN (6) Picture top and bottom pin distortion compensation amount adjustment
(top/bottom gain control for V parabola wave)
0h = –0.4V (small horizontal size at picture top and bottom: max. compensation)
3Fh = +0.4V (large horizontal size at picture top and bottom: min. compensation)

TRAPEZIUM (4) Horizontal trapezium distortion amount compensation
(phase control for parabola wave)
0h = 1.5ms advance (large horizontal size at picture top: small horizontal size at bottom)
Fh = 1.5ms delay (small horizontal size at picture top: large horizontal size at bottom)

ASPECT (6) Aspect ratio control (gain control for sawtooth wave)
0h = 75% 16:9 CRT Full
2Fh = 100% 4:3 CRT Full
3Fh = 110%

SCROLL (6) Vertical picture scroll control when a 16:9 CRT is in zoom mode
0h = Scrolls 32H toward picture bottom and zooms picture bottom
1Fh = Center
3Fh = Scrolls 32H toward picture top and zooms picture top

UPPER VLIN (4) Adjusts vertical linearity of picture top.
0h = 100% (picture top/picture bottom)
1Fh = 85% (picture top/picture bottom, picture top size is compressed)

LOWER VLIN (4) Adjusts vertical linearity of picture bottom.
0h = 100% (picture bottom/picture top)
1Fh = 75% (picture bottom/picture top, picture bottom size is compressed)

V UNDER SCAN (1) This mode is for compressing the vertical sawtooth wave.
0 = OFF
1 = ON
Compressed to 50% when ASPECT = 0h
Compressed to 75% when ASPECT = 3Fh
RGB vertical blanking is increased by 10H at both top and bottom at this time.

V ZOOM (1) Zoom mode ON/OFF switch for 16:9 CRTs
0 = Zoom OFF
1 = Zoom ON (Top and bottom of picture are together cut 25% when ASPECT = 2Fh.
RGB output also undergoes blanking during this interval.)

EW DC (1) This mode lowers the DC level of the V parabola wave when 4:3 deflection is used for a 16:9 CRT.
0 = OFF
1 = ON (DC level lowered) It is necessary at this time to readjust for pin distortion when EWDC = 0 is used for the picture distortion compensation.

5. Status Registers

H LOCK (1) Lock status for H Sync and H VCO
0 = Free-running status
1 = H Sync and H VCO are locked

IKR (1) AKB operation status
0 = AKB loop not stable
1 = AKB loop stable

V NG (1) V protect status
0 = V protect OFF (IC normal operation status)
1 = V protect ON (RGB output undergoes complete blanking at this time)

H NG (1) X-ray protect status
0 = H drive output ON
1 = H drive output OFF (HD output is high impedance at this time and RGB output undergoes blanking. It is necessary to turn the IC's power OFF then ON again to cancel this status.)

APC LOCK (1) Lock status for input chroma signal and APC for PAL/NTSC
0 = APC not locked
(Color killer when APC LOCK = 0 and SECAM = 0)
1 = APC locked

PAL (1) PAL identification status
When NO COLOR = 0
0 = NTSC
1 = PAL or NO SIG (KILLER ID ON)
When NO COLOR = 1
0 = NTSC or NO SIG (KILLER ID ON)
1 = PAL

SECAM (1) SECAM identification status
0 = Identified as not SECAM
(Color killer when APC LOCK = 0 and SECAM = 0)
1 = Identified as SECAM

FIELD ID (1) V drive oscillation frequency
0 = 60Hz mode
1 = 50Hz mode

H CENT (1) H VCO status
0 = The H VCO oscillation frequency is higher than the horizontal frequency of the input signal selected by the VIDEO SW
1 = The H VCO oscillation frequency is lower than the horizontal frequency of the input signal selected by the VIDEO SW

X'TAL ID (2) Crystal selection status
0 = Identified as X'TAL1 (Pin 48 crystal)
1 = Identified as X'TAL2 (Pin 47 crystal)
2 = Identified as X'TAL3 (Pin 46 crystal)

NO VSYNC (1) VSS presence status
Weak electromagnetic field detection can be performed according to RF LEVEL status.
0 = VSS present
1 = VSS not present

RF LEVEL (2) RF weak electromagnetic field level
0 = Strong electromagnetic field
1 = Medium electromagnetic field
2 = Weak electromagnetic field
3 = Very weak electromagnetic field

I²C Bus Power-On Initial Settings

The initial settings listed here for power-on when V drive starts to oscillate are reference values; the actual settings may be determined as needed according to the conditions under which the set is to be used.

Register Table

"∗": Undefined

Control Registers

Sub Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
x x x 0 0 0 0 0 00 h	0	0	0	1	1	0	0	0
x x x 0 0 0 0 1 01 h	0	0	0	0	0	0	0	0
x x x 0 0 0 1 0 02 h	1	1	1	1	0	1	1	0
x x x 0 0 0 1 1 03 h	1	1	1	1	1	1	0	0
x x x 0 0 1 0 0 04 h	0	1	1	1	1	1	0	0
x x x 0 0 1 0 1 05 h	0	1	1	1	1	1	0	0
x x x 0 0 1 1 0 06 h	0	1	1	1	1	1	0	0
x x x 0 0 1 1 1 07 h	0	1	1	1	0	1	1	1
x x x 0 1 0 0 0 08 h	0	1	1	1	0	1	1	1
x x x 0 1 0 0 1 09 h	0	1	1	1	1	1	1	0
x x x 0 1 0 1 0 0A h	0	1	1	1	1	1	0	0
x x x 0 1 0 1 1 0B h	0	1	1	1	1	1	0	0
x x x 0 1 1 0 0 0C h	0	1	1	1	0	1	1	1
x x x 0 1 1 0 1 0D h	0	0	0	0	0	0	0	0
x x x 0 1 1 1 0 0E h	0	1	1	1	1	1	∗	0
x x x 0 1 1 1 1 0F h	0	1	1	1	1	1	0	1
x x x 1 0 0 0 0 10 h	0	1	1	1	0	1	1	1
x x x 1 0 0 0 1 11 h	0	1	1	1	1	1	∗	0
x x x 1 0 0 1 0 12 h	0	1	1	1	1	1	∗	∗
x x x 1 0 0 1 1 13 h	0	1	1	1	1	1	∗	∗
x x x 1 0 1 0 0 14 h	0	1	1	1	1	1	∗	∗
x x x 1 0 1 0 1 15 h	0	1	1	1	0	1	1	1
x x x 1 0 1 1 0 16 h	0	1	1	1	0	1	1	1
x x x 1 0 1 1 1 17 h	0	1	1	1	0	1	1	1
x x x 1 1 0 0 0 18 h	1	0	1	1	1	1	0	0
x x x 1 1 0 0 1 19 h	0	1	1	1	1	1	0	∗
x x x 1 1 0 1 0 1A h	0	0	0	0	0	0	0	0
x x x 1 1 0 1 1 1B h	0	0	0	0	0	1	1	0
x x x 1 1 1 0 0 1C h	0	1	1	1	1	1	0	1

Description of Operation

1. Power-On Sequence

The CXA2060BS does not have an internal power-on sequence. Therefore, all power-on sequences are controlled by the set microcomputer (I^2C bus controller).

(1) Power-on

The IC is reset and the RGB outputs are all blanked. H drive starts to oscillate, but oscillation is at the maximum frequency (16kHz or more) and is not synchronized with the input signal in order to prevent FBT (flyback transformer for generating high voltage) H squealing. Output of vertical signal V TIM starts, but V drive is DC output. Bus registers which are set by power-on reset are as follows.

P ON = 0: RGB all blanked ON
HD W = 0: Normal mode
V ON = 0: V output stopped mode
FH HIGH = 0: H oscillator maximum frequency mode
AGING = 0: All white output aging mode OFF
YUV OUT = 0

(2) Bus register data transfer

The register setting sequence differs according to the set sequence. Register settings for the following sequence are shown as an example.

Set sequence	CXA2060BS register settings
Power-on	Reset status in (1) above.
↓	↓
Degauss	Reset status in (1) above. The CRT is degaussed in a completely darkened condition.
↓	↓
V drive oscillation	The IC is set to the power-on initial settings. (See the following page.) A sawtooth wave is output to V drive and the IC waits for the vertical deflection to stabilize. The H drive oscillator frequency goes to the standard frequency.
↓	↓
AKB operation start	R ON, G ON and B ON are set to 0. P ON is set to 1 and a reference pulse is output from RGBOUT. Then, the IC waits for the cathode to warm up and the beam current to start flowing.
↓	↓
AKB loop stable	Status register IKR is monitored. IKR = 0: Unstable IKR = 1: Stable Note that the time until IKR = 1 is returned differs according to the initial status of the cathode. Also note that the time until IKR = 1 results may differ from the actual time until the cathode current stabilizes. It is recommended that video output start after IKR = 1 has been established for 1 or 2 seconds.
↓	↓
Video output	R ON, G ON and B ON are set to 1 and the video signal is output from RGBOUT.

(3) Power-on initial settings

The initial settings listed here for power-on when V drive starts to oscillate are reference values; the actual settings may be determined as needed according to the conditions under which the set is to be used.

P ON	= 0	RGB all blanked
HD W	= 0	Normal
AXIS PAL	= 0	PAL axis forced OFF
V ON	= 1	V drive oscillation
FH HIGH	= 1	H oscillation frequency standard
YUV OUT	= 0	R2 IN/G2 IN/B2 IN signal input mode
AGING	= 0	Aging Mode OFF
VIDEO SEL	= 0	TV signal input (User)
S SEL	= 0	TV/CVBS1/CVBS2 input or Mute selection (User)
R ON	= 0	Rch video output blanked
G ON	= 0	Gch video output blanked
B ON	= 0	Bch video output blanked
Y SEL	= 0	YUV SW standard operation
X'TAL	= 3	AUTO
COL SYSTEM	= 3	AUTO
COL LOOP	= 1	Automatic identification for PAL/SECAM/NTSC/NTSC4.43
C BPF	= 1	C BPF ON
C TRAP OFF	= 0	C TRAP ON
PICTURE	= 3Fh	MAX (User Control)
NO COLOR	= 0	PAL identification output to status (when there is no signal)
FSC SW	= 0	FSC OFF
COLOR	= 1Fh	Center (User Control)
C OFF	= 0	Chroma signal ON
KILLER OFF	= 0	Color killer normal mode
HUE	= 1Fh	Center (User Control)
SHP F0	= 0	2.5MHz
AXIS NTSC	= 0	Japan axis
BRIGHT	= 1Fh	Center (User Control)
DC TRAN	= 0	100%
PRE/OVER	= 0	Sharpness Pre/Over ratio 1:1
SHARPNESS	= 7h	Center (User Control)
R CUTOFF	= 7h	Center (Adjust)
G CUTOFF	= 7h	Center (Adjust)
B CUTOFF	= 7h	Center (Adjust)
R DRIVE	= 1Fh	Center (Adjust)
ABL MODE	= 1	Picture ABL/Bright ABL combination mode
ABL VTH	= 0	Vth = 3V
G DRIVE	= 1Fh	Center (Adjust)
DY COL	= 0	Dynamic Color OFF
RGB SEL	= 0	YS1 SW normal mode
B DRIVE	= 1Fh	Center (Adjust)
GAMMA	= 0	Gamma OFF
H OSC	= 7h	Center (Adjust)
Y DELAY	= 7h	Center (Adjust)
FIELD FREQ	= 0	AUTO
CD MODE	= 0	Normal

(Power-on initial settings continued)

INTERLACE	= 0	Interlace Mode
H SS	= 0	Slice level 1/3 (from sync tip)
V SS	= 0	Slice level 1/3 (from sync tip)
V SIZE	= 1Fh	Center (Adjust)
H MASK	= 0	Macrovision countermeasure OFF
V POSITION	= 1Fh	Center (Adjust)
AFC GAIN	= 1	Gain medium
S CORRECTION	= 7h	Center (Adjust)
V LINEALITY	= 7h	Center (Adjust)
H SIZE	= 1Fh	Center (Adjust)
EW DC	= 0	OFF
H POSITION	= 1Fh	Center (Adjust)
PIN AMP	= 1Fh	Center (Adjust)
CORNER PIN	= 1Fh	Center (Adjust)
TRAPEZIUM	= 7h	Center (Adjust)
EHT COMP	= 7h	Center (Adjust)
AFC BOW	= 7h	Center (Adjust)
AFC ANGLE	= 7h	Center (Adjust)
LEFT HBLK	= 7h	HBLK width min.
RIGHT HBLK	= 7h	HBLK width min.
ASPECT	= 2Fh	100%
HBLK	= 0	Control OFF
V UNDER SCAN	= 0	OFF
SCROLL	= 1Fh	Center (User Control)
V ZOOM	= 0	Zoom OFF
UPPER VLIN	= 0h	100% (No compression)
LOWER VLIN	= 0h	100% (No compression)
VTIM SEL	= 0	V retrace pulse timing pulse
ID STOP	= 1	Center
ID START	= 2	Center
BELL F0	= 1Fh	Center
ID LEVEL	= 1	Center

2. Various Mode Settings

The CXA2060BS contains bus registers for deflection compensation which can be set for various wide modes. Wide mode setting registers can be used separately from registers for normal picture distortion adjustment, and once picture distortion adjustment has been performed in full mode, wide mode settings can be made simply by changing the corresponding register.

- Vertical picture distortion adjustment registers
  V SIZE, V POSITION, S CORRECTION, V LINEARITY
- Horizontal picture distortion adjustment registers
  H SIZE, EW DC, PIN AMP, CORNER PIN, TRAPEZIUM, AFC BOW, AFC ANGLE, H POSITION
- Wide mode setting registers
  LEFT HBLK, RIGHT HBLK, ASPECT, HBLK, V UNDER SCAN, SCROLL, V ZOOM,
  UPPER VLIN, LOWER VLIN

Various mode settings

Setting	CRT size	Soft size	Mode name	I^2C bus register
1)-1	16:9	16:9	Full	Standard value for 16:9 CRTs
1)-2	16:9	4:3	Wide full	Standard value for 16:9 CRTs
2)	16:9	4:3 16:9	Normal	ASPECT = 0h: V size 75% HBLK = 1: HBLK width adjustment ON LEFT HBLK = Adjustment RIGHT HBLK = Adjustment PIN AMP = Adjustment EW DC = 1
3)	16:9	4:3	Zoom	ASPECT = 2Fh: V size 100% V ZOOM = 1: Zoom ON (V size limited to 75%) SCROLL = 0h: Zoom bottom of picture 1Fh: Zoom center of picture 3Fh: Zoom top of picture
4)	16:9	4:3 (16:9 + subtitles)	Subtitle-in	ASPECT = 2Fh: V size 100% UP VLIN = Adjustment: Top of picture slightly compressed LO VLIN = Adjustment: Bottom of picture greatly compressed V ZOOM = 1: V size limited to 75% SCROLL = Adjustment
5)	16:9	4:3	Split screen mode	V UNDER SCAN = 1: Compressed
6)	16:9	4:3	Wide zoom	ASPECT = Adjustment: V size 90% UP VLIN = Adjustment LO VLIN = Adjustment (S CORR = Adjustment) Top and bottom of picture compressed
7)	4:3	4:3	4:3 normal	Standard value for 4:3 CRTs
8)	4:3	16:9	V compression	ASPECT = Adjustment V UNDER SCAN = 1: V size 80% (Compressed to a total of 75%)

* Since the amount of compensation for distortion in the vertical position of a CRT does not change due to the above modes, it is possible to use initial values for all screen distortion registers.

Mode examples are given below. The 570 actual number of scanning lines displayed under PAL (480 lines for NTSC) will be used in the description. Data stored in the wide mode setting registers is also given.
Note that actual adjustment values may differ slightly due to variations among different ICs.
Standard setting data differs for 16:9 CRTs and 4:3 CRTs.

(Standard value)

Register	16:9 CRT	4:3 CRT
ASPECT	0h	2Fh
SCROLL	1Fh	1Fh
V ZOOM	1	0
UPPER VLIN	0h	0h
LOWER VLIN	0h	0h
V UNDER SCAN	0	0
HBLK	0	0
LEFT HBLK	7h	7h
RIGHT HBLK	7h	7h

1) Full mode

This mode reproduces the full 570 (NTSC: 480) lines on a 16:9 CRT. Normal 4:3 images are compressed vertically, but in the case of a squeezed video source which compresses 16:9 images to 4:3 images, 16:9 images are reproduced in their original 16:9 aspect ratio. The register settings are the 16:9 CRT standard values.

2) Normal mode

In this mode, 4:3 images are reproduced without modification on a 16:9 CRT. A black border appears at the left and right of the picture.
In this mode, the H deflection size must be compressed by 25% compared to full mode.
The CXA2060BS performs compression with a register (EW DC) that compresses the H size.
Because excessive current flows to the horizontal deflection circuit in this case, adequate consideration must be given to the allowable power dissipation, etc., of the horizontal deflection coil in the design of the set. In addition, this concern can also be addressed through measures taken external to the IC, such as switching the horizontal deflection coil.
Full mode should be used when performing memory processing to add a black border to the video signal.
H blanking of the image normally uses the flyback pulse input from HP/PROTECT (Pin 18). However, the blanking width can be varied according to the control register setting when blanking is insufficient for the right and left black borders.
Change the following three settings with respect to the 16:9 CRT standard values for the register settings.

HBLK = 1
LEFT HBLK = Adjustment value
RIGHT HBLK = Adjustment value

The H angle of deflection decreases, causing it to differ from the PIN compensation amount during H size full status. Therefore, in addition to the wide mode registers, PIN AMP must also be readjusted only for this mode.

3) Zoom mode

In this mode, 4:3 images are reproduced on a 16:9 CRT by enlarging the picture without other modification. The top and bottom of normal 4:3 images are lost, but almost the entire picture can be reproduced for vista size video software, etc. which already has black borders at the top and bottom. Setting the ASPECT register to 2Fh (100%) allows zooming to be performed for 4:3 images without distortion. In this case, the number of scanning lines is reduced to 430 lines compared to 570 lines for full mode. The zooming position can be shifted vertically by the SCROLL register.

V blanking of the image normally begins from V sync and continues for 2H after the AKB reference pulse, but the top and bottom parts which are lost are also blanked during this mode.

Adjust the following two registers with respect to the 16:9 CRT standard values for the register settings.

ASPECT = 2Fh
SCROLL = 1Fh or user control

4) Subtitle-in mode

When Cinema Scope images which have black borders at the top and bottom of the picture are merely enlarged with the zoom mode in 3) above, the subtitles present in the black borders may be lost. Therefore, this mode is used to super-compress only the subtitle part and reproduce it on the display.

Add the LOWER VLIN adjustment to the zoom mode settings for the register settings.

ASPECT = 2Fh
SCROLL = 1Fh or user control
LOWER VLIN = Adjustment value

LOWER VLIN causes the linearity at the bottom of the picture to deteriorate. Therefore, UPPER VLIN should also be adjusted if the top and bottom of the picture are to be made symmetrical. Since the picture is compressed vertically, the number of scanning lines exceeds 430 lines.

5) Two-picture mode

This mode is used to reproduce two 4:3 video displays on a 16:9 CRT such as for P and P.

To achieve this, the V size must be further compressed from the condition where ASPECT = 0 (V size 75%: full mode). This IC performs this compression with V UNDER SCAN.

16:9 CRT standard values are used with only V UNDER SCAN changed to 1 for the register settings.

V UNDER SCAN = 1

6) Wide zoom mode

This mode reproduces 4:3 video software naturally on wide displays by enlarging 4:3 images without other modification and compressing the parts of the image which protrude from the picture into the top and bottom parts of the picture. The display enlargement ratio is controlled by ASPECT, and the compression ratios at the top and bottom of the picture are controlled by UPPER VLIN and LOWER VLIN.

Adjust the following three registers with respect to the 16:9 CRT standard values for the register settings.

ASPECT = Adjustment value
UPPER VLIN = Adjustment value
LOWER VLIN = Adjustment value

7) 4:3 CRT normal mode

This is the standard mode for 4:3 CRTs.

The register settings are the 4:3 CRT standard values.

8) V compression mode

This mode is used to reproduce M-N converter output consisting of 16:9 images expanded to 4:3 aspect ratio and other squeezed signals without distortion on a 4:3 CRT. In this case, the V size must be compressed to 75%. This is done using V UNDER SCAN in 5) above.

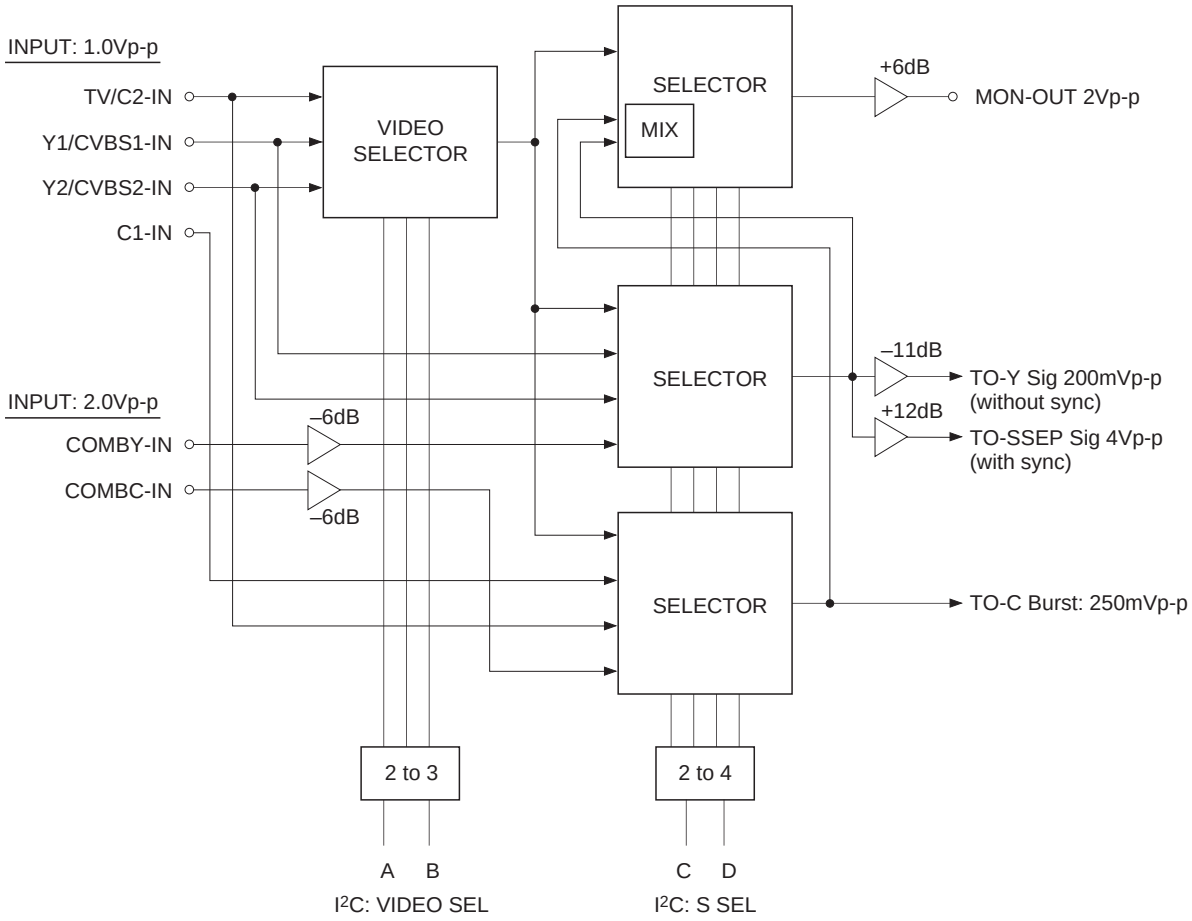
Setting V UNDER SCAN to ON compresses the V size to 75%. Fine adjustment of the V size is possible by adding the ASPECT adjustment.

4:3 CRT standard values are used with the ASPECT and V UNDER SCAN settings changed for the register settings.

ASPECT = Adjustment

V UNDER SCAN = 1

VIDEO SW



A	B	C	D	TO-Y	TO-C	MON-OUT
0	0	0	0	TV	TV	TV
0	1	0	0	CVBS1	CVBS1	CVBS1
1	0	0	0	CVBS2	CVBS2	CVBS2
1	1	0	0	NOSIG	NOSIG	NOSIG
1	1	0	1	Y1	C1	Y1 + C1
1	1	1	0	Y2	C2	Y2 + C2
0	0	1	1	COMBY	COMBC	TV
0	1	1	1	COMBY	COMBC	CVBS1
1	0	1	1	COMBY	COMBC	CVBS2
1	1	1	1	NOSIG	NOSIG	NOSIG

[Color Status]

Input	APC LOCK	PAL	SECAM	X'TAL ID	FIELD ID
3.58 NTSC	1	0	0	01	0
4.43 NTSC	1	0	0	00	0
PAL	1	1	0	00	1
PAL60	1	1	0	00	0
SECAM	0	0	1	00	1
PAL-M	1	1	0	00	0
PAL-N	1	1	0	10	1
No color signal	0	0	0	**	*

3. Signal Processing

The CXA2060BS consists of separate blocks for sync signal processing, H deflection signal processing, V deflection signal processing and Y/C and RGB signal processing, all controlled by an I^2C bus.

1) Sync signal processing

The Y signal selected by the video switch is sync separated by a horizontal/vertical sync separation circuit.
A phase comparison between the horizontal sync split signal obtained and the H VCO output signal is conducted and an AFC loop is configured, and an H pulse synchronized to H sync is created within the IC. When AFC is locked to H sync, 1 is output to the status register (H LOCK). This can be used to detect the presence of a video signal.
The vertical sync split signal is sent to the V countdown block and V deflection timing is obtained by the appropriate window processing. V cycle timing such as the AKB reference pulse is generated using this V timing pulse.
The V retrace timing pulse and sync split signal are output on V TIM (Pin 5) according to the V TIMSEL register setting.

2) H deflection signal processing

A phase comparison is conducted between the H pulse obtained from sync processing and the H deflection pulse input on Pin 18 (HP/PROTECT) and the horizontal position of the picture displayed on the CRT is controlled by controlling the phase of H drive output. The compensation signal created using the vertical sawtooth wave is superimposed and vertical picture distortion compensation is also performed.
The H deflection pulse is used for H blanking of the video signal. If the width of the H deflection pulse is narrow, a pulse created by the IC can be added and the result used as the H blanking pulse (HBLK).
Although Pin 18 is for normal pulse input, the pin is kept lowered to near GND level, H drive output is stopped and 1 is output to the status register (H NG). It is necessary to turn the IC's power OFF and ON again in order to cancel this status.

3) V deflection signal processing

The vertical sawtooth wave oscillates in sync with the V timing pulse cycle output by the countdown. After wide deflection processing is added to this sawtooth wave, it undergoes picture distortion adjustment by the function circuits V drive and EW drive, respectively, and the result is output as the V drive and EW drive signals.

4) Y signal processing

The Y/CVBS signal selected by the video switch is sent to the Y signal processing circuit.
The Y signal is sent to the RGB signal processing circuit via a trap filter for eliminating the chroma signal, a delay line, sharpness control, clamp, and black expansion circuits. In addition, the output of the Y signal processing circuit can be monitored using Pin 32 (R2 IN) by setting register YUV OUT to 1. (At this time, be sure to connect a 10kΩ resistor to Vcc as a load for Pin 32.)
Also, a differential waveform of the Y signal synchronized with YOUT (RGB OUT) is output from Pin 15 as VM OUT.
When the CVBS signal is selected, set the C TRAP OFF register to 0 (trap filter ON), and when the Y signal split from Y/C separation is selected, set this register to 1 (trap filter OFF).
The internal filter f0 is adjusted automatically within the IC. Since the filter f0 does not settle down while the color killer is operating, be sure to set the trap filter to OFF if it is an obstacle.

5) C signal processing

The TV, CVBS or chroma (PAL, NTSC) signals (specified input: burst level 300mVp-p) selected by the Video SW pass through an ACC, chroma band-pass filter, chroma amplifier, and demodulation circuit to form the color difference signals R-Y and B-Y. After being processed by 1HDL the signals are input to the RGB signal processing circuit.

The output signals (color difference signals) of this C signal processing circuit can be monitored, just like Y output, using Pin 30 (B2 IN) and Pin 31 (G2 IN) by setting the register YUV OUT to 1. B-Y is output from Pin 30 (B2 IN) and R-Y is output from Pin 31 (G2 IN). (At this time, be sure to connect a 10kΩ resistor to Vcc as a load for Pins 30 and 31.)

The color killer is activated when the burst level falls –36dB or more below the specified input.

The SECAM signal (specified input: R-YID: 215mVp-p, B-YID: 167mVp-p) passes through an ACC, bell filter, limiter amplifier, demodulation circuit, line blanking circuit, and de-emphasis circuit to form the color difference signals R-Y and B-Y. After being processed by 1HDL the signals are input to the RGB signal processing circuit.

In addition, the color system (PAL, NTSC or SECAM) and sub-carrier frequency (4.43MHz or 3.58MHz) are automatically identified according to the input chroma signal. Circuits such as the internal VCO, demodulation circuit and color axis circuit of the RGB signal processing block (described below) are automatically adjusted.

The system is selected either automatically by the I^2C bus (COL SYSTEM and X'TAL) or by forcible modes.

The color system status selected using the status registers NTSC/PAL, SECAM and X'TAL ID is output (refer to the color status table).

6) RGB signal processing

The Y and color difference signals obtained by the Y/C signal processing circuit are first input to the YUV SW, then selected and switched with the external Y and color difference signals. After the selected Y and color difference signals are used to form the G-Y signal in the next axis circuit (including color control), they are used for the RGB signals.

Next, these signals pass through the external RGB signal SW circuits YS1 SW and YM SW (half-tone SW), external RGB signal SW circuit YS2 SW, dynamic color, picture control, gamma correction, clamp, brightness control, drive control, and cutoff control circuits, and are then output on Pin 22 (ROUT), Pin 23 (GOUT), and Pin 24 (BOUT).

An external RGB signal (100 IRE 100% white: 0.7Vp-p) conforming to normal video signal specifications is input to Pins 26, 27 and 28 and Pins 30, 31 and 32.

The voltage added to Pin 3 (ABL IN) is compared to the reference voltage within the IC and then integrated by the capacitor connected to Pin 42 (ABL FIL) to form a control signal used for picture control and brightness control. The ABL mode can be selected using the register ABL MODE for switching such that only picture control is performed or so that both picture control and brightness control are performed. There is a protective function such that brightness control is activated even when only picture control is being performed if beam current flows excessively.

This IC includes two functions for performing white balance and black balance adjustments: drive control for performing gain adjustment between RGB outputs and cutoff control for performing DC level adjustments between RGB outputs. These can be independently controlled for three channels by the I^2C bus. In addition to this, the cutoff control function also includes an auto-cutoff function (AKB) which performs automatic adjustment by forming a loop between the IC and CRT. This can compensate for temporal variations of the CRT.

Auto-cutoff functions are as follows.

- R, G, and B reference pulses for auto cutoff, shifted 1H each in the order mentioned, appear at the top of the picture (actually, in the overscan portion). The reference pulse uses 1H in the V blanking interval, and is output from each R, G and B output pin.
- The RGB cathode current (IK) is input to Pin 21 (IK IN).
- The cathode current input to Pin 21 (IK IN) is converted to a voltage within the IC. The reference pulse interval of this voltage is compared with the reference voltage within the IC, and a current generated by this voltage difference is used to charge a capacitor within the IC. This charge is held at times other than the reference pulse interval.
- The DC level of the RGB output changes according to the voltage generated by the capacitor. A loop functions to make the voltage converted from the current input to Pin 21 (IK IN) match the reference voltage within the IC.

The IC internal reference voltages for R, G and B undergo cutoff control by the I^2C bus and can be independently adjusted. The cathode signal current flowing during the reference pulse interval should be about 13µA at the cutoff control center. The IC can also handle up to 100µA cathode leak current flowing during blanking. Large current flows during the video interval, and this leads to destruction around IK IN, be absolutely sure to connect a zener diode of about 4V to the IK IN pin.

4. Notes on Operation

Because the R, G and B signals and deflection signals output from the CXA2060BS are DC direct connected, the pattern (set board) must be designed with consideration given to minimizing interference from around the power supply and GND. Do not separate the GND patterns for each pin; a solid earth is ideal. Locate the power supply side of the by-pass capacitor which is inserted between the power supply and GND as near to the pin as possible. Also, locate the crystal oscillator and IREF resistor as near to the pin as possible, and be sure that signal lines do not pass close to these pins. Drive the Y, external Y/color difference and external RGB signals at a sufficiently low impedance, as these signals are clamped when they are input using the capacitor connected to the input pin.

Use a resistor (such as a meal film resistor) with an error of less than 1% for the IREF pin.

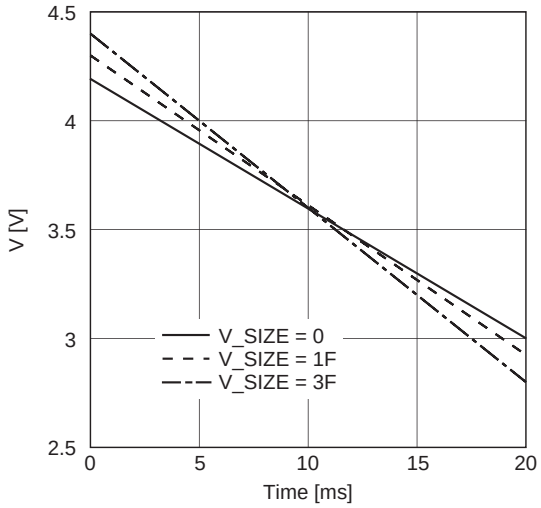
Be sure that Vcc1 and Vcc2 have the same electric potential.

Use crystals manufactured by Daishinku Corp. Properties of this IC are not guaranteed if used with crystals from another manufacturer.

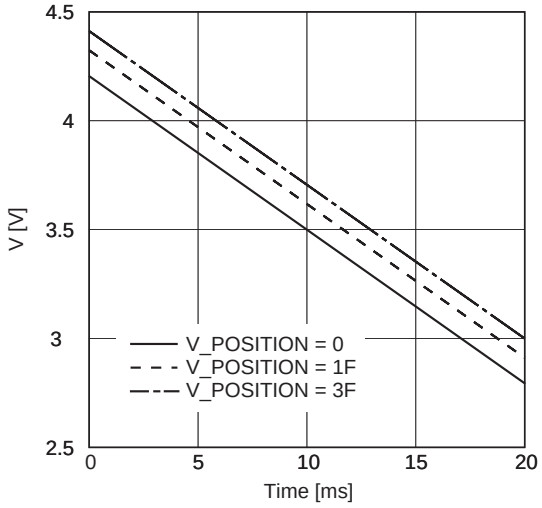
Curve Data

I²C bus data conforms to the "I²C Bus Register Initial Settings" of the Electrical Characteristics Measurement Conditions.

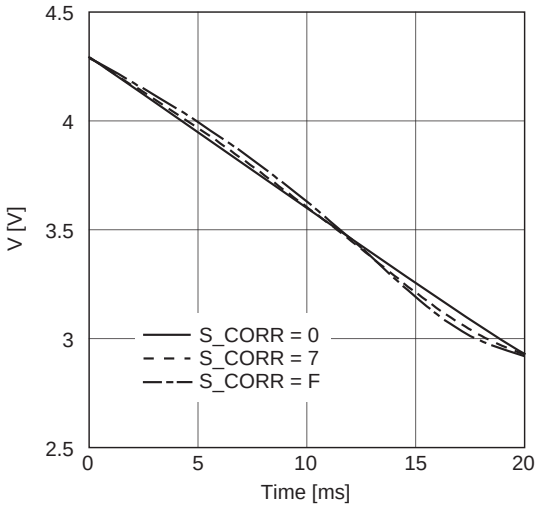
V_SIZE



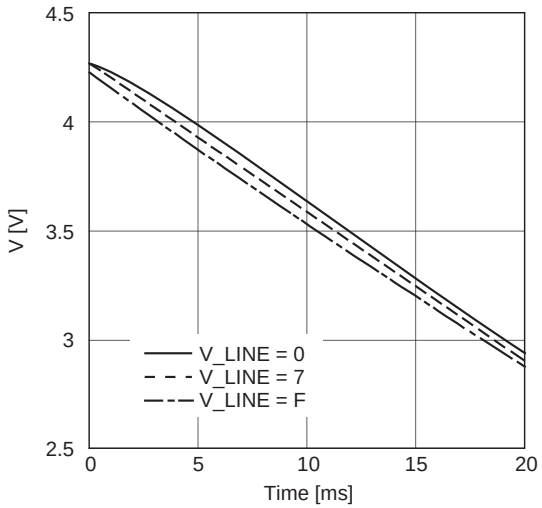
V_POSITION



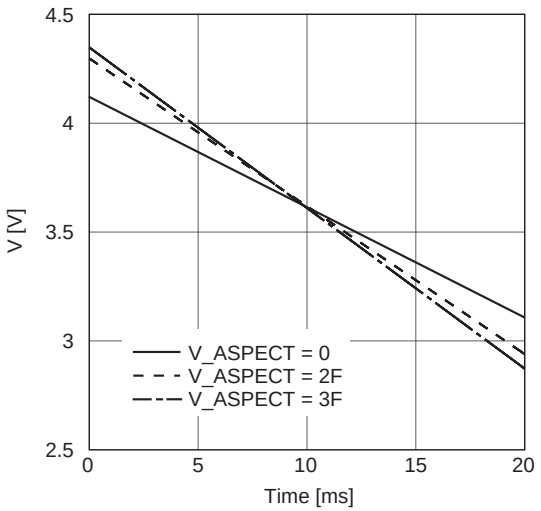
S_CORR



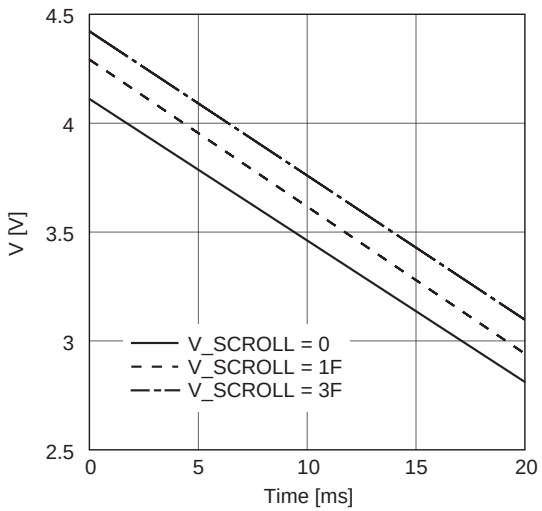
V_LINE



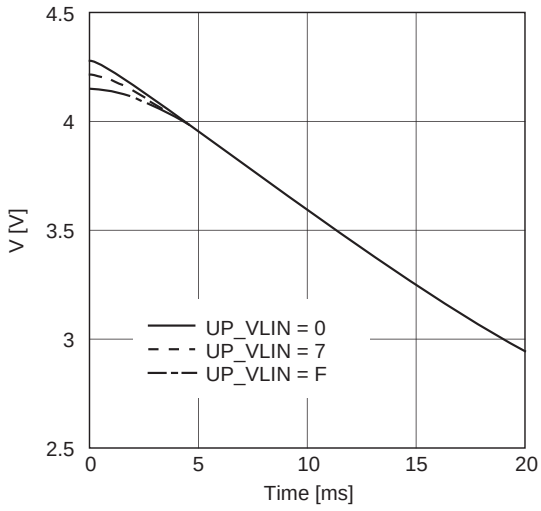
V_ASPECT



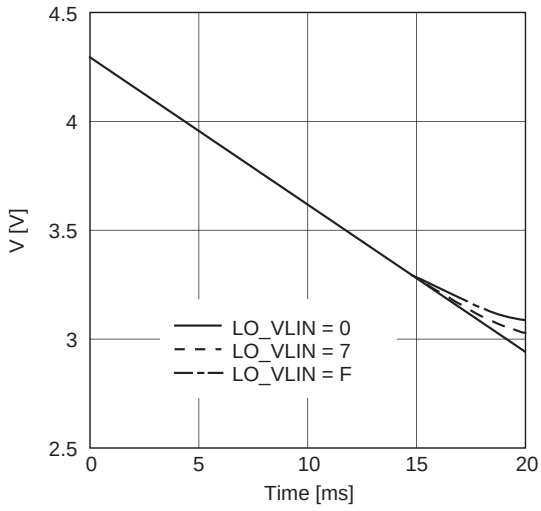
V_SCROLL



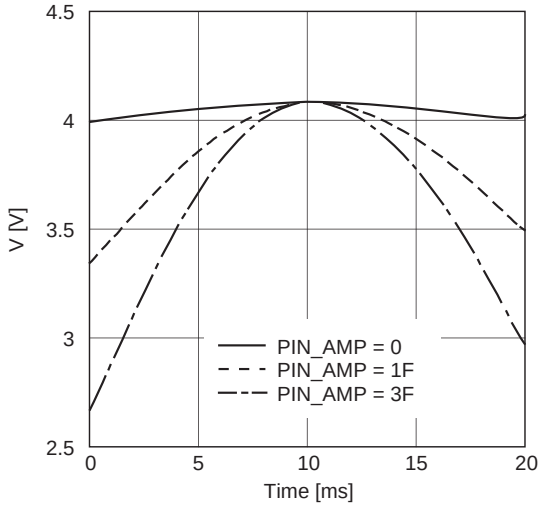
UP_VLIN



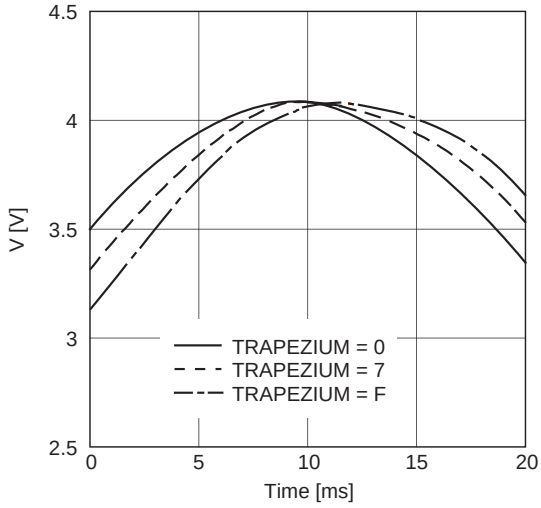
LO_VLIN



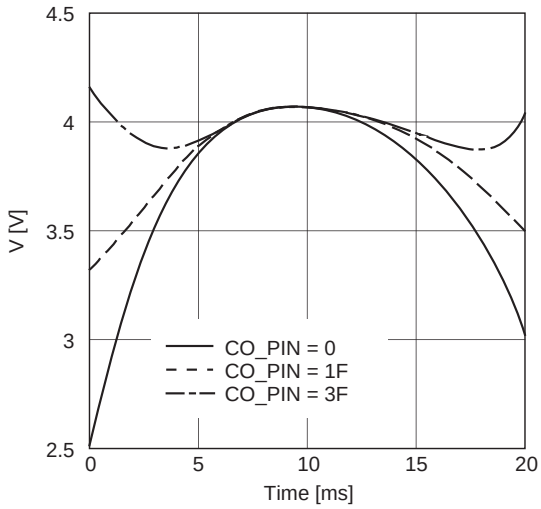
PIN_AMP



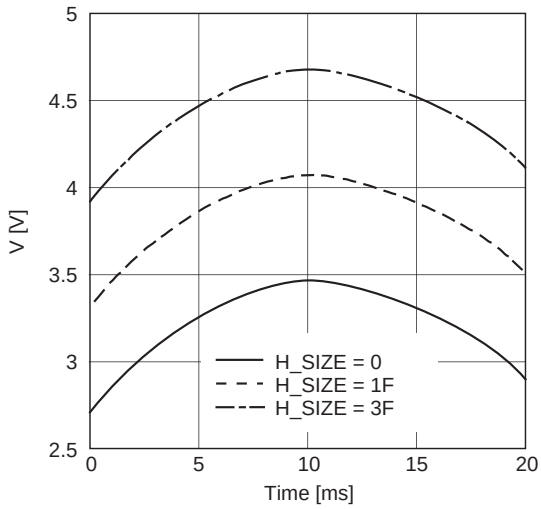
TRAPEZIUM



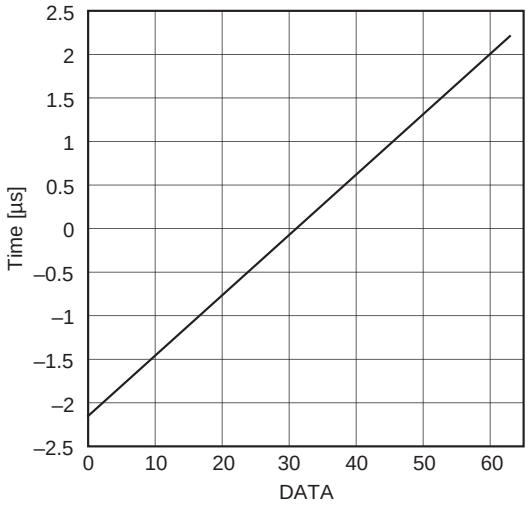
CO_PIN



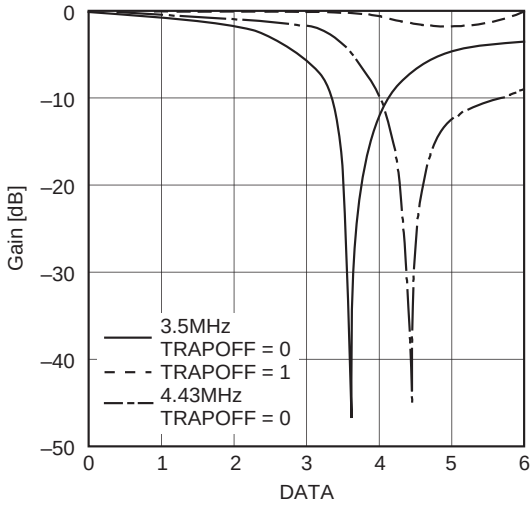
H_SIZE



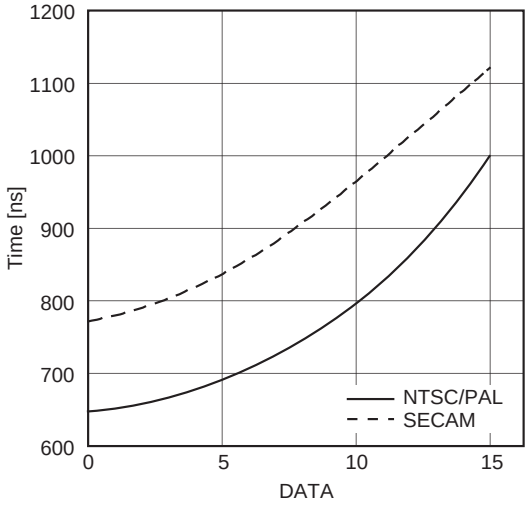
H_POSITION



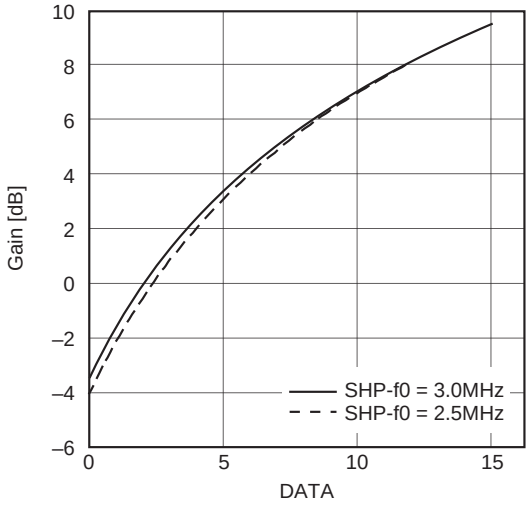
TRAP OFF



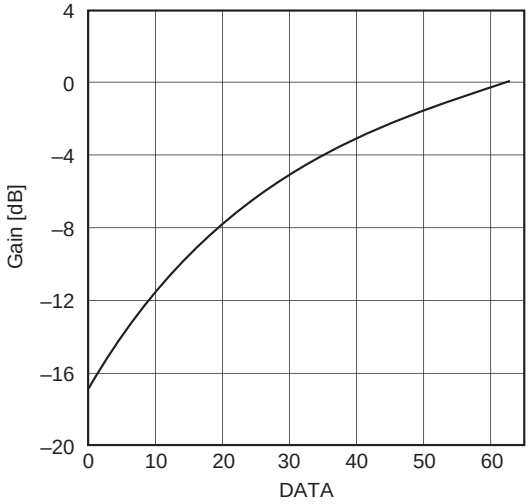
Y_DELAY



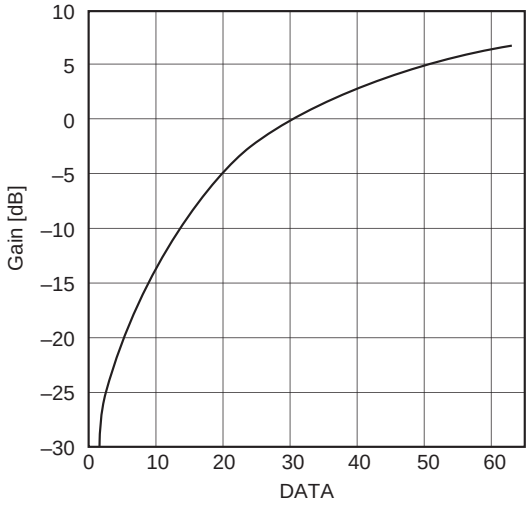
SHARPNESS



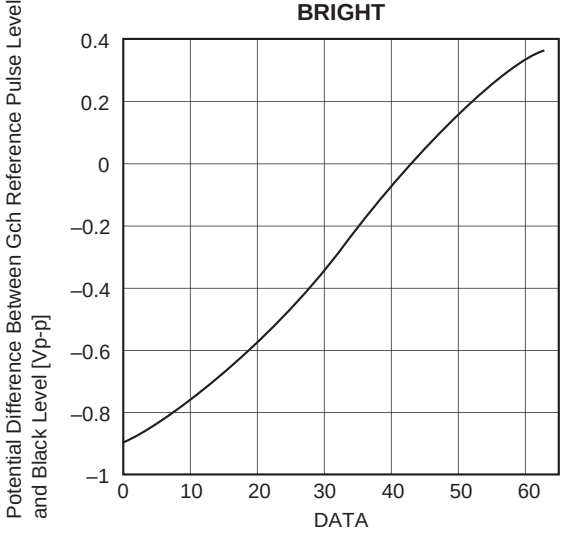
PICTURE



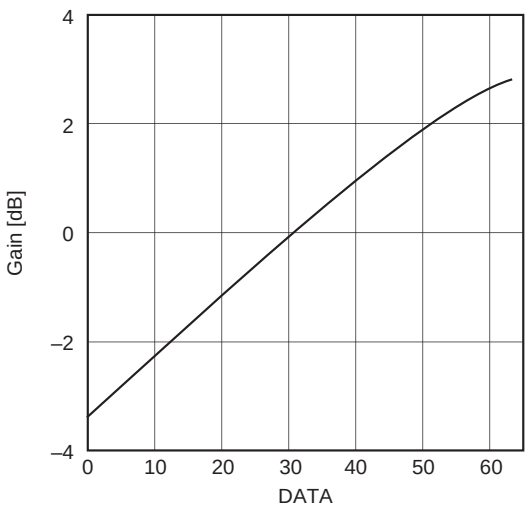
COLOR



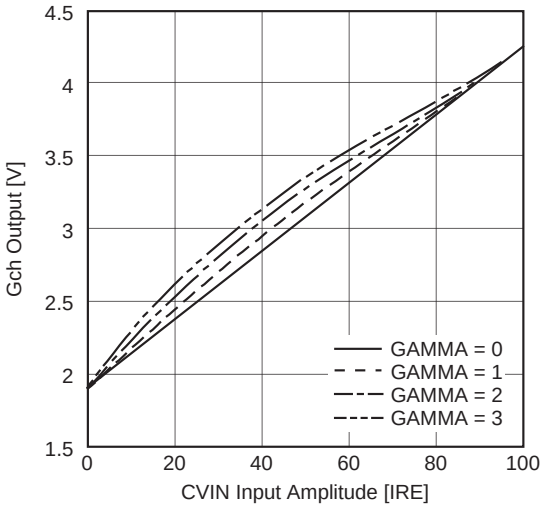
BRIGHT



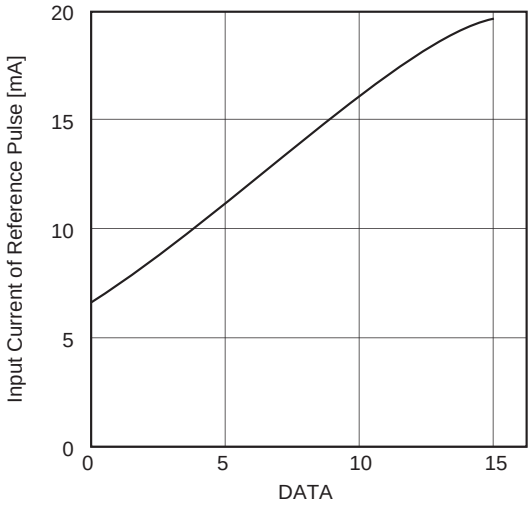
R-DRIVE, G-DRIVE, B-DRIVE



GAMMA

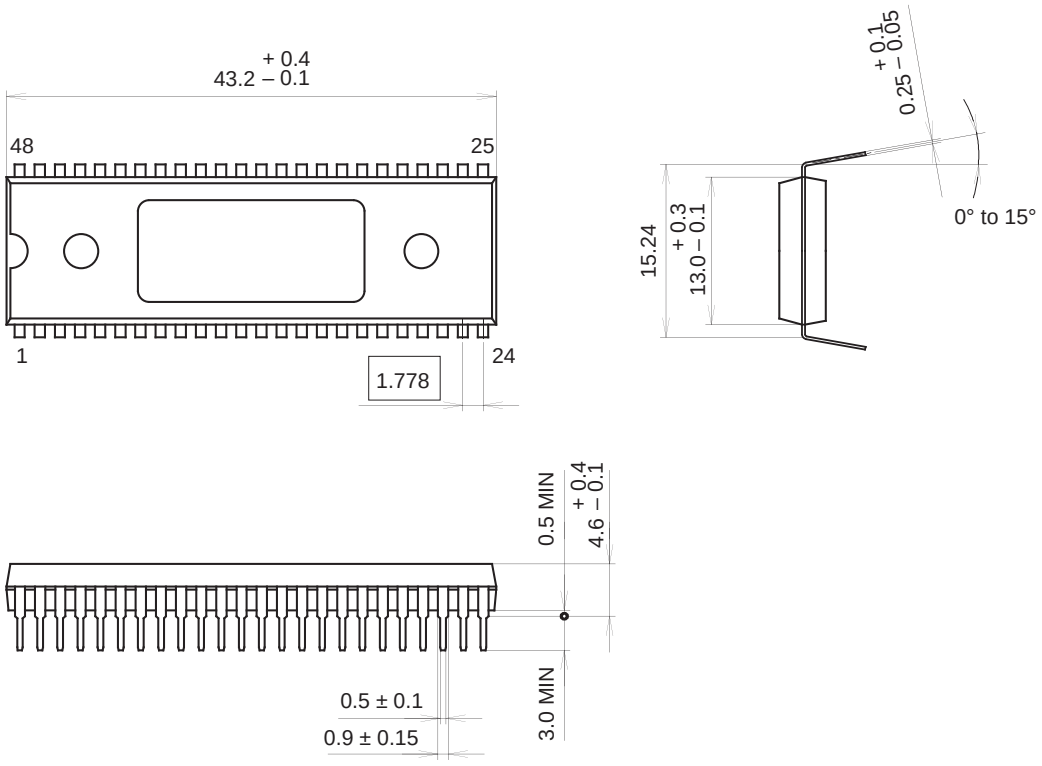


CUT_OFF (R, G, B)



Package Outline Unit: mm

48PIN SDIP (PLASTIC)



Two kinds of package surface:
1.All mat surface type.
2.Center part is mirror surface.

SONY CODE	SDIP-48P-02
EIAJ CODE	SDIP048-P-0600
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	5.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).