SCLS337I - MARCH 1996 - REVISED FEBRUARY 2000

•	Members of the Texas Instruments <i>Widebus</i> ™ Family <i>EPIC</i> ™ (Enhanced-Performance Implanted CMOS) Process	SN54AHCT16374 WD PACKAGE SN74AHCT16374 DGG, DGV, OR DL PACKAGE (TOP VIEW) $1\overline{OE}$ $\begin{bmatrix} 1 & 48 \\ 1 & 48 \end{bmatrix}$ 1CLK
•	Inputs Are TTL-Voltage Compatible	
•	Distributed V _{CC} and GND Pins Minimize High-Speed Switching Noise	1Q2 3 46 1D2 GND 4 45 GND
•	Flow-Through Architecture Optimizes PCB Layout	1Q3 5 44 1D3 1Q4 6 43 1D4
٠	Latch-Up Performance Exceeds 250 mA Per JESD 17	V _{CC} 7 42 V _{CC} 1Q5 8 41 1D5 1Q6 9 40 1D6
٠	ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)	1Q6 9 40 1D6 GND 10 39 GND 1Q7 11 38 1D7 1Q8 12 37 1D8
٠	Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very	2Q1
	Small-Outline (DGC), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings	GND 15 34 GND 2Q3 16 33 2D3 2Q4 17 32 2D4 V _{CC} 18 31 V _{CC}
desc	ription	2Q5 19 30 2D5 2Q6 20 29 2D6
	The 'AHCT16374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads.	GND 21 28 GND 2Q7 22 27 2D7 2Q8 23 26 2D8 2OE 24 25 2CLK

outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

OE does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AHCT16374 is characterized for operation over the full military temperature range of -55° C to 125° C. The SN74AHCT16374 is characterized for operation from -40° C to 85° C.



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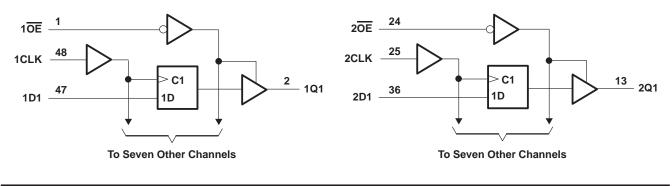
	FUNCTIC (each 8-b		
	INPUTS		OUTPUT
OE	CLK	Q	
L	\uparrow	Н	Н
L	\uparrow	L	L
L	H or L	Х	Q ₀
Н	Х	Х	z

logic symbol[†]

			_		
1 <mark>0E</mark>	1	1EN			
1CLK	48	> C1			
2 <mark>0E</mark>	24	2EN			
2CLK	25	> C2			
ZULK		Ľ "			
1D1	47	1D 1	∠	2	Q1
1D2	46			3	Q2
1D3	44			5	Q3
1D4	43		-	6	Q4
1D5	41	-	-	8	Q5
1D6	40		-	9	Q6
1D7	38		-	11	Q7
1D8	37		-	12	Q8
2D1	36	2D 2	▽	13	Q1
2D2	35		<u> </u>	14	Q2
2D3	33			16	Q3
2D4	32			17	Q4
2D4	30			19	Q5
2D5	29		_	20	Q6
2D0	27		_	22	Q7
2D7 2D8	26	<u> </u>		23	Q8
200				2	QU

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

	V nA nA nA M VW VW VW
Storage temperature range, T _{stg} 65°C to 150°	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		SN54AHCT		SN74AHC	T16374	UNIT
		MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2	N	2		V
VIL	Low-level input voltage		0.8		0.8	V
VI	Input voltage	0	5.5	0	5.5	V
Vo	Output voltage	0	VCC	0	VCC	V
ЮН	High-level output current	200	-8		-8	mA
IOL	Low-level output current	0	8		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	9	20		20	ns/V
ТА	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vee	Τį	Δ = 25°C	;	SN54AHC	T16374	SN74AHC	T16374	UNIT	
PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
Varia	I _{OH} = -50 μA	4.5 V	4.4	4.5		4.4		4.4		V	
VOH	I _{OH} = –8 mA	4.5 V	3.94			3.8		3.8		v	
VOL	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V	
VOL	I _{OL} = 8 mA	4.5 V			0.36		0.44		0.44	v	
lj	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1	4	±1*		±1	μΑ	
I _{OZ}	$V_{O} = V_{CC}$ or GND, $V_{I} = V_{IH}$ or V_{IL}	5.5 V			±0.25	UC7	±2.5		±2.5	μΑ	
ICC	$V_I = V_{CC} \text{ or } GND, \qquad I_O = 0$	5.5 V			4	20	40		40	μΑ	
_vcc_t	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35	4	1.5		1.5	mA	
Ci	$V_I = V_{CC}$ or GND	5 V		2.5	10				10	pF	
Co	$V_{O} = V_{CC}$ or GND	5 V		3.5						pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

[†] This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54AHCT	16374	SN74AHC	UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
tw	Pulse duration, CLK high or low	6.5		6.5	2	6.5		ns
t _{su}	Setup time, data before CLK1	2.5		2.5		2.5		ns
t _h	Hold time, data after CLK↑	2.5		2.5		2.5		ns



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switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

	FROM	то	LOAD	Т	Δ = 25°C	;	SN54AHC	T16374	SN74AHC	T16374		
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
4			C _L = 15 pF	90*	140*		80*		110			
f _{max}			C _L = 50 pF	85	130		75		75		MHz	
^t PLH	CLK	Q	$C_{1} = 15 \text{ pF}$		6.5*	9.4*	1*	10.5*	1	10.5	ns	
^t PHL	ULK	Q	C _L = 15 pF		6.5*	9.4*	1*	10.5*	1	10.5	115	
^t PZH	OE	Q	C _I = 15 pF		6.5*	9.5*	1*	10.5*	1	10.5	ns	
^t PZL	ÛE	Q	CL = 15 pr		6.5*	9.5*	1*	10.5*	1	10.5	115	
^t PHZ	OE	Q	C ₁ = 15 pF		6.2*	10.2*	1*	F 11*	1	11	ns	
^t PLZ	ÛE	Q			6.2*	10.2*	15	11*	1	11	110	
^t PLH	CLK	Q	C _I = 50 pF		7.3	10.4	70 0	11.5	1	11.5	ns	
^t PHL	OLK	Q	0L = 30 pi		7.1	10.4	04	11.5	1	11.5	115	
^t PZH	OE	Q	$C_{1} = 50 \text{pF}$		6.2	10.5	1	11.5	1	11.5	ns	
^t PZL	ÛE	Q	0L = 30 pi		5.1	10.5	1	11.5	1	11.5	115	
^t PHZ	OE	Q	C _I = 50 pF		7.1	11.2	1	12	1	12	ns	
t _{PLZ}	UE		Ο _L = 30 μr		7.9	11.2	1	12	1	12	115	
^t sk(o)			C _L = 50 pF			1**				1	ns	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

	PARAMETER	SN74	AHCT16	6374	UNIT
		MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.36	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.1	-0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		4.7		V
VIH(D)	High-level dynamic input voltage	2			V
V _{IL(D)}	Low-level dynamic input voltage			0.8	V

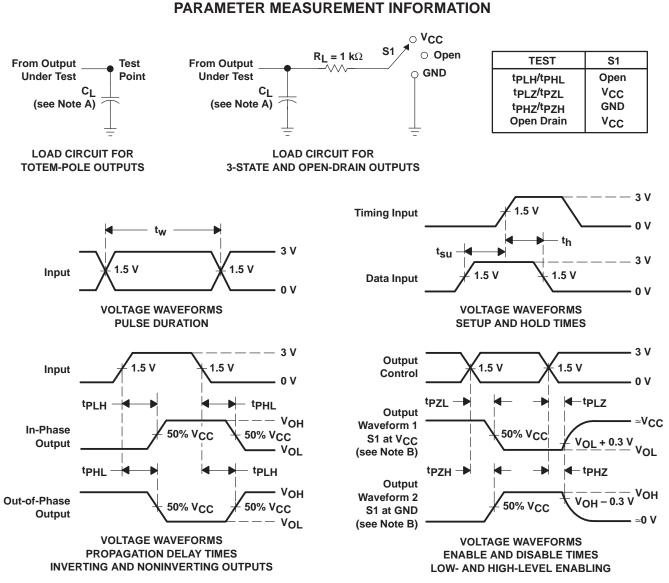
NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25° C

	PARAMETER Dd Power dissipation capacitance		ONDITIONS	TYP	UNIT
Cpd	Power dissipation capacitance	No load,	f = 1 MHz	27	pF



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NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_f \leq 3 ns, t_f \leq 3 ns.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74AHCT16374DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHCT16374DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHCT16374DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHCT16374DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHCT16374DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16374DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16374DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16374DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16374DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16374DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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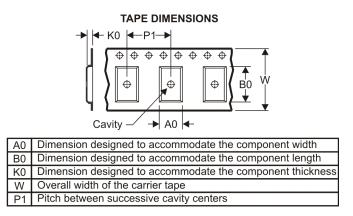
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal													
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant	
SN74AHCT16374DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1	
SN74AHCT16374DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1	
SN74AHCT16374DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1	

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11-Aug-2009



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT16374DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0
SN74AHCT16374DGVR	TVSOP	DGV	48	2000	346.0	346.0	33.0
SN74AHCT16374DLR	SSOP	DL	48	1000	346.0	346.0	49.0

MECHANICAL DATA

MSSO001C - JANUARY 1995 - REVISED DECEMBER 2001

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

DL (R-PDSO-G**)



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118



MECHANICAL DATA

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



MECHANICAL DATA

PLASTIC SMALL-OUTLINE

MPDS006C - FEBRUARY 1996 - REVISED AUGUST 2000

DGV (R-PDSO-G**)

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins MO-153

14/16/20/56 Pins – MO-194



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