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# LPM2100 bm NB+GSM Module Hardware Usage Guide

V1.3

Shanghai Yuge Information Technology Co., Ltd.

## 更新记录

| 版本 | 日期 | 作者 | 描述 |
|---|---|---|---|
| V1.0 | 2019/3/21 | John.zhang | Fix and add some configuration information |
| V1.1 | 2019/5/10 | John.zhang | Modify some information about hardware V1.1 interface changes |
| V1.2 | 2019/8/5 | John.zhang | Unified limit operating temperature<br>Modify information related to IO voltage domain<br>Modify some editing errors<br>Add GSM power consumption |
| V1.3 | 2019/9/5 | John.zhang | Increase B20/B28 |

# Contents

# Figure

# Table

# Chapter 1. Introduction

This document is the hardware solution manual for the wireless solution product LPM2100 bm NB-IoT+GSM module. It is intended to describe the hardware components and functional characteristics of the module solution, application interface definition and application instructions, electrical performance and mechanical characteristics. Combined with this and other application documents, users can quickly use this module to design wireless products.

# Chapter 2. Module review

## 2.1 Module introduction

- LPM2100 bm physical characteristics
- LPM2100 bm application

➢ Physical characteristics

✧ The LPM2100 bm is a multi-band NB-IoT + GSM quad-band dual-mode module that complies with 3GPP Release 13.

✧ This series of modules has 98 pins, (23.6 ± 0.15) mm × (19.9 ± 0.15) mm × (2.2 ± 0.15) mm, which can meet almost all M2M requirements.

✧ This series of modules is a chip module, which is packaged in LCC and provides customers with a rich hardware interface.

✧ LPM2100 bm series modules use low-power technology, sleep standby power consumption is less than 1mA, power consumption can be as low as 5uA during deep sleep.

➢ Application

✧ Smart city (smart parking, water/gas meters, street lights, smoke alarms, garbage bins, manhole covers, containers, etc.)

✧ Consumption and medical (wearing devices, VIP tracking, life support, remote clinical tracking, etc.)

✧ Industrial and agricultural intelligent monitoring (machine alarm, gas detection, irrigation, soil pH, etc.)

✧ Agriculture and the environment (agricultural applications, environmental monitoring, etc.)

✧ Logistics support (industrial assets, container tracking, location and status updates, etc.).

**NOTE**

"*" indicates that it is under development.

## 2.2 Main performance

Table 2-1 Key Features

| Characteristic | Description |
|---|---|

| | |
|---|---|
| Physical characteristics | (23.6mm×19.9mm×2.2mm) ±0.15mm |
| Application processor | 192MHz MIPS processor with 16KB I-Cache and 16KB |
| Operating Voltage | 3.5V - 4.2V Typical Voltage 3.7V |
| Power saving | PSM mode power consumption < 5uA |
| Sleep standby | Sleep mode current < 1mA (NB-IoT)<br>Sleep mode current < 2mA (GSM) |
| Application interface | Power interface<br>Six-way universal GPIO interface<br>One-way standard SIM interface, support 3.0V/1.8V, support hot swap function*<br>One way hardware reset interface<br>Two-way UART serial interface<br>One way SPI interface<br>One-way network status indication interface<br>All the way PSM_EINT# interface<br>One way ADC detection interface |
| Working frequency | NB-IoT：Band3,Band5,Band8,B20,B28<br>GSM：GSM900,GSM850,DCS1800,PCS1900 |
| Operating mode | Multimode NB-IoT/GSM/GPRS<br>The module can automatically search for the mode, prefer NB-IoT, or set the mode with the AT command. |
| Network protocol feature | UDP/TCP/CoAP/LWM2M<br>PPP/SSL/DTLS/FTP<br>HTTP/MQTT/HTTPS |
| Data transmission characteristics | NB-IoT: Single-tone: 25.5 kbps (DL), 16.7 kbps (UP)<br>NB-IoT: Multi-tone: 25.5 kbps (DL), 62.5 kbps (UP)<br>GPRS maximum downlink rate 107kbps, maximum uplink rate 85.6kbps |
| Antenna interface | Main antenna 50 ohm interface<br>BT antenna 50 ohm interface* |

| | |
|---|---|
| Firmware upgrade | Serial port upgrade |
| temperature range | Normal operating temperature －35° C to + 75° C<br>Extreme operating temperature －40° C to +85° C<br>Storage temperature: -45° C to + 90° C |
| AT command | Support for standard AT instruction sets (Hayes 3GPP TS |

## 2.3 Module functional block diagram

The functional block diagram of the LPM2100 bm module mainly contains the following units：

- ✧ Baseband processing unit
- ✧ Power management unit
- ✧ RF transceiver unit
- ✧ RF front end unit
- ✧ Peripheral interface

The functional block diagram of the LPM2100 bm module is shown below：

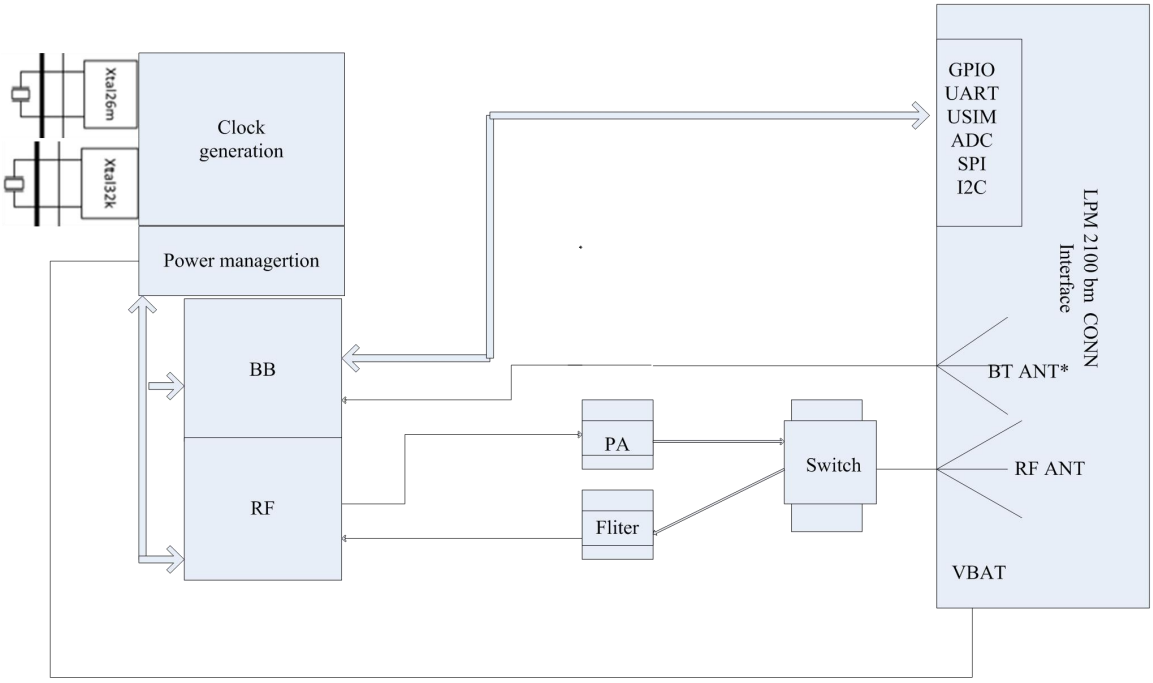



Figure 2-1 Functional block diagram of the LPM2100 bm module

## 2.4 Module working mode

Table 2-2 Working mode

| Operating mode | Description |
|---|---|
| Shut down | Module does not work in shutdown |

| | |
|---|---|
| Flight mode | The module turns off the module RF circuit and cannot interact with the network. |
| Sleep | The module turns off most of the functions and will be synchronized with the network. |
| Idle | Power on and successfully register the network, in idle state |
| Data transmission | The module is working and has data interaction with the network. |
| PSM mode | After entering the PSM mode, the module can achieve the minimum power consumption, and the internal power of the module is turned off. The software except the RTC stops running, and the serial port cannot be used. |

# Chapter 3. Interface application description

## 3.1 Chapter overview

The LPM2100 bm module has a total of 98 pins and includes the following partial unit interface functions. The functions of each unit interface will be described in detail in later chapters.

- ✧ Power interface
- ✧ SIM interface
- ✧ UART interface
- ✧ Network status indication interface
- ✧ SPI interface
- ✧ RF antenna interface (RF main antenna / BT antenna *)
- ✧ I2C interface.

## 3.2 Module interface

### 3.2.1 LPM2100 bm Pin map

LPM2100 bm pin assignment is as follows：

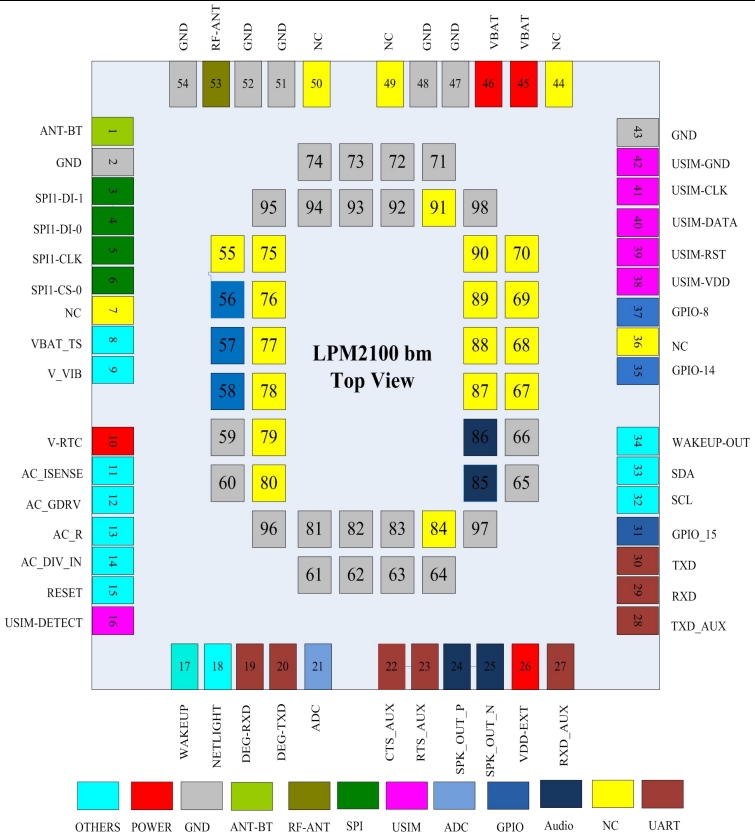



Figure 3-1 LPM2100 bm pin assignment diagram

**NOTE**

① The SIM card port level supports 1.8V and 3.0V.

② This module defines that the NC pin is floating and must not be used.

③ The module WAKEUP (PSM_EINT) pin voltage domain is 1.1V.

### 3.2.2 Module pin description

The module interface pin definition is described below：

Table 3-1 Pin Parameter Abbreviations

| Symbol sign | Description |
|---|---|
| IO | Input or output |
| PI | Power input |
| PO | Power Output |
| AI | Analog input |
| AO | Analog output |
| DI | Digital input |
| DO | Digital output |

Table 3-2 Interface definition

| Pin | Pin name | IO | Functional description | Remarks |
|---|---|---|---|---|
| **Powered by** | | | | |
| 45,46 | VBAT | PI | Module power supply | 3.5~4.2V |
| 26 | VDD_EXT | PO | Internal regulated power supply output 1.8V or 2.8V (software can be customized, default 2.8V) | IO voltage domain |
| **System switch control** | | | | |
| 15 | RESET | DI | Hardware reset control, active low | |
| **SIM interface** | | | | |
| 16 | SIM_DECT | DI | SIM card hot plug detection | Internal level has been pulled up |
| 38 | SIM_VDD | PO | Output to the SIM card supply voltage | Keep away from interference sources |
| 39 | SIM_RST | DO | SIM card reset output | Keep away from interference sources |
| 40 | SIM_DATA | IO | SIM card bus data | Internal 10K pull-up resistor |
| 41 | SIM_CLK | DO | SIM card clock output | Keep away from interference sources |
| 42 | SIM_GND | | SIM card Groud | GND |
| **Status indication** | | | | |
| 18 | NETLIGHT | DO | Network status indication | IO voltage domain |
| **Main serial interface** | | | | |
| 29 | RXD | DI | Master data reception | IO voltage domain |
| 30 | TXD | DO | Master data transmission | IO voltage domain |
| **Debug serial interface** | | | | |
| 19 | DBG_RXD | DI | Module debug data reception | Debug serial port |
| 20 | DBG_TXD | DO | Module debug data | Debug serial port |

| | | | | |
|---|---|---|---|---|
| | | | transmission | |
| **Secondary serial interface** | | | | |
| 27 | RXD_AUX | DI | Data reception | IO voltage domain |
| 28 | TXD_AUX | DO | Data transmission | IO voltage domain |
| 22 | CTS_AUX | DO | Clear send | IO voltage domain |
| 23 | RTS_AUX | DI | Request to send | IO voltage domain |
| **I2C interface** | | | | |
| 32 | SCL | DO | I2C bus clock output | Internal 10K pull-up resistor |
| 33 | SDA | IO | I2C bus data input and output | Internal 10K pull-up resistor |
| **SPI interface** | | | | |
| 3 | SPI_DI_1 | DI | Host input slave output | IO voltage domain |
| 4 | SPI_DI_0 | DO | Host output slave input | IO voltage domain |
| 5 | SPI_CLK | DO | Serial clock signal | IO voltage domain |
| 6 | SPI_CS | DO | Chip select signal | IO voltage domain |
| **CHARGE interface*** | | | | |
| 8 | VBAT_TS | DI | Battery in-position detection | Can be left unconnected when not in use |
| 11 | AC_ISENSE | DI | Charging current size detection | Reserved |
| 12 | AC_GDRV | DO | Control external NMOS charging pin | Reserved |
| 13 | AC_R | DI | External charge detection interrupt pin | Reserved |
| 14 | AC_DIV_IN | DI | External charger voltage detection pin | 1/3 partial pressure is required for use |
| **ADC function pin** | | | | |
| 21 | ADC | AI | Universal analog to digital converter interface | IO voltage domain |
| **Analog voice function pin*** | | | | |
| 24 | SPK_P | AO | SPK positive differential | Reserved |

| | | | | |
|---|---|---|---|---|
| | | | output | |
| 25 | SPK_N | AO | SPK's negative differential output | Reserved |
| 85 | MIC-N | AI | MIC negative differential input | Reserved |
| 86 | MIC-P | AI | Positive differential input of MIC | Reserved |
| **Universal input and output interface** | | | | |
| 31 | GPIO_15 | IO | Universal input/output port | |
| 35 | GPIO_14 | IO | Universal input/output port | |
| 37 | GPIO_8 | IO | Universal input/output port | |
| 56 | GPIO_35 | IO | Universal input/output port | |
| 57 | GPIO_42 | IO | Universal input/output port | |
| 58 | GPIO_43 | IO | Universal input/output port | |
| **Antenna interface** | | | | |
| 53 | RF-ANT | IO | RF antenna interface | 50 Ω characteristic impedance |
| 1* | BT-ANT* | IO | BT antenna interface* | Reserved* |
| **Other function pins** | | | | |
| 9 | V_VIB | PO | Vibration drive* | Reserved* |
| 10 | V_RTC | PO | Output supply voltage | Provide 1.1V voltage domain |
| 17 | WAKEUP (PSM_EINT) | PI | Hardware control PSM pull high wake up | 1.1V voltage domain |
| 34 | WAKEUP_OUT | DO | Wake up host | |
| 7,36,44,49,50,55,67,68,69,70,75,76,77,78,79,80,84,85,86,87,90,91 | NC | | NC | Leave empty when not in use |

| | | | | |
|---|---|---|---|---|
| 2,43,47,48,51<br>52,54,59,60,<br>61,62,63,64,<br>65,66,71,72,<br>73,74,81,82,<br>83,92,93,94,<br>95,96,97,98 | GND | | Ground signal | |

## 3.3 Power interface

The LPM2100 bm module power connector consists of two parts：

- ✧ VBAT is the working power of the module;
- ✧ VDD_EXT is the internal LDO output IO voltage domain (current load up to 50mA) for external use.

### 3.3.1 VBAT interface

The power supply VBAT has a power-on voltage range of 3.5~4.2V. The module powers the internal RF and baseband circuitry through the VBAT pin. Under the premise of ensuring that the VBAT power supply is sufficient, it is recommended to be close to the power input and put 10pF, 0.1uF,1uF ceramic capacitor and 100uF tantalum capacitor. VBAT PCB traces are as short and thick as possible.

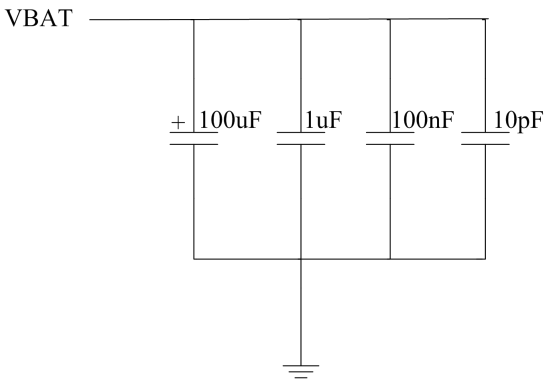



Figure 3-2 VBAT power supply

**NOTE**

① To prevent damage to the module from surges and overvoltages, it is recommended to connect a 5.1V/500mW Zener diode to the VBAT pin of the module.

② It is recommended to add multiple different capacitance capacitors (10pF, 1uF, 100nF, 100uF) to the VBAT pin and place them near the VBAT pin.

### 3.3.2 VDD_EXT Voltage output

After the LPM2100 bm module is powered on normally, the 26th pin will output the IO voltage domain, and the current load will be 50mA. The external master can read the voltage of VDD_EXT to judge whether the module is powered on. VDD_EXT can also be used as an external power supply, such as a level shifting chip.

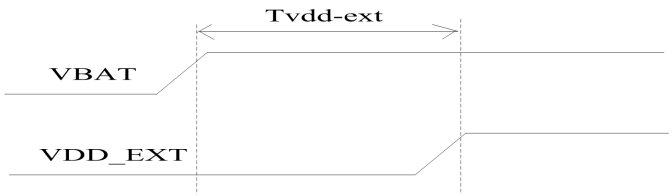



Figure 3-3 VDD_EXT power output timing diagram

## 3.4 Switching machine reset mode

### 3.4.1 Boot

The LPM2100 bm module VBAT is automatically powered on after power-on. The user can check whether the module is powered on by querying the high and low levels of the VDD_EXT pin.

The following picture shows the boot sequence diagram：

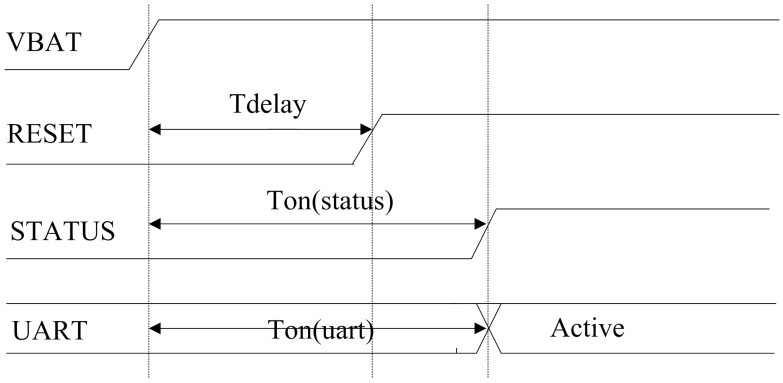



Figure 3-4 boot timing diagram

Table 3-3 Boot timing parameters

| Symbol | Description | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Tdelay | | | TBD | - | s |
| Ton(status) | Boot time (according to *status* status) | | TBD | - | s |

| | | | | | |
|---|---|---|---|---|---|
| Ton(uart) | Boot time (according to *uart* status) | | TBD | - | s |

### 3.4.2 Module shutdown

The LPM2100 bm module can be powered off by the VBAT pin or by using the AT "at+cpof" command.

When the module is powered on, the VBAT pin stops the power supply module and shuts down.

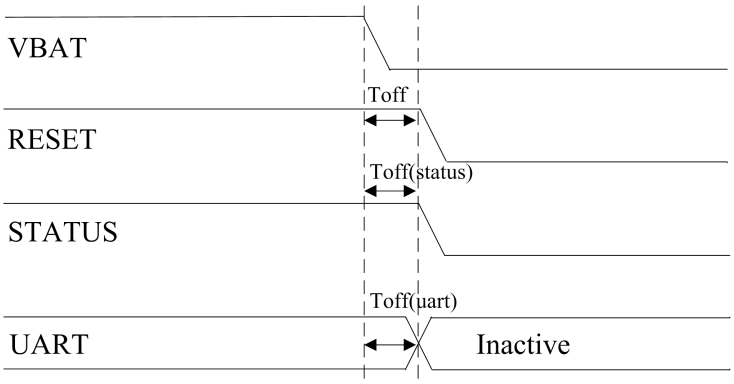



Figure 3-5 Shutdown timing diagram

Table 3-4 Shutdown timing parameters

| Symbol | Description | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Toff | | | TBD | - | s |
| Toff(status) | Shutdown time (according to status status) | | TBD | - | s |
| Toff(uart) | Shutdown time (according to uart status) | | TBD | - | s |

### 3.4.3 Reset

The PIN15 signal of the LPM2100 bm module is the RESET reset pin. The application detects that the module is abnormal. When the software does not respond, the module can be reset. Pull the pin low for 100-450ms to reset the module. The RESET pin is sensitive to interference. A 10 nF to 0.1 μ F capacitor can be placed near the signal for signal filtering. Keep away from RF interference signals when routing.

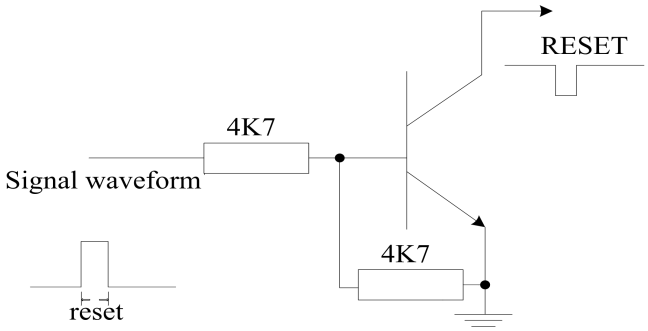



Figure 3-6 Reset reference circuit

Table 3-5 RESET pin parameters

| symbol | description | Min | Typical | Max | unit |
|---|---|---|---|---|---|
| Treset | Low pulse width | 100 | | 600 | ms |
| VIH | RESET input high level voltage | 0.68 | 1.07 | 1.41 | V |
| VIL | RESET input low level voltage | -0.3 | 0 | 0.68 | V |

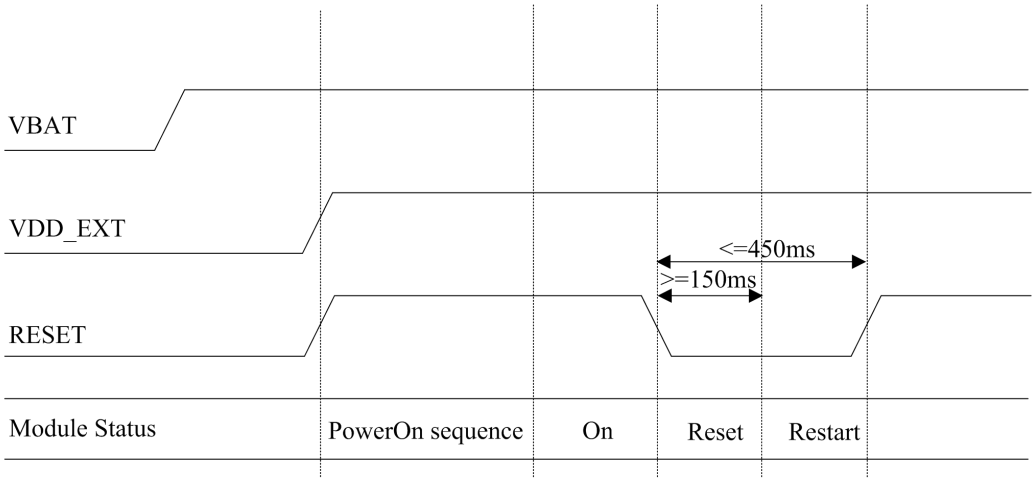



Figure 3-7 Reset timing diagram

The LPM2100 bm module supports AT command reset, and the AT command AT+TRB can be used to restart the module. Detailed instructions can be found in the "RDA_AT Command Manual" provided by the domain.

## 3.5 UART interface

The LPM2100 bm module provides three sets of UART interfaces. Main serial port, debug serial port, auxiliary serial port. The serial port level is the IO output level value. The module is a DCE (Data Communication Equipment) device.

The main serial port can realize AT interactive instructions and peripheral data interaction.

Debug the serial port to upgrade the firmware, view log information, and so on.

The module serial port baud rate can be set to 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600bps baud rate, the default is 57600bps.

Table 3-6 Serial port pin definitions

| Pin | Pin name | IO | Functional description | Remarks |
|---|---|---|---|---|
| **Main serial interface** | | | | |
| 29 | RXD | DI | Master data reception | IO voltage domain |
| 30 | TXD | DO | Master data transmission | IO voltage domain |
| **Debug serial interface** | | | | |
| 19 | DBG_RXD | DI | Module debug data reception | Debug serial port |
| 20 | DBG_TXD | DO | Module debug data transmission | Debug serial port |
| **Secondary serial interface** | | | | |
| 27 | RXD_AUX | DI | Data reception | IO voltage domain |
| 28 | TXD_AUX | DO | Data transmission | IO voltage domain |
| 22 | CTS_AUX | DO | Clear send | IO voltage domain |
| 23 | RTS_AUX | DI | Request to send | IO voltage domain |

Table 3-7 Serial port logic levels

| parameter | Min | Max | unit |
|---|---|---|---|
| VIL | 0 | 0.3*VDD_EXT | V |
| VIH | 0.7*VDD_EXT | VDD_EXT | V |
| VOL | 0 | 0.3*VDD_EXT | V |
| VOH | 0.7*VDD_EXT | VDD_EXT | V |

### 3.5.1Serial application circuit

If you need to use a 4-wire serial port, you can refer to the following connection methods:

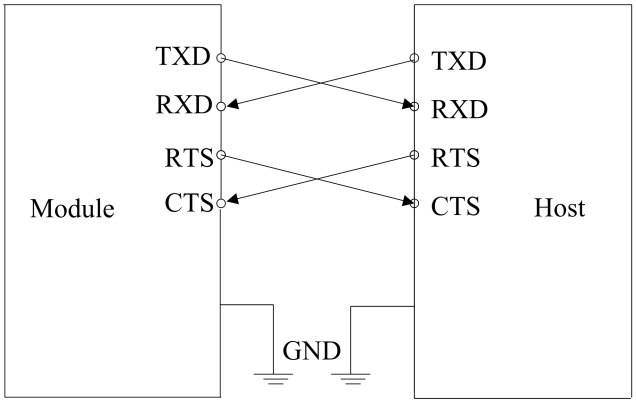



Figure 3-8 Full-featured serial port design

If you need to use a 2-wire serial port, you can refer to the following serial port design.

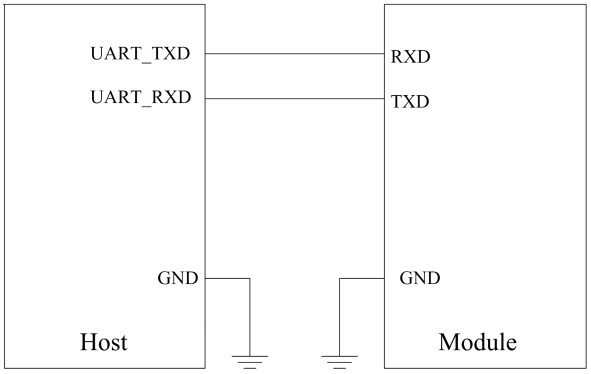



Figure 3-9 UART serial port design

The module serial port TTL is the IO output level value. If the serial port needs to be connected to the 3.3V level MCU, an external level conversion chip needs to be added externally to achieve level matching. The chip connection method can refer to the following circuit：

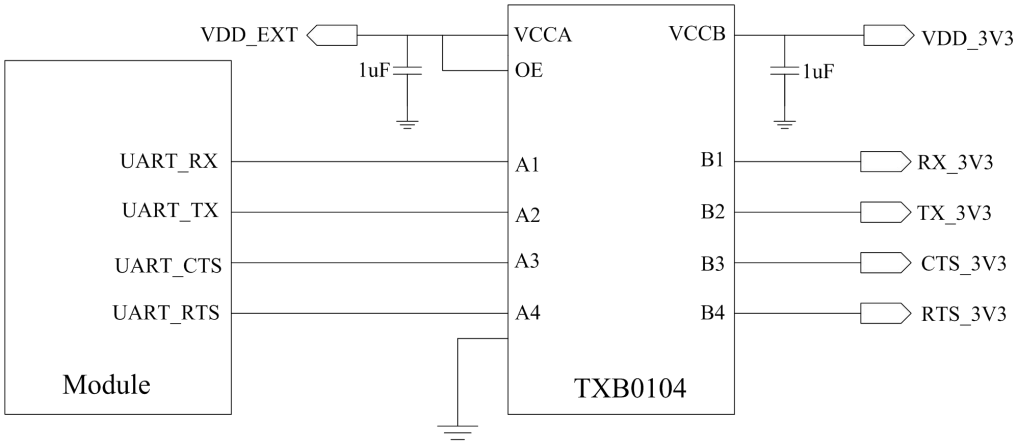


Figure 3-10 UART level conversion circuit

## 3.6 Power saving technology

LPM2100 bm supports three power saving modes：

- ✓ PSM (Power Saving Mode)
- ✓ DRX (Discontinuous Reception)
- ✓ eDRX (Extended DRX, extended discontinuous reception mode)

### 3.6.1 PSM

The main purpose of the PSM function is to reduce module power consumption and extend battery life. The module consumes a maximum of 5uA in PSM mode.

Suitable for services that have no delay requirement for downlink data, adopt battery-powered methods, such as meter reading services.

The process of the module entering the PSM is as follows: When the module establishes a connection with the network or updates the location tracking area (TAU), it will apply to enter the PSM in the request message, and the network configures the T3324 timer value return module and starts the timer. When the T3324 timer expires, the module enters the PSM. The module cannot apply to enter the PSM mode during emergency services or when initializing the public data network.

When the module is in the PSM mode, related activities such as searching for cell messages, cell reselection, and connecting to the network are turned off. However, the T3412 timer continues to work.

There are two ways for the module to exit the PSM mode: one data terminal device actively sends data wake-up, and the other is when the T3412 timer expires, the TAU starts, and the module exits the PSM.。

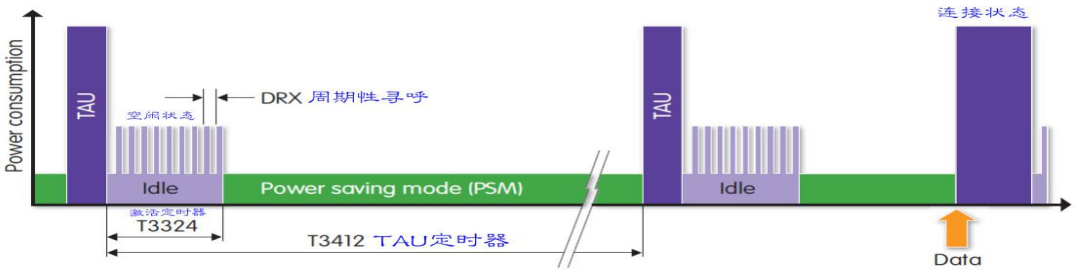



Figure 3-11 PSM power saving technology

### 3.6.2 DRX

The DRX cycle is short (1.28s, 2.56s, 5.12s, or 10.24s is determined by the carrier network side). The downlink service is considered to be reachable at any time with a small

delay. The module will detect whether there is a downlink service arrival, which is suitable for services with high latency requirements. Module equipment generally adopts the way of power supply, such as street light business.

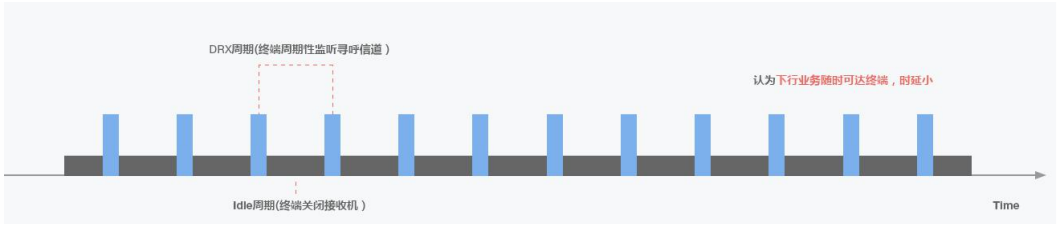



Figure 3-12 DRX power saving technology

### 3.6.3 eDRX

During each eDRX cycle, there is a Paging Time Window (PTW). The terminal listens to the paging channel in the PTW according to the DRX cycle (the DRX cycle time is short, and the terminal can be considered to be not sleeping and always reachable). Data, the rest of the terminal is in a sleep state.

In eDRX mode, the terminal device can be considered as reachable at any time, but the delay is large. The delay depends on the eDRX cycle configuration, which can balance the low power consumption and the delay. Such as remote shutdown of the gas business.


Figure 3-13 eDRX power saving technology

## 3.7 SIM interface

The LPM2100 bm module provides an ISO 7816-3 compliant SIM card interface. The SIM card power supply is provided by the module's internal power manager and supports 1.8V/3.0V.

Table 3-8 SIM card signal definition

| Pin | Signal name | IO | Functional description | Remarks |
|---|---|---|---|---|
| 16 | SIM_DECT | DI | SIM card hot plug detection* | (Internal level has been pulled up) |
| 38 | SIM_VDD | PO | Output to the SIM card supply | Keep away from |

| | | | | |
|---|---|---|---|---|
| | | | voltage | interference sources |
| 39 | SIM_RST | DO | SIM card reset output | Keep away from interference sources |
| 40 | SIM_DATA | IO | SIM card bus data | Internal 10K pull-up resistor |
| 41 | SIM_CLK | DO | SIM card clock output | Keep away from interference sources |
| 42 | SIM_GND | | SIM card ground | |

### 3.7.1 SIM card reference circuit

The LPM2100 bm module does not have a SIM card slot. Users need to design a SIM card slot on their own interface board.

SIM card interface reference circuit is as follows：

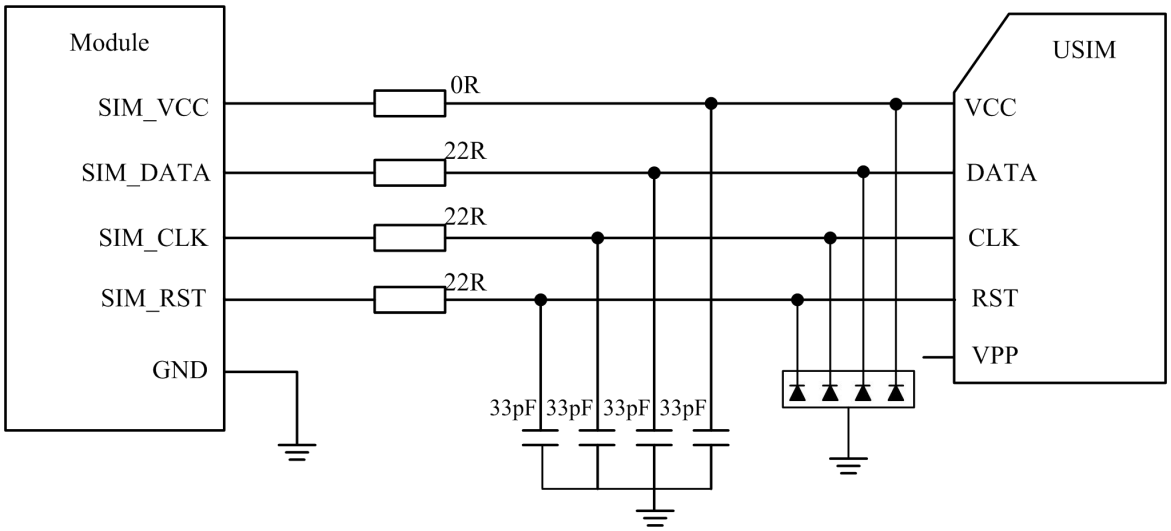



Figure 3-14 SIM circuit design

**NOTE**

① It is recommended to select ONSEMI's SMF15C device for ESD protection on the SIM card interface line. The peripheral circuit device should be placed close to the card holder. The SIM card holder is close to the module layout.

② The SIM card circuit is susceptible to radio frequency interference and does not recognize or remove the card. Therefore, the card slot should be placed as far as possible from the RF radiation of the antenna. The trace should be as far away as possible from the RF, power supply and high-speed signal lines.

③ The SIM_DECT has been internally pulled up to VDD_EXT with a 100K resistor and no external pull-up is required.

④ SIM_DECT is the SIM card inserted or not inserted detection pin, the default is high level, the SIM card status can be detected by this PIN pin during hot plug application.

⑤ To avoid transient voltage overload, the SIM interface requires a 22R resistor in series with each other on the signal line path.

⑥ The ground of the SIM card holder and the ground of the module should maintain good connectivity.

### 3.7.2 SIM_DECT Hot Swap Reference Design*

The LPM2100 bm module supports SIM card hot swapping.

The SIM_DECT pin acts as an input detection pin to determine whether the SIM card is inserted or not. The SIM_DECT pin defaults to a high level. The hot plug function can be turned on or off by AT+HOSCFG. This function is disabled by default (see the “RDA_AT Command Manual” provided in the domain for details).

Table 3-9 SIM card hot swap detection pin definition

| NO | Pin detection status | Functional description |
|---|---|---|
| 1 | high | SIM card insertion, SIM_DECT is high |
| 2 | low | SIM card is pulled out, SIM_DECT is low |

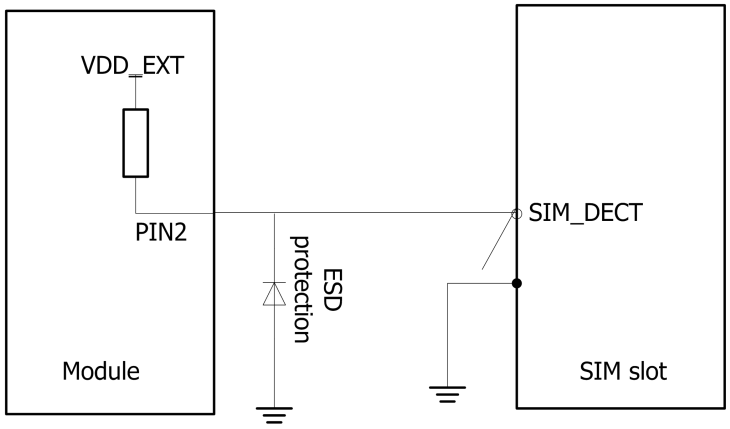



Figure 3-15 SIM card hot swap detection circuit*

**NOTE**

① It is recommended to add a diode protection next to the SIM_DECT pin of the module.

② When using a normally closed SIM card holder or a normally open SIM card holder, the detection level can be set by the AT command. If AT+HOSCFG=1,1 is set, the state of the SIM card is high when it is in position. When AT+HOSCFG=1,0 is set, the state of the SIM card is low when it is in position. When AT+HOSCFG=0,0 is set. The SIM card hot plug function is turned off.

③ "*" indicates that it is under development。

## 3.8 ADC interface

The LPM2100 bm module provides a 10-bit analog-to-digital conversion input interface for sample monitoring such as external temperature. The ADC pin voltage can be read by the AT command.

In order to improve the accuracy of the ADC, the ADC trace should have a good reference ground.

Table 3-10 ADC Signal Definition

| Pin | Signal name | IO | High value | Description |
|---|---|---|---|---|
| 21 | ADC | AI | Universal analog to digital converter interface | |

## 3.9 SPI interface

The LPM2100 bm module provides a set of SPI interfaces with an interface voltage of IO output level.

Table 3-11 SPI Signal Definition

| Pin | Pin name | IO | Functional description | Remarks |
|---|---|---|---|---|
| 3 | SPI-DI-1 | DI | Host input slave output | IO voltage domain |
| 4 | SPI-DI-0 | DO | Host output slave input | IO voltage domain |
| 5 | SPI-SCLK | DO | Serial clock signal | IO voltage domain |
| 6 | SPI-CS | DO | Chip select signal | IO voltage domain |

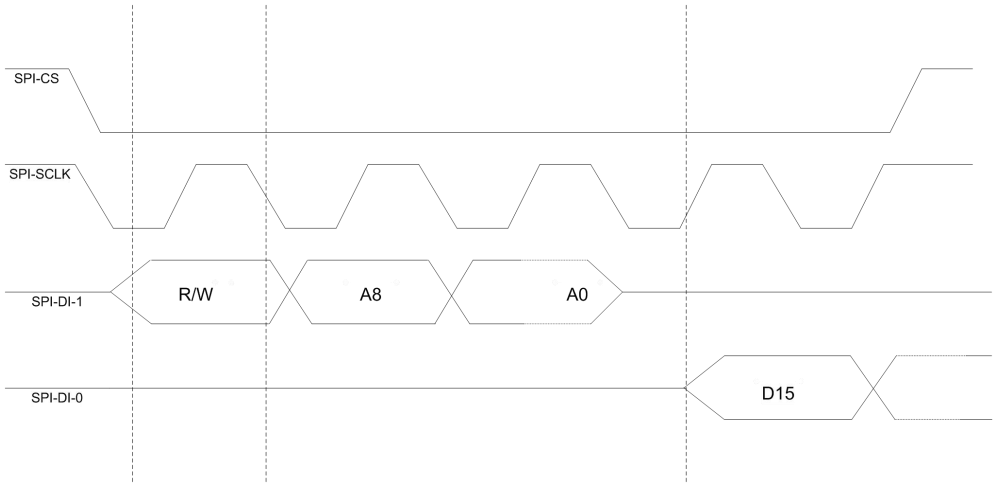



Figure 3-16 SPI read timing diagram

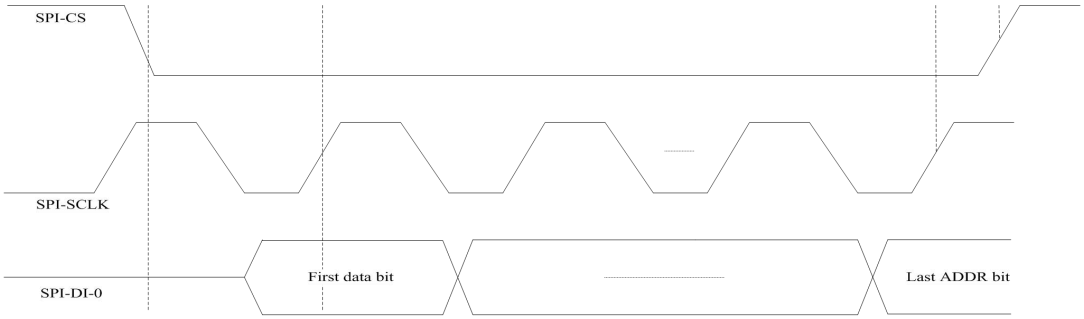



Figure 3-17 SPI write timing diagram

## 3.10 I2C bus

The LPM2100 bm module provides a set of hardware 5.0 protocol bidirectional serial bus with a clock rate of 400KHZ and an interface voltage of IO output level.

Table 3-12 I2C pin definition

| Pin | Pin name | IO | Functional description | Remarks |
|---|---|---|---|---|
| 32 | SCL | DO | I2C bus clock output | Internal resistance pull-up |
| 33 | SDA | IO | I2C bus data input and output | Internal resistance pull-up |

I2C reference circuit as shown below：

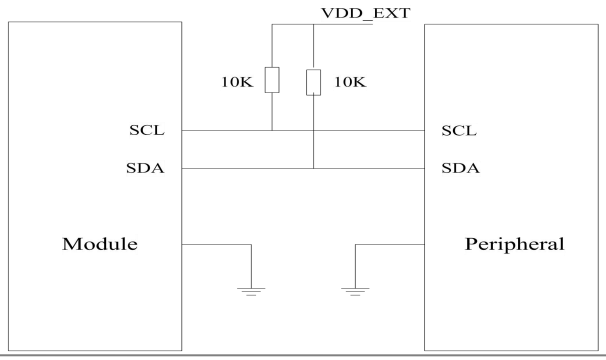


Figure 3-18 I2C interface reference circuit

NOTE

The I2C_SCL and I2C_SDA pins are internally pulled up, so the external pull-up resistor can be ignored during use.

## 3.11 Network indication interface*

The LPM2100 bm module provides a NETLIGHT pin to indicate network communication status and can be used to drive LED lights that indicate network status.

Table 3-13 Network indicator pin definition

| Pin | Pin name | IO | Functional description |
|---|---|---|---|
| 18 | NETLIGHT | DO | Network status indication |

Table 3-14 Network indication status

| status | LED display status |
|---|---|
| Module not running or module not registered | Slow flash |
| Module is registering network | Fast flash |
| Module is connected to the network | Constantly bright |

LED network indicator reference design is as follows：

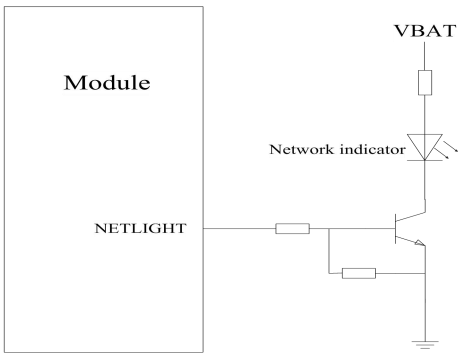



Figure 3-19 Network indicator circuit diagram

NOTE

The size of the resistor in the network indicator circuit diagram can be adjusted according to the LED lamp parameters.

## 3.12 General purpose GPIO interface

The LPM2100 bm module provides six GPIOs. Some of these GPIOs can be reused for multiple functions. Consult the module provider for specific usage.

Table 3-15 General GPIO Pin Definitions

| Pin | Pin name | IO | Functional description | Remarks |
|---|---|---|---|---|
| 31 | GPIO_15 | IO | Universal input/output port | Reserved |
| 35 | GPIO_14 | IO | Universal input/output port | Reserved |
| 37 | GPIO_8 | IO | Universal input/output port | Reserved |
| 56 | GPIO_35 | IO | Universal input/output port | Reserved |
| 57 | GPIO_42 | IO | Universal input/output port | Reserved |
| 58 | GPIO_43 | IO | Universal input/output port | Reserved |

## 3.13 Other interface

### 3.13.1 WAKEUP interface

The LPM2100 bm module supports the PSM function and wakes up the module by pulling the WAKEUP pin high.

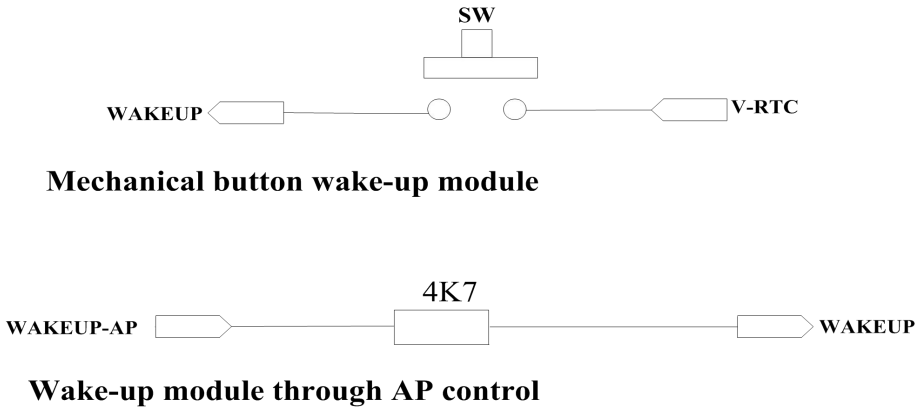



Figure 3-20 WAKEUP wake-up module reference circuit

### 3.13.2 WAKEUP_OUT interface*

The LPM2100 bm module supports the WAKEUP_OUT function. When the module is in the sleep state, if a wake-up event is received, the pin will wake up the host by pulling high.

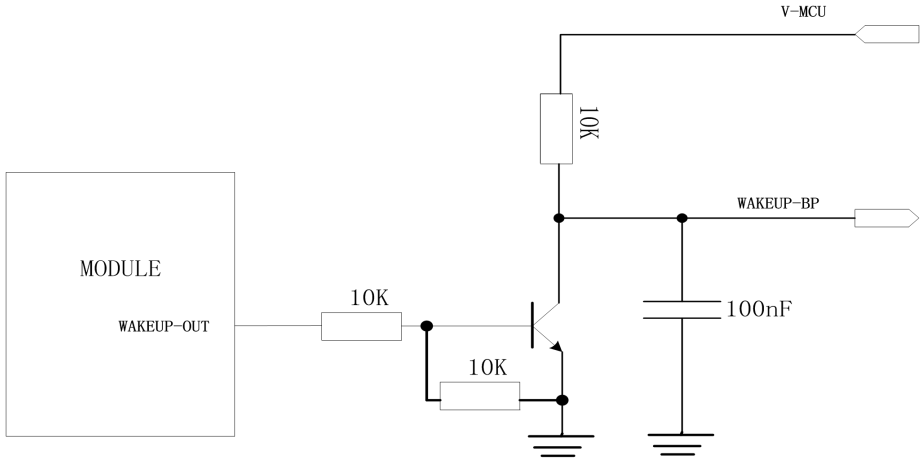



Figure 3-21 WAKEUP_OUT wake-up host reference circuit

# Chapter 4. Overall RF technical indicators

## 4.1 Chapter overview

- ✧ The LPM2100 bm module RF overall specifications include the following sections:
- ✧ Antenna design;
- ✧ RF PCB design;
- ✧ RF connector
- ✧ working frequency
- ✧ Conducted transmission power and receiving sensitivity;
- ✧ RF power consumption characteristics.

## 4.2 Antenna design

### 4.2.1 Main antenna

Pin 53 of the LPM2100 bm module provides the main antenna interface. In the circuit design, the trace between the module and the antenna must be guaranteed to 50 ohms.

The antenna is a sensitive device that is susceptible to the external environment. For example, module size, antenna position, footprint size, and surrounding grounding can all affect antenna performance.

The module antenna pins are defined as follows：

Table 4-1 RF Pin Definitions

| Pin | Pin name | IO | Functional description | Remarks |
|---|---|---|---|---|
| 53 | RF_ANT | IO | Main antenna interface | 50Ω characteristic impedance |

The 53 pin of the LPM2100 bm module is the main antenna interface. To facilitate the debugging of the antenna, it is necessary to add a π-type matching circuit to the main board, and take the 50Ω impedance line. The recommended circuit is as shown below：

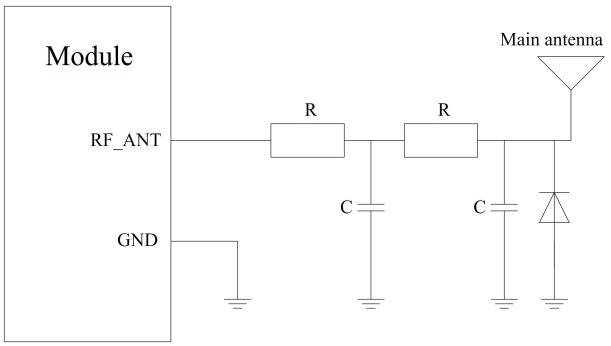


Figure 4-1 Main antenna matching circuit diagram

**NOTE**

LPM2100 bm module RF antenna is extracted by pad method。

① The antenna impedance trace needs to be away from the digital signal line, power supply and other interference signals.

② The antenna impedance traces need to be three-dimensionally packaged, and more holes are added on both sides of the trace to isolate.

③ The antenna line loss is less than 0.3dB, so keep the PCB trace as short as possible.

④ The parasitic capacitance of the TVS tube pin itself in antenna matching must be small to avoid signal interference. Parasitic capacitance must be less than 0.5pF or even lower。

### 4.2.2 Bluetooth antenna*

The LPM2100 bm module provides a BT antenna interface. In the circuit design, the trace between the module and the antenna must be guaranteed to 50 ohms.

The 1 pin of the LPM2100 bm module is the BT antenna interface. To facilitate the antenna debugging, it is necessary to add a π -type matching circuit to the main board and take the 50-ohm impedance line. The recommended circuit is as follows:

The module Bluetooth antenna pin is defined as follows：

Table 4-2 Bluetooth pin definition

| Pin | Pin name | IO | Functional description | Remarks |
|---|---|---|---|---|
| 1 | BT-ANT | DI | Bluetooth antenna interface | 50 ohm characteristic impedance* |

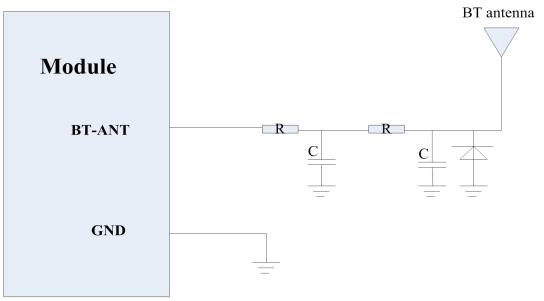



Figure 4-2 Bluetooth antenna matching circuit diagram

**NOTE**

LPM2100 bm module BT antenna is extracted by pad method。

① The antenna impedance trace needs to be away from the digital signal line, power supply and other interference signals, away from the noise source.

② It is also necessary to place the module away from the circuit that is prone to heat.

③ The length of the antenna feed should be minimized to reduce signal attenuation.

④ The antenna impedance traces need to be three-dimensionally packaged, and more holes are added on both sides of the trace to isolate.

⑤ The antenna line loss is less than 0.3dB, so keep the PCB trace as short as possible.

⑥ The parasitic capacitance of the TVS tube pin itself in antenna matching must be small to avoid signal interference. Parasitic capacitance must be less than 0.5pF or even lower。

## 4.3 RF PCB design

For the user, the characteristic impedance of all RF signal lines should be controlled at 50Ω. The impedance of the RF signal line is determined by the dielectric constant of the material, the trace width (W), the ground clearance (S), and the height of the reference ground plane (H). Please use the impedance simulation tool to calculate the impedance value of the RF trace. The control of the PCB characteristic impedance is usually in the form of microstrip lines and coplanar waveguides.

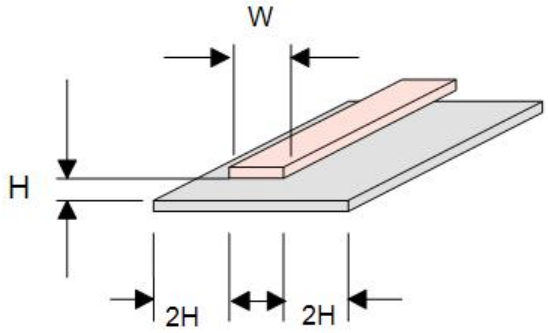



Figure 4-3 Complete structure of the microstrip line

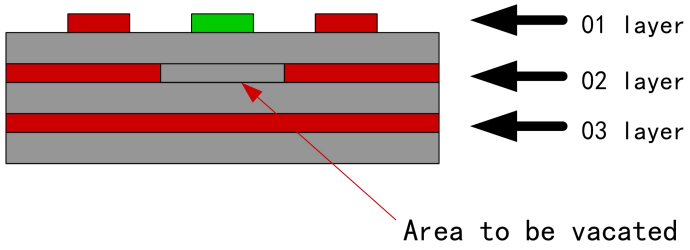



Figure 4-4 Reference ground is the third layer microstrip transmission line structure

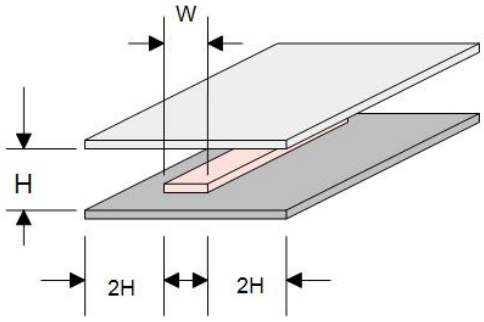



Figure 4-5 Complete structure of the strip line

## 4.4 RF connector

If you need to use the RF connector connection during the design process, the antenna connector must use a 50 ohm characteristic impedance coaxial connector. Hirose's UF.L-R-SMT connector is recommended.

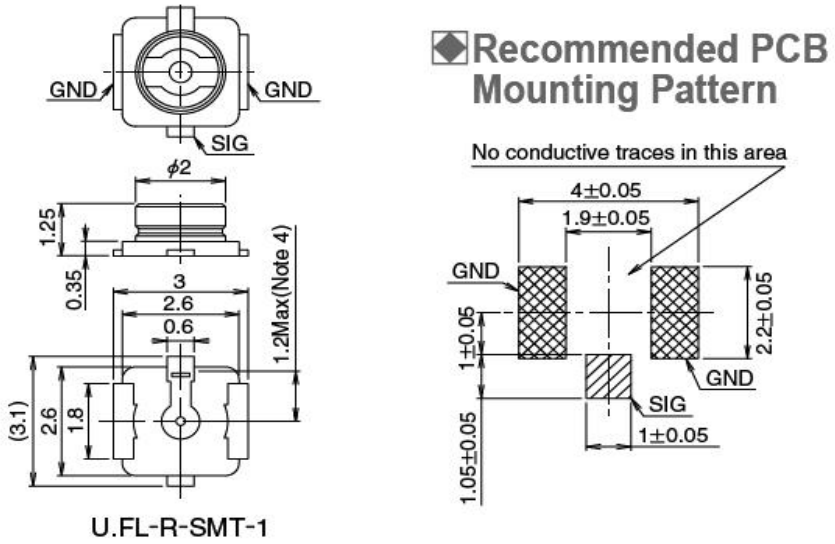



Figure 4-6 RF connector size chart

The RF connector plug for this connector is HRS's U.FL-LP series.

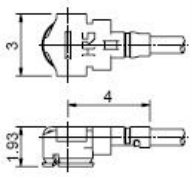
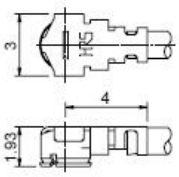
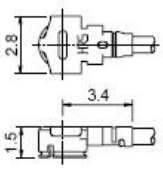
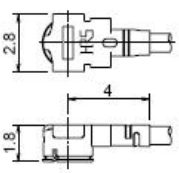
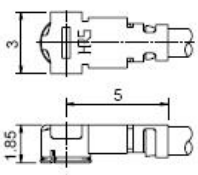
| Part No. | U.FL-LP-040 | U.FL-LP-066 | U.FL-LP(V)-040 | U.FL-LP-062 | U.FL-LP-088 |
|---|---|---|---|---|---|
| |  |  |  |  |  |
| Mated Height | 2.5mm Max. (2.4mm Nom.) | 2.5mm Max. (2.4mm Nom.) | 2.0mm Max. (1.9mm Nom.) | 2.4mm Max. (2.3mm Nom.) | 2.4mm Max. (2.3mm Nom.) |
| Applicable cable | Dia. 0.81mm Coaxial cable | Dia. 1.13mm and Dia. 1.32mm Coaxial cable | Dia. 0.81mm Coaxial cable | Dia. 1mm Coaxial cable | Dia. 1.37mm Coaxial cable |
| Weight (mg) | 53.7 | 59.1 | 34.8 | 45.5 | 71.7 |
| RoHS | YES | | | | |

Figure 4-7 Antenna connector matching plug diagram

Table 4-3 Main parameters of the RF connector

| **Rated condition** | | **Environmental conditions** |
|---|---|---|
| Frequency Range | DC to 6GHZ | －40℃ to＋80℃ |
| Characteristic impedance | 50 Ω | －40℃ to＋80℃ |

## 4.5 Working frequency

Table 4-4 RF frequency table

| **LPM2100_bm** | **Support band** | **Uplink frequency** | **Download frequency** |
|---|---|---|---|
| LPM2100_ bm | B3 | 1710 MHz－1785 MHz | 1805 MHz－1880 MHz |
| | B5 | 824 MHz － 849 MHz | 869 MHz － 894 MHz |
| | B8 | 880 MHz － 915 MHz | 925 MHz － 960 MHz |
| | B20 | 832 MHz － 862 MHz | 791 MHz － 821 MHz |
| | B28 | 703 MHz － 748 MHz | 758 MHz － 803 MHz |
| | GSM850 | 824 MHz － 849 MHz | 869 MHz － 894 MHz |
| | GSM900 | 880 MHz － 915 MHz | 925 MHz － 960 MHz |
| | DCS1800 | 1710 MHz－1785 MHz | 1805 MHz－1880 MHz |
| | PCS1900 | 1850 MHz－1910 MHz | 1930 MHz－1990 MHz |
| BT* | Reserved | Reserved | |

## 4.6 Conducted transmit power and receive sensitivity

Table 4-5 Conducted emission power indicators

| Frequency band | Maximum | Minimum |
|---|---|---|
| B3 | 23dBm±2dB | <44dBm |
| B5 | 23dBm±2dB | <44dBm |
| B8 | 23dBm±2dB | <44dBm |
| B20 | 23dBm±2dB | <44dBm |
| B28 | 23dBm±2dB | <44dBm |
| GSM850 | 33dBm±2dB | 5dBm±5dB |
| GSM900 | 33dBm±2dB | 5dBm±5dB |
| DCS1800 | 30dBm±2dB | 0dBm±5dB |
| PCS1900 | 30dBm±2dB | 0dBm±5dB |

Table 4-6 Conducted Receiver Sensitivity Indicators

| Directory (sensitivity) | 3GPP protocol requirements | Min | Typical |
|---|---|---|---|
| B3 | -108.2 | <-108.2 | -127dBm±1dB |
| B5 | -108.2 | <-108.2 | -127dBm±1dB |
| B8 | -108.2 | <-108.2 | -127dBm±1dB |
| B20 | -108.2 | <-108.2 | -127dBm±1dB |
| B28 | -108.2 | <-108.2 | -127dBm±1dB |
| G850/G900 | -102.4 | <-102.4 | -112dBm±1dB |
| DCS/PCS | -102.4 | <-102.4 | -110dBm±1dB |

## 4.7 RF power consumption characteristics

Table 4-7 Power consumption

| BAND | Power MAX | Call Current（mA） | |
|---|---|---|---|
| | | Power | Avg Current |
| B3 | 22.3 | Max power | 142 |
| B5 | 23 | Max power | 129 |
| B8 | 22.3 | Max power | 125 |
| B20 | 23 | Max power | 130 |
| B28 | 22.3 | Max power | 134 |

| | | | |
|---|---|---|---|
| GSM850 | 32 | Max power | 165 |
| GSM900 | 32 | Max power | 180 |
| DCS180 | 30 | Max power | 158 |
| PCS1900 | 30 | Max power | 128 |

# Chapter 5. Interface electrical characteristics

## 5.1 Chapter overview

- ✧ temperature range
- ✧ Module IO level
- ✧ power supply
- ✧ Electrostatic property
- ✧ Reliability index.

## 5.2 Range of working temperature

Table 5-1 LPM2100 bm module temperature range

| Parameter | Minimum value | Maximum value |
|---|---|---|
| Normal operating temperature | -35° C | 75° C |
| Extreme working temperature | -40° C | 85° C |
| storage temperature | -45° C | 90° C |

## 5.3 Module IO level

The port IO level of the LPM2100 bm module is as follows:

Which corresponds to 1.8V SIM application, SIM_VDD is 1.8V; corresponding to 3V SIM application, SIM_VDD is 3V.

Table 5-2 Electrical characteristics of the LPM2100 bm module

| Parameter | Parameter Description | Minimum value | Maximum value |
|---|---|---|---|
| VIH | High level input voltage | 0.7* VDD_EXT | VDD_EXT |
| VIL | Low level input voltage | - | 0.3*VDD_EXT |
| VOH | High level output voltage | 0.7*VDD_EXT | VDD_EXT |
| VOL | Low level output voltage | 0 | |

## 5.4 Power supply

LPM2100 bm module input power requirements are as follows：

Table 5-3 Operating voltage of the LPM2100 bm module

| Parameter | Description | Minimum | Typical | Maximum |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| VBAT | Module operating voltage | 3.5V | 3.7V | 4.2V |

The power-on time of any interface of the module must not be earlier than the boot time of the module, otherwise the module may be abnormal or damaged.

## 5.5 Electrostatic property

There is no overvoltage protection inside the LPM2100 bm module. When using the module, the static electricity should be protected to ensure product quality.

ESD design recommendations：

- ✧ The SIM card external pin of the module needs to be protected by adding TVS.
- ✧ At the module input power supply, increase the TVS.
- ✧ The protective device PCB layout should be as close as possible to the “V” shaped line to avoid the “T” shaped line.
- ✧ The ground plane around the module guarantees integrity and should not be split.
- ✧ ESD control of the surrounding environment and operators needs to be paid during module production, assembly and laboratory testing.

Table 5-4 LPM2100 bm ESD features

| Test port | Contact discharge | Air discharge | Unit |
|---|---|---|---|
| SIM interface | ±6 | ±10 | KV |
| VBAT power supply | ±6 | ±10 | KV |
| RF_ANT | ±6 | ±10 | KV |
| Other PORT | ±6 | ±10 | KV |

## 5.6 Reliability index

Table 5-5 Reliability test

| Test items | Test Conditions | Guideline | Experimental result |
|---|---|---|---|
| Low temperature work | Temperature: －20oC<br>Working mode: normal work<br>Test duration: 24 h | IEC60068-2-1 | Visual inspection: normal<br>Function check: normal<br>RF indicator check: normal |
| High temperature work | Temperature: 70oC<br>Working mode: normal work<br>Test duration: 24 h | JESD22-A108-C | Visual inspection: normal<br>Function check: normal<br>RF indicator check: normal |

| | | | |
|---|---|---|---|
| Temperature cycle | High temperature: 70oC<br>Low temperature: －20oC<br>Working mode: normal work<br>Test duration: 30<br>Cycles;1 h+1h /cycle | JESD22-A 105-B | Visual inspection: normal<br>Function check: normal<br>RF indicator check: normal |
| Drop test | Height 0.8 m, 6 sides each time, dropped to the horizontal marble platform<br>Working mode: no packaging, no<br>Power on, do not boot | IEC60068-2-32 | Visual inspection: normal<br>Function check: normal<br>RF indicator check: normal |

# Chapter 6. Structural and mechanical properties

## 6.1 Chapter overview

- ✧ Exterior
- ✧ Module mechanical size

## 6.2 Exterior

The LPM2100 bm module is a PCBA with a single-sided layout. The appearance of the module is as follows：

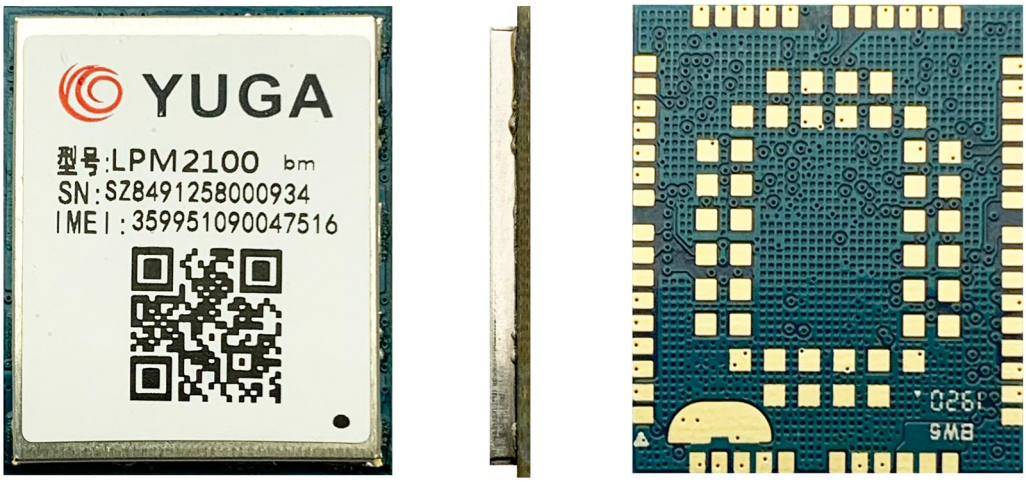



Figure 6-1 Appearance of the LPM2100 bm module

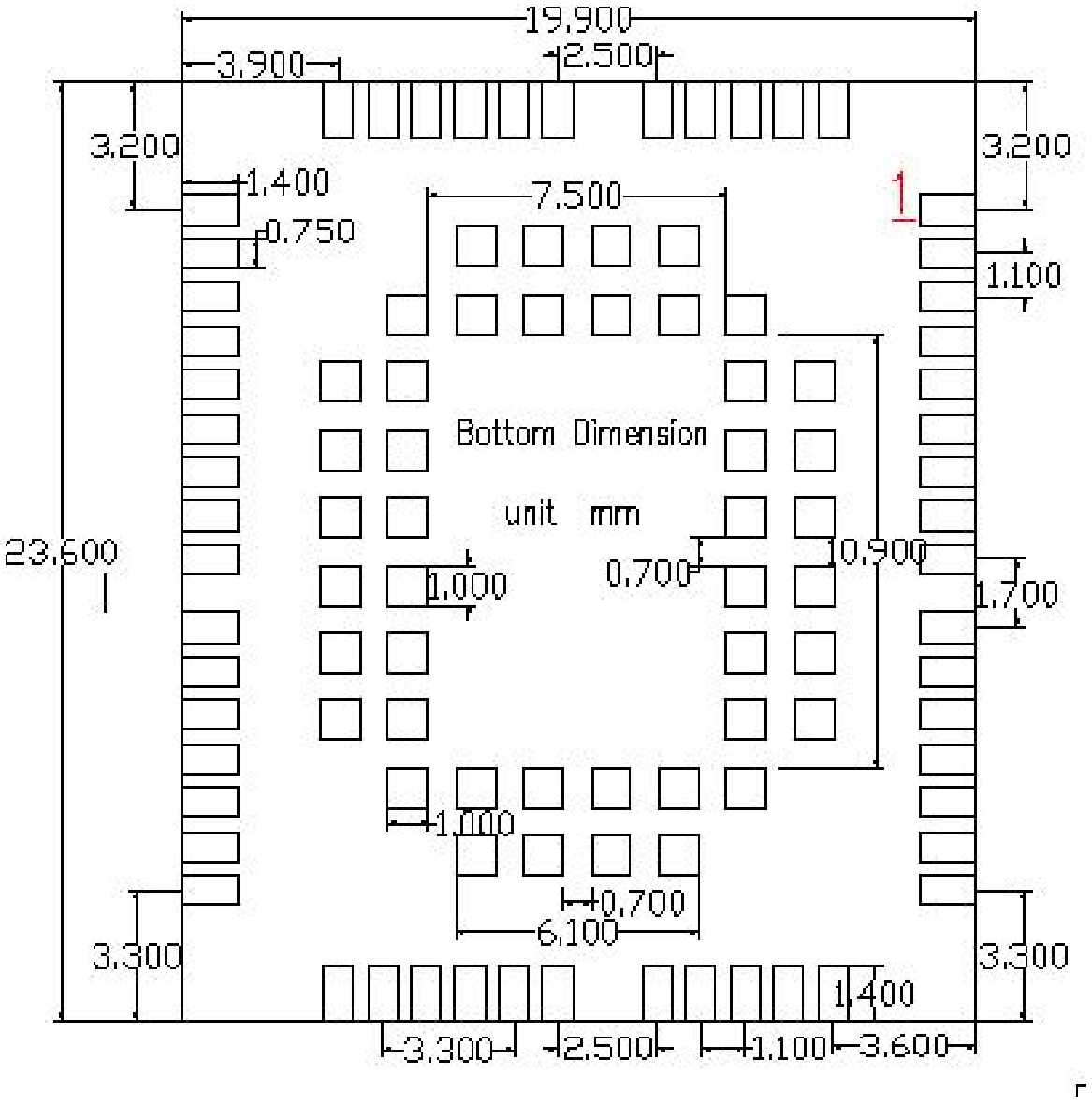



Figure 6-1 Appearance of the LPM2100 bm module

# Chapter 7. Production and packaging

## 7.1 Chapter overview

✧ Module packaging and storage

✧ Production welding.

## 7.2 Module packaging and storage

The LPM2100 bm module is packaged in a tray and packaged in a vacuum sealed bag. The 1000PCS is a plate and shipped as a vacuum sealed bag.

The storage of the LPM2100 bm module module is subject to the following conditions：

✧ The module has a moisture sensitivity rating of 3 levels.

✧ When the ambient temperature is greater than 40 degrees Celsius and the air humidity is less than 90%, the module can be stored in a vacuum sealed bag for 12 months.

✧ When the vacuum sealed bag is opened, if the ambient temperature of the module is lower than 30 degrees Celsius and the air humidity is less than 60%, the factory can complete the patch within 72 hours, and the module can directly perform reflow soldering or other high temperature process.

✧ If the module is in other conditions, it needs to be baked before the patch.

✧ If the module needs to be baked, please remove the module and bake it for 8 hours at 125 degrees Celsius (allowing fluctuations of up to 5 degrees Celsius).

## 7.3 Production welding

The LPM2100 bm module is packaged in an anti-static tray. The SMT line needs to be equipped with a Tray module. It is recommended to use a reflow oven above 7 temperature zones.

✧ To ensure the quality of the module paste, the thickness of the stencil corresponding to the pad portion of the LPM2100 bm module is recommended to be 0.18 mm.

✧ The recommended reflow temperature is 235~245oC, which cannot exceed 260oC.

✧ When the PCB is laid out on both sides, the LCC module layout must be machined on the 2nd side. Avoid module falling parts, welding and welding, and poor internal welding of the module caused by the gravity of the module.

The recommended furnace temperature curve is shown below：

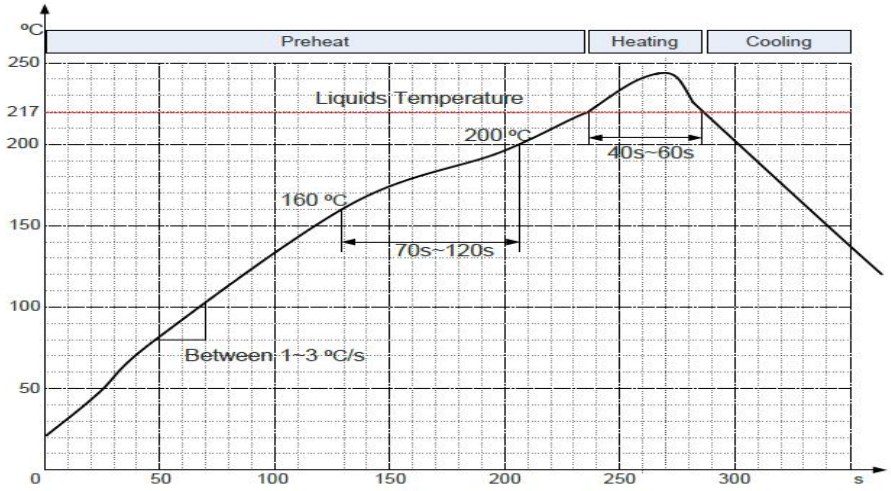



Figure 7-1 Reflow soldering temperature graph

Table 7-1 Reflow process parameter table

| Warm zone | Time | Key parameter |
|---|---|---|
| Preheating zone（40℃～165℃） | | Heating rate：1℃/s～3℃/s |
| Temperature zone（160℃～210℃） | (t1～t2)：70s～120s | |
| Recirculation zone（＞217℃） | (t3～t4)：40s～60s | Peak temperature：235℃～245℃ |
| Cooling zone | Cooling rate：2℃/s ≤ Slope ≤ 5℃C/s | |

# Chapter 8. Abbreviation

Table 8-1 Abbreviations

| Abbreviations | Full name |
|---|---|
| 3GPP | Third Generation Partnership Project |
| AMR | Adaptive Multi-rate |
| CTS | Clear to Send |
| DTR | Data Terminal Ready |
| DL | Down Link |
| DTE | Data Terminal Equipment |
| EMC | Electromagnetic Compatibility |
| ESD | Electrostatic Discharge |
| LED | Light-Emitting Diode |
| NC | Not Connected |
| SIM | Universal Subscriber Identity Module |
| TVS | Transient Voltage Suppressor |
| PCB | Printed Circuit Board |
| TX | Transmitting Direction |
| UART | Universal Asynchronous Receiver-Transmitter |
| QPSK | Quadrature Phase Shift Keying |
| RF | Radio Frequency |