MULTI-INNO TECHNOLOGY CO., LTD.

LCD MODULE SPECIFICATION

Model : MI28864AO

Revision	0.0
Engineering	
Date	
Our Reference	

SPECIFICATION

PART NO. : MI28864AO

OLED 2.67"
288X64

PRODUCT CONTENTS

		Customer	
Written by	**Hujiabin**	**Approved by**	
Checked by	**Zhangweicang**		
Approved by	**Sujunhai**		

REVISION HISTORY

Rev.	Contents	Date
0.0	Preliminary 2008-9-22	

■ PHYSICAL DATA

No.	Items:	Specification:	Unit
1	Diagonal Size	2.67	Inch
2	Resolution	288(H) x 64(V)	Lines
3	Active Area	66.22 (W) x 14.70(H)	mm
4	Outline Dimension (Panel)	82.00 (W) x 25.50(H)	mm
5	Pixel Pitch	0.23 (W) x 0.23 (H)	mm
6	Pixel Size	0.205 (W) x 0.205(H)	mm
7	Driver IC	SSD1332	-
8	Display Color	White	-
9	Grayscale	16 Level	-
10	Interface	Parallel / Serial	-
11	IC package type	COF	-
12	Thickness	1.5±0.1	mm
13	Weight	TBD	g
14	Duty	1/64	-

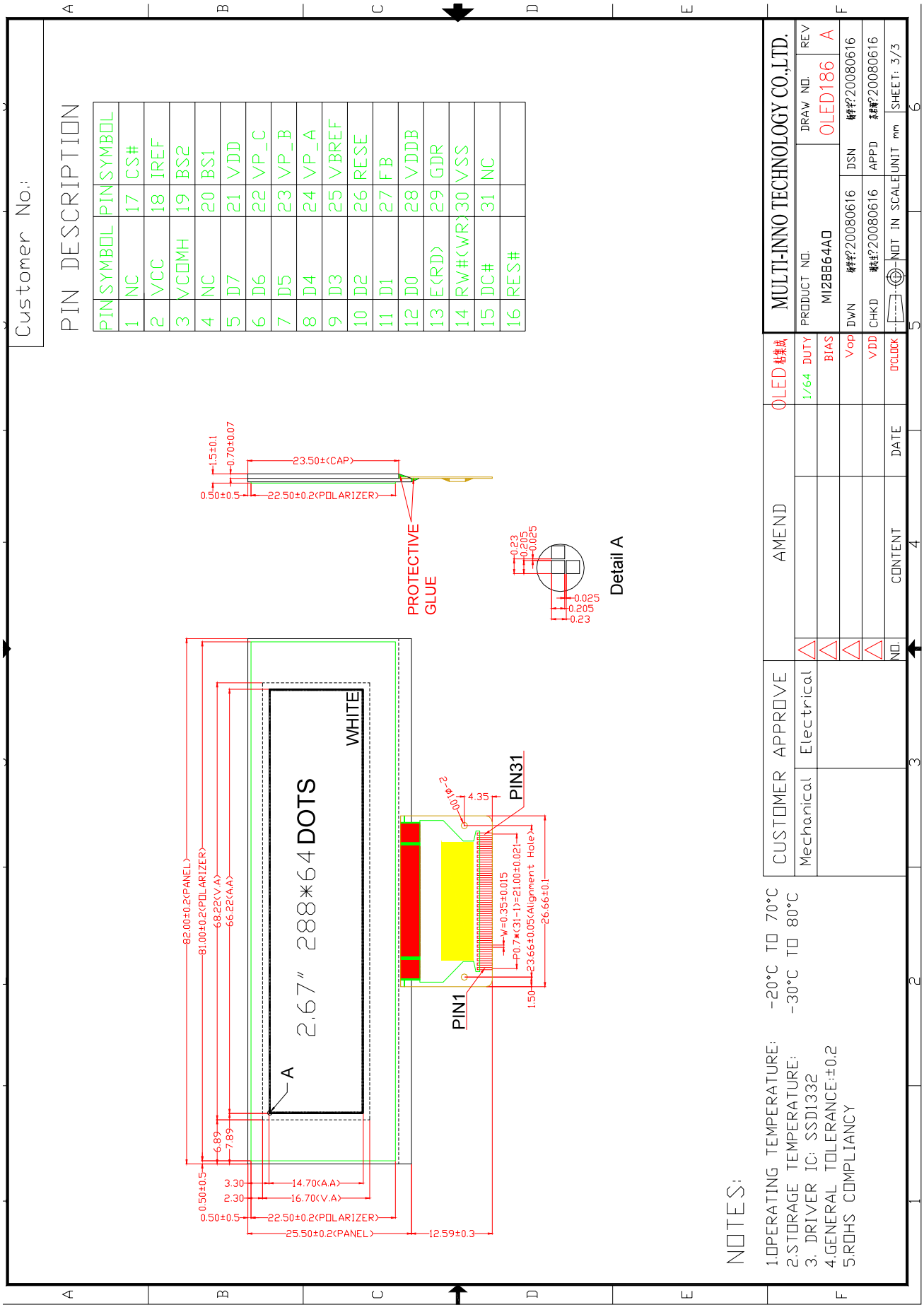
■ ABSOLUTE MAXIMUM RATINGS

Unless otherwise specified, V_{SS} = 0V (Ta = 25℃)

Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	Logic	V_{DD}	-0.3	-	4.0	V
	Driving	V_{CC}	0	-	19.0	V
Operating Temperature		Top	-20	-	70	℃
Storage Temperature		Tst	-30	-	80	℃
Humidity		-	-	-	90	%RH

NOTE:
Permanent device damage may occur if **ABSOLUTE MAXIMUM RATINGS** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ EXTERNAL DIMENSIONS



■ ELECTRICAL CHARACTERISTICS

◆DC Characteristics

Unless otherwise specified, V_{SS} = 0V ,V_{DD}=2.4V to 3.5V (Ta = 25℃)

Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	Logic	V_{DD}	2.4	3.0	3.5	V
	Operating	V_{CC}	7.0	13.0	16.0	V
Input Voltage	High Voltage	V_{IH}	0.8 x V_{DD}	-	V_{DD}	V
	Low Voltage	V_{IL}	V_{SS}	-	0.2 x V_{DD}	V
Output Voltage	High Voltage	V_{OH}	0.9 x V_{DD}	-	V_{DD}	V
	Low Voltage	V_{OL}	V_{SS}	-	0.1 x V_{DD}	V

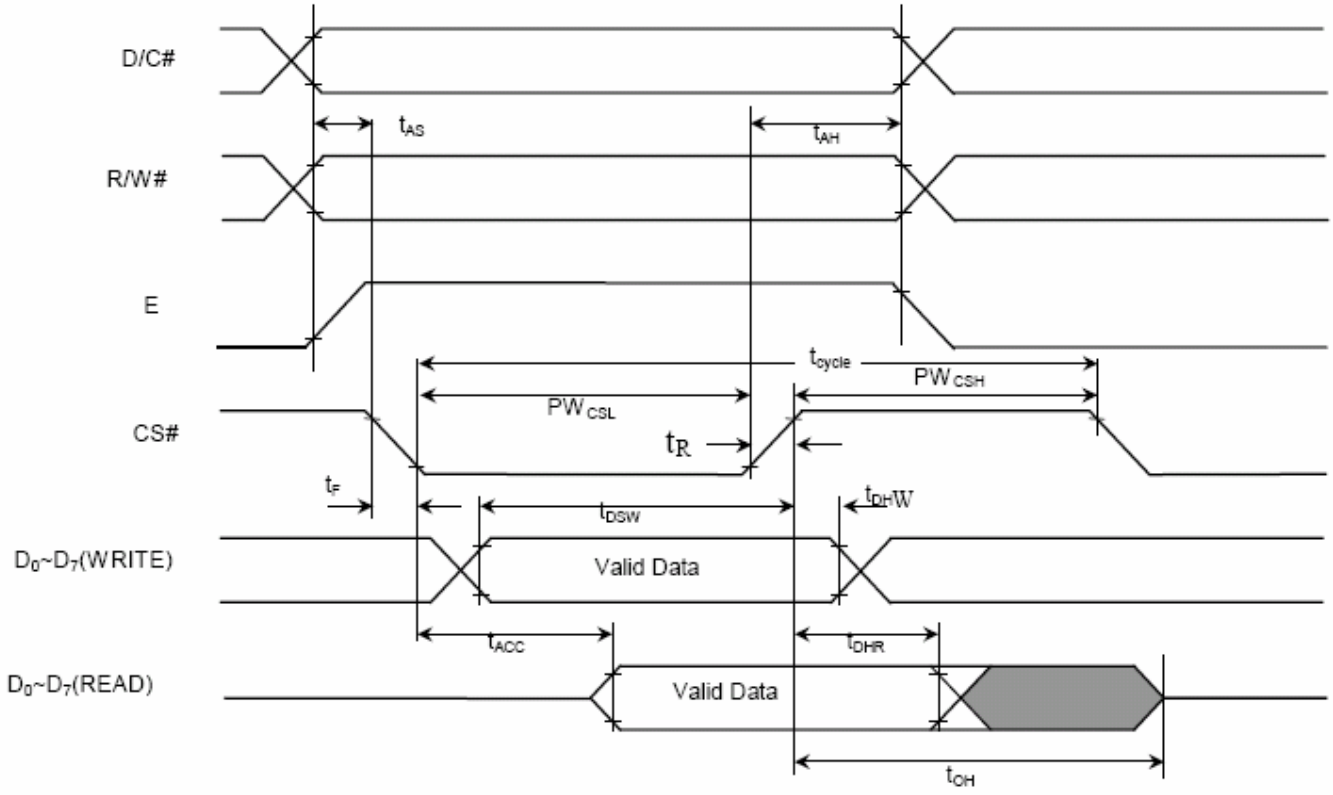
◆AC Characteristics

Use 8080/6800-Series MPU Parallel Interface or Serial Interface

1. 6800 Series MPU Parallel Interface

(V_{DD} - V_{SS} = 2.4 to 3.5V)

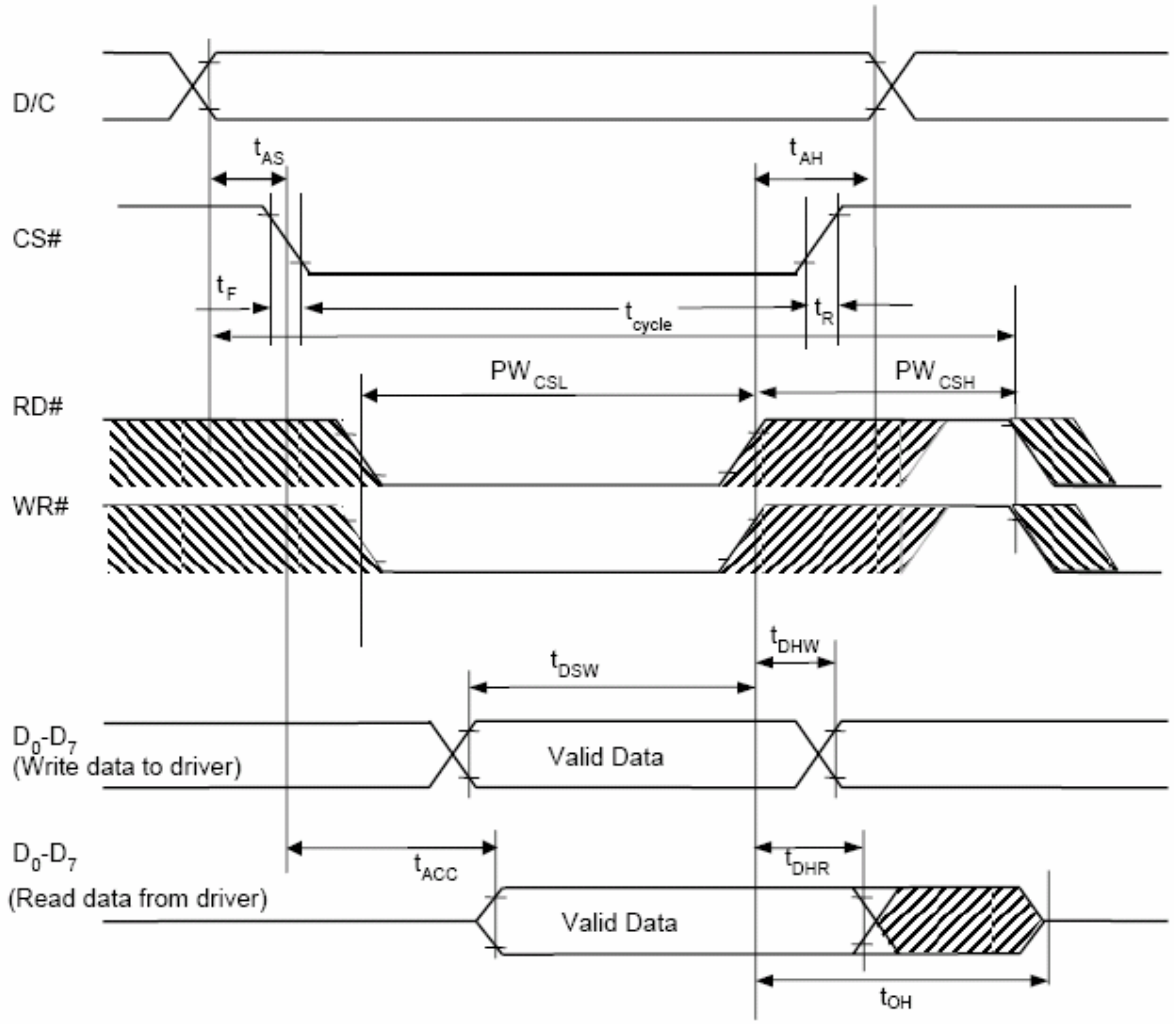
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



2. 8080 Series MPU Parallel Interface

(V_{DD} - V_{SS} = 2.4 to 3.5V)

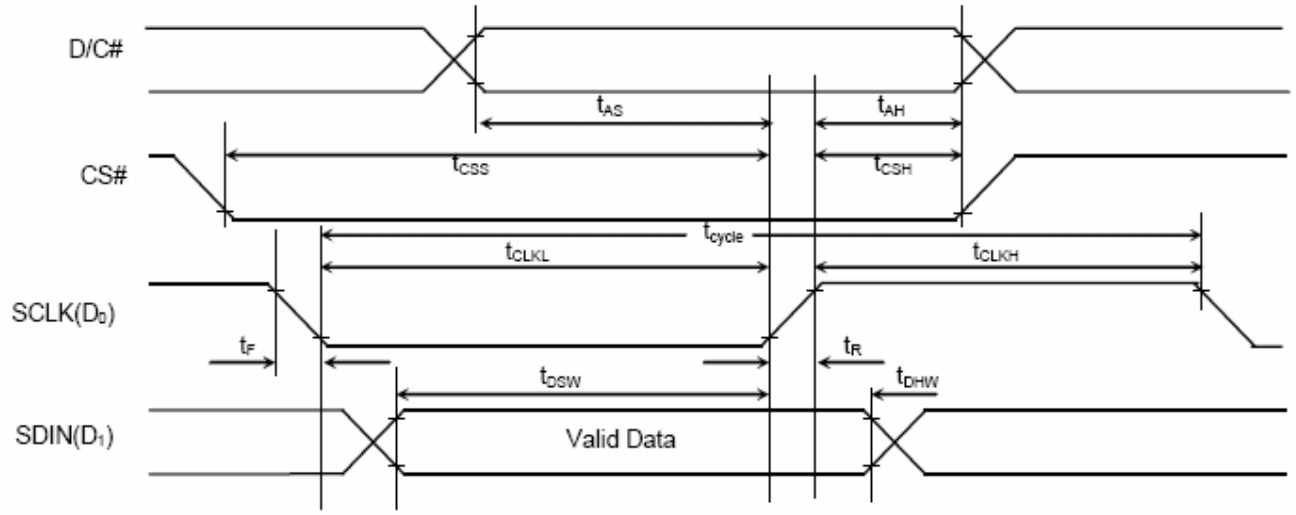
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

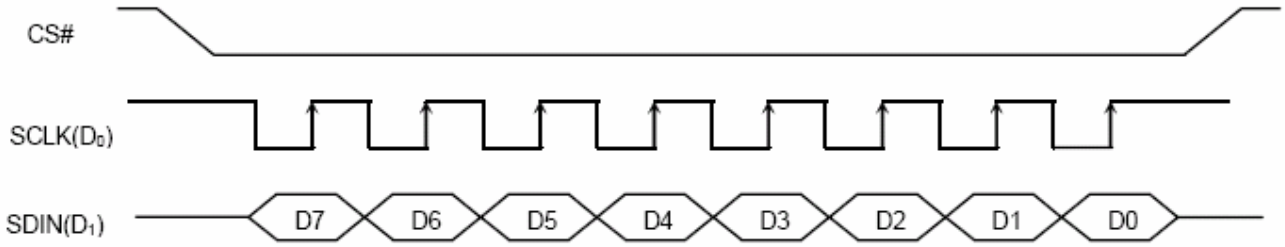


3. Serial Interface

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = -40 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns





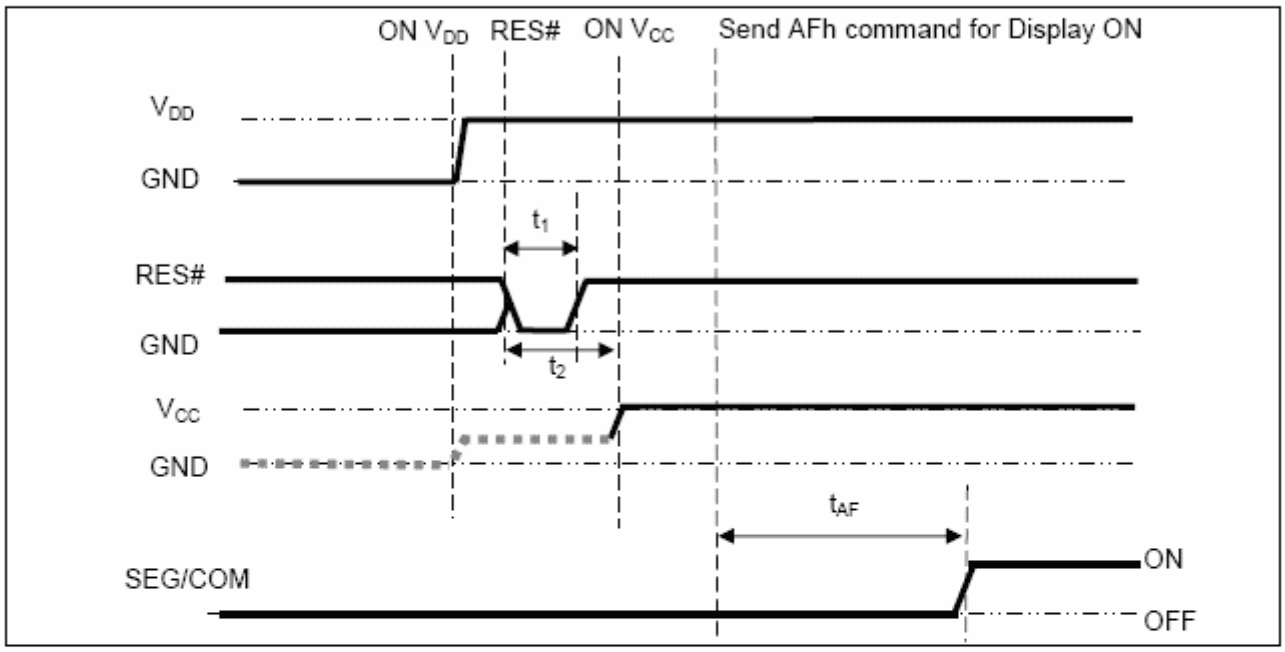
■ TIMING OF POWER SUPPLY

The following figures illustrate the recommended power ON and power OFF sequence

Power ON sequence:

1. Power ON V_{DD}.
2. After V_{DD} become stable, set RES# pin LOW (logic LOW) for at least 3us (t_1) and then HIGH (logic HIGH).
3. After set RES# pin LOW (logic LOW), wait for at least 3us (t_2). Then Power ON V_{CC}.[1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

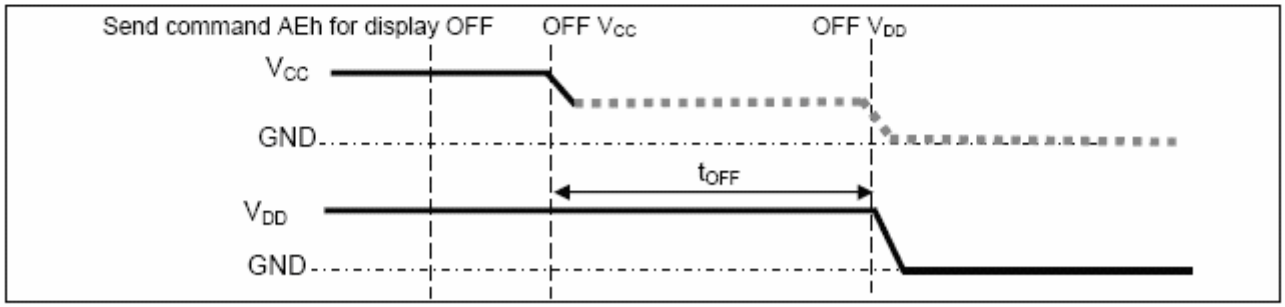
The Power ON sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Wait until panel discharges completely.
3. Power OFF V_{CC}.[1], [2]
4. Wait for t_{OFF}. Power OFF V_{DD}. (where Minimum t_{OFF}=0ms, Typical t_{OFF}=100ms)

The Power OFF sequence



Note:

[1] Since an ESD protection circuit is connected between V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 16 and Figure 17.

[2] V_{CC} should be kept float when it is OFF.

■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25℃)

Items		Symbol	Min.	Typ.	Max.	Unit	Remark
Operating Luminance		L	-	TBD*	-	cd /m^2	White
Power Consumption		P	-	TBD	-	mW	30% pixels ON
Frame Frequency		Fr	-	100	-	Hz	
Color Coordinate	White	CIE x	0.25	0.30	0.35	CIE1931	Darkroom
		CIE y	0.31	0.36	0.41		
Response Time	Rise	Tr	-	-	0.02	ms	-
	Decay	Td	-	-	0.02	ms	-
Contrast Ratio*		Cr	10000:1	-	-		Darkroom
Viewing Angle Uniformity		△ θ	160	-	-	Degree	-
Operating Life Time*		Top	60,000	-	-	Hours	L=80cd/m^2

Note:

1. **TBD**
2. **Contrast ratio** is defined as follows:

$$\text{Contrast ratio} = \frac{\text{Photo – detector output with OLED being “white”}}{\text{Photo – detector output with OLED being “black”}}$$

3. **Life Time** is defined when the Luminance has decayed to less than 50% of the initial Luminance specification. (30% pixels scrolling display on)
(The initial value should be closed to the typical value after adjusting.)

■ INTERFACE PIN CONNECTIONS

No	Symbol	Description
1	NC	No connection
2	VCC	High voltage supply for OLED panel
3	VCOMH	High level voltage output of COM signal
4	NC	No connection
5	D7	Data bus or High impedance in Serial mode
6	D6	Data bus or High impedance in Serial mode
7	D5	Data bus or High impedance in Serial mode
8	D4	Data bus or High impedance in Serial mode
9	D3	Data bus or High impedance in Serial mode
10	D2	Data bus or High impedance in Serial mode
11	D1	Data bus or as SI in Serial mode
12	D0	Data bus or as SCL in Serial mode
13	E/RD	MCU interface input pin
14	R/W	MCU interface input pin
15	D/C	Data/Command data control pin
16	/RES	MCU control or RC for low pulse start up
17	/CS	The chip select pin. Low is enabled
18	IREF	Current reference pin
19	BS2	It is a switch to select the input data to parallel or series
20	BS1	It is the MPU interface switched pad(L:6800; H:8080)
21	VDD	Logic voltage supply for IC
22	VP C	Pre charge driving voltage for segment pins SC0~SC95
23	VP B	Pre charge driving voltage for segment pins SB0~SB95
24	VP A	Pre charge driving voltage for segment pins SA0~SA95
25	VBREF	Internal voltage reference pad for the booster circuit
26	RESE	A source current pad of the external NMOS of the booster
27	FB	A feedback voltage for the booster circuit
28	VDDB	Voltage supply for the booster circuit
29	GDR	Driving the gate of the external NMOS of the booster circuit
30	VSS	Ground
31	NC	No connection

■ COMMAND TABLE

(To write commands to command registers, the MCU interface pins are set as: D/C = 0, R/W(WR#) = 0, E (RD#)=1)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	15	0	0	0	1	0	1	0	1	Set Column Address	A[6:0] sets the column start address from 0-95, RESET=00d. B[6:0] sets the column end address from 0-95 RESET=95d.
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[6: 0]	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	75	0	1	1	1	0	1	0	1	Set Row Address	A[5:0] sets the row start address from 0-63, RESET=00d. B[5:0] sets the row end address from 0-63, RESET=63d.
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[5:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0		
0	81	1	0	0	0	0	0	0	1	Set Contrast for Color A (Segment Pins :SA0 – SA95)	Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increases. RESET = 80h
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	82	1	0	0	0	0	0	1	0	Set Contrast for Color B (Segment Pins :SB0 – SB95)	Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increases. RESET = 80h
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	83	1	0	0	0	0	0	1	1	Set Contrast for Color C (Segment Pins :SC0 – SC95)	Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increases. RESET = 80h
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	87	1	0	0	0	0	1	1	1	Master Current Control	Set A[3:0] from 0000, 0001… to 1111 to adjust the master current attenuation factor from 1/16, 2/16… to 16/16. RESET =1111b, for no attenuation.
0	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0		
0	A0	1	0	1	0	0	0	0	0	Set Re-map & Data Format	A[0]=0, Horizontal address increment (RESET) A[0]=1, Vertical address increment A[1]=0, Column address 0 is mapped to SEG0 (RESET) A[1]=1, Column address 95 is mapped to SEG0 A[4]=0, Scan from COM 0 to COM [N –1] A[4]=1, Scan from COM [N-1] to COM0. Where N is the Multiplex ratio. A[5]=0, Disable COM Split Odd Even (RESET) A[5]=1, Enable COM Split Odd Even A[7:6]=00; 256 color format = 01; 65k color format(RESET)
0	A[7:0]	A_7	A_6	A_5	A_4	*	*	A_1	A_0		

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	A1 A[5:0]	1 *	0 *	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set display RAM display start line register from 0-63. Display start line register is reset to 00h after RESET.
0 0	A2 A[5:0]	1 *	0 *	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	Set vertical scroll by COM from 0-63. The value is reset to 00H after RESET.
0	A4~A7	1	0	1	0	0	1	X_1	X_0	Set Display Mode	A4h=Normal Display (RESET) A5h=Entire Display On, all pixels turn on at GS level 63 A6h=Entire Display Off, all pixels turn off A7h=Inverse Display
0 0	A8 A[5:0]	1 *	0 *	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	The next command determines multiplex ratio N from 16MUX-64MUX, RESET=63d (64MUX) A[5:0]=0-14d (invalid entry)
0 0	AD A[7:0]	1 1	0 0	1 0	0 0	1 1	1 A_2	0 1	1 A_0	Set Master Configuration	A[0]=0, Select external V_{CC} supply at Display ON A[0]=1, Select internal booster at Display ON (RESET) A[2]=0, Select External V_P voltage supply A[2]=1, Select Internal V_P (RESET)
0	AE~AF	1	0	1	0	X_3	1	1	1	Set Display On/Off	AEh=Display off (RESET) AFh=Display on
0 0	B0 A[7:0]	1 0	0 0	1 0	1 A_4	0 0	0 0	0 A_1	0 0	Set Power Save	A[7:0]=00 (RESET) A[7:0]=12, power saving mode
0 0	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Phase 1 and 2 period adjustment	A[3:0] Phase 1 period in 1~16 DCLK clocks [RESET=4h] A[7:4] Phase 2 period in 1~16 DCLK clocks [RESET=7h]
0 0	B3 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Display Clock Divider / Oscillator Frequency	A[3:0] [DIVIDER, RESET=0] DCLK is generated from CLK divided by DIVIDER +1 (i.e., 1 to 16) A[7:4] Fosc frequency, RESET=D0H Frequency increases as level increases

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	The next 32 bytes of command set the current drive pulse width of gray scale level GS1, GS3, GS5 …GS63 as below: A[7:0]=PW1, RESET=1, it equals 1 DCLK clock B[7:0]=PW3, RESET=5, it equals 3 DCLK clocks C[7:0]=PW5, RESET= 9 : : : AE[7:0]=PW61, RESET=121 AF[7:0]=PW63, RESET=125, it equals 125 DCLK clocks Note: GS0 has no pre-charge and current drive stages. For GS2 GS4…GS62, they are derived by driver itself with: PWn = (PWn-1+PWn+1)/2 Max pulse width is 125
0	A[7:0]--PW1	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[7:0]--PW3	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	C[7:0]--PW5	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	:										
0	:										
0	:										
0	AE[7:0]--PW61	AE_7	AE_6	AE_5	AE_4	AE_3	AE_2	AE_1	AE_0		
0	AF[7:0]--PW63	AF_7	AF_6	AF_5	AF_4	AF_3	AF_2	AF_1	AF_0		
0	B9	1	0	1	1	1	0	0	1	Enable Linear Gray Scale Table	Enable build-in linear gray scale table (RESET=Enable) PW1=1,PW2=3,PW3=5 … PW61=121,PW62=123,PW63=125
0	BB ~ BD	1	0	1	1	1	X_2	X_1	X_0	V_{PA}, V_{PB}, V_{PC} level setting for Color A,B,C	011b for Color A, 100b for Color B, 101b for Color C A[7:0] 00000000 0.43*V_{REF} 00111111 0.83* V_{REF} 01111111 1.0* V_{REF} 1xxxxxxx connects to V_{COMH} (RESET)
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	BE	1	0	1	1	1	1	1	0	Set V_{COMH}	A[5:0] 000000 0.43* V_{REF} 111111 0.83* V_{REF} (RESET)
0	A[5:0]	0	0	A_5	A_4	A_3	A_2	A_1	A_0		
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation

Read Command Table

(D/C=0, R/W (WR#)=1, E (RD#)=1 for 6800 or E (RD#)=0 for 8080)

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read *	D_7 : "1" for Command lock D_6 : "1" for display OFF / "0" for display ON D_5 : Reserve D_4 : Reserve D_3 : Reserve D_2 : Reserve D_1 : Reserve D_0 : Reserve

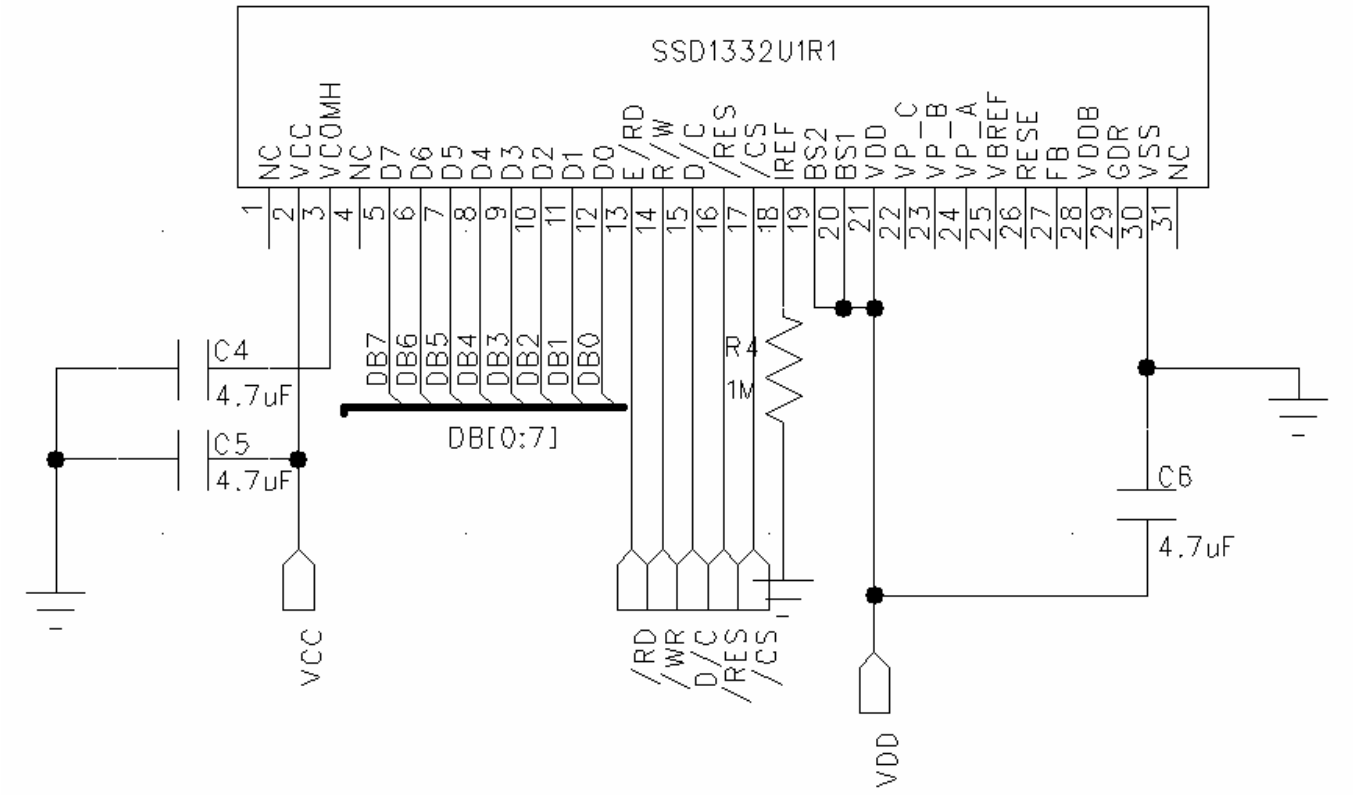
Note: Patterns other than that given in Command Table are prohibited to enter to the chip as a command; otherwise, unexpected result will occur.

■ INITIALIZATION CODE

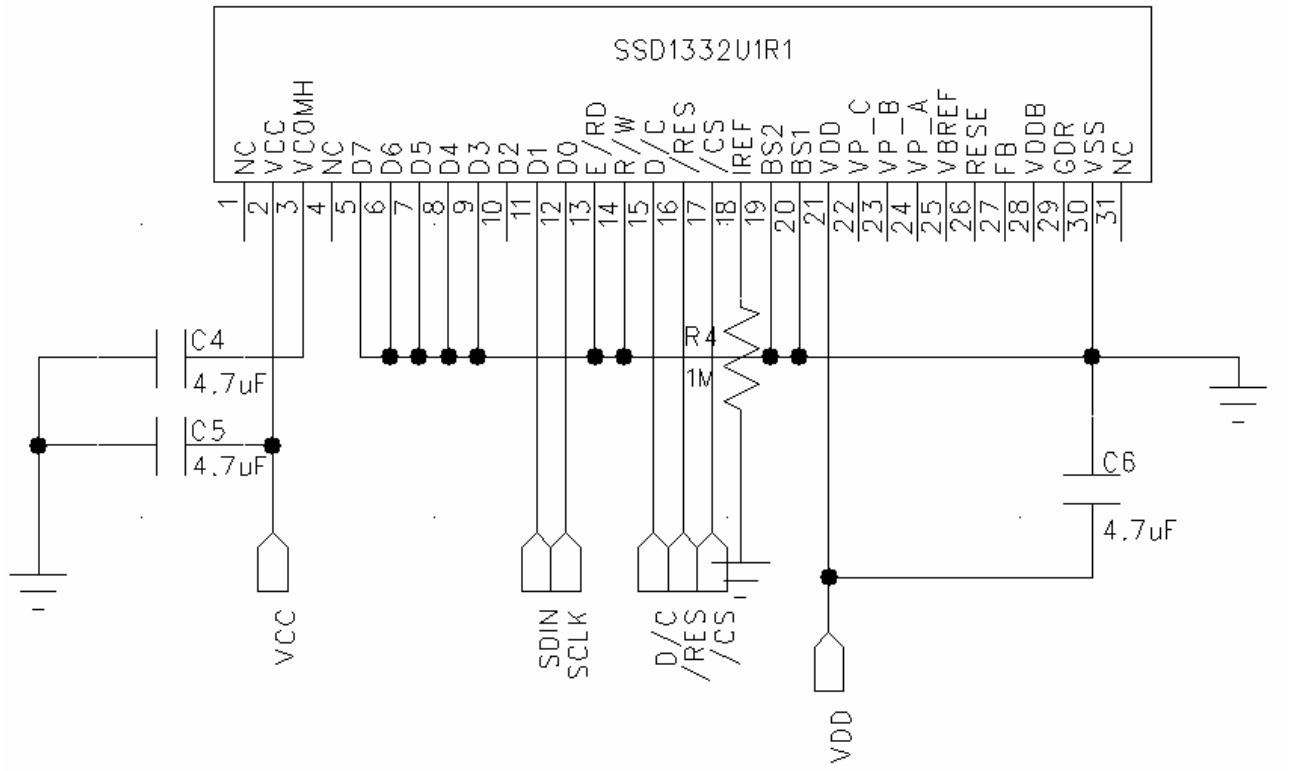
```
Void  init_oled()
{
  WOLEDCOM(0xAE); //Display OFF

  WOLEDCOM(0x15); //Set Column ADDR
  WOLEDCOM(0x00); //Start ADDR
  WOLEDCOM(0x5F); //End ADDR
  WOLEDCOM(0x75); //Set Row ADDR
  WOLEDCOM(0x00); //Start ADDR
  WOLEDCOM(0x3F); //End ADDR

  WOLEDCOM(0x81); //Set Contrast for RED
  WOLEDCOM(0x80);
  WOLEDCOM(0x82); //Set Contrast for GREEN
  WOLEDCOM(0x80);
  WOLEDCOM(0x83); //Set Contrast for BLUE
  WOLEDCOM(0x80);

  WOLEDCOM(0x87); //Set Master Current Control
  WOLEDCOM(MASTER);

  WOLEDCOM(0xA0); //Set Re-map&Data Format
  WOLEDCOM(0x62);
  WOLEDCOM(0xA1); //Set Display Start Line
  WOLEDCOM(0x00);
  WOLEDCOM(0xA2); //Set Display Offset
  WOLEDCOM(0x00);
  WOLEDCOM(0xA4); //Set Display Mode(A4~A7)

  WOLEDCOM(0xA8); //Set Multiplex Ratio
  WOLEDCOM(0x3F);

  WOLEDCOM(0xAD); //Set Master Configuration
  WOLEDCOM(0x8E);

  WOLEDCOM(0xB0); //Set Power Save
  WOLEDCOM(0x00);

  WOLEDCOM(0xB1); //Phase1&Phase2 Period adjustment
  WOLEDCOM(0x35);
  WOLEDCOM(0xB3); //Display Clock Divider/Oscillator Frequency
  WOLEDCOM(0xD0);

  WOLEDCOM(0xB9); //Enable Linear Gray Scale Table

  WOLEDCOM(0xBB); //VPA Level setting for RED
  WOLEDCOM(0x50); //connects to Vcomh
  WOLEDCOM(0xBC); //VPB Level setting for GREEN
  WOLEDCOM(0x50); //connects to Vcomh
  WOLEDCOM(0xBD); //VPC Level setting for BLUE
  WOLEDCOM(0x50); //connects to Vcomh

  WOLEDCOM(0xBE); //Set Vcomh
  WOLEDCOM(0x3F);

  WOLEDCOM(0xAF); //Display ON
}
```

■ SCHEMATIC EXAMPLE

◆8080 Series Interface Application Circuit(External V_{CC}=13.0V):



◆Serial Interface Application Circuit(External V_{CC}=13.0V):



NOTE:

1. **R1=(V_{CC}-3)V/10uA=(13-3)V/10uA≈1MΩ,C4=C5=C6=4.7uF,in which C4 should be connected a tantalum capacitor between GND ;**
2. **The V_{CC} should connect a external voltage;**
3. **In Serial interface mode ,the read function is not possible.**

■ RELIABILITY TESTS

Item		Condition	Criterion
High Temperature Storage (HTS)		80±2℃, 200 hours	1. After testing, the function test is ok. 2. After testing, no addition to the defect. 3. After testing, the change of luminance should be within +/- 50% of initial value. 4. After testing, the change for the mono and area color must be within (+/-0.02, +/-0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates. 5. After testing, the change of total current consumption should be within +/- 50% of initial value.
High Temperature Operating (HTO)		70±2℃, 96 hours	
Low Temperature Storage (LTS)		-30±2℃, 200 hours	
Low Temperature Operating (LTO)		-20±2℃, 96 hours	
High Temperature / High Humidity Storage (HTHHS)		50±3℃, 90%±3%RH, 120 hours	
Thermal Shock (Non-operation) (TS)		-20±2℃ ~ 25℃ ~ 70±2℃ (30min) (5min) (30min) 10cycles	
Vibration (Packing)	10~55~10Hz,amplitude 1.5mm, 1 hour for each direction x, y, z	1. One box for each test. 2. No addition to the cosmetic and the electrical defects.	
Drop (Packing)	Height : 1 m, each time for 6 sides, 3 edges, 1 angle		
ESD (finished product housing)	±4kV (R: 330Ω C: 150pF , 10times, air discharge)	1. After testing, cosmetic and electrical defects should not happen. 2. In case of malfunction or defect caused by ESD damage, it would be judged as a good part if it would be recovered to normal state after resetting.	

Note： 1) For each reliability test, the sample quantity is 3, and only for one test item.
2) The HTHHS test is requested the Pure Water(Resistance＞10MΩ).
3) The test should be done after 2 hours of recovery time in normal environment.

■OUTGOING QUALITY CONTROL SPECIFICATION

◆Standard

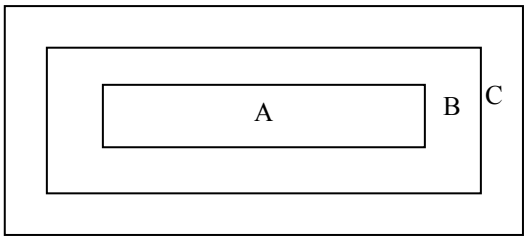
According to GB/T2828.1-2003/ISO 2859-1： 1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

◆Definition

1 Major defect : The defect that greatly affect the usability of product.

2 Minor defect : The other defects, such as cosmetic defects, etc.

3 Definition of inspection zone:



Zone A: Active Area

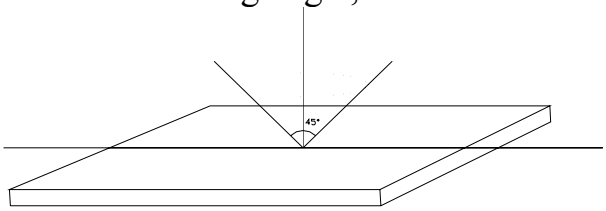
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer`s product.

◆Inspection Methods

1 The general inspection : under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45º viewing angle, under 25±5℃.



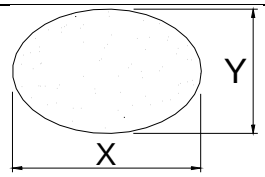
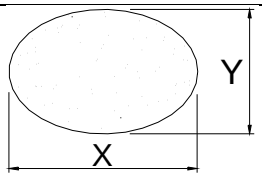
2 The luminance and color coordinate inspection : By PR705 or BM-7 or the equal equipments, in the dark room, under 25±5℃.

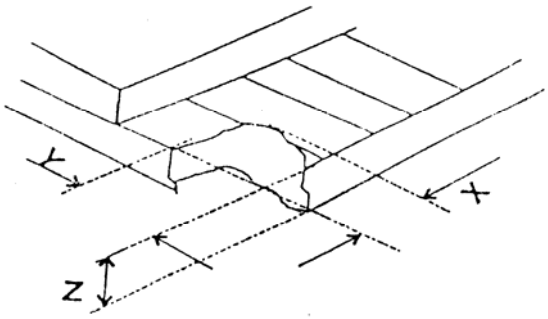
◆Inspection Criteria

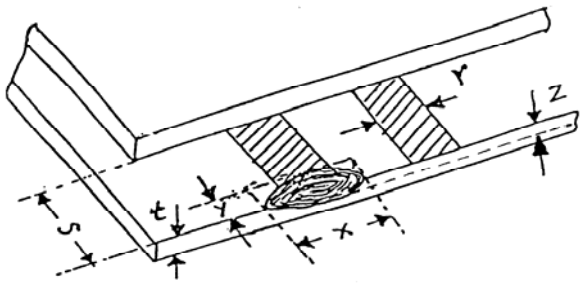
1 Major defect : AQL= 0.65

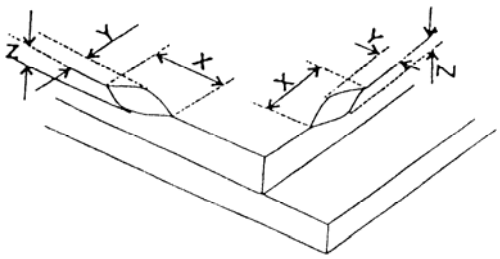
Item	Criterion
Function Defect	1. No display or abnormal display is not accepted
	2. Open or short is not accepted.
	3. Power consumption exceeding the spec is not accepted.
Outline Dimension	Outline dimension exceeding the spec is not accepted.
Glass Crack	Glass crack tends to enlarge is not accepted.

2 Minor Defect : AQL= 1.5

<table>
<tr><td>Item</td><td colspan="4">Criterion</td></tr>
<tr><td rowspan="5">Spot Defect (dimming and lighting spot)</td><td colspan="2">Size (mm)</td><td colspan="2">Accepted Qty</td></tr>
<tr><td colspan="2"></td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="3">  </td><td>Φ≦0.10</td><td colspan="2">Ignored</td></tr>
<tr><td>0.10＜Φ≦0.15</td><td>3</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.15＜Φ≦0. 20</td><td>1</td></tr>
<tr><td colspan="4">Note : Φ= (x + y) / 2</td><td>0.20＜Φ</td><td>0</td></tr>
<tr><td rowspan="5">Line Defect (dimming and lighting line)</td><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.03</td><td colspan="2">Ignored</td></tr>
<tr><td>L≦3.0</td><td>0.03＜W≦0.05</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>L≦2.0</td><td>0.05＜W≦0.08</td><td>1</td></tr>
<tr><td>/</td><td>0.08＜W</td><td>As spot defect</td></tr>
<tr><td colspan="5">Remarks: The total of spot defect and line defect shall not exceed 4 pcs.</td></tr>
<tr><td>Polarizer Stain</td><td colspan="4">Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.</td></tr>
<tr><td rowspan="8">Polarizer Scratch</td><td colspan="4">1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.</td></tr>
<tr><td colspan="4">2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :</td></tr>
<tr><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.03</td><td colspan="2">Ignore</td></tr>
<tr><td>5.0＜L≦10.0</td><td>0.03＜W≦0.05</td><td>2</td><td rowspan="3">Ignore</td></tr>
<tr><td>L≦5.0</td><td>0.05＜W≦0.08</td><td>1</td></tr>
<tr><td>/</td><td>0.08＜W</td><td>0</td></tr>
<tr><td rowspan="5">Polarizer Air Bubble</td><td colspan="2">Size</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4">  </td><td>Φ≦0.20</td><td colspan="2">Ignored</td></tr>
<tr><td>0.20＜Φ≦0.50</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.50＜Φ≦0.80</td><td>1</td></tr>
<tr><td>0.80＜Φ</td><td>0</td></tr>
</table>

<table>
<tr><td rowspan="4">Glass Defect (Glass Chiped)</td><td>1. On the corner
(mm)
 

<table><tr><td>x</td><td>≤ 2.0</td></tr><tr><td>y</td><td>≤ S</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>2. On the bonding edge
(mm)
 

<table><tr><td>x</td><td>≤ a / 2</td></tr><tr><td>y</td><td>≤ s / 3</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>3. On the other edges
(mm)
 

<table><tr><td>x</td><td>≤ a / 5</td></tr><tr><td>y</td><td>≤ 1.0</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>Note: t: glass thickness ; s: pad width ; a: the length of the edge</td></tr>
<tr><td>TCP Defect</td><td>Crack, deep fold and deep pressure mark on the TCP are not accepted</td></tr>
<tr><td>Pixel Size</td><td>The tolerance of display pixel dimension should be within ±20% of the spec</td></tr>
<tr><td>Luminance</td><td>Refer to the spec or the reference sample</td></tr>
<tr><td>Color</td><td>Refer to the spec or the reference sample</td></tr>
</table>

■ CAUTIONS IN USING OLED MODULE

◆Precautions For Handling OLED Module:

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
   i. Avoid drop from high, avoid excessive impact and pressure.
   ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
   iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
   iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
   v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
   vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
   i. Be sure to ground the body when handling the OLED Modules.
   ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
   iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
   iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
   v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
   vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrade the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence: $V_{DD} \rightarrow V_{CC}$, and power off sequence: $V_{CC} \rightarrow V_{DD}$.
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module’ s life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and datasheet of IC controller, otherwise something wrong may be seen.

13.When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆Precautions For Soldering OLED Module:

1. Soldering temperature : 260°C ± 10°C.
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

◆ Precautions For Storing OLED Module:

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between 0°C and 30°C , the relative humidity not over 60%.

◆ Limited Warranty

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) Multi-inno will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with Multi-inno OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to Multi-inno within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of Multi-inno is limited to repair and/or replacement on the terms above. Multi-inno will not be responsible for any subsequentor consequential events.

◆Return OLED Module Under Warranty:

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.

◆PRIOR CONSULT MATTER

1. For Multi-inno standard products ,we keep the right to change material ,process … for improving the product property without any notice on our customer.
2. If you have special requirement about reliability condition, please let us know before you start the test on our samples.