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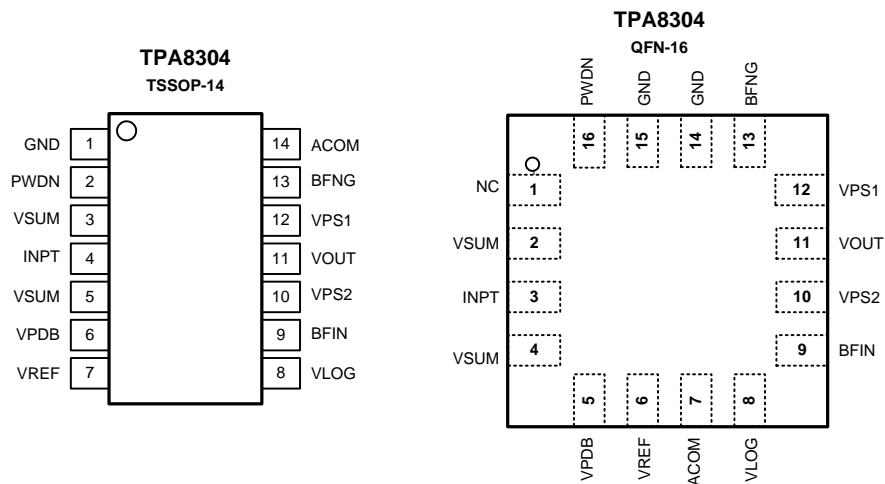
## Revision History

| Date       | Revision | Notes   |
|------------|----------|---|
| 2019/9/10  | Rev.0    | Initial Version   |
| 2019/12/9  | Rev.0.01 | Add Application Information: Using the Fixed Bias   |
| 2020/11/16 | Rev.A    | Add phase margin and gain margin of Output Buffer, Pin BFIN, BFNG, VOUT in Electrical Characteristics |
| 2021/5/30  | Rev.A.1  | Update description  |

## Order Information

| Order Number | Operating Temperature Range | Package      | Marking Information | MSL | Transport Media, Quantity |
|--------------|-----------------------------|--------------|---------------------|-----|---------------------------|
| TPA8304-TS2R | -40 to 85°C                 | 14-Pin TSSOP | A8304               | 3   | Tape and Reel, 3000       |
| TPA8304-QF4R | -40 to 85°C                 | 16-Pin QFN   | A8304               | 3   | Tape and Reel, 4000       |

## Pin Configuration and Description



| Pin No. of TSSOP | Pin No. of QFN | Pin Name | Description   |
|------------------|----------------|----------|---|
| 1                | 14, 15         | GND      | Power Supply Ground Connection.   |
| 2                | 16             | PWDN     | Power-Down Control Input. Device is active when PWDN is taken LOW.  |
| 3, 5             | 2, 4           | VSUM     | Guard Pins. Used to shield the INPT current line.   |
| 4                | 3              | INPT     | Photodiode Current Input.   |
| 6                | 5              | VPDB     | Photodiode Biaseer Output. Connect this pin to the photodiode cathode when using adaptive bias control; Otherwise, leave this pin floating. |
| 7                | 6              | VREF     | Voltage Reference Output of 2 V.  |
| 8                | 8              | VLOG     | Output of the Logarithmic Front-End Processor.  |
| 9                | 9              | BFIN     | Buffer Amplifier Noninverting Input   |
| 10               | 10             | VPS2     | Positive Supply.  |
| 11               | 11             | VOUT     | Buffer Amplifier Output   |
| 12               | 12             | VPS1     | Positive Supply.  |
| 13               | 13             | BFNG     | Buffer Amplifier Inverting Input.   |
| 14               | 7              | ACOM     | Analog Reference Ground.  |
|                  | 1              | NC       | Pins labeled NC can be allowed to float, but it is better to connect these pins to ground.  |
|                  | 17             | EPAD     | Exposed Pad. Connect the exposed pad to the VSUM pins to provide low leakage guard.   |

## Absolute Maximum Ratings <sup>Note 1</sup>

| Parameters                              | Rating       |
|---|--------------|
| Supply Voltage,                         | 6.5 V        |
| Input Current to INPT <sup>Note 2</sup> | ±20mA        |
| Maximum Junction Temperature            | 125°C        |
| Operating Temperature Range             | –40 to 85°C  |
| Storage Temperature Range               | –65 to 150°C |
| Lead Temperature (Soldering, 10 sec)    | 260°C        |

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300mV beyond the power supply, the input current should be limited to less than 10mA.

## ESD Rating / Latch Up

| Symbol | Parameter                | Condition   | Minimum Level | Unit |
|--------|--------------------------|---|---------------|------|
| HBM    | Human Body Model ESD     | ANSI/ESDA/JEDEC JS-001, INPT pin                  | 500           | V    |
|        |                          | ANSI/ESDA/JEDEC JS-001, All other pin except INPT | 2             | kV   |
| CDM    | Charged Device Model ESD | ANSI/ESDA/JEDEC JS-002                            | 1             | kV   |
| LU     | Latch Up                 | 25degree  | 200           | mA   |
| LU     | Latch Up                 | 125degree   | 150           | mA   |

## Thermal Information

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|--------------|---------------|---------------|------|
| 16-Pin QFN   | 75            | 54            | °C/W |
| 14-Pin TSSOP | 180           | 35            | °C/W |

## Electrical Characteristics

All test condition is  $V_S = 5V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

| Symbol  | Parameter                                | Conditions  | $T_A$                         | Min  | Typ | Max  | Unit              |
|---|--|---|-------------------------------|------|-----|------|-------------------|
| <b>Power Supply, Pin VPS2, VPS1, GND</b>          |  |   |                               |      |     |      |                   |
| $V_S$   | Supply Voltage Range                     |   |                               | 4.5  |     | 5.5  | V                 |
| $I_Q$   | Quiescent Current per Amplifier          |   |                               |      | 8   | 10   | mA                |
| $I_{SN}$  | Shutdown Current                         | In disable state                                      |                               |      | 40  |      | $\mu A$           |
| <b>Input Interface, Pin INPT, VSUM</b>            |  |   |                               |      |     |      |                   |
|   | Specified Current Range                  | Flows toward INPT                                     |                               | 1    |     |      | nA                |
|   |  |   |                               |      | 10  | 12   |                   |
|   | Input Node Voltage                       |   |                               | 1.05 | 1.2 | 1.35 | V                 |
|   | Input Node Voltage Drift                 |   |                               |      | 20  |      | $\mu V/^\circ C$  |
|   | $V_{INPT} - V_{SUM}$                     |   |                               | -20  |     | 20   | mV                |
| <b>Photodiode Bias, between Pin VPDB and INPT</b> |  |   |                               |      |     |      |                   |
|   | Minimum Value                            | $I_{PD} = 100 \text{ pA}$                             |                               |      | 100 |      | mV                |
|   | Transresistance                          |   |                               |      | 150 |      | mV/mA             |
| <b>Logarithmic Output, Pin VLOG</b>               |  |   |                               |      |     |      |                   |
|   | Slope                                    |   |                               | 195  | 200 | 205  | mV/dec            |
|   |  |   | $0^\circ C$ to $70^\circ C$   | 192  |     | 208  |                   |
|   | Intercept                                |   |                               | 60   | 100 | 140  | pA                |
|   |  |   | $0^\circ C$ to $70^\circ C$   | 35   |     | 175  |                   |
|   | Law Conformance Error                    | $10 \text{ nA} < I_{PD} < 10 \text{ mA}$ , peak error |                               |      | 0.2 | 0.25 | dB                |
|   |  | $1 \text{ nA} < I_{PD} < 10 \text{ mA}$ , peak error  |                               |      | 0.5 | 0.75 | dB                |
|   | Maximum Output Voltage                   |   |                               |      | 1.6 |      | V                 |
|   | Minimum Output Voltage                   |   |                               |      | 0.1 |      | V                 |
|   | Output Resistance                        |   |                               | 4.95 | 5   | 5.05 | k $\Omega$        |
| <b>Reference Output, Pin VREF</b>                 |  |   |                               |      |     |      |                   |
|   | Output Voltage                           |   |                               | 1.96 | 2   | 2.04 | V                 |
|   |  |   | $-40^\circ C$ to $85^\circ C$ | 1.95 |     | 2.05 |                   |
|   | Output Resistance                        |   |                               |      | 2   |      | $\Omega$          |
| <b>Output Buffer, Pin BFIN, BFNG, VOUT</b>        |  |   |                               |      |     |      |                   |
|   | Input Offset Voltage                     |   |                               | -10  |     | 10   | mV                |
|   | Input Bias Current                       |   |                               |      | 100 |      | pA                |
|   | Output Voltage Swing to Power and Ground | $R_L = 1 \text{ k}\Omega$ to ground                   |                               |      | 100 |      | mV                |
|   | Output Resistance                        |   |                               |      | 0.5 |      | $\Omega$          |
|   | Wideband Noise <sup>Note3</sup>          | $I_{PD} > 1 \text{ }\mu A$                            |                               |      | 1   |      | $\mu V/\sqrt{Hz}$ |
|   | Small Signal Bandwidth <sup>Note3</sup>  | $I_{PD} > 1 \text{ }\mu A$                            |                               |      | 10  |      | MHz               |
|   | Slew Rate                                | 0.2 V to 4.8 V output swing                           |                               |      | 15  |      | V/ $\mu s$        |

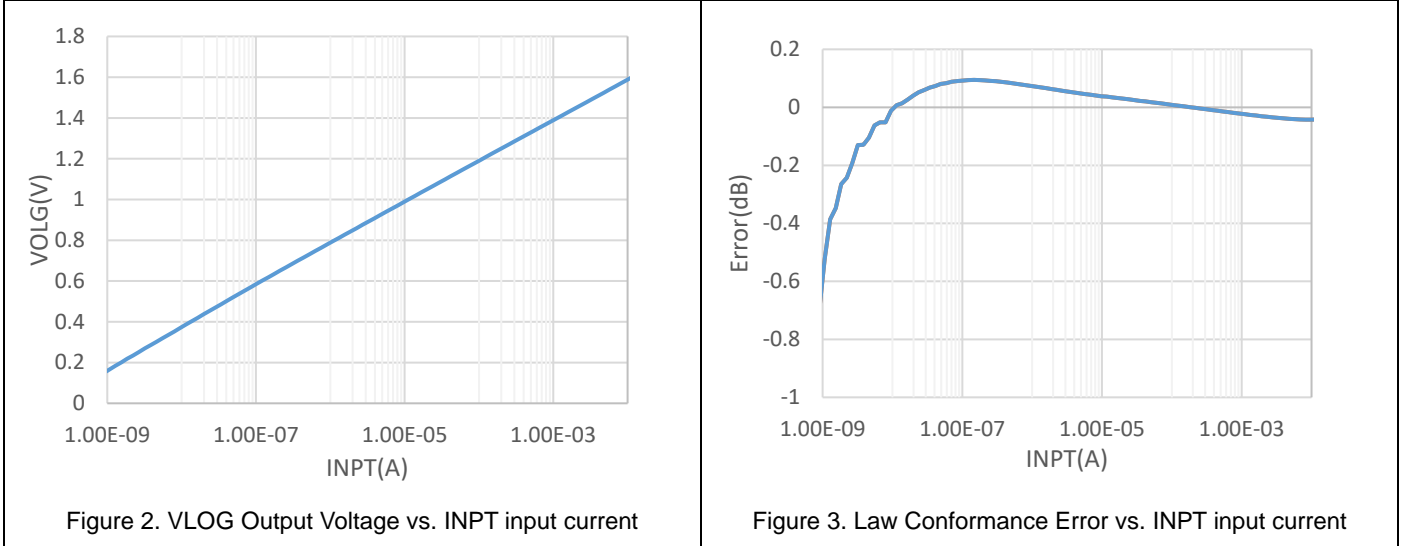
| Symbol                            | Parameter               | Conditions                    | T <sub>A</sub> | Min | Typ | Max | Unit |
|-----------------------------------|-------------------------|-------------------------------|----------------|-----|-----|-----|------|
|                                   | Phase Margin            | C <sub>L</sub> =100pF         |                |     | 60  |     | °    |
|                                   | Gain Margin             | C <sub>L</sub> =100pF         |                |     | 10  |     | dB   |
| <b>Power Down Input, Pin PWDN</b> |                         |                               |                |     |     |     |      |
|                                   | Logic Level, High State | V <sub>S</sub> = 4.5V to 5.5V | -40°C to 85°C  | 2   |     |     | V    |
|                                   | Logic Level, Low State  | V <sub>S</sub> = 4.5V to 5.5V | -40°C to 85°C  |     |     | 1   | V    |

Note3: Output noise and incremental bandwidth are functions of input current

| Step Response time from input to VLOG, 0°C to 70°C |             |     |     |              |     |     |      |
|--|-------------|-----|-----|--------------|-----|-----|------|
| Conditions   | Rising Time |     |     | Falling Time |     |     | Unit |
|  | Min         | Typ | Max | Min          | Typ | Max | µs   |
| 10nA to 100nA                                      |             | 2   |     |              | 4   |     | µs   |
| 10nA to 1µA  |             | 0.5 |     |              | 3   |     | µs   |
| 10nA to 10µA                                       |             | 0.2 |     |              | 5   |     | µs   |
| 10nA to 100µA                                      |             | 0.2 |     |              | 10  |     | µs   |
| 10nA to 1mA  |             | 0.2 |     |              | 15  |     | µs   |

## Typical Performance Characteristics

V<sub>s</sub> = 5V, unless otherwise specified.





## Application Information

### Basic Configuration to Use TPA8304

The basic configuration (see Figure 4) includes a 2.5x gain to amplify the VLOG voltage by the buffer amplifier. This increases the slope of 10 mV/dB(200 mV/DEC) at the VLOG pin to 25 mV/dB(500 mV/DEC) at VOUT. For the full dynamic range of 140 dB, the output swing is 4.0 V, which can be accommodated by the rail-to-rail output stage when using the recommended 5 V supply.

The capacitor C1 and R1 on INPT pin is recommended to not assemble as TPA8304 use advance technology to keep the loop stability and fast the step response. If C1 and R1 must be used for the compatibility to ADI ADL5303 and AD8304, the recommended value is 470pF for C1 and 750Ω for R1, which make the output noise larger and step response slower than the not assemble configuration. The capacitor CF from VLOG to ground forms an optional single-pole low-pass filter. Because the resistance at this pin is 5 kΩ, an -3 dB corner frequency can be realized to minimize the output noise. A capacitor between VSUM and ground is essential for minimizing the noise on this node. When the bias voltage at either VPDB or VREF is not needed, these pins should be left unconnected.

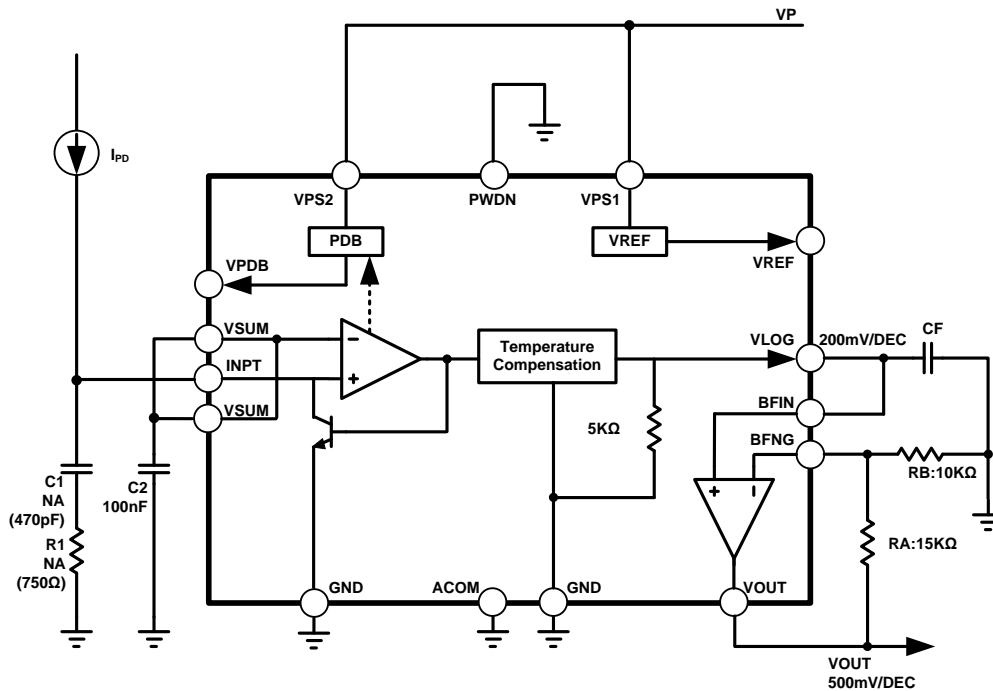


Figure 4 Basic Configuration

The relationship between the input current,  $I_{PD}$ , applied to the INPT pin, and the voltage appearing at the VLOG pin is:

$$V_{LOG} = V_Y * \text{LOG}_{10}(I_{PD}/I_Z)$$

Where:

$V_Y$  is the voltage slope (in the case of base-10 logarithms, it is also referred to as volts per decade).

$I_Z$  is the fixed current in the logarithmic equation called the intercept.

In the basic configuration, the scaling is chosen so that  $V_Y$  is trimmed to 200 mV/decade (10 mV/dB). The intercept is positioned at 100 pA; the output voltage,  $V_{LOG}$ , crosses zero when  $I_{PD}$  is of this value. However, the actual VLOG must always be slightly above ground. Using Equation 1, the output for any value of  $I_{PD}$  can be calculated. For the specified input current of 1nA to 10mA of INPT:

$$1\text{nA} : \quad V_{LOG} = 0.2 \text{ V } \text{LOG}_{10} (1 \text{ nA}/100 \text{ pA}) = 0.2 \text{ V}$$

$$10\text{mA} : \quad V_{LOG} = 0.2 \text{ V } \text{LOG}_{10} (10 \text{ mA}/100 \text{ pA}) = 1.6 \text{ V}$$

In practice, both the slope and intercept can be altered, to either higher or lower values, without any significant loss of calibration accuracy, by using one or two external resistors, often in conjunction with the 2 V voltage reference at the VREF pin.

### Using the Adaptive Bias

For most photodiode applications, the placement of the anode above ground is acceptable in some case, as long as the positive bias on the cathode is enough to support the peak current for a particular diode, limited by its series resistance. To address this matter, the TPA8304 provides for a diode bias that increases linearly with the input current. This bias voltage appears at the VPDB pin, and varies from 1.3 V (reverse-biasing the diode by 0.1 V) for  $I_{PD} = 100 \text{ pA}$  and rises to 2.8 V (for a diode bias of 1.7 V) at  $I_{PD} = 10 \text{ mA}$ . The adaptive biasing function is valuable in minimizing dark current while preventing the loss of photodiode bias at high currents. Use of the adaptive bias feature is shown in Figure 5.

Capacitor CPB, between the photodiode cathode at the VPDB pin and ground, is used to lower the impedance at this node and improve the high frequency accuracy at current levels where the TPA8304 bandwidth is high. CPB also provide a high frequency path for any high frequency modulation on the optical signal. A suitable CPB value (1nF to 33nF) is recommended in the practice for fast falling step response. An undershoot appearing on output in VLOG pin when the large falling step input (For example, 1mA to 1nA) if large CPB value (>33nF) is used.

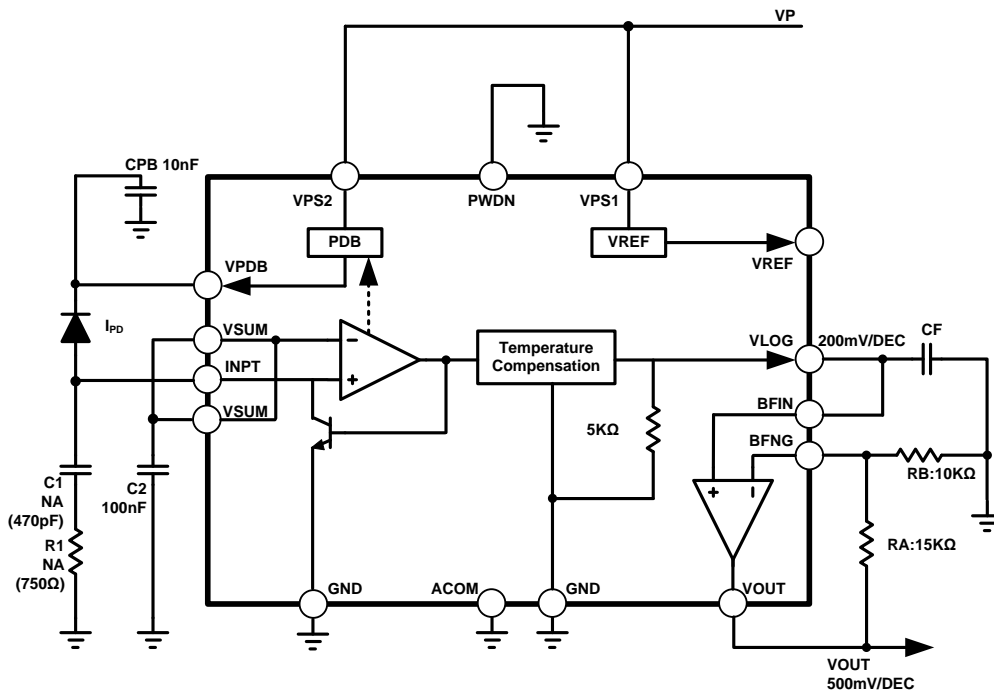


Figure 5 Using the Adaptive Bias

### Using the Fixed Bias

For some photodiode applications, the fixed bias voltage is used for a photodiode. As the INPT pin has around 1.2V voltage, the voltage cross the photodiode must be carefully considered especially on the chip power on or off process. Refer to the Figure 6, the current of photodiode must be limited to the value of rating current, otherwise the photodiode may be damaged by large current. To keep the photodiode safe, the system design should be guaranteed:

- Keep the voltage of VBIAS is always equal or larger than the VP(power supply of TPA8304), especially on power on or off process. Use the same source for VBIAS and VP is recommended.
- Or use resistor RLIMIT to limit the current of photodiode into safe value if the previous solution is not available.

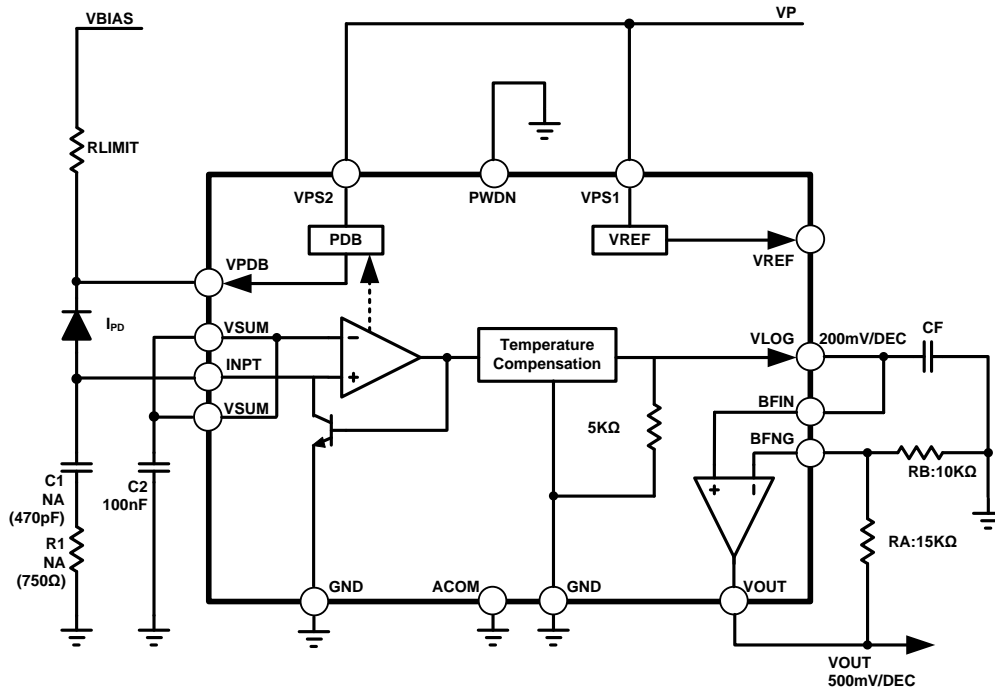
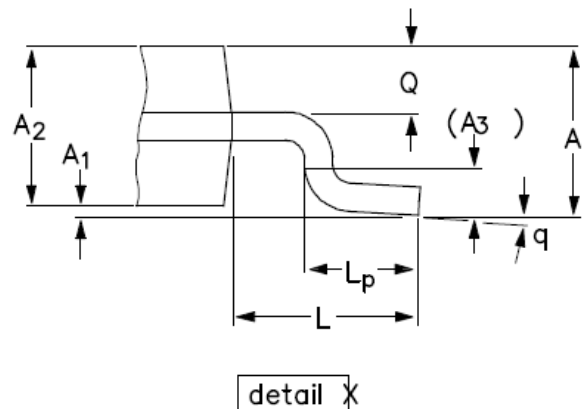
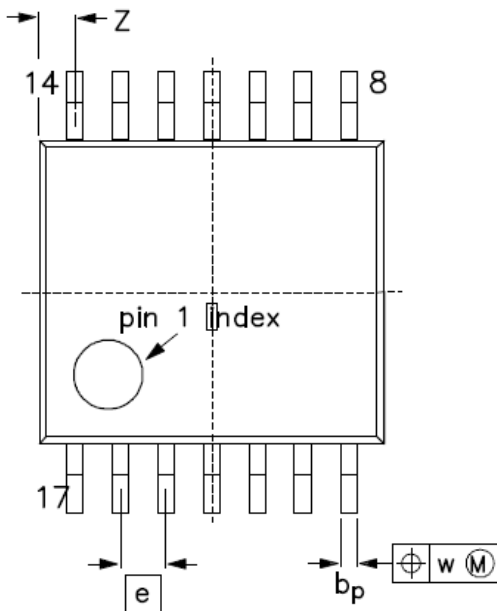
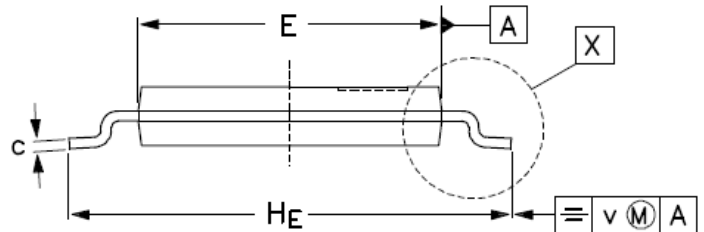
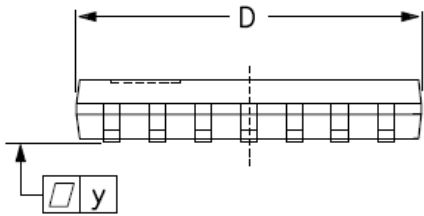


Figure 6 Using the Fixed Bias

Package Outline Dimensions

TSSOP-14



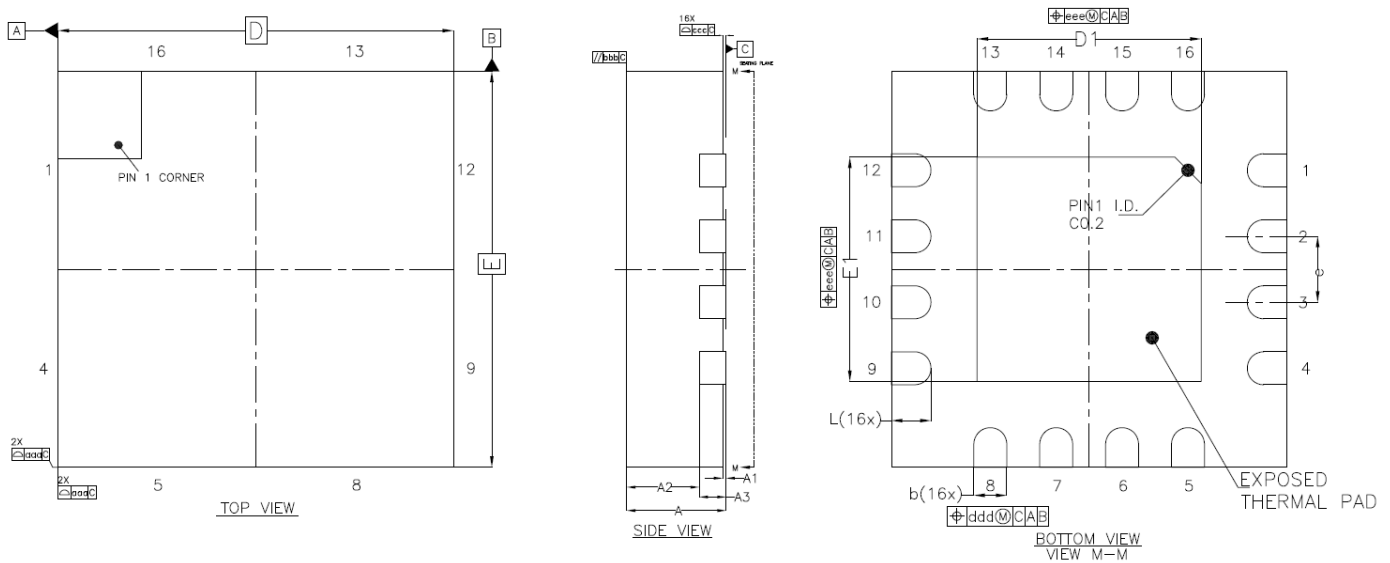
DIMENSIONS (mm are the original dimensions)

| UNIT | A <sub>max.</sub> | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c          | D(1)       | E(2)       | e    | H <sub>E</sub> | L | L <sub>p</sub> | Q          | v   | w    | y   | z(1)         | q        |
|------|-------------------|----------------|----------------|----------------|----------------|------------|------------|------------|------|----------------|---|----------------|------------|-----|------|-----|--------------|----------|
| mm   | 1.1               | 0.15<br>0.05   | 0.95<br>0.80   | 0.25           | 0.30<br>0.19   | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2     | 1 | 0.75<br>0.50   | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.72<br>0.38 | 8°<br>0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

QFN-16



| DESCRIPTION                    | SYMBOL | MILLIMETER |      |      |      |
|--------------------------------|--------|------------|------|------|------|
|                                |        | MIN        | NOM  | MAX  |      |
| TOTAL THICKNESS                | A      | 0.70       | 0.75 | 0.80 |      |
| STAND OFF                      | A1     | 0.00       | --   | 0.05 |      |
| MOLD THICKNESS                 | A2     | 0.50       | 0.55 | 0.60 |      |
| L/F THICKNESS                  | A3     | 0.203 REF  |      |      |      |
| LEAD WIDTH                     | b      | 0.20       | 0.25 | 0.30 |      |
| BODY SIZE                      | X      | D          | 2.95 | 3.00 | 3.05 |
|                                | Y      | E          | 2.95 | 3.00 | 3.05 |
| LEAD PITCH                     | e      | 0.50 BSC   |      |      |      |
| LEAD LENGTH                    | L      | 0.25       | 0.30 | 0.35 |      |
| EP SIZE                        | X      | D1         | 1.65 | 1.70 | 1.75 |
|                                | Y      | E1         | 1.65 | 1.70 | 1.75 |
| Tolerance of form and position |        |            |      |      |      |
| PACKAGE EDGE TOLERANCE         | aaa    | 0.1        |      |      |      |
| MOLD FLATNESS                  | bbb    | 0.1        |      |      |      |
| LEAD COPLANARITY               | ccc    | 0.08       |      |      |      |
| LEAD POSITION OFFSET           | ddd    | 0.1        |      |      |      |
| EXPOSED PAD OFFSET             | eee    | 0.1        |      |      |      |

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