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#### TS5A9411

SCDS241B-MAY 2008-REVISED DECEMBER 2016

# TS5A9411 10- $\Omega$ 1:2 SPDT Analog Switch Single-Channel 2:1 Multiplexer and Demultiplexer

#### Features 1

- Specified Break-Before-Make Switching
- Low ON-State Resistance (10- $\Omega$  Maximum at V<sub>CC</sub> = 5 V)
- Low Power Consumption
- TTL- and CMOS-Compatible Control Input
- Low Input and Output Capacitance
- **Excellent ON-State Resistance Matching**
- Low Total Harmonic Distortion
- 2.25-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Control Inputs Are 5.5-V Tolerant

### 2 Applications

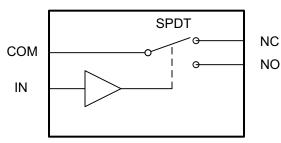
- **Cell Phones** •
- **Communication Systems**
- Portable Test Equipment •
- **Battery Operated Systems**
- Sample-and-Hold Circuits

### 3 Description

The TS5A9411 device is a bidirectional, single-pole double-throw (SPDT) analog switch that is designed to operate from 2.25 V to 5.5 V. The device offers low ON-state resistance, low leakage, and low power with a break-before-make feature. These features make this device suitable for portable and battery-powered applications.

Device Information <sup>(1)</sup>					
PART NUMBER	PACKAGE	BODY SIZE (NOM)			
TS5A9411	SOT (6)	2.00 mm × 1.25 mm			

(1) For all available packages, see the orderable addendum at the end of the data sheet.



#### **Simplified Schematic**



**ISTRUMENTS** 

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### **4** Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

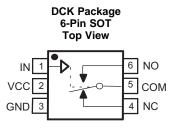
#### Changes from Revision A (July 2008) to Revision B

# Page

•	Added Device Information table, Pin Configuration and Functions section, Specifications section, ESD Ratings table, Recommended Operating Conditions table, Detailed Description section, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.	1
•	Deleted Ordering Information table; see Package Option Addendum at the end of the data sheet	1
•	Deleted Summary of Characteristics table	1
•	Moved ON-state switch current and ON-state peak switch current From: <i>Absolute Maximum Ratings</i> table To: <i>Recommended Operating Conditions</i> table	4
•	Added Thermal Information table	4
•	Changed Package thermal impedance, R <sub>0JA</sub> , value in <i>Thermal Information</i> table From: 259°C/W To: 346.7°C/W	4
•	Deleted Charge Injection vs V <sub>COM</sub> graph from Typical Characteristics	7
•	Changed graph title From: OFF Isolation vs Crosstalk ( $V_{CC} = 3 V$ ) To: Crosstalk and Insertion Loss vs Frequency ( $V_{CC} = 3 V$ ) in <i>Typical Characteristics</i>	7
•	Changed V+ to $V_{CC}$ and IN to $V_{IN}$ on all images in <i>Parameter Measurement Information</i>	8



### 5 Pin Configuration and Functions



#### **Pin Functions**

PIN   NAME NO.		I/O	DESCRIPTION
NAME	NO.	1/0	DESCRIPTION
СОМ	5	I/O	Common signal path
GND	3	—	Digital ground
IN	1	I	Digital control input. High = COM connected to NO; Low = COM connected to NC.
NC	4	I/O	Normally closed signal path
NO	6	I/O	Normally open signal path
VCC	2	_	Power supply

### 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

	MIN	MAX	UNIT
Supply voltage	-0.3	6	V
Analog voltage <sup>(3)</sup>	-0.3	V <sub>CC</sub> + 0.3	V
Digital input voltage	-0.5	V <sub>CC</sub> + 0.3	V
Analog port diode current ( $V_{NC}$ , $V_{NO}$ , $V_{COM} < 0$ )	-50		mA
Digital input clamp current ( $V_I < 0$ )	-50		mA
Continuous current through VCC		100	mA
Continuous current through GND	-100		mA
Storage temperature, T <sub>stg</sub>	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

(3) This value is limited to 5.5 V (maximum).

### 6.2 ESD Ratings

	V <sub>(ESD)</sub> Electrostatic discharge		VALUE	UNIT
v		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
V <sub>(ESD)</sub>	D) Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	v

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.25	5.5	V
V <sub>NO</sub>		NC	0	$V_{CC}$	
V <sub>NC</sub>	Analog voltage	NO	0	V <sub>CC</sub>	V
V <sub>COM</sub>	_	СОМ	0	V <sub>CC</sub>	
VI	Digital input voltage		0	5.5	V
ON-state switch current ( $V_{NO}$ , $V_{NC}$ , $V_{COM}$ = 0 to $V_{CC}$ )		-50	50	mA	
	ON-state peak switch current ( $V_{NO}$ ,	$V_{NC}$ , $V_{COM} = 0$ to $V_{CC}$ ) <sup>(1)</sup>	-200	200	mA

(1) Pulse at 1-ms duration < 10% duty cycle

#### 6.4 Thermal Information

		TS5A9411	
	THERMAL METRIC <sup>(1)</sup>	DCK (SOT)	UNIT
		12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	346.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	163.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	154.5	°C/W
ΨJT	Junction-to-top characterization parameter	17.4	°C/W
ΨJB	Junction-to-board characterization parameter	153.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

### 6.5 Electrical Characteristics: 5-V Supply

#### $V_{CC} = 5 \text{ V}, \text{ } \text{T}_{\text{A}} = 25^{\circ}\text{C} \text{ (unless otherwise noted)}$

PARAMETER		TES	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG	SWITCH							
-	ON state registeres	$V_{NO} \mbox{ or } V_{NC}$ = 3 V, $V_{CC}$ = 4.5 V, $I_{COM}$ = –10 mA, Switch ON, see Figure 5		$T_A = 25^{\circ}C$		5.3	9	Ω
r <sub>ON</sub>	ON-state resistance			$-40^{\circ}C \le T_A \le 85^{\circ}C$			10	Ω
٨٣	ON-state resistance match	$V_{NO} \text{ or } V_{NC} = 3 \text{ V}, \text{ V}_{CC} = 4.5 \text{ V},$				0.03	0.3	Ω
∆r <sub>ON</sub>	between channels	$I_{COM} = -10$ mA, Switch ON, see Figure 5		$-40^{\circ}C \le T_A \le 85^{\circ}C$			0.3	52
r <sub>ON(FLAT)</sub>	ON-state resistance flatness	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_{CC}, V_{CC} = 0$ $I_{COM} = -10 \text{ mA}, \text{ Switch ON}, \text{ set}$				2		Ω
I <sub>NC(OFF)</sub> ,		$V_{NC}$ or $V_{NO} = 1$ V and $V_{COM} = 1$ V to 4.5 V, or		$T_A = 25^{\circ}C$	-500		500	pА
I <sub>NO(OFF)</sub>	NC, NO OFF leakage current	$V_{NC}$ or $V_{NO} = 4.5$ V and $V_{COM} = 1$ V; $V_{CC} = 5.5$ V, Switch OFF, see Figure 6		$-40^{\circ}C \le T_A \le 85^{\circ}C$	-3		3	nA
I <sub>NC(ON)</sub> ,		$ \begin{array}{l} V_{NC} \text{ or } V_{NO} = 1 \text{ V and } V_{COM} = 1 \text{ V, or} \\ V_{NC} \text{ or } V_{NO} = 4.5 \text{ V and } V_{COM} = 4.5 \text{ V;} \\ V_{CC} = 5.5 \text{ V, Switch ON, see Figure 7} \end{array} $		$T_A = 25^{\circ}C$	-500		500	pА
I <sub>NO(ON)</sub>	NC, NO ON leakage current			$-40^{\circ}C \le T_A \le 85^{\circ}C$	-3		3	nA
		$      V_{NC} \text{ or } V_{NO} = \text{Open}, V_{COM} = 1 \text{ V or } 4.5 \text{ V}, \\ V_{CC} = 5.5 \text{ V}, \text{ Switch ON, see Figure 7} $		$T_A = 25^{\circ}C$	-500		500	pА
I <sub>COM(ON)</sub>	COM ON leakage current			$-40^{\circ}C \le T_A \le 85^{\circ}C$	-3		3	nA
DIGITAL I	NPUT (IN) <sup>(1)</sup>							
V	Input logic high	40°C < T < 95°C	$4.5 \ \forall \leq \forall_{CC} \leq 5.5$	5 V	2.4		5.5	V
V <sub>IH</sub>	input logic nigh	$-40^{\circ}C \le T_{A} \le 85^{\circ}C \qquad \qquad V_{CC} = 4.5 \text{ V}$			2		5.5	v
VIL	Input logic low	$4.5 \text{ V} \le \text{V}_{CC} \le 5.5 \text{ V}, -40^{\circ}\text{C} \le \text{T}_{A} \le 85^{\circ}\text{C}$			0		0.8	V
	Input loakago current	$V_{I} = 5.5 \text{ V or } 0, V_{CC} = 5.5 \text{ V}$		$T_A = 25^{\circ}C$	-0.05		0.05	
I <sub>IH</sub> , I <sub>IL</sub>	Input leakage current			$-40^{\circ}C \le T_A \le 85^{\circ}C$	-0.05		0.05	μA
DYNAMIC	;							
+	Turnon time	$V_{COM}$ = 3 V, $R_L$ = 300 $\Omega$ , $C_L$ =	$V_{CC} = 5 V, T_A = 2$	25°C			9	ns
t <sub>ON</sub>		35 pF, see Figure 9	$4.5 V \le V_{CC} \le 5.5$	5 V, –40°C ≤ T <sub>A</sub> ≤ 85°C			10	115

 All unused digital inputs of the device must be held at V<sub>CC</sub>or GND to ensure proper device operation. See Implications of Slow or Floating CMOS Inputs (SCBA004).

### **Electrical Characteristics: 5-V Supply (continued)**

$V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ (unless otherwise noted)
---

	PARAMETER	TES	T CONDITIONS		MIN	TYP	MAX	UNIT
	T	$V_{COM} = 3 V, R_1 = 300 \Omega, C_1 =$	$V_{CC} = 5 \text{ V}, \text{ T}_{A} = 25^{\circ}\text{C}$				7	
t <sub>OFF</sub>	Turnoff time	35 pF, see Figure 9					7.5	ns
	Break-before-make time	$V_{NC} = V_{NO} = 3 \text{ V}, \text{ R}_{\text{L}} = 300 \Omega, \text{ O}$	$V_{\rm NC} = V_{\rm NO} = 3 \text{ V}, \text{ R}_{\rm L} = 300 \ \Omega, \text{ C}_{\rm L} = 35 \text{ pF}, \text{ see}$ $T_{\rm A} = 25^{\circ}\text{C}$		1			22
t <sub>BBM</sub>	break-beiore-make time	Figure 10		$-40^{\circ}C \le T_A \le 85^{\circ}C$	0.9			ns
Q <sub>C</sub>	Charge injection	$V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF,$	$c_{SEN} = 0$ , $R_{GEN} = 0$ , $C_L = 1$ nF, see Figure 14			12.5		рС
$\begin{array}{c} C_{NC(OFF)},\\ C_{NO(OFF)} \end{array}$	NC, NO OFF capacitance	$V_{NC}$ or $V_{NO} = V_{CC}$ or GND, f = 7	$_{\rm NC}$ or V $_{\rm NO}$ = V $_{\rm CC}$ or GND, f = 1 MHz, Switch OFF, see Figure 8			3.5		pF
C <sub>NC(ON)</sub> , C <sub>NO(ON)</sub>	NC, NO ON capacitance	$V_{NC}$ or $V_{NO} = V_{CC}$ or GND, f = 7	$V_{NC}$ or $V_{NO} = V_{CC}$ or GND, f = 1 MHz, see Figure 8			8.5		pF
C <sub>COM(ON)</sub>	COM ON capacitance	$V_{COM} = V_{CC}$ or GND, f = 1 MHz	$C_{COM} = V_{CC}$ or GND, f = 1 MHz, Switch ON, see Figure 8			8.5		pF
CI	Digital input capacitance	$V_{I} = V_{CC}$ or GND, f = 1 MHz, se	/ <sub>I</sub> = V <sub>CC</sub> or GND, f = 1 MHz, see Figure 8			25		pF
BW	Bandwidth	$R_L = 50 \Omega$ , Switch ON, see Figu	$R_L = 50 \ \Omega$ , Switch ON, see Figure 11			100		MHz
O <sub>ISO</sub>	OFF isolation	$R_L = 50 \Omega, C_L = 5 pF, f = 1 MH$	z, Switch OFF, see	Figure 12		-84		dB
X <sub>TALK</sub>	Crosstalk	$R_L = 50 \Omega, C_L = 5 pF, f = 1 MH$	$R_L = 50 \Omega$ , $C_L = 5 pF$ , f = 1 MHz, Switch ON, see Figure 13			-85		dB
THD	Total harmonic distortion	$R_L = 600 \Omega, C_L = 50 pF, f = 20$	$R_L = 600 \Omega$ , $C_L = 50 pF$ , f = 20 Hz to 20 kHz, see Figure 15			0.03%		
SUPPLY								
	Desitive supply surrent			$T_A = 25^{\circ}C$		0.01		
I <sub>CC</sub>	Positive supply current	$v_1 = v_{CC}$ or GND, $v_{CC} = 5.5 v$ ,	$V_{I} = V_{CC}$ or GND, $V_{CC} = 5.5$ V, Switch ON or OFF				0.5	μA

### 6.6 Electrical Characteristics: 3-V Supply

 $V_{CC} = 3 \text{ V}, \text{ T}_{A} = 25^{\circ}\text{C}$  (unless otherwise noted)

	PARAMETER	TE	MIN	TYP	MAX	UNIT		
ANALOG	SWITCH							
_		$V_{NO}$ or $V_{NC} = 1.5 V$ , $V_{CC} = 2.5$	7 V.	T <sub>A</sub> = 25°C		11.5	15	Ω
r <sub>ON</sub>	ON-state resistance	$I_{COM} = -10$ mA, Switch ON, s	ee Figure 5	$-40^{\circ}C \le T_A \le 85^{\circ}C$			20	
٨٣	ON-state resistance match	$V_{NO} \text{ or } V_{NC} = 1.5 \text{ V}, V_{CC} = 2.7 \text{ V}$	7 V,	T <sub>A</sub> = 25°C		0.05	0.3	Ω
∆r <sub>ON</sub>	between channels	$I_{COM} = -10$ mA, Switch ON, s	$I_{COM} = -10$ mA, Switch ON, see Figure 5 $-40^{\circ}C \le T_A \le 85^{\circ}C$				0.3	12
r <sub>ON(FLAT)</sub>	ON-state resistance flatness	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_{CC}, I_{COM}$	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_{CC}, I_{COM} = -10 \text{ mA}, \text{ Switch ON, see Figure 5}$					Ω
$V_{NC}$ or $V_{NO} = 1$ V and $V_{COM} =$				$T_A = 25^{\circ}C$	-400		400	pА
I <sub>NO(OFF)</sub>	NC, NO OFF leakage current		$_{\rm NC}$ or V_{\rm NO} = 3 V and V <sub>COM</sub> = 1 V; $_{\rm CC}$ = 3.3 V, Switch OFF, see Figure 6 –40°C $\leq$ $^{-40^{\circ}}$ C		-2		2	nA
I <sub>NC(ON)</sub> ,		$V_{NC}$ or $V_{NO}$ = 1 V and $V_{COM}$ =		T <sub>A</sub> = 25°C	-400		400	pА
I <sub>NO(ON)</sub>	NC, NO ON leakage current	$V_{NC}$ or $V_{NO}$ = 3 V and $V_{COM}$ = $V_{CC}$ = 3.3 V, Switch ON, see	–40°C ≤ T <sub>A</sub> ≤ 85°C	-2		2	nA	
	$V_{NC}$ or $V_{NO}$ = Oper		Dpen, $V_{COM} = 1 \text{ V or } 3 \text{ V}$ , $T_A = 25^{\circ}\text{C}$				400	pА
I <sub>COM(ON)</sub>	COM ON leakage current	$V_{CC} = 3.3 \text{ V}$ , Switch ON, see	Figure 7	$-40^{\circ}C \le T_A \le 85^{\circ}C$	-2		2	nA
DIGITAL I	INPUT (IN) <sup>(1)</sup>							
VIH	Input logic high	$-40^{\circ}C \le T_A \le 85^{\circ}C$			2		5.5	V
V <sub>IL</sub>	Input logic low	$-40^{\circ}C \le T_A \le 85^{\circ}C$			0		0.8	V
	Input leakage current	$V_1 = 5.5 \text{ V or } 0, V_{CC} = 3.6 \text{ V}$		$T_A = 25^{\circ}C$	-0.05		0.05	μA
I <sub>IH</sub> , I <sub>IL</sub>	input leakage current	$v_{\rm I} = 3.5 \ v \ 01 \ 0, \ v_{\rm CC} = 3.0 \ v$		$-40^{\circ}C \le T_A \le 85^{\circ}C$	-0.05		0.05	μΑ
DYNAMIC	;							
t	Turnon time	$V_{COM}$ = 3 V, $R_{L}$ = 300 $\Omega$ ,	$V_{CC} = 3.3 \text{ V}, \text{ T}_{A}$	<sub>A</sub> = 25°C			13	ns
t <sub>ON</sub>	rumon ume	$C_L = 35 \text{ pF}, \text{ see Figure 9}$	$2.7~{\rm V} \leq {\rm V}_{\rm CC} \leq 3$	3.3 V, −40°C ≤ T <sub>A</sub> ≤ 85°C			15	115
t	Turnoff time	$V_{COM}$ = 3 V, $R_{L}$ = 300 $\Omega$ ,	$V_{CC} = 3.3 \text{ V}, \text{ T}_{A}$	<sub>A</sub> = 25°C			7.5	ns
t <sub>OFF</sub>	rumon ume	$C_L = 35 \text{ pF}, \text{ see Figure 9}$	$2.7~{\rm V} \leq {\rm V}_{\rm CC} \leq 3$	3.3 V, −40°C ≤ T <sub>A</sub> ≤ 85°C			8.5	115
t	Break-before-make time	$V_{\rm NC} = V_{\rm NO} = 3 \text{ V}, \text{ R}_{\rm L} = 300 \Omega$	, V <sub>CC</sub> = 3.3 V,	$T_A = 25^{\circ}C$	1			ns
t <sub>BBM</sub>		$C_L = 35 \text{ pF}, \text{ see Figure 10}$		$-40^{\circ}C \le T_A \le 85^{\circ}C$	0.9			115
Q <sub>C</sub>	Charge injection	$V_{GEN} = 0, R_{GEN} = 0, C_{L} = 1 n$	F, see Figure 14			6		рС

 All unused digital inputs of the device must be held at V<sub>CC</sub>or GND to ensure proper device operation. See Implications of Slow or Floating CMOS Inputs (SCBA004).

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### **Electrical Characteristics: 3-V Supply (continued)**

$V_{\alpha\alpha} =$	3 V	Т. =	25°C	(unless	otherwise	noted)
VCC -	υν,	ι <u>Δ</u> —	200	(unicoo		noteu)

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT			
C <sub>NC (OFF)</sub> , C <sub>NO(OFF)</sub>	NC, NO OFF capacitance	$V_{NC}$ or $V_{NO} = V_{CC}$ or GND, f = 1 MHz, Switch OFF, s	3.5		pF			
C <sub>NC(ON)</sub> , C <sub>NO(ON)</sub>	NC, NO ON capacitance	$V_{NC}$ or $V_{NO} = V_{CC}$ or GND, f = 1 MHz, Switch OFF, s	; or $V_{NO} = V_{CC}$ or GND, f = 1 MHz, Switch OFF, see Figure 8 8.5					
C <sub>COM(ON)</sub>	COM ON capacitance	<sub>COM</sub> = V <sub>CC</sub> or GND, f = 1 MHz, Switch OFF, see Figure 8 8.5						
CI	Digital input capacitance	$V_I = V_{CC}$ or GND, f = 1 MHz, see Figure 8	2.5		pF			
BW	Bandwidth	$R_L = 50 \Omega$ , Switch ON, see Figure 11	$R_{\rm L}$ = 50 $\Omega$ , Switch ON, see Figure 11					
O <sub>ISO</sub>	OFF isolation	$R_L = 50 \Omega$ , f = 1 MHz, Switch OFF, see Figure 12		-84		dB		
X <sub>TALK</sub>	Crosstalk	$R_L = 50 \Omega$ , f = 1 MHz, Switch ON, see Figure 13		-85		dB		
THD	Total harmonic distortion	$R_L = 600 \ \Omega$ , $C_L = 50 \ pF$ , f = 20 Hz to 20 kHz, see Fi	gure 15	0.09%				
SUPPLY			U					
-			T <sub>A</sub> = 25°C	0.01				
I <sub>CC</sub> Positive supply current		$V_{I} = V_{CC}$ or GND, $V_{CC} = 3.6$ V, Switch ON or OFF	$-40^{\circ}C \le T_A \le 85^{\circ}C$	С		μA		

### 6.7 Electrical Characteristics: 2.5-V Supply

 $V_{CC}$  = 2.5 V,  $T_A$  = 25°C (unless otherwise noted)

	PARAMETER	TE	MIN	TYP	MAX	UNIT		
ANALOG	SWITCH							
		$V_{NO}$ or $V_{NC} = 1 V$ , $V_{CC} = 2.25$	ν,	T <sub>A</sub> = 25°C		15	25	-
r <sub>ON</sub>	ON-state resistance	$I_{COM} = -10$ mA, Switch ON, s		$-40^{\circ}C \le T_A \le 85^{\circ}C$			28	Ω
4	ON-state resistance match	$V_{NO}$ or $V_{NC} = 1 V$ , $V_{CC} = 2.25$	5 V,	$T_A = 25^{\circ}C$		0.06	0.3	Ω
$\Delta r_{ON}$	between channels	$I_{COM} = -10$ mA, Switch ON, s	ee Figure 5	$-40^{\circ}\mathrm{C} \leq \mathrm{T_{A}} \leq 85^{\circ}\mathrm{C}$			0.3	12
r <sub>ON(FLAT)</sub>	ON-state resistance flatness	$0 \le (V_{NO} \text{ or } V_{NC}) \le V_{CC}, V_{CC} :$ $I_{COM} = -10 \text{ mA}, \text{ Switch ON, s}$				4		Ω
I <sub>NC(OFF)</sub> ,		$V_{NC}$ or $V_{NO}$ = 1.5 V and $V_{CON}$		$T_A = 25^{\circ}C$	-300		300	pА
I <sub>NO(OFF)</sub>	NC, NO OFF leakage current	$V_{NC}$ or $V_{NO}$ = 1.5 V and $V_{CON}$ $V_{CC}$ = 2.75 V, Switch OFF, set		$-40^{\circ}\mathrm{C} \leq \mathrm{T_{A}} \leq 85^{\circ}\mathrm{C}$	-1		1	nA
haan			$V_{\rm NC}$ or $V_{\rm NO}$ = 1.5 V and $V_{\rm COM}$ = 0.5 V to 1.5 V, or		-300		300	pА
I <sub>NC(ON)</sub> , I <sub>NO(ON)</sub>	NC, NO ON leakage current	$V_{NC}$ or $V_{NO}$ = 1.5 V and $V_{CON}$ $V_{CC}$ = 2.75 V, Switch ON, see		$-40^{\circ}C \le T_A \le 85^{\circ}C$	-1		1	nA
		$V_{NC}$ or $V_{NO}$ = Open, $V_{COM}$ = 0	0.5 V or 1.5 V,	$T_A = 25^{\circ}C$	-300		300	pА
I <sub>COM(ON)</sub>	COM ON leakage current	$V_{CC} = 2.75$ V, Switch ON, see	e Figure 7	$-40^{\circ}\mathrm{C} \leq \mathrm{T_{A}} \leq 85^{\circ}\mathrm{C}$	-1		1	nA
DIGITAL I	NPUT (IN) <sup>(1)</sup>							
V <sub>IH</sub>	Input logic high			$-40^{\circ}C \le T_A \le 85^{\circ}C$	2		5.5	V
VIL	Input logic low			$-40^{\circ}\mathrm{C} \leq \mathrm{T_{A}} \leq 85^{\circ}\mathrm{C}$	0		0.4	V
I <sub>IH</sub> , I <sub>IL</sub>	Input leakage current	$V_1 = 5.5$ V or 0 V, $V_{CC} = 2.75$	V	$T_A = 25^{\circ}C$	-0.05		0.05	μA
ηH, ηL	input leakage current	vi = 5.5 v 6i 6 v, vcc = 2.75	v	$-40^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq 85^{\circ}\text{C}$	-0.05		0.05	μΛ
DYNAMIC		- <b>F</b>						
		$V_{COM} = 2 V, R_{L} = 300 \Omega,$	$V_{CC}$ = 2.5 V, $T_{A}$ =	$V_{CC} = 2.5 \text{ V}, \text{ T}_{A} = 25^{\circ}\text{C}$			18	L
t <sub>ON</sub>	Turnon time	$C_{COM} = 2.0, R_{L} = 300 \text{ sz},$ $C_{L} = 35 \text{ pF}, \text{ see Figure 9}$	$\begin{array}{l} 2.25 \ V \leq V_{CC} \leq 2.7 \\ -40^{\circ}C \leq T_{A} \leq 85^{\circ}C \end{array}$				20	ns
			$V_{CC}$ = 2.5 V, $T_A$ =	25°C			8	l
t <sub>OFF</sub>	Turnoff time	$\label{eq:V_COM} \begin{array}{l} V_{COM} = 2 \; V, \; R_{L} = 300 \; \Omega, \\ C_{L} = 35 \; pF, \; see \; Figure \; 9 \end{array}$	$\begin{array}{l} 2.25 \text{ V} \leq \text{V}_{\text{CC}} \leq 2.7 \\ -40^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq 85^{\circ}\text{C} \end{array}$				9.5	ns
	Drock before make time	$V_{\rm NC} = V_{\rm NO} = 2 \text{ V}, \text{ R}_{\rm L} = 300 \Omega$	, C <sub>L</sub> = 35 pF, see	$T_A = 25^{\circ}C$	1			
t <sub>BBM</sub>	Break-before-make time	Figure 10		$-40^{\circ}\mathrm{C} \leq \mathrm{T_{A}} \leq 85^{\circ}\mathrm{C}$	0.9			ns
Q <sub>C</sub>	Charge injection	$V_{GEN} = 0, R_{GEN} = 0, C_L = 1 n$	F, see Figure 14			4.5		рС
C <sub>NC (OFF)</sub> , C <sub>NO(OFF)</sub>	NC, NO OFF capacitance	$V_{\rm NC}$ or $V_{\rm NO}$ = $V_{\rm CC}$ or GND, f =	= 1 MHz, Switch OFF,	see Figure 8		3.5		pF
C <sub>NC(ON)</sub> , C <sub>NO(ON)</sub>	NC, NO ON capacitance	$V_{\rm NC}$ or $V_{\rm NO}$ = $V_{\rm CC}$ or GND, f =	= 1 MHz, Switch OFF,	see Figure 8		8.5		pF

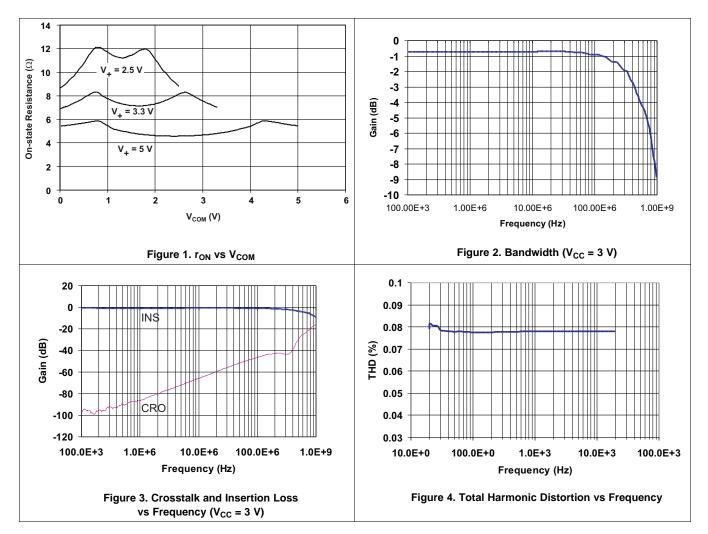
#### All unused digital inputs of the device must be held at V<sub>CC</sub>or GND to ensure proper device operation. See Implications of Slow or Floating CMOS Inputs (SCBA004).

### **Electrical Characteristics: 2.5-V Supply (continued)**

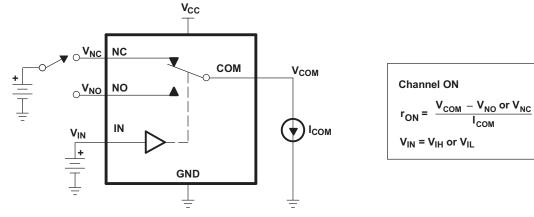
$V_{00} = 2.5 \text{ V}$ T <sub>0</sub> = 25°C	(unless otherwise noted)
$V_{CC} = 2.5 V_{1} = 25 O$	

PARAMETER		TEST CONDITIONS	MIN TYP	MAX	UNIT			
C <sub>COM(ON)</sub>	COM ON capacitance	$V_{COM} = V_{CC}$ or GND, f = 1 MHz, Switch OFF, see Fig.	V <sub>COM</sub> = V <sub>CC</sub> or GND, f = 1 MHz, Switch OFF, see Figure 8 8.5					
Ci	Digital input capacitance	$V_I = V_{CC}$ or GND, f = 1 MHz, see Figure 8	= V <sub>CC</sub> or GND, f = 1 MHz, see Figure 8 2.5					
BW	Bandwidth	$R_L = 50 \Omega$ , Switch ON, see Figure 11	_ = 50 Ω, Switch ON, see Figure 11 100					
O <sub>ISO</sub>	OFF isolation	$R_L = 50 \Omega$ , f = 1 MHz, Switch OFF, see Figure 12	$R_L = 50 \Omega$ , f = 1 MHz, Switch OFF, see Figure 12					
X <sub>TALK</sub>	Crosstalk	$R_L = 50 \Omega$ , f = 1 MHz, Switch ON, see Figure 13		-84		dB		
THD	Total harmonic distortion	$R_L = 600 \Omega$ , $C_L = 50 pF$ , f = 20 Hz to 20 kHz, see Fig.	jure 15	0.15%				
SUPPLY								
	De siti es sus studios sus st		$T_A = 25^{\circ}C$	0.01				
I <sub>CC</sub> Positive supply current		$V_1 = V_{CC}$ or GND, $V_{CC} = 2.75$ V, Switch ON or OFF	$-40^{\circ}C \le T_A \le 85^{\circ}C$		0.5	μA		

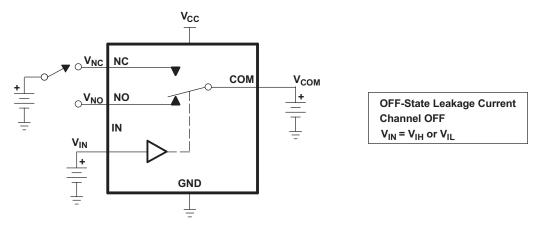
### 6.8 Typical Characteristics



### 7 Parameter Measurement Information

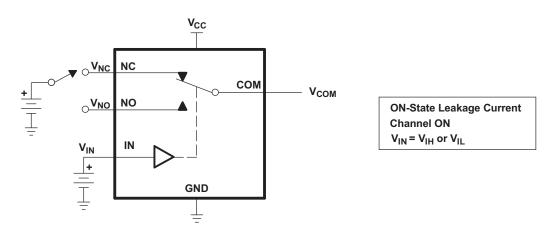






INC(OFF), INC(PWROFF), INO(OFF), INO(PWROFF), ICOM(OFF), ICOM(PWROFF)



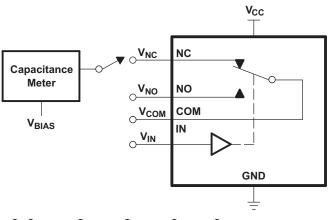


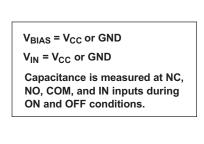
I<sub>COM(ON)</sub>, I<sub>NC(ON)</sub>, I<sub>NO(ON)</sub>





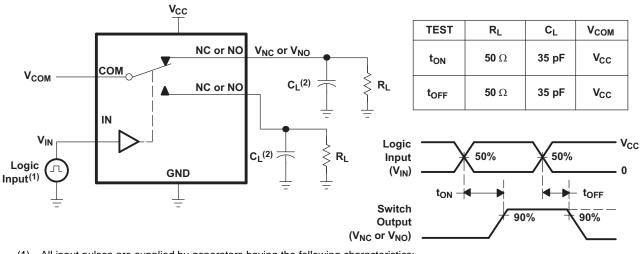






 $C_{I},\ C_{COM(ON)},\ C_{NC(OFF)},\ C_{NO(OFF)},\ C_{NC(ON)},\ C_{NO(ON)}$ 

Figure 8. Capacitance



(1) All input pulses are supplied by generators having the following characteristics:

- PRR ≤ 10 MHz
- Z<sub>O</sub> = 50 Ω
- t<sub>r</sub> < 5 ns
- t<sub>f</sub> < 5 ns

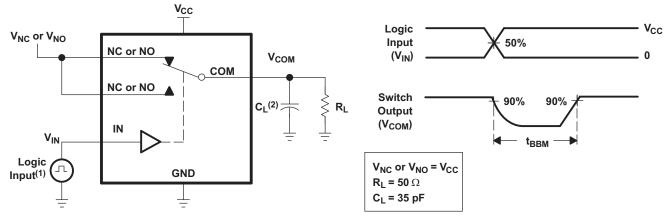
(2)  $C_L$  includes probe and jig capacitance.

### Figure 9. Turnon and Turnoff Time

**NSTRUMENTS** 

**Texas** 

### Parameter Measurement Information (continued)



(1) All input pulses are supplied by generators having the following characteristics:

- PRR ≤ 10 MHz
- Z<sub>Ω</sub> = 50 Ω
- t<sub>r</sub> < 5 ns
- t<sub>f</sub> < 5 ns
- (2)  $C_L$  includes probe and jig capacitance.



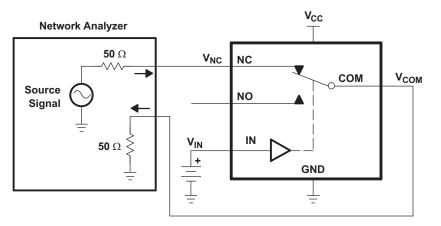
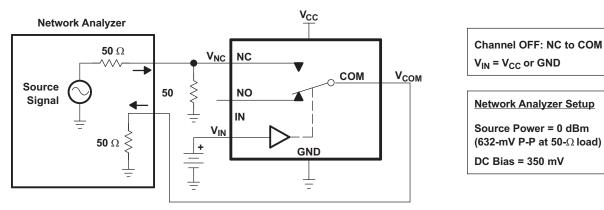


Figure 11. Bandwidth





Channel ON: NC to COM

Network Analyzer Setup

(632-mV P-P at 50-Ω load)

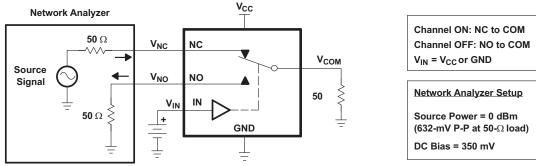
Source Power = 0 dBm

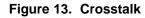
 $V_{IN} = V_{CC} \text{ or } GND$ 

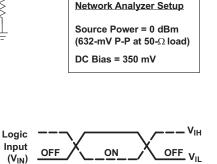
DC Bias = 350 mV

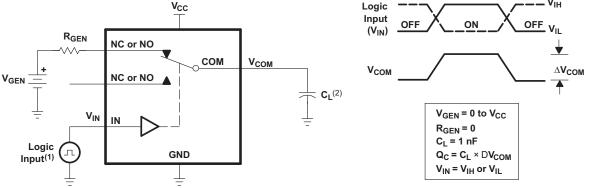








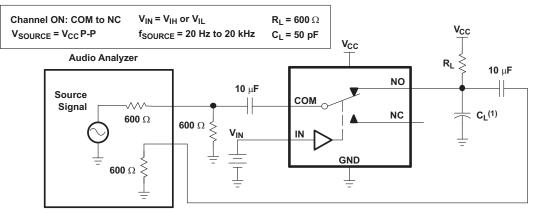




(1) All input pulses are supplied by generators having the following characteristics:

- PRR ≤ 10 MHz
- Z<sub>O</sub> = 50 Ω
- t<sub>r</sub> < 5 ns
- t<sub>f</sub> < 5 ns
- (2)  $C_L$  includes probe and jig capacitance.

Figure 14. Charge Injection



(1)  $C_L$  includes probe and jig capacitance.



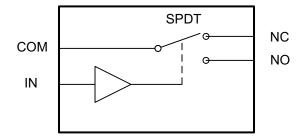
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### 8 Detailed Description

#### 8.1 Overview

The TS5A9411 device is a 1:2 or single-pole-double-throw (SPDT) solid-state analog switch. The TS5A9411, like all analog switches, is bidirectional. When powered on, each COM pin is connected to the NC pin or NO pin depending on the status of the IN pin. If IN is low, COM is connected to NC. If IN is high, COM is connected to NO. The TS5A9411 is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

#### 8.2 Functional Block Diagram



#### 8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A9411 make this switch an excellent choice for analog signals that require minimal distortion. The 2.25-V to 5.5-V operation allows compatibility with more voltage nodes, and the bidirectional I/Os can pass analog signals from 0 V to  $V_{CC}$  with low distortion.

#### 8.4 Device Functional Modes

Table 1 lists the functional modes of the TS5A9411. If IN pin is low, COM is connected to NC. If IN is high, COM is connected to NO.

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
Н	OFF	ON

#### Table 1. Function Table



### 9 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

#### 9.1 Application Information

The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs. The device is used in systems where multiple analog or digital signals must be selected to pass across a single line.

#### 9.2 Typical Application

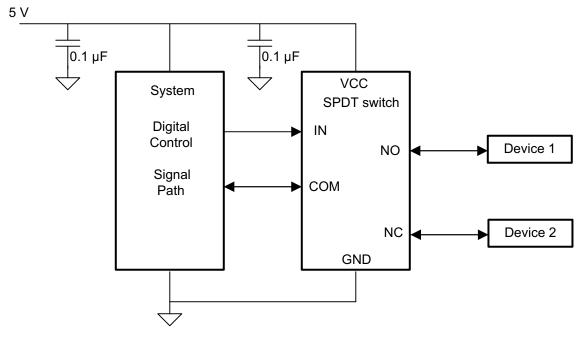


Figure 16. Typical Application Diagram

#### 9.2.1 Design Requirements

Pull the digitally controlled input select pin (IN) to  $V_{CC}$  or GND to avoid unwanted switch states that could result if the logic control pin is left floating.

#### 9.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the input or output signal swing of the device is dependent of the supply voltage ( $V_{CC}$ ).

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### Typical Application (continued)

#### 9.2.3 Application Curve

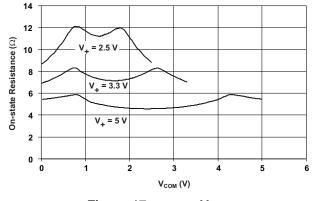


Figure 17. r<sub>on</sub> vs V<sub>COM</sub>

### **10 Power Supply Recommendations**

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence VCC on first, followed by NO, NC, or COM pins.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the  $V_{CC}$  supply to other components. A 0.1- $\mu$ F capacitor, connected from VCC to GND, is adequate for most applications.

### 11 Layout

#### 11.1 Layout Guidelines

TI recommends placing a bypass capacitor as close to the supply pins (VCC and –VCC) as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum. Minimize trace lengths and vias on the signal paths to preserve signal integrity.

### 11.2 Layout Example

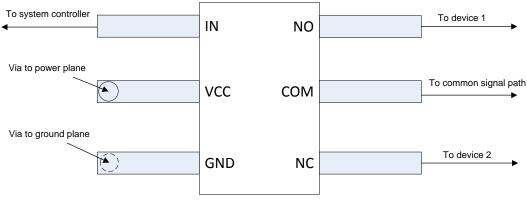


Figure 18. Layout Recommendation

### **12** Device and Documentation Support

# 12.1 Device Support

#### 12.1.1 Device Nomenclature

BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
C <sub>COM(ON)</sub>	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON.
C <sub>NC(OFF)</sub>	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF.
C <sub>NC(ON)</sub>	Capacitance at the NC port when the corresponding channel (NC to COM) is ON.
C <sub>NO(OFF)</sub>	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF.
C <sub>NO(ON)</sub>	Capacitance at the NO port when the corresponding channel (NO to COM) is ON.
Cı	Capacitance of control input (IN).
I <sub>cc</sub>	Static power-supply current with the control (IN) pin at $V_{CC}$ or GND.
I <sub>COM(ON)</sub>	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open.
ICOM(PWROFF)	Leakage current measured at the COM port during the power-down condition ( $V_{CC} = 0$ ).
I <sub>IH</sub> , I <sub>IL</sub>	Leakage current measured at the control input (IN).
I <sub>NC(OFF)</sub>	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions.
I <sub>NC(ON)</sub>	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open.
I <sub>NO(OFF)</sub>	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions.
I <sub>NO(ON)</sub>	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open.
O <sub>ISO</sub>	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
Q <sub>C</sub>	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$ , $C_L$ is the load capacitance and $\Delta V_{COM}$ is the change in analog output voltage.
$\Delta r_{ON}$	Difference of r <sub>ON</sub> between channels in a specific device.
r <sub>on</sub>	Resistance between COM and NC or COM and NO ports when the channel is ON.
r <sub>on(flat)</sub>	Difference of r <sub>ON</sub> in a channel over the specified range of conditions.
t <sub>BBM</sub>	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
t <sub>OFF</sub>	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.
t <sub>on</sub>	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is



#### **Device Support (continued)**

defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.

- V<sub>COM</sub> Voltage at COM.
- VI Voltage at the control input (IN).
- **V**<sub>IH</sub> Minimum input voltage for logic high for the control input (IN).
- V<sub>IL</sub> Maximum input voltage for logic low for the control input (IN).
- V<sub>NC</sub> Voltage at NC.
- V<sub>NO</sub> Voltage at NO.
- **X<sub>TALK</sub>** Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.

#### **12.2 Documentation Support**

#### 12.2.1 Related Documentation

For related documentation see the following: Implications of Slow or Floating CMOS Inputs (SCBA004)

#### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### **12.4 Community Resources**

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E<sup>™</sup> Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support TI's Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 12.5 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

#### **12.6 Electrostatic Discharge Caution**



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.7 Glossary

### SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.



### 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



25-Oct-2016

### PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A9411DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(32F ~ 32R) (32H ~ 32P)	Samples
TS5A9411DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(32F ~ 32R) (32H ~ 32P)	Samples
TS5A9411DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(32F ~ 32R) 32H	Samples
TS5A9411DCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(32F ~ 32R) 32H	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



25-Oct-2016

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# PACKAGE MATERIALS INFORMATION

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### TAPE AND REEL INFORMATION





### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A9411DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TS5A9411DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3

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# PACKAGE MATERIALS INFORMATION

3-Aug-2017



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A9411DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
TS5A9411DCKT	SC70	DCK	6	250	202.0	201.0	28.0

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AB.



# LAND PATTERN DATA



NOTES:

- A. All linear dimensions are in millimeters.B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



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