High Performance Power Factor Preregulator

FEATURES

- Controls Boost PWM to Near Unity Power Factor

- Fixed Frequency Average Current Mode Control Minimizes Line Current Distortion

- Built-in Active Snubber (ZVT) allows Operation to 500kHz, improved EMI and Efficiency

- Inductor Current Synthesizer allows Single Current Transformer Current Sense for Improved Efficiency and Noise Margin

- Accurate Analog Multiplier with Line Compensator allows for Universal Input Voltage Operation

- High Bandwidth (5MHz), Low Offset Current Amplifier

- Overvoltage and Overcurrent protection

- Two UVLO Threshold Options

- 150µA Startup Supply Current Typical

- Precision 1% 7.5V Reference

DESCRIPTION

The UC3855A/B provides all the control features necessary for high power, high frequency PFC boost converters. The average current mode control method allows for stable, low distortion AC line current programming without the need for slope compensation. In addition, the UC3855 utilizes an active snubbing or ZVT (Zero Voltage Transition technique) to dramatically reduce diode recovery and MOSFET turn-on losses, resulting in lower EMI emissions and higher efficiency. Boost converter switching frequencies up to 500kHz are now realizable, requiring only an additional small MOSFET, diode, and inductor to resonantly soft switch the boost diode and switch. Average current sensing can be employed using a simple resistive shunt or a current sense transformer. Using the current sense transformer method, the internal current synthesizer circuit buffers the inductor current during the switch on-time, and reconstructs the inductor current during the switch off-time. Improved signal to noise ratio and negligible current sensing losses make this an attractive solution for higher power applications.

The UC3855A/B also features a single quadrant multiplier, squarer, and divider circuit which provides the programming signal for the current loop. The internal multiplier current limit reduces output power during low line conditions. An overvoltage protection circuit disables both controller outputs in the event of a boost output OV condition.

Low startup supply current, UVLO with hysteresis, a 1% 7.5V reference, voltage amplifier with softstart, input supply voltage clamp, enable comparator, and overcurrent comparator complete the list of features. Available packages include: 20 pin N, DW, Q, J, and L.
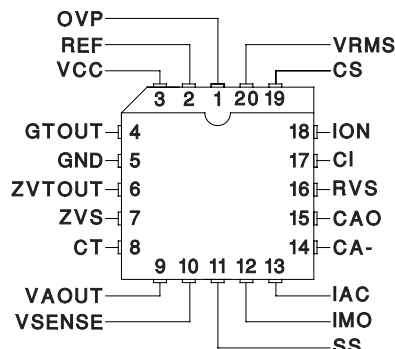
BLOCK DIAGRAM

License Patent from Pioneer Magnetics. Pin numbers refer to DIL-20 J or N packages.
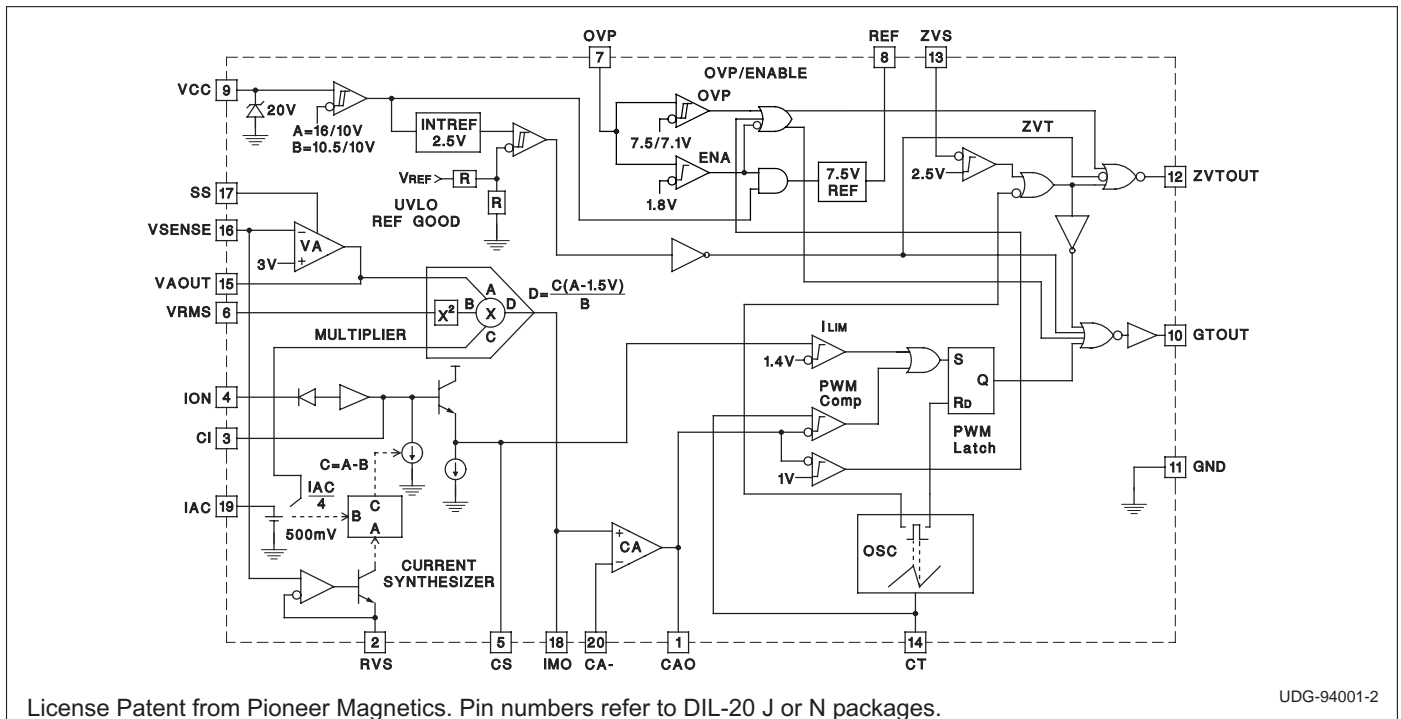
UDG-94001-2

ABSOLUTE MAXIMUM RATINGS

Supply Voltage VCC. . . . . Internally Limited
VCC Supply Clamp Current 20mA
PFC Gate Driver Current (continuous) . . . . ± 0.5A
PFC Gate Driver Current (peak) . . . . ± 1.5A
ZVT Drive Current (continuous) . . . . ± 0.25A
ZVT Drive Current (peak). . . . . ± 0.75A
Input Current (IAC, R_T, RVA) 5mA
Analog Inputs (except Peak Limit). . . . . –0.3 to 10V
Peak Limit Input . . . . –0.3 to 6.5V
Softstart Sinking Current 1.5mA
Storage Temperature . . . . –65°C to +150°C
Junction Temperature. –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . +300°C
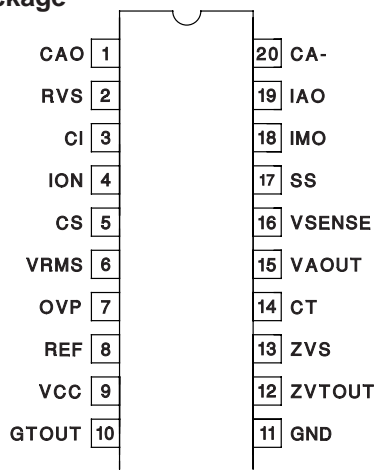
Currents are positive into, negative out of the specified termi-
nal. Consult Packaging Section of Databook for thermal limita-
tions and considerations of packages. All voltages are
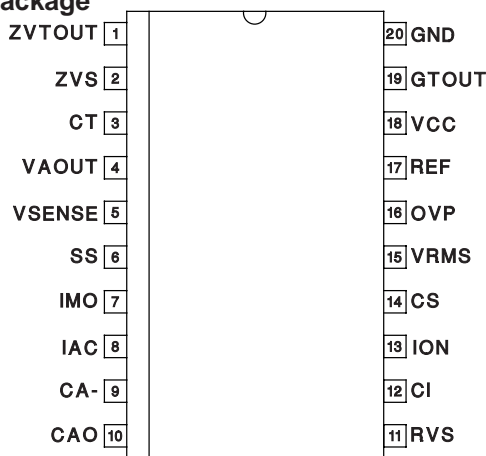referenced to GND.

CONNECTION DIAGRAMS

PLCC-20 & LCC-20 (Top View)
Q or L Package

OVP
REF — VRMS
VCC — CS
3 2 1 20 19
GTOUT — 4 | 18 — ION
GND — 5 | 17 — CI
ZVTOUT — 6 | 16 — RVS
ZVS — 7 | 15 — CAO
CT — 8 | 14 — CA-
9 10 11 12 13
VAOUT — IAC
VSENSE — IMO
SS

DIL–20 (Top View)
J or N Package

CAO	1		20	CA-
RVS	2		19	IAO
CI	3		18	IMO
ION	4		17	SS
CS	5		16	VSENSE
VRMS	6		15	VAOUT
OVP	7		14	CT
REF	8		13	ZVS
VCC	9		12	ZVTOUT
GTOUT	10		11	GND

SOIC-20 (Top View)
DW Package

ZVTOUT	1		20	GND
ZVS	2		19	GTOUT
CT	3		18	VCC
VAOUT	4		17	REF
VSENSE	5		16	OVP
SS	6		15	VRMS
IMO	7		14	CS
IAC	8		13	ION
CA-	9		12	CI
CAO	10		11	RVS

ELECTRICAL CHARACTERISTICS: Unless otherwise specified: VCC = 18V, RVS = 23k, CT = 470pF, CI = 150pF, VRMS = 1.5V, IAC = 100μA, I_{SENSE} = 0V, CAO = 4V, VAOUT= 3.5V, VSENSE = 3V. –40°C to 85°C (UC2855A/B), 0°C to 70°C (UC3855A/B).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply Current, OFF	CAO, VAOUT = 0V, VCC = UVLO –0.3V		150	500	μA
Supply Current, OPERATING			17	25	mA
VCC Turn-On Threshold	UC3855A		15.5	17.5	V
VCCTurn-Off Threshold	UC3855A,B	9	10		V
VCC Turn-On Threshold	UC3855B		10.5	10.8	V
VCC Clamp	I(VCC) = $I_{CC(on)}$ + 5mA	18	20	22	V
Voltage Amplifier					
Input Voltage		2.9		3.1	V
VSENSE Bias Current		–500	25	500	nA
Open Loop Gain	V_{OUT} = 2 to 5V	65	80		dB
V_{OUT} High	I_{LOAD} = –300μA	5.75	6	6.25	V
V_{OUT} Low	I_{LOAD} = 300μA		0.3	0.5	V
Output Short Circuit Current	V_{OUT} = 0V		0.6	3	mA

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ELECTRICAL CHARACTERISTICS: Unless otherwise specified: VCC = 18V, RVS = 23k, CT = 470pF, CI = 150pF, VRMS = 1.5V, IAC = 100µA, I_{SENSE} = 0V, CAO = 4V, VAOUT= 3.5V, VSENSE = 3V. –40°C to 85°C (UC2855A/B), 0°C to 70°C (UC3855A/B).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Amplifier					
Input Offset Voltage	V_{CM} = – 2.5V	–4		4	mV
Input Bias Current (Sense)	V_{CM} = 2.5V	–500		500	nA
Open Loop Gain	V_{CM} = 2.5V, V_{OUT} = 2 to 6V	80	110		dB
V_{OUT} High	I_{LOAD} = –500µA		6		V
V_{OUT} Low	I_{LOAD} = 500µA		0.3	0.5	V
Output Short Circuit Current	V_{OUT} = 0V		1	3	mA
Common Mode Range		–0.3		5	V
Gain Bandwidth Product	F_{IN} = 100kHz, 10mV, P–P, T_A = 25°C	2.5	5		MHz
Reference					
Output Voltage	I_{REF} = 0mA, T_A = 25°C	7.388	7.5	7.613	V
	I_{REF} = 0mA	7.313	7.5	7.688	V
Load Regulation	I_{REF} = 1 to 10 mA	–15		15	mV
Line Regulation	VCC = 15 to 35V	–10		10	mV
Short Circuit Current	REF = 0V	20	45	65	mA
Oscillator					
Initial Accuracy	T_A = 25°C	170	200	230	kHz
Voltage Stability	V_{CC} = 12 to 18V		1		%
Total Variation	Line, Temp.	160		240	kHz
Ramp Amplitude (P–P)	Outputs at 0% duty cycle	4.7		5.7	V
Ramp Valley Voltage		1.1		1.6	V
Enable/OVP/Current Limit					
Enable Threshold			1.8	2.2	V
OVP Threshold			7.5	7.66	V
OVP Hysteresis		200	400	600	mV
OVP Propagation Delay			200		ns
OVP Input Bias Current	V= 7.5V		1	10	µA
PK$_{LIMIT}$ Threshold		1.25	1.5	1.75	V
PK$_{LIMIT}$ Input Current	$V_{PKLIMIT}$ = 1.5V		100		µA
PK$_{LIMIT}$ Prop. Delay			100		ns
Soft Start					
Soft Start Charge Current		-10	-13	-20	µA
Soft Start Discharge Current		2	10	20	mA
Multiplier					
Output Current - IAC Limited	IAC = 100µA, VRMS = 1V	–235	–205	–175	µA
Output Current - Zero	IAC = 0µA	–2	–0.2	2	µA
Output Current - Power Limited	VRMS = 1.5V, VAOUT = 5.5V	–250	–209	–160	µA
Output Current	VRMS = 1.5V, VAOUT = 2V		–26		µA
	VRMS = 1.5V VAOUT = 5V		–190		µA
	VRMS = 5V, VAOUT = 2V		–3		µA
	VRMS = 5V, VAOUT = 5V		–17		µA
Gain Constant	Refer to Note 1	–0.95	–0.85	–0.75	1/V

ELECTRICAL CHARACTERISTICS: Unless otherwise specified: VCC = 18V, RVS = 23k, CT = 470pF, CI = 150pF, VRMS = 1.5V, IAC = 100µA, I$_{SENSE}$ = 0V, CAO = 4V, VAOUT= 3.5V, VSENSE = 3V. –40°C to 85°C (UC2855A/B), 0°C to 70°C (UC3855A/B).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate Driver Output					
Output High Voltage	I$_{OUT}$ = –200mA, VCC = 15V	12	12.8		V
Output Low Voltage	I$_{OUT}$ = 200mA		1	2.2	V
Output Low Voltage	I$_{OUT}$ = 10mA		300	500	mV
Output Low (UVLO)	I$_{OUT}$ = 50mA, VCC = 0V		0.9	1.5	V
Output RISE/FALL Time	C$_{LOAD}$ = 1nF		35		ns
Output Peak Current	C$_{LOAD}$ = 10nF	0.5	1.5		A
ZVT					
ZVS Threshold		2.3	2.6	2.9	V
Input Bias Current	V = 2.5V, V$_{CT}$ = 0		6	20	µA
Propagation Delay	Measured at ZVTOUT		100		ns
Maximum Pulse Width			400		ns
Output High Voltage	I$_{OUT}$ = –100mA, V$_{CC}$ = 15V	12	12.8		V
Output Low Voltage	I$_{OUT}$ = 100mA		1	2.2	V
	I$_{OUT}$ = 10mA		300	900	mV
Output Low (UVLO)	I$_{OUT}$ = 50mA, V$_{CC}$ = 0V		0.9	1.5	V
Output RISE/FALL Time	C$_{LOAD}$ = 1nF		35		ns
Output Peak Current	C$_{LOAD}$ = 10nF	0.25	0.75		A
Current Synthesizer					
I$_{ON}$ to CS Offset	VION = 0V		30	50	mV
CI Discharge Current	IAC = 50µA	105	118	140	µA
	IAC = 500µA		5		µA
IAC Offset Voltage		0.3	0.65	1.1	V
ION Buffer Slew Rate			10		V/µs
ION Input Bias Current	V$_{ION}$ = 2V		2	15	µA
RVS Output Voltage	23k from RVS to GND	2.87	3	3.13	V

Note 1: Gain constant (K) = $\dfrac{IAC \bullet (VA_{OUT} - 1.5V)}{(V_{RMS}{}^2 \bullet IMO)}$ at V$_{RMS}$ = 1.5V, VA$_{OUT}$ = 5.5V.

PIN DESCRIPTIONS

CA   This is the inverting input to the current amplifier. Connect the required compensation components between this pin and CAOUT. The common mode operating range for this input is between –0.3V and 5V.

CAO: This is the output of the wide bandwidth current amplifier and one of the inputs to the PWM duty cycle comparator. The output signal generated by this amplifier commands the PWM to force the correct input current. The output can swing from 0.1V to 7.5V.

CI: The level shifted current sense signal is impressed upon a capacitor connected between this pin and GND. The buffered current sense transformer signal charges the capacitor when the boost switch is on. When the switch is off, the current synthesizer discharges the capacitor at a rate proportional to the dI/dt of the boost inductor current. In this way, the discharge current is approximately equal to

$$\frac{3V}{R\,RVS} - \frac{IAC}{4}.$$

Discharging the CI capacitor in this fashion, a "reconstructed" version of the inductor current is generated using only one current sense transformer.

PIN DESCRIPTIONS (cont.)

CS: The reconstructed inductor current waveform generated on the CI pin is level shifted down a diode drop to this pin. Connect the current amplifier input resistor between CS and the inverting input of the current amplifier. The waveform on this pin is compared to the multiplier output waveform through the average current sensing current amplifier. The input to the peak current limiting comparator is also connected to this pin. A voltage level greater than 1.5 volts on this pin will trip the comparator and disable the gate driver output.

CT: A capacitor from CT to GND sets the PWM oscillator frequency according to the following equation:

$$f \approx \frac{1}{11200 \bullet CT}.$$

Use a high quality ceramic capacitor with low ESL and ESR for best results. A minimum CT value of 200pF insures good accuracy and less susceptibility to circuit layout parasitics. The oscillator and PWM are designed to provide practical operation to 500kHz.

GND: All voltages are measured with respect to this pin. All bypass and timing capacitors connected to GND should have leads as short and direct as possible.

GTOUT: The output of the PWM is a 1.5A peak totem pole MOSFET gate driver on GTOUT. A series resistor between GTOUT and the MOSFET gate of at least 10 ohms should be used to limit the overshoot on GTOUT. In addition, a low VF Schottky diode should be connected between GTOUT and GND to limit undershoot and possible erratic operation.

IAC: This is a current input to the multiplier. The current into this pin should correspond to the instantaneous value of the rectified AC input line voltage. This is accomplished by connecting a resistor directly between IAC and the rectified input line voltage. The nominal 650mV level present on IAC negates the need for any additional compensating resistors to accommodate for the zero crossings of the line. A current equal to one fourth of the IAC current forms one of the inductor current synthesizer inputs.

IMO: This is the output of the multiplier, and the non-inverting input of the current amplifier. Since this output is a current, connect a resistor between this pin and ground equal in value to the input resistor of the current amplifier. The common mode operating range for this pin is –0.3V to 5V.

ION: This pin is the current sensing input. It should be connected to the secondary side output of a current sensing transformer whose primary winding is in series with the boost switch. The resultant signal applied to this input is buffered and level shifted up a diode to the CI capacitor on the CI pin. The ION buffer has a source only output. Discharge of the CI cap is enabled through the current synthesizer circuitry. The current sense transformer termination resistor should be designed to obtain a 1V input signal amplitude at peak switch current.

OVP: This pin senses the boost output voltage through a voltage divider. The enable comparator input is TTL compatible and can be used as a remote shutdown port. A voltage level below 1.8V, disables VREF, oscillator, and the PWM circuitry via the enable comparator. Between 1.8V and VREF (7.5V) the UC is enabled. Voltage levels above 7.5V will set the PWM latch via the hysteretic OVP comparator and disable both ZVTOUT and GTOUT until the OVP level has decayed by the nominal hysteresis of 400mV. If the voltage divider is designed to initiate an OVP fault at 5% of OV, the internal hysteresis enables normal operation again when the output voltage has reached its nominal regulation level. Both the OVP and enable comparators have direct logical connections to the PWM output and exhibit typical propagation delays of 200ns.

REF: REF is the output of the precision reference. The output is capable of supplying 25mA to peripheral circuitry and is internally short circuit current limited. REF is disabled and low whenever VCC is below the UVLO threshold, and when OVP is below 1.8V. A REF "GOOD" comparator senses REF and disables the stage until REF has attained approximately 90% of its nominal value. Bypass REF to GND with a 0.1µF or larger ceramic capacitor for best stability.

RVS: The nominal 3V signal present on the VSENSE pin is buffered and brought out to the RVS pin. A current proportional to the output voltage is generated by connecting a resistor between this pin and GND. This current forms the second input to the current synthesizer.

SS: Soft-start V_{SS} is discharged for V_{VCC} low conditions. When enabled, SS charges an external capacitor with a current source. This voltage is used as the voltage error signal during start-up, enabling the PWM duty cycle to increase slowly. In the event of a V_{VCC} dropout, the OVP/EN is forced below 1.8V (typ), SS quickly discharges to disable the PWM.

PIN DESCRIPTIONS (cont.)

VAO: This is the output of the voltage amplifier. At a given input RMS voltage, the voltage on this pin will vary directly with the output load. The output swing is limited from approximately 100mV to 6V. Voltage levels below 1.5V on this pin will inhibit the multiplier output.

VCC: Positive supply rail for the IC. Bypass this pin to GND with a 1μF low ESL, ESR ceramic capacitor. This pin is internally clamped to 20V. Current into this clamp should be limited to less than 10mA. The UC3855A has a 15.5V (nominal) turn on threshold with 6 volts of hysteresis while the UC3855B turns on at 10.5V with 500mV of hysteresis.

VRMS: This pin is the feedforward line voltage compensation input to the multiplier. A voltage on VRMS proportional to the AC input RMS voltage commands the multiplier to alter the current command signal by $1/VRMS^2$ to maintain a constant power balance. The input to VRMS is generally derived from a two pole low pass filter/voltage divider connected to the rectified AC input voltage. This feature allows universal input supply voltage operation and faster response to input line fluctuations for the PFC boost preregulator. For most designs, a voltage level of 1.5V on this pin should correspond to low line, and 4.7V for high line. The input range for this pin extends from 0 to 5.5V.

VSENSE: This pin is the inverting input of the voltage amplifier and serves as the output voltage feedback point for the PFC boost converter. It senses the output voltage through a voltage divider which produces a nominal 3V. The voltage loop compensation is normally connected between this pin and VAO. The VSENSE pin must be above 1.5V at 25°C, (1.9V at –55°C) for the current synthesizer to work properly.

ZVS: This pin senses when the drain voltage of the main MOSFET switch has reached approximately zero volts, and resets the ZVT latch via the ZVT comparator. A minimum and maximum ZVTOUT pulse width are programmable from this pin. To directly sense the ≈400V drain voltage of the main switch, a blocking diode is connected between ZVS and the high voltage drain. When the drain reaches 0V, the level on ZVS is ≈0.7V which is below the 2.6V ZVT comparator threshold. The maximum ZVTOUT pulse width is approximately equal to the oscillator blanking period time.

ZVTOUT: The output of the ZVT block is a 750mA peak totem pole MOSFET gate driver on ZVTOUT. Since the ZVT MOSFET switch is typically 3X smaller than the main switch, less peak current is required from this output. Like GTOUT, a series gate resistor and Schottky diode to GND are recommended. This pin may also be used as a high current synchronization output driver.

For more information see Unitrode Applications Note U-153.
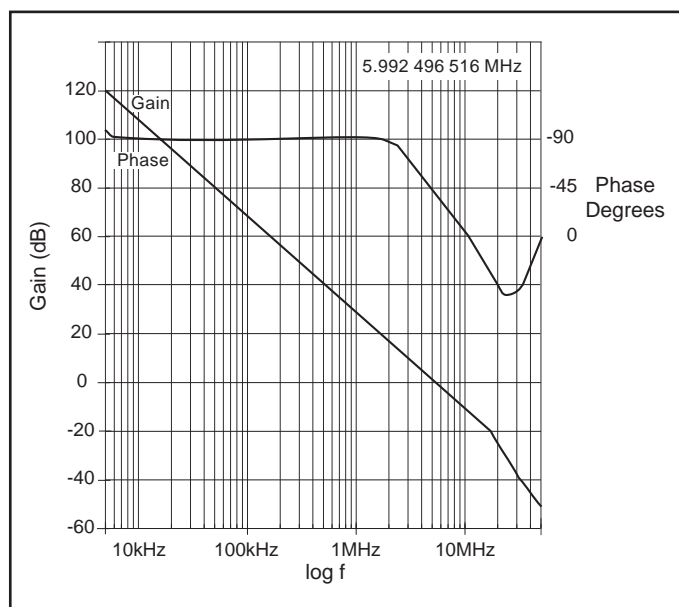
Figure 1. Current Amplifier Frequency Response
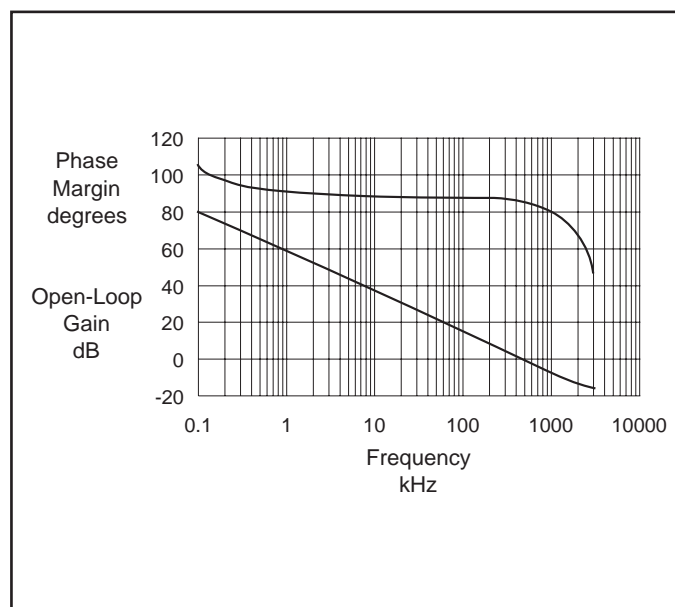
Figure 2. Voltage Amplifier Gain Phase vs Frequency
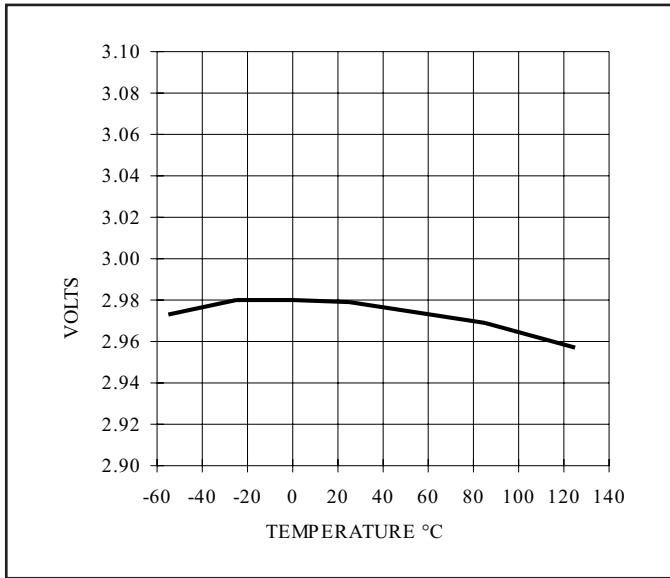
Figure 3. Voltage Amplifier Input Threshold
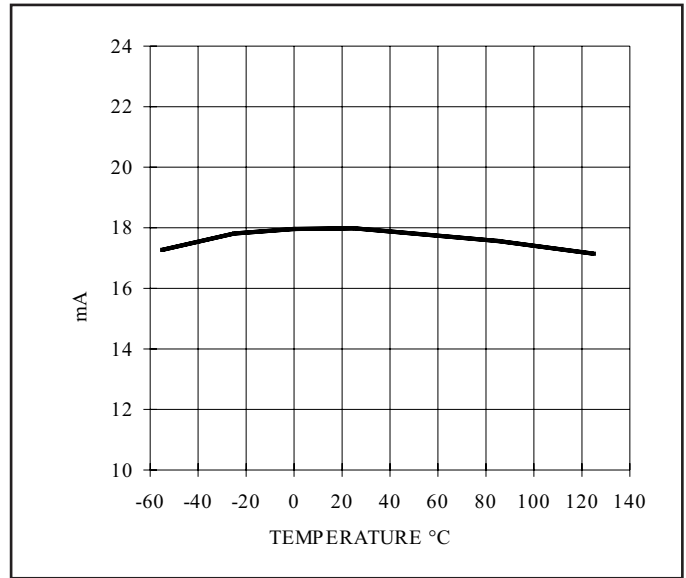
Figure 4. Supply Current ON
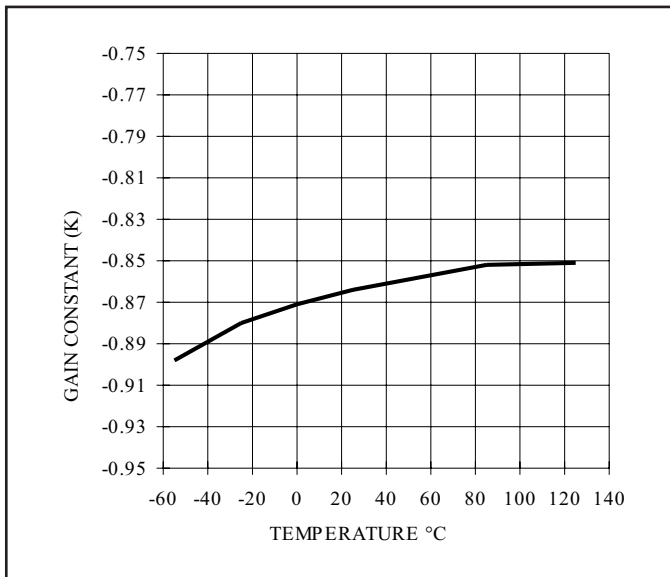
Figure 5. Multiplier Current Gain Constant
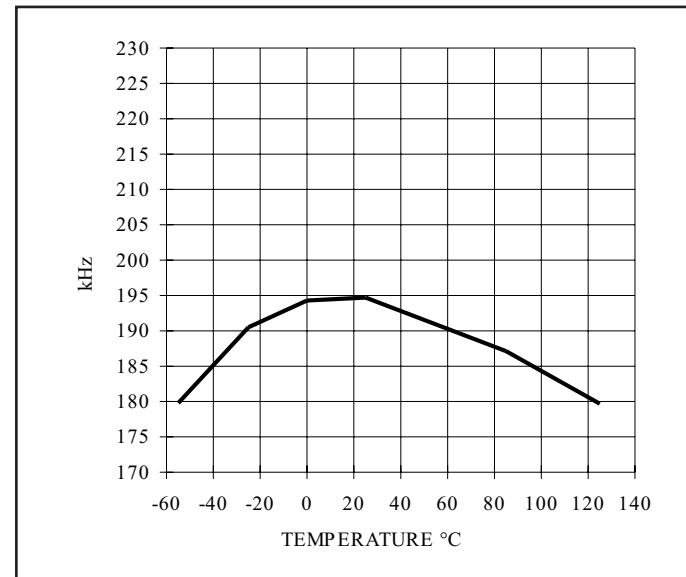
Figure 6. Oscillator Initial Accuracy

TYPICAL APPLICATION

UDG-95165-1

Figure 7. Typical Application

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2855ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2855ADW	Samples
UC2855BDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2855BDW	Samples
UC2855BDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2855BDW	Samples
UC2855BDWTR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2855BDW	Samples
UC2855BDWTRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2855BDW	Samples
UC2855BN	ACTIVE	PDIP	N	20	18	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	N / A for Pkg Type	-40 to 85	UC2855BN	Samples
UC2855BNG4	ACTIVE	PDIP	N	20	18	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type	-40 to 85	UC2855BN	Samples
UC3855ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3855ADW	Samples
UC3855ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3855ADW	Samples
UC3855ADWTR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3855ADW	Samples
UC3855BDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3855BDW	Samples
UC3855BDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3855BDW	Samples
UC3855BDWTR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3855BDW	Samples
UC3855BDWTRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3855BDW	Samples
UC3855BN	ACTIVE	PDIP	N	20	18	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	N / A for Pkg Type	0 to 70	UC3855BN	Samples
UC3855BNG4	ACTIVE	PDIP	N	20	18	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type	0 to 70	UC3855BN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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![TEXAS INSTRUMENTS logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3855ADWTR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3855ADWTR	SOIC	DW	20	2000	367.0	367.0	45.0

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) ⚠D

0.045 (1,14) / 0.030 (0,76) ⚠D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option ⚠D

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E   12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
⚠C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
⚠D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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10.63 / 9.97 TYP

PIN 1 ID AREA

A

1

13.0 / 12.6 NOTE 3

10

B

7.6 / 7.4

NOTE 4

20

18X 1.27

11

2X 11.43

20X 0.51 / 0.31

⊕ 0.25 Ⓜ C A B

C

SEATING PLANE

⌒ 0.1 C

2.65 MAX

SEE DETAIL A

0.33 / 0.10 TYP

GAGE PLANE

0.25

0° - 8°

1.27 / 0.40

0.3 / 0.1

DETAIL A
TYPICAL

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

20

SYMM

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

SYMM

20

10

11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.