LMZ1050x Evaluation Board

National Semiconductor
Application Note 2022
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Introduction

The LMZ1050x SIMPLE SWITCHER® power module is a complete, easy-to-use DC-DC solution capable of driving up to 3A, 4A, or 5A load with exceptional power conversion efficiency, output voltage accuracy, line and load regulation. The LMZ1050x is available in an innovative package that enhances thermal performance and allows for hand or machine soldering.

The LMZ1050x can accept an input voltage rail between 2.95V and 5.5V and deliver an adjustable and highly accurate output voltage as low as 0.8V. One megahertz fixed frequency PWM switching provides a predictable EMI characteristic. Two external compensation components can be adjusted to set the fastest response time, while allowing the option to use ceramic and/or electrolytic output capacitors. Externally programmable soft-start capacitor facilitates controlled startup. The LMZ1050x is a reliable and robust solution with the following features: lossless cycle-by-cycle peak current limit to protect for over current or short-circuit fault, thermal shutdown, input under-voltage lock-out, and pre-biased startup.

Board Specifications

- V_{IN} = 2.95V to 5.5V
- V_{OUT} = 2.5V (default output voltage setting, refer to *Table 2* for other output settings)
- ±2.5% feedback voltage accuracy at 2.5V output (Including line and load regulation from T_J = -40°C to 125°C)
- ±1.63% feedback voltage accuracy over temperature
- I_{OUT} = 0A to 3A, 4A, and 5A
- θ_{JA} = 20°C / W, θ_{JC} = 1.9°C / W
- Designed on four layers, the top and bottom layers are 1oz. copper and the two inner layers are 1/2 oz. copper weight
- Measures 2.25 in. x 2.25 in. (5.8 cm x 5.8 cm) and is 62mil (.062") thick on a FR4 laminate

Evaluation Board Design Concept

The evaluation board is designed to demonstrate low conducted noise on the input and output lines, as seen in *Figure 11*and *Figure 14*. Four input capacitors (C_{in1} - C_{in4}) and three output capacitors (C_{o1} - C_{o3}) are populated for this purpose. All the input and output filter capacitors are not necessary to comply with radiation standards. For a circuit example that passes radiated emissions standards (EN55022, class B) please refer to *Figure 19*. Additionally, C_{in5} is present to reduce the resonance of the input line produced by the inductance and resistance in the cables connecting the bench power supply to the evaluation board and the input capacitors.

Additional Component Footprints

When the tracking feature of the LMZ1050x is used, remove the soft-start capacitor C_{SS} and use a resistor divider on designators R_{trkb} and R_{trkt}. The ground and V_{trk} post have been provided for easy connection.

The LMZ1050x eval board incorporates a precision enable circuit which is pulled high by a 100 kΩ pull up resistor to VIN. This allows the user to pull low on the enable pin to ground. The top enable resistor is R_{ent} and the bottom enable resistor is R_{enb}. Refer to the Design Guideline and Operating Description section of the LMZ1050x data sheet for detailed design implementation.

Select FPGAs specify input inrush currents for particular power-up sequences and others require sequencing rails to avoid start-up or latch-up problems. To prevent early turn-on of the LMZ1050x in systems with multiple power rails, precision enable and tracking are useful as the main input voltage rail rises at power-up.

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Component Circuit Schematic

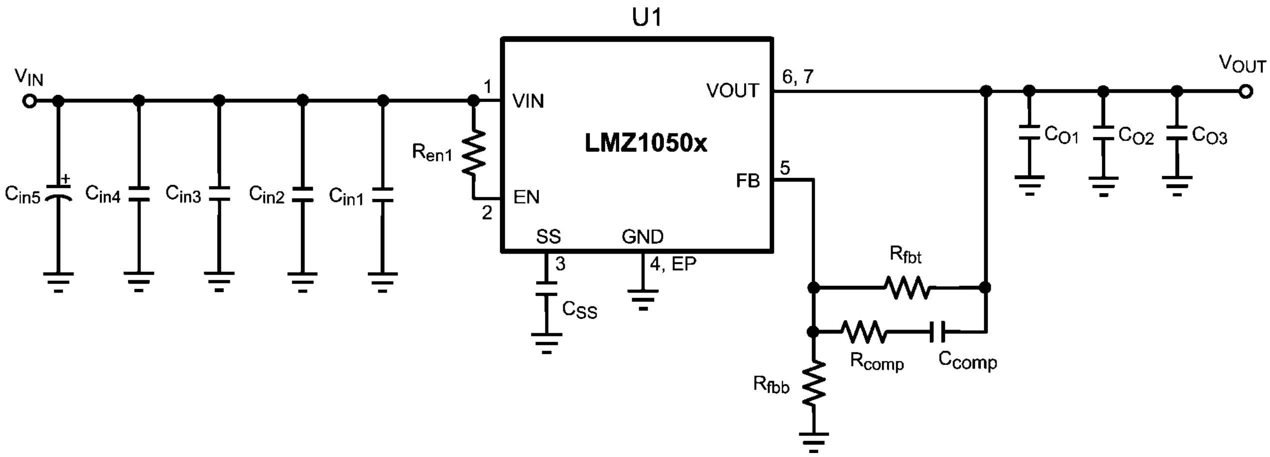

FIGURE 1. Component Schematic for Evaluation Board

TABLE 1. Bill of Materials for Evaluation Board, V_{IN} = 3.3V to 5V, V_{OUT} = 2.5V

Designator	Description	Case Size	Manufacturer	Manufacturer P/N	Quantity
U1	SIMPLE SWITCHER®	TO-PMOD-7	National Semiconductor	LMZ1050xTZ-ADJ	1
C_{in1}	1 µF, X7R, 16V	0805	TDK	C2012X7R1C105K	1
C_{in2}, C_{O1}	4.7 µF, X5R, 6.3V	0805	TDK	C2012X5R0J475K	2
C_{in3}, C_{O2}	22 µF, X5R, 16V	1210	TDK	C3225X5R1C226M	2
C_{in4}	47 µF, X5R, 6.3V	1210	TDK	C3225X5R0J476M	1
C_{in5}	220 µF, 10V, AL-Elec	E	Panasonic	EEE1AA221AP	1
C_{O3}	100 µF, X5R, 6.3V	1812	TDK	C4532X5R0J107M	1
R_{fbt}	75 kΩ	0805	Vishay Dale	CRCW080575K0FKEA	1
R_{fbb}	34.8 kΩ	0805	Vishay Dale	CRCW080534K8FKEA	1
R_{comp}	1.1 kΩ	0805	Vishay Dale	CRCW08051K10FKEA	1
C_{comp}	180 pF, ±5%, C0G, 50V	0603	TDK	C1608C0G1H181J	1
R_{en1}	100 kΩ	0805	Vishay Dale	CRCW0805100KFKEA	1
C_{SS}	10 nF, ±5%, C0G, 50V	0805	TDK	C2012C0G1H103J	1

TABLE 2. Output Voltage Setting (R_{fbt} = 75 kΩ)

V_{OUT}	R_{fbb}
3.3 V	23.7 kΩ
2.5 V	34.8 kΩ
1.8 V	59 kΩ
1.5 V	84.5 kΩ
1.2 V	150 kΩ
0.9 V	590 kΩ

Complete Circuit Schematic

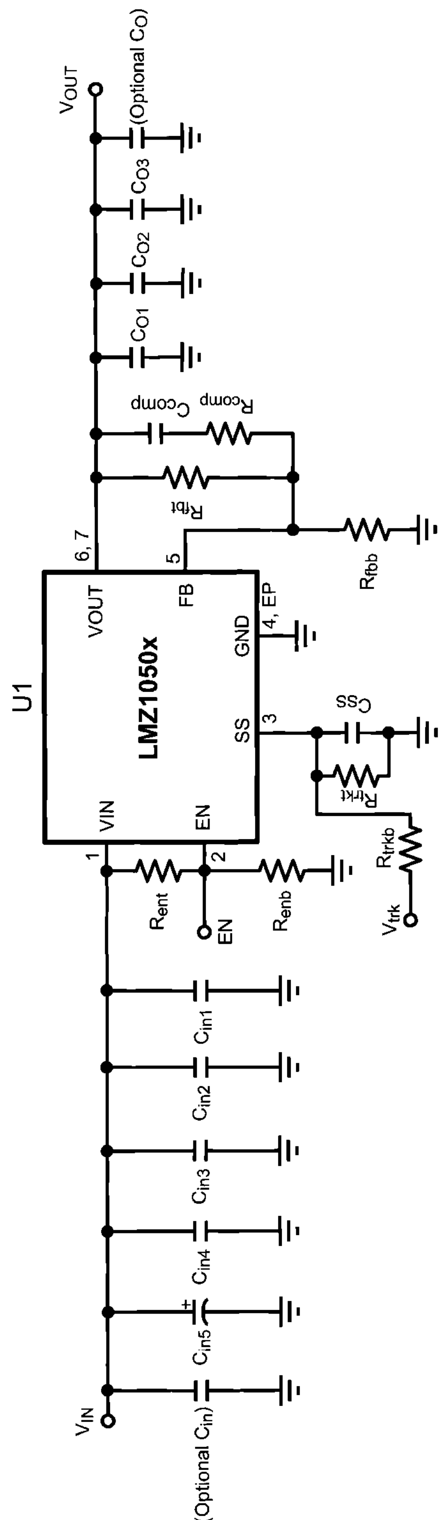

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FIGURE 2. Complete Evaluation Board Schematic

Connection Diagram

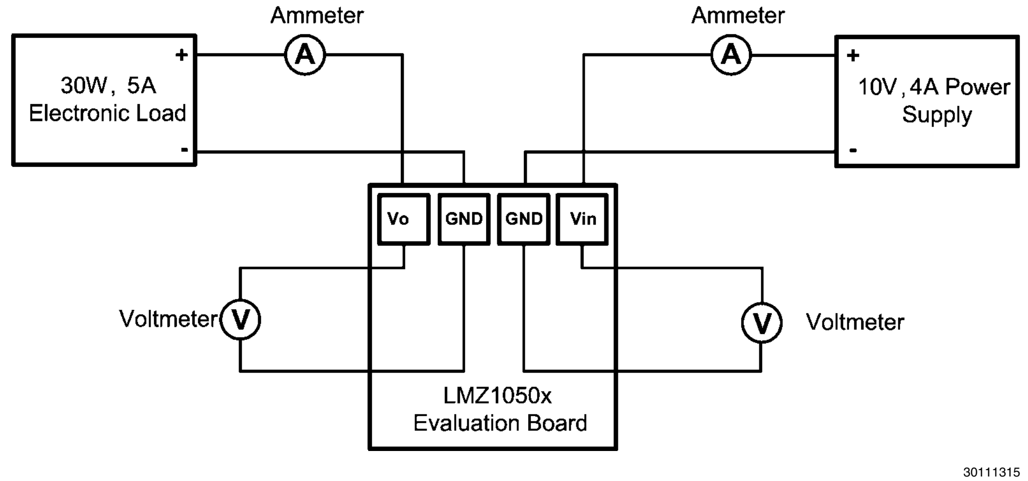


FIGURE 3. Efficiency Measurement Setup

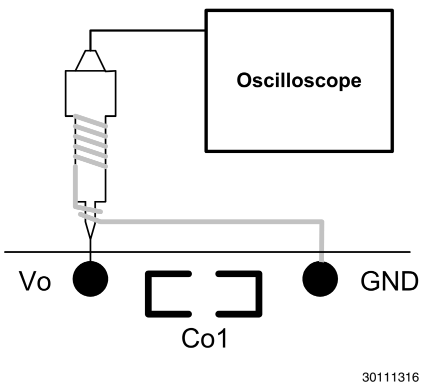
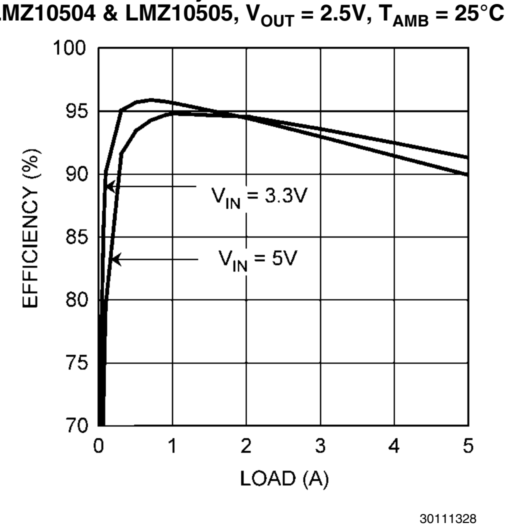
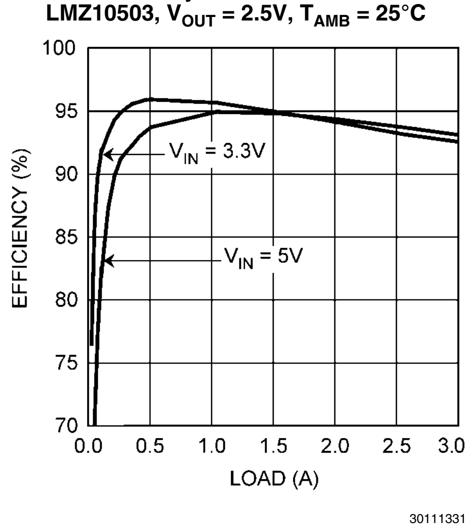


FIGURE 4. Output Voltage Ripple Measurement Setup

Efficiency vs. Load Current
LMZ10504 & LMZ10505, V_{OUT} = 2.5V, T_{AMB} = 25°C



Efficiency vs. Load Current
LMZ10503, V_{OUT} = 2.5V, T_{AMB} = 25°C



Performance Characteristics

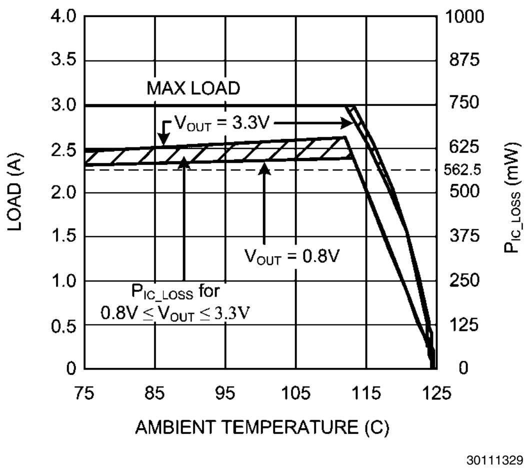


FIGURE 5. Current Derating vs. Ambient Temperature LMZ10503, V_{IN} = 5.0V, θ_{JA} = 20°C/W

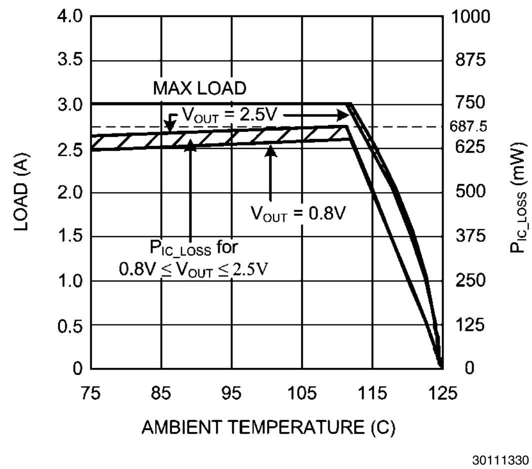


FIGURE 8. Current Derating vs. Ambient Temperature LMZ10503, V_{IN} = 3.3V, θ_{JA} = 20°C/W

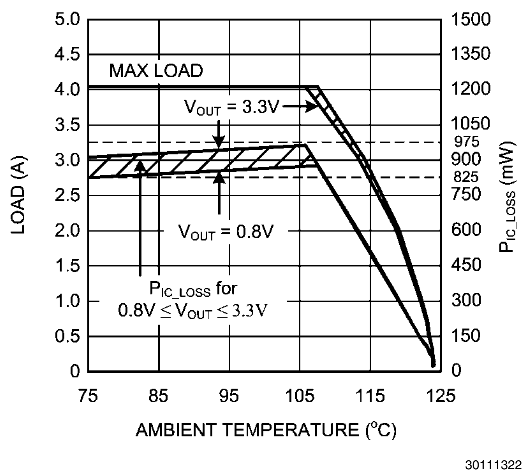


FIGURE 6. Current Derating vs. Ambient Temperature LMZ10504, V_{IN} = 5.0V, θ_{JA} = 20°C/W

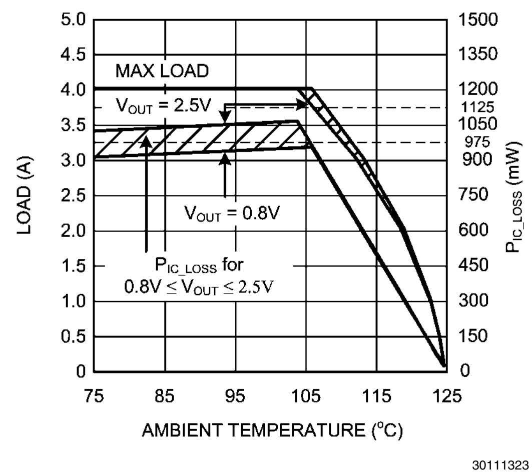


FIGURE 9. Current Derating vs. Ambient Temperature LMZ10504, V_{IN} = 3.3V, θ_{JA} = 20°C/W

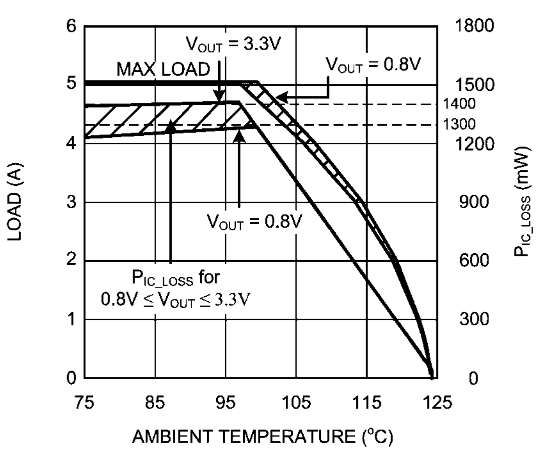


FIGURE 7. Current Derating vs. Ambient Temperature LMZ10505, V_{IN} = 5.0V, θ_{JA} = 20°C/W

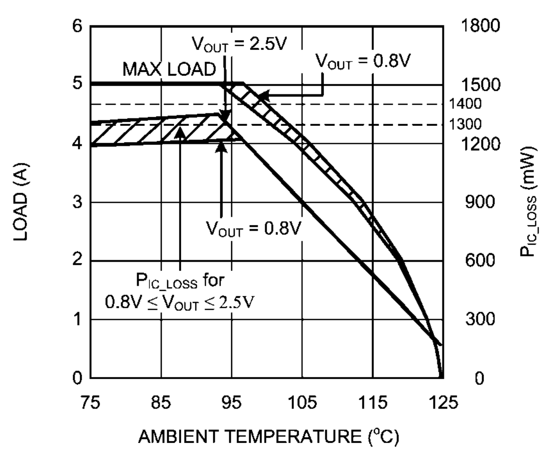


FIGURE 10. Current Derating vs. Ambient Temperature LMZ10505, V_{IN} = 3.3V, θ_{JA} = 20°C/W

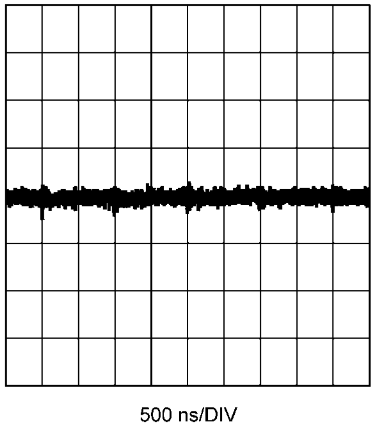


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FIGURE 11. Output Voltage Ripple
V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 3A, 4A, & 5A
LMZ10503 / LMZ10504 / LMZ10505

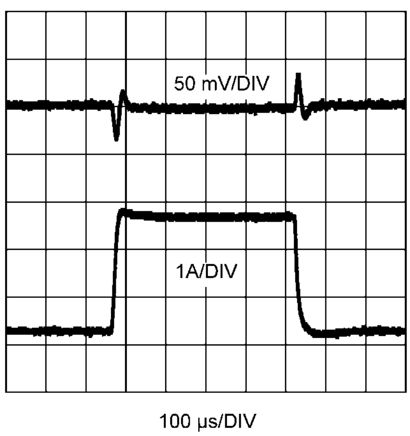

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FIGURE 12. Load Transient Response
V_{IN} = 5.0V, V_{OUT} = 2.5V
LMZ10503, I_{OUT} = 400 mA to 2.7A, 20 MHz Bandwidth Limit

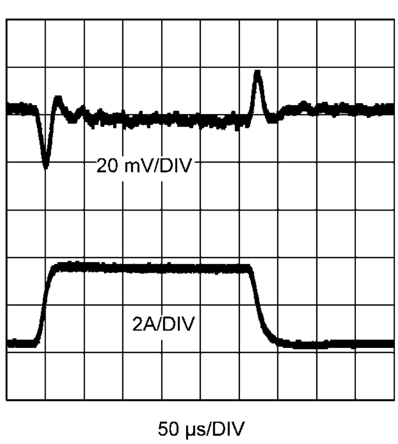

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FIGURE 13. Load Transient Response
V_{IN} = 5V, V_{OUT} = 2.5V
LMZ10504, I_{OUT} = 400 mA to 3.6A, 20 MHz Bandwidth Limit

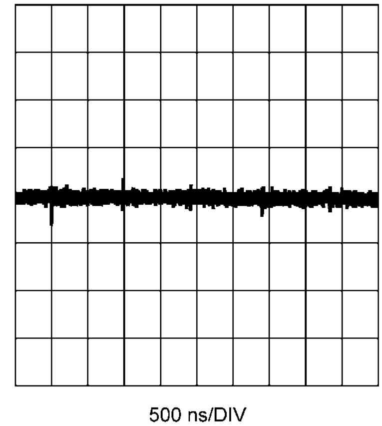

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FIGURE 14. Output Voltage Ripple
V_{IN} = 3.3V, V_{OUT} = 2.5V, I_{OUT} = 3A, 4A, & 5A
LMZ10503 / LMZ10504 / LMZ10505

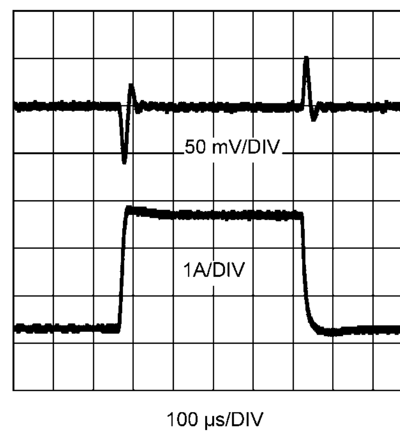

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FIGURE 15. Load Transient Response
V_{IN} = 3.3V, V_{OUT} = 2.5V
LMZ10503, I_{OUT} = 300 mA to 2.7A, 20 MHz Bandwidth Limit

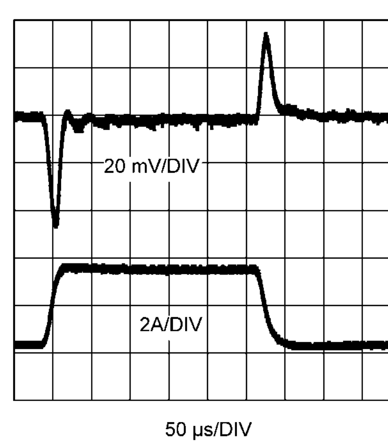

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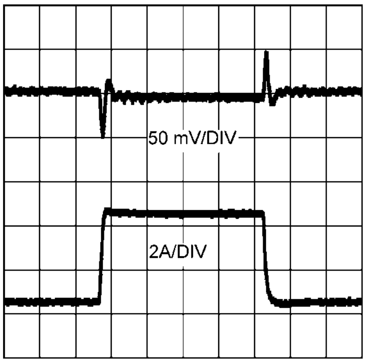
FIGURE 16. Load Transient Response
V_{IN} = 3.3V, V_{OUT} = 2.5V
LMZ10504, I_{OUT} = 400 mA to 3.6A, 20 MHz Bandwidth Limit



100 µs/DIV

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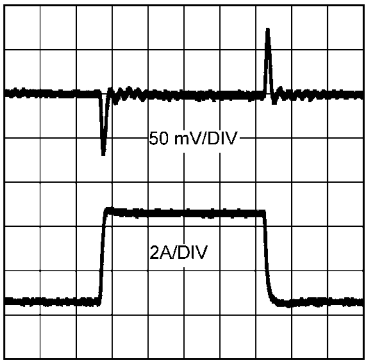
FIGURE 17. Load Transient Response
V_{IN} = 5.0V, V_{OUT} = 2.5V
LMZ10505, I_{OUT} = 500 mA to 4.5A, 20 MHz Bandwidth Limit



100 µs/DIV

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FIGURE 18. Load Transient Response
V_{IN} = 3.3V, V_{OUT} = 2.5V
LMZ10505, I_{OUT} = 500 mA to 4.5A, 20 MHz Bandwidth Limit

Circuit Example: Complies with EN55022 Class B Radiated Emissions

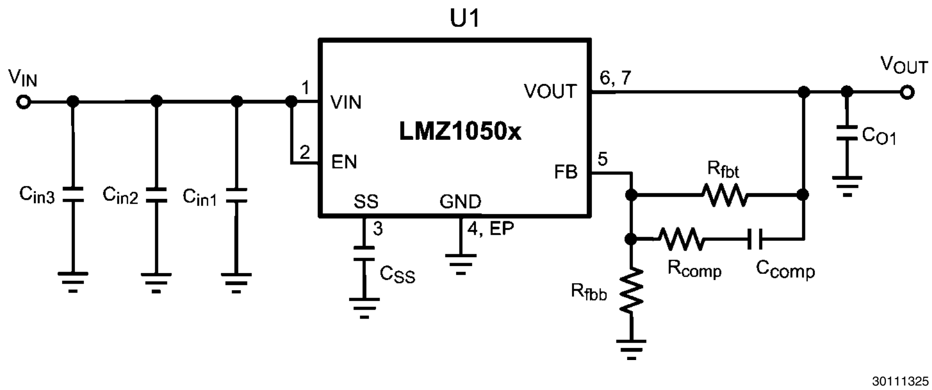

FIGURE 19. Component Schematic, V_{IN} = 5V, V_{OUT} = 2.5V, Complies with EN55022 Class B Radiated Emissions

TABLE 3. Bill of Materials

Designator	Description	Case Size	Manufacturer	Manufacturer P/N	Quantity
U1	SIMPLE SWITCHER®	TO-PMOD-7	National Semiconductor	LMZ10503/4/05TZ-ADJ	1
C_{in1}	1 µF, X7R, 16V	0805	TDK	C2012X7R1C105K	1
C_{in2}	4.7 µF, X5R, 6.3V	0805	TDK	C2012X5R0J475K	1
C_{in3}	47 µF, X5R, 6.3V	1210	TDK	C3225X5R0J476M	1
C_{O1}	100 µF, X5R, 6.3V	1812	TDK	C4532X5R0J107M	1
R_{fbt}	75 kΩ	0805	Vishay Dale	CRCW080575K0FKEA	1
R_{fbb}	34.8 kΩ	0805	Vishay Dale	CRCW080534K8FKEA	1
R_{comp}	1.1 kΩ	0805	Vishay Dale	CRCW08051K10FKEA	1
C_{comp}	180 pF, ±5%, C0G, 50V	0603	TDK	C1608C0G1H181J	1
C_{SS}	10 nF, ±5%, C0G, 50V	0805	TDK	C2012C0G1H103J	1

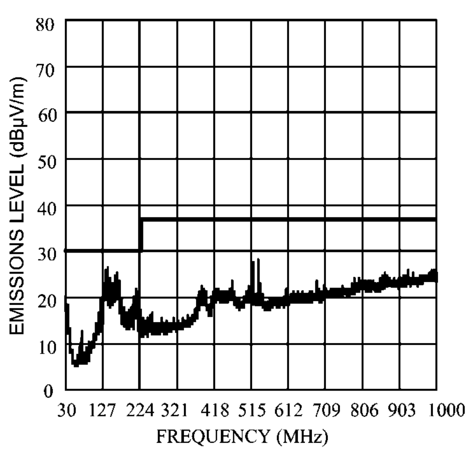

FIGURE 20. Radiated Emissions (EN55022, Class B)
V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 3A
Tested on LMZ10503 Evaluation Board

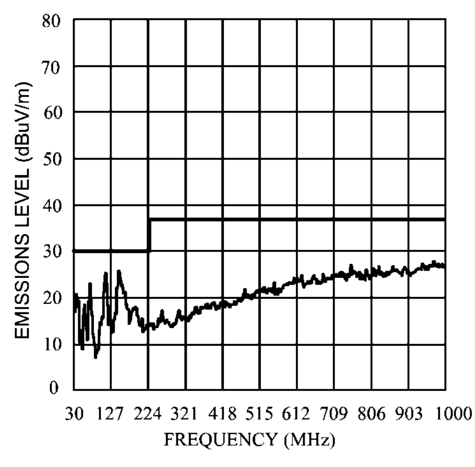

FIGURE 21. Radiated Emissions (EN55022, Class B)
V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 4A
Tested on LMZ10504 Evaluation Board

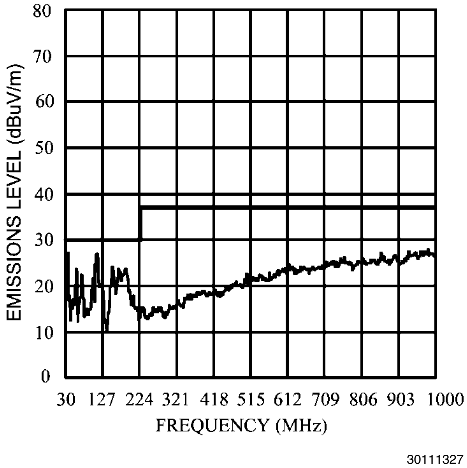

FIGURE 22. Radiated Emissions (EN55022, Class B)
V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 5A
Tested on LMZ10505 Evaluation Board

PCB Layout Diagram

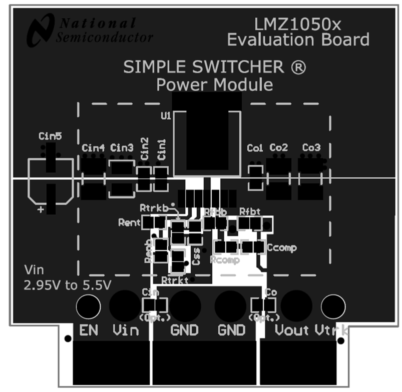

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FIGURE 23. Top Layer

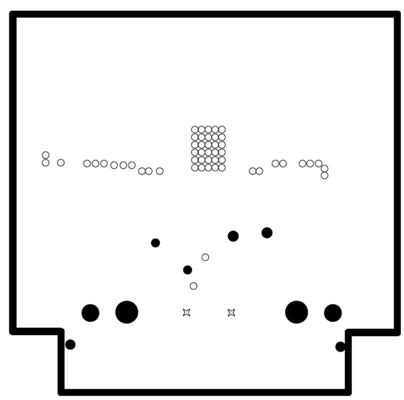

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FIGURE 24. Internal Layer I (Ground)

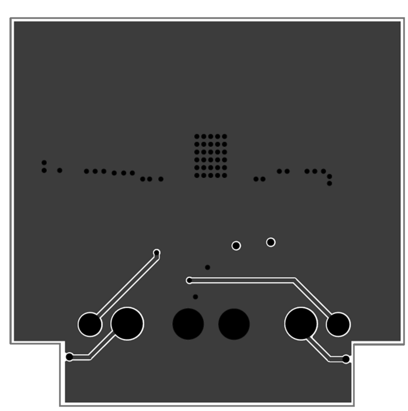

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FIGURE 25. Internal Layer II (Ground)

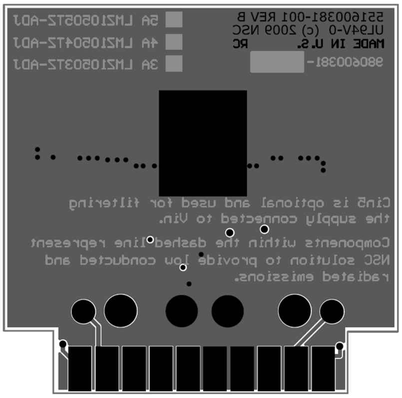

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FIGURE 26. Bottom Layer

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