

PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION

The M52340SP is a single-chip semiconductor integrated circuit to process signals of a color TV. Circuits to process video IF, sound IF, video, color, and deflection signals, a I²C bus control circuit, and D/A are build in this device.

This IC can be used not only for popular-type TV sets but also for middle-class TV sets. Combined with a SECAM chroma decoder, the M52325AP, this device can process signals of every type of TVs in the world by discriminating them fully automatically.

FEATURES

- A built-in I²C bus control circuit makes it possible to reduce the number of peripheral parts and rationalize production lines.
- Various filters (TRAP, BPF, Y-DL, RGB clamp) are build in this IC.
- PLL detection system is introduced to process video IF and voice IF. Furthermore, AFT coil is not necessary.
- DL aperture control
- Color signal frequency and vertical frequency of TVs of every type can be discriminated fully automatically.
- Horizontal/vertical countdown system
- V-pulse output
- RGB output

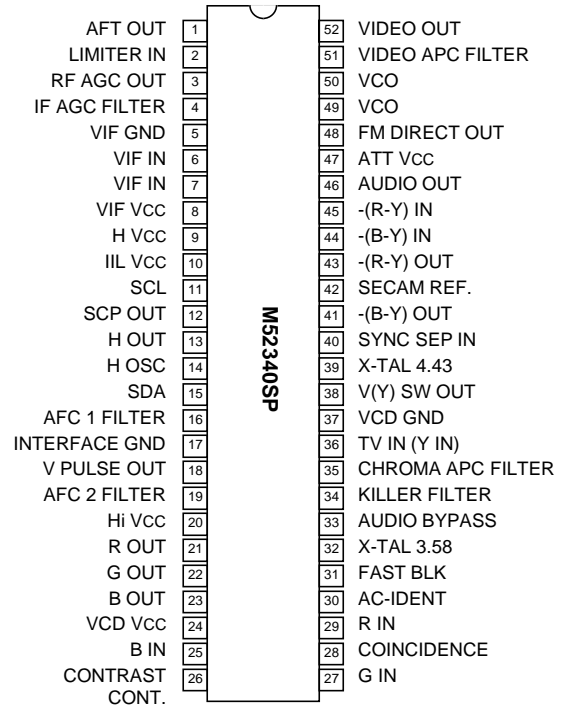
APPLICATION

PAL/NTSC system color TV

RECOMMENDED OPERATING CONDITION

Supply voltage	4.75V to 5.25V (pins 8 and 24)
	7.6V to 8.4V (pins 9, 20, and 47)
Rated supply voltage	5.0V (pins 8 and 24)
	8.0V (pins 9, 20, and 47)
Maximum output current	5.0mA (pin 18)
	5.0mA (pin 13)

PIN CONFIGURATION (TOP VIEW)

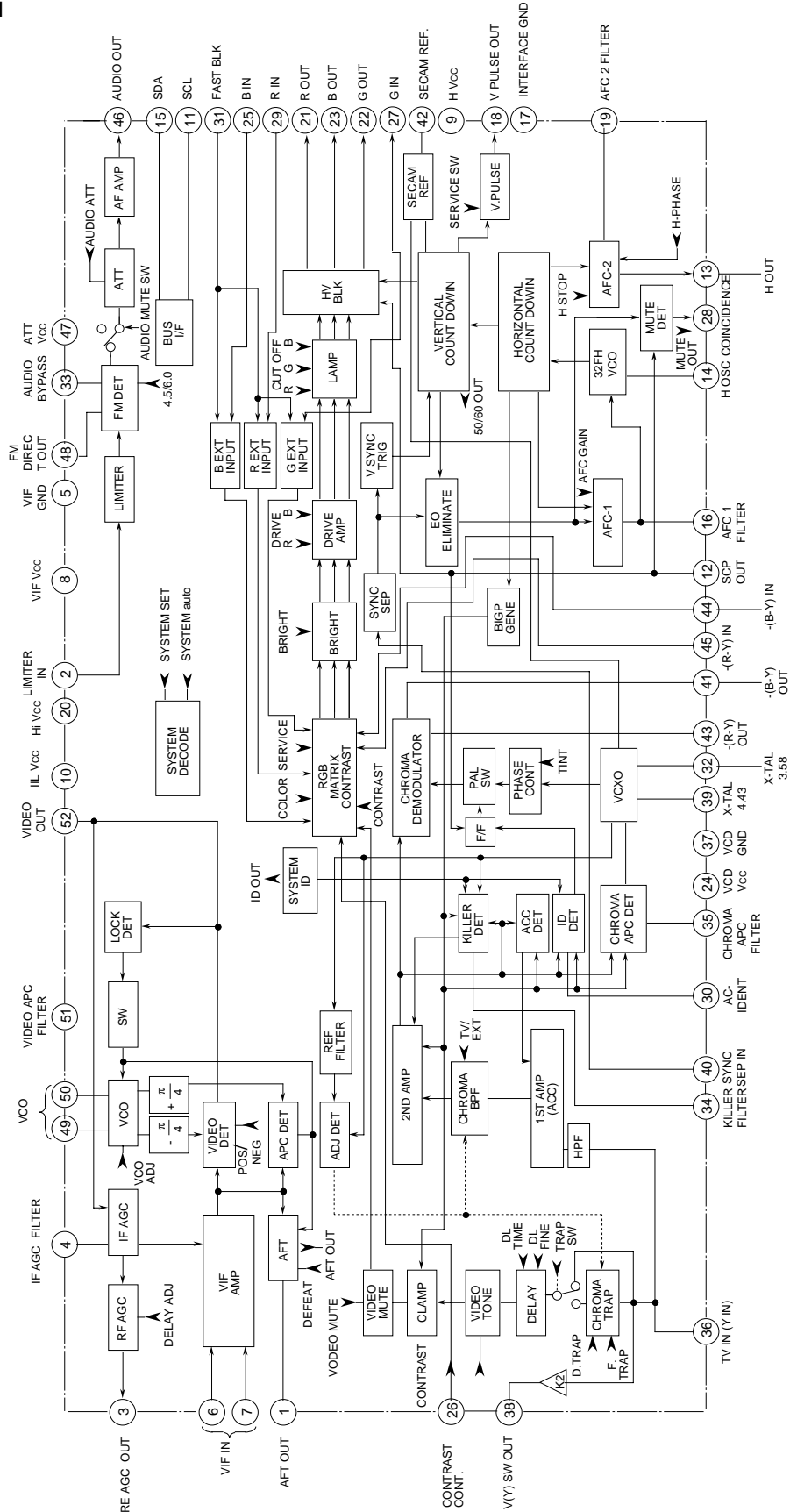


Outline 52P4B

NC : NO CONNECTION

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BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Ta=25 °C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V _{cc}	Supply voltage	5.0, 8.0	V
P _d	Power dissipation	1.4	W
T _{opr}	Operating temperature	-20 to 65	°C
T _{stg}	Storage temperature	-40 to 150	°C
Surge	Electrostatic discharge	±200 (-150 for only minus side of pin 18)	V

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ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Input signal Input pin	SW conditions PIN conditions	S 2	S 4	S P	S 16	S 31	S P	S 40	S P	S 13	S 16	S 18	S 21	S 22	S 23	S 26	S 36	S 38	S 40	S 41	S 43	S 46	S 48	S 52	S 58	S 59	Vcc				Limits			Unit																									
																													Test conditions		P	P	P	P	P		P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	Min.	Typ.	Max.
																													SW conditions																																
	Standard conditions of circuit current		SW	1	1	1	1	1	1	0	0															5V	8V	8V	5V	8V																															
Icc8	Pin 8 current		PIN																								M					20.0	27.0	33.0		mA																									
Icc9	Pin 9 current		PIN																												12.0	18.0	24.0		mA																										
Icc20	Pin 20 current		PIN																												9.0	15.0	21.0		mA																										
Icc24	Pin 24 current		PIN																												55.0	80.0	105.0		mA																										
Icc47	Pin 47 current		PIN																											1.4	2.0	2.4		mA																											
	VIF block																																																												
—	Standard conditions of IF parameters		SW	1	1	1	1	1	1	0	0																																																		
Vdc NEG	Video detector output DC voltage (NEG)		PIN																												4.8	5.2	5.5		V																										
Vdc POS	Video detector output DC voltage (POS)		PIN																												2.1	2.3	2.5		V																										
Vo NEG	Video detector output (NEG)	V	SG1	0	0																										1.9	2.2	2.5		V																										
Vo POS	Video detector output (POS)	V	SG2	0	0																										1.9	2.2	2.5		V																										
P/N	Video S/N	V	SG3	0	0																										50	55	—		dB																										
Vf	Video frequency characteristics	V	SG4	0	0																										4.5	5.5	—		MHz																										
Vin min	Input sensitivity	V	SG5	0	0																										—	47	52		dBμ																										
Vin max	Maximum permissible Input	V	SG6	0	0																										102	107	—		dBμ																										
GR	AGC control range	—																													50	60	—		dBμ																										
V4H	Maximum IF AGC voltage	—																													4.0	4.4	4.8		V																										
V4T	IF AGC voltage (80dBu)	V	SG7	0	0																										2.6	3.0	3.4		V																										

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ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Input signal		SW conditions	Test conditions																	Limits								
					Input pin	SG name conditions	Vcc																	Min.	Typ.	Max.	Unit			
							S	S	S	S	S	S	S	S	S	P	P	P	P	P	P	P	P					P	P	P
V4L	Minimum IF AGC voltage	V	SG8	SW																				1.9	2.3	2.7	V			
V1	AFT defeat voltage			PIN	M																			3.7	4.0	4.3	V			
μAFT N	AFT detector sensitivity (NEG)	V	SG9	SW	0																			43	61	79	kHz/mV			
V1H N	Maximum AFT voltage (NEG)	V	SG10	SW	PIN	M																		7.2	7.7	—	V			
V1L N	Minimum AFT voltage (NEG)	V	SG11	SW	PIN	M																		—	0.3	0.8	V			
V3H	Maximum RF AGC voltage	V	SG3	SW	PIN	M																		7.2	7.7	—	V			
V3L	Minimum RF AGC voltage	V	SG3	SW	PIN	M																		—	0.3	0.8	V			
CRU	Capture range (U)	V	SG9	SW	PIN																M			0.8	1.2	—	MHZ			
CRL	Capture range (L)	V	SG9	SW	PIN																M			2.2	2.6	—	MHZ			
CRT	Capture range (T)	—	—	SW	PIN																			3.0	3.8	—	MHZ			
IM	Intermodulation	V	SG12	SW	PIN																M			31	36	—	dB			
DG	DG	V	SG13	SW	PIN																M			—	3	7	%			
DP	DP	V	SG13	SW	PIN																M			—	3	7	deg			
SPN	Sync ratio (NEG)	V	SG13	SW	PIN																M			25.0	28.5	32.0	%			
DLPH	Maximum delay point (NEG/POS)	V	SG14	SW	PIN	M																		90	96	—	dBμ			
DLPL	Minimum delay point (NEG/POS)	V	SG15	SW	PIN	M																		—	70	76	dBμ			
SIF block																														
—	Standard conditions of SIF parameters	—	—	SW	0	1	1	1	1	1	0	0																		
VAF	AF output DC voltage	—	—	PIN																				5V	8V	8V	5V	8V		
		—	—	SW																					2.4	2.8	3.2	V		

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ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test conditions																				Limits			Unit		
		Input signal		SW conditions		S		S		S		S		S		S		S		Min.	Typ.	Max.					
		Input pin	SG name conditions	SW conditions	PIN conditions	2	4	16	31	40	44	45	18	21	22	23	26	36	40				41	43		46	48
APC1	APC pull-in range 1	V1	VS4P	SW	PIN																±400	±700	—	Hz			
R/BP	Demodulated output ratio (R-Y/B-Y)	V1	VS4P	SW	PIN																0.45	0.6	0.75	ratio			
θ _{R-Y} P	Demodulated phase angle θ _{R-Y}	V1	VS4P	SW	PIN																80	90	100	deg			
CC	Carrier leak at demodulated output	V1	VS4P	SW	PIN																0	50	100	mV _{P-P}			
DDH	Difference of demodulated output on line	V1	4.2M SIN wave	SW	PIN																—	—	100	mV			
Cn3	Standard chroma output 3	V1	SS3N	SW	PIN																500	700	900	mV _{P-P}			
Cn4	Standard chroma output 4	V1	SS3N	SW	PIN																490	600	750	mV _{P-P}			

Chroma block (NTSC)

Symbol	Parameter	Test conditions																				Limits			Unit
		Input signal		SW conditions		S		S		S		S		S		S		S		Min.	Typ.	Max.			
		Input pin	SG name conditions	SW conditions	PIN conditions	2	4	16	31	40	44	45	18	21	22	23	26	36	40				41	42	
VikN	Killer operating input level (NTSC)	V1	VS3N	SW	PIN																	—	-45	-38	dB
killN	Killer color residual (NTSC)	V1	VS3N	SW	PIN																	0	30	60	mV _{P-P}
APC2	APC pull-in range 2	V1	VS3N	SW	PIN																±400	±600	—	Hz	
R/BN	Demodulated output ratio R-Y/B-Y	V1	VS3N	SW	PIN																0.4	0.6	0.8	ratio	
θ _{R-Y} N	Demodulated phase angle θ _{R-Y}	V1	VS3N	SW	PIN																80	95	110	deg	
TC1	TINT control characteristic 1	V1	VS3N	SW	PIN																25	45	60	deg	
TC2	TINT control characteristic 2	V1	VS3N	SW	PIN																25	45	60	deg	
SRA	SECAM REF output AC voltage	—	—	SW	PIN																180	300	420	mV _{P-P}	
SRD	SECAM REF output DC voltage	—	—	SW	PIN																4.0	4.5	5.0	V	

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ELECTRICAL CHARACTERISTICS TEST METHOD

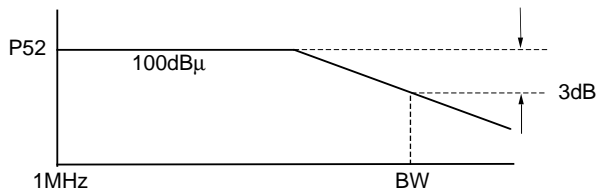
P/N Video S/N

1. Input SG3 and measure the rms value of output signal at pin 52.
2. P/N is defined as follows:

$$P/N = 20 \log \frac{V_{\text{ONEG Measured Value}}(V_{P-P}) \times 10^3}{\text{Measured Value}(mV_{\text{rms}})} \quad (\text{dB})$$

BW Video frequency characteristics

1. Input SG4 and set the frequency f_2 to 37.9MHz so that the beat element of 1MHz is output to pin 52.
2. Then set the applied voltage at pin 4 so that the beat element of 1MHz at pin 52 may be 100dB μ .
3. Decrease f_2 to the level at which the beat element becomes 3dB smaller than the element of 1MHz, and read the value at that level.



Vin min. Input sensitivity

1. Decrease SG5 level until the video detector output is 3dB smaller than the measured value of Parameter V3 "Video detector output".

Vin max. Maximum permissible input

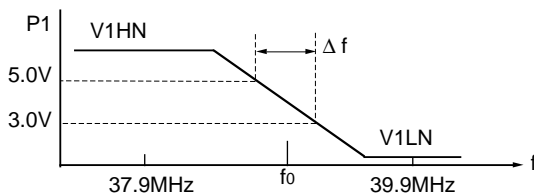
1. Input 90dBu SG6.
2. VA is the output level at pin 52. Increase SG6 voltage until the output at pin 52 becomes 3dB smaller than VA. The input level at that time is the maximum permissible input.

μ AFTN AFT detector sensitivity (NEG)

V1HN Maximum AFT voltage (NEG)

V1LN Minimum AFT voltage (NEG)

See the following figure.

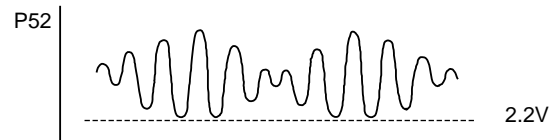


μ AFTN is defined as follows:

$$\mu\text{AFTN} = \frac{(5.0-3.0) \times 10^3 \text{ mV}}{\Delta f \text{ KHz}} \quad (\text{mV/KHz})$$

IM Intermodulation

1. Adjust the applied voltage at pin 4 so that the lowest output signal voltage at pin 52 is 2.2V.



2. Measure elements of 1.07MHz and 4.43MHz of output at pin 52.
3. IM is defined as follows:

$$IM = 20 \log \frac{\text{Element of 1.07MHz}}{\text{Element of 4.43MHz}} \quad (\text{dB})$$

ATT Maximum attenuation

1. Measure the element of 400Hz of output at pin 46.
2. ATT is defined as follows:

$$ATT = 20 \log \frac{V_{0AF\text{max}}}{\text{Measured value}} \quad (\text{dB})$$

LIM Input limiting sensitivity

Decrease the input level of SG18. Measure the input level when the element of 400Hz at pin 46 is 3dB smaller than V_{0AFM} (S6:Maximum AF output (6.0M)).

AMR AMR

1. V_{am} is the element of 400Hz at pin 46.
2. AMR is defined as follows:

$$AMR = 20 \log \frac{V_{0AFS}(mV_{\text{rms}})}{V_{am}(mV_{\text{rms}})} \quad (\text{dB})$$

AF S/N AF S/N

1. Measure the noise (20Hz to 100KHz) of output at pin 46.
2. AF S/N is defined as follows:

$$AF \text{ S/N} = 20 \log \frac{V_{0AF\text{max}}}{\text{Measured value}} \quad (\text{dB})$$

Cn1 Standard chroma output 1 (PAL)

Cn2 Standard chroma output 2 (PAL)

1. Input SS4P to VI IN.
2. Measure output amplitude, Cn1 and Cn2, at pins 41 and 43 respectively.

ACC1 ACC characteristics 1

1. Input VS4P (eb=570mV:level+6dB) to VI IN.
2. Measure the output amplitude at pin 41.
3. ACC1 is defined as follows:

$$ACC1 = 20 \log \frac{\text{Measured value } (V_{P-P})}{Cn1 (V_{P-P})} \quad (\text{dB})$$

ACC2 ACC characteristics 2

1. Input VS4P (input level:-20dB) to VI IN.
2. Measure the output amplitude at pin 41.
3. ACC2 is defined as follows:

$$ACC2 = 20 \log \frac{\text{Measured value } (V_{P-P})}{Cn1 (V_{P-P})} \quad (\text{dB})$$

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OL Overload characteristics

1. Input VS4P (ec=800mV_{P-P}:chroma+3dB) to VI IN.
2. Measure the output amplitude at pin 41.
3. OL is defined as follows:

$$OL = 20 \log \frac{\text{Measured value (V}_{P-P})}{C_{n1} (V_{P-P})} \text{ (dB)}$$

VikP Killer operating input level (PAL)

1. Input VS4P (level:variable) to VI IN at input level 0dB.
2. Lower the input level with monitoring the output amplitude at pin 41 and measure the input level when output amplitude is not found.

KilIP Killer color residual (PAL)

1. Input VS4P (level:-40dB) to VI IN.
2. Measure the output amplitude at pin 41.

APC1 APC pull-in range 1

1. Input VS4P (f=eb=ec=variable) to VI IN.
2. Change the input signal frequency and measure the frequency range from the point at which signal is output to pin 41 and to the point that no signal is output to the pin. The reference value is 4.433619MHz.

R-Y/B-YP Demodulation output ratio

1. Input VS4P (eb=single chroma=ec+50KHz) to VI IN.
2. V41 is the output amplitude at pin 41.
3. V43 is the output amplitude at pin 43.
4. R-Y/B-YP is defined as follows:

$$R-Y/B-YP = 20 \log \frac{V_{43} (V_{P-P})}{V_{41} (V_{P-P})} \text{ (dB)}$$

R-YP Demodulated phase angle

1. Input VS4P (eb=single chroma=ec+50KHz) to VI IN.
2. V41 is the output amplitude at pin 41.
3. V43 is the output amplitude at pin 43.
4. R-YP is defined as follows:

$$q \text{ R-YP} = \tan^{-1} \frac{V_{43} \times 3.8}{(V_{41} \times 1.9) + 45^\circ} \text{ (deg)}$$

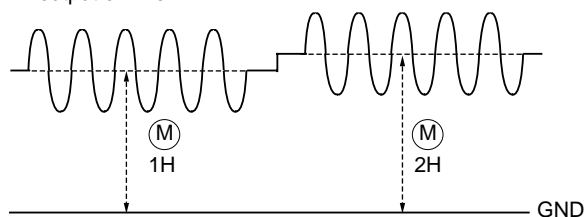
* Vector should be found with taking the gain ratio of a demodulator into consideration.

CC Demodulated output carrier leak

Measure the element of 4.43MHz of the demodulated output in no-input state.

DDH Difference of demodulated output on line

1. Input 4.2MHz CW (Vi=575mV_{P-P}) to VI IN.
2. Measure the center DC voltage of output beat amplitude for two lines at pins 41 and 43. The absolute value of the difference in DC voltage is the difference of demodulated output on line.

**Cn3,Cn4 Standard chroma output 3,4 (NTSC)**

1. Input SS3N to VI IN
2. Cn3 and Cn4 are output amplitude measured at pins 41 and 43 respectively.

VikN Killer operating input level (NTSC)

1. Input VS3N (level:variable) to VI IN at input level 0dB.
2. Lower the input level with monitoring the output amplitude at pin 41 and measure the input level when output amplitude is not found.

KilIN Killer color residual (NTSC)

1. Input VS3N (level:-40dB) to VI IN.
2. Measure the output amplitude at pin 41.

APC2 APC pull-in range 2

1. Input VS3N (f=eb=ec=variable) to VI IN.
2. Change the input signal frequency and measure the frequency range from the point at which no signal is output to pin 41 and to the point at which signal is output to the pin. (Pull-in state) The reference value is 3.579545MHz.

R-Y/B-YN Demodulated output ratio

1. Input VS3N (eb=single chroma=ec+50KHz) to VI IN.
2. V41 is the output amplitude at pin 41.
3. V43 is the output amplitude at pin 43.
4. R-Y/B-YN is defined as follows:

$$R-Y/B-YN = 20 \log \frac{V_{43} (V_{P-P})}{V_{41} (V_{P-P})} \text{ (dB)}$$

q R-YN Demodulated phase angle

1. Input VS3N (eb=single chroma=ec+50KHz) to VI IN.
2. V41 is the output amplitude at pin 41.
3. V43 is the output amplitude at pin 43.
4. R-YN is defined as follows:

$$q \text{ R-YP} = \tan^{-1} \frac{V_{43} \times 3.8}{(V_{41} \times 1.9) + 45^\circ} \text{ (deg)}$$

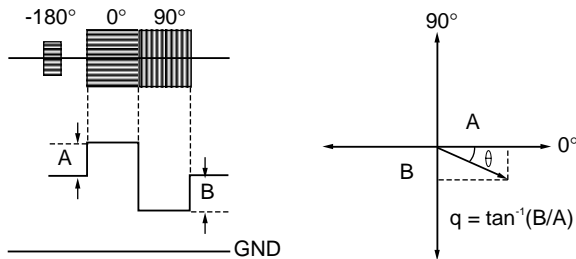
* Vector should be found with taking the gain ratio into consideration.

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TC1 Tint control characteristics 1

TC2 Tint control characteristics 2

1. Input VS3N (see the following figure) to VI IN. Based on the output voltage at pin 41, find the absolute angle as shown in the above figure.



2. Tint data center (63) is defined as the reference angle (TC). Find angles at tint data max. and tint data min. TC1 and TC2 are differences in angle between TC_{MAX} and TC and between TC_{MIN} and TC and defined as follows.
 $TC1 = TC_{MAX} - TC$ (deg)
 $TC2 = TC - TC_{MIN}$ (deg)

SRA SECAM REF output AC voltage

SRD SECAM REF output DC voltage

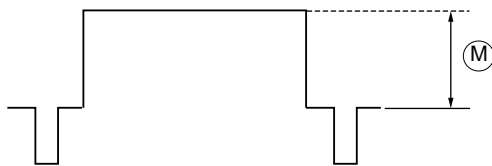
Measure the amplitude (SRA) and DC voltage (SRD) of the element of 4.43MHz of output at pin 42.

AUTO 1 to 6 System confirmation 1 to 6

Set to AUTO mode and confirm that bus for each output signal is read correctly.

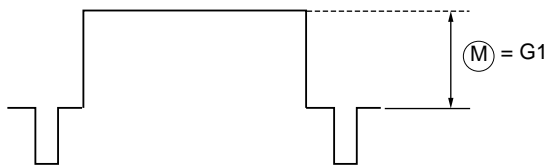
Ymax Maximum video output

1. Input SGA to VI IN
2. Measure the amplitude (P-P) except that at blanking part of output at pins 21,22 and 23. This amplitude is defined as G1.



GY Video Standard video output

1. Input SGA to VI IN
2. Measure the amplitude (P-P) except that at blanking part of output at pins 21,22 and 23. This amplitude is defined as G1.



3. GY is defined as follows:
 $GY = 20 \log (G1V_{P-P}/0.714V_{P-P})$ (dB)

BW Video frequency characteristics

1. Input SGB (5MHz, 0.4V_{P-P}) to VI IN.
2. Measure the amplitude (P-P) except that at blanking part of the output at pin 22. The amplitude is defined as YB.
3. BW is defined as follows:
 $BW = 20 \log (YB V_{P-P}/GY V_{P-P})$ (dB)

2AGY Standard double-width amplifier output

1. Input SGA to VI IN.
2. Measure the amplitude (P-P) except that at blanking part of output at pin 22.

CTR1 Chroma trap attenuation 1 (common to R/G/B output)

1. Input SS3N to VI IN. Measure the frequency level of 3.58MHz at trap data 0. The level is defined as No.
2. Then, measure the level at trap data 1.
3. CTR1 is defined as follows.
 $CTR1 = 20 \log \frac{\text{Measured value (mV}_{P-P})}{N_0 \text{ (mV}_{P-P})}$ (dB)

TRF1 Trap fine adj. attenuation 1 (common to R/G/B output)

1. Input SS3N to VI IN.
2. Measure the output amplitude of the element of 3.58MHz when trap fine adj. switch is on. (TRFon)
3. TRF1 is defined as follows.
 $TRF1 = 20 \log \frac{\text{TRFon (mV}_{P-P})}{N_0 \text{ (mV}_{P-P})}$ (dB)

DTR1 D. trap attenuation 1 (common to R/G/B output)

1. Input SS3N to VI IN.
2. Measure the output amplitude of the element of 3.58MHz when D. trap switch is on. (DTRon)
3. DTR1 is defined as follows.
 $DTR1 = 20 \log \frac{\text{DTRon (mV}_{P-P})}{N_0 \text{ (mV}_{P-P})}$ (dB)

CTR2 Chroma trap attenuation 2 (common to R/G/B output)

1. Input SS4P to VI IN and measure the frequency level of 4.43MHz at trap data 0. The level is defined as P₀.
2. Then, measure the level at trap data 1.
3. CTR2 is defined as follows.
 $CTR2 = 20 \log \frac{\text{Measured value (mV}_{P-P})}{P_0 \text{ (mV}_{P-P})}$ (dB)

TRF2 Trap fine adj. attenuation 2

1. Input SS4P to VI IN.
2. Measure the output amplitude of the element of 4.43MHz when trap fine adj. switch is on. (TRFon)
3. TRF2 is defined as follows.
 $TRF2 = 20 \log \frac{\text{TRFon (mV}_{P-P})}{P_0 \text{ (mV}_{P-P})}$ (dB)

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DTR2 D. trap attenuation 2

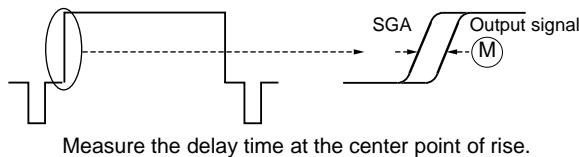
1. Input SS4P to VI IN.
2. Measure the output amplitude of the element of 4.43MHz when D. trap switch is on. (DTRon)
3. DTR2 is defined as follows.

$$DTR2 = 20 \log \frac{DTRon (mVP-P)}{P_0 (mVP-P)} \text{ (dB)}$$

Note: In parameters Y5, Y6, Y8 and Y9, limits are defined based on the maximum attenuation by comparing each one.

YDL1 YDL value 1

1. Input SGA to VI IN.
2. Measure the delay time from signal input to output at pins 21, 22 and 23.

**YDL2, 3 and 4 YDL value 2, 3 and 4.**

1. Input SGA to VI IN.
2. Measure the delay time from signal output at pins 21, 22 and 23 to YDL1.

GTnor Video tone 1

1. Input SGB (f=3MHz) to VI IN.
2. Measure output amplitude at pins 21, 22 and 23.

GTmax Video tone 2

1. Input SGB (f=3MHz) to VI IN.
2. Measure output amplitude at pins 21, 22 and 23.
3. GTmax is defined as follows:

$$GTmax = 20 \log \frac{\text{Measured value (VP-P)}}{GTnor (VP-P)} \text{ (dB)}$$

GTmin Video tone 3

1. Input SGB (f=3MHz) to VI IN.
2. Measure output amplitude at pins 21, 22 and 23.
3. GTmin is defined as follows:

$$GTmin = 20 \log \frac{\text{Measured value (VP-P)}}{GTnor (VP-P)} \text{ (dB)}$$

GT2M Video tone 4

1. Input SGB (f=2MHz) to VI IN.
2. Measure output amplitude at pins 21, 22 and 23.
3. GT2M is defined as follows:

$$GT2M = 20 \log \frac{\text{Measured value (VP-P)}}{GTnor (VP-P)} \text{ (dB)}$$

GT5M Video tone 5

1. Input SGB (f=5MHz) to VI IN.
2. Measure output amplitude at pins 21, 22 and 23.
3. GT5M is defined as follows:

$$GT5M = 20 \log \frac{\text{Measured value (VP-P)}}{GTnor (VP-P)} \text{ (dB)}$$

GYnor Contrast characteristics 1

1. Input SGB (f=100KHz) to VI IN.
2. Measure output amplitude at pins 21, 22 and 23.

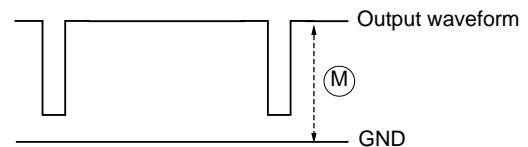
GYmin Contrast characteristics 2

1. Input SGB (f=100KHz) to VI IN.
2. Measure output amplitude at pins 21, 22 and 23.
3. GYmin is defined as follows:

$$GYmin = 20 \log \frac{\text{Measured value (VP-P)}}{GYnor (VP-P)} \text{ (dB)}$$

Lum nor Brightness control characteristics 1**Lum max Brightness control characteristics 2****Lum min Brightness control characteristics 3**

1. No signal is input. (Only SG50 is input to SY IN.)
2. Measure DC voltage of output at pins 21, 22 and 23 except that at blanking part.

**D(R) Drive control characteristics R**

1. Input SGA to VI IN.
2. Measure DRmin and DRmax which are output amplitude at pin 21 at D(R) data min and D(R) data max respectively.
3. D(R) is defined as follows:

$$D(R) = 20 \log \frac{DRmax(VP-P)}{DRmin (VP-P)} \text{ (dB)}$$

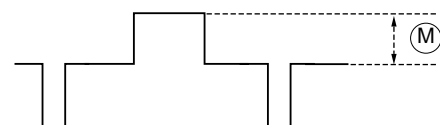
D(B) Drive control characteristics B

1. Input SGA to VI IN.
2. Measure DBmin and DBmax which are output amplitude at pin 23 at D(B) data min and D(B) data max respectively.
3. D(B) is defined as follows:

$$D(B) = 20 \log \frac{DBmax(VP-P)}{DBmin (VP-P)} \text{ (dB)}$$

EXR EXT(R) I/O characteristics**EXG EXT(G) I/O characteristics****EXB EXT(B) I/O characteristics**

1. Input SGD to FB, ER, EG and EB.
2. Measure output amplitude which is higher than the pedestal level at pins 21, 22 and 23. The amplitude at blanking part should not be measured.



PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

OFRG Offset voltage between R and G

OFBG Offset voltage between B and G

1. Measure DC voltage of output at pins 21,22 and 23 except that at blanking part.
2. OFRG and OFBG are defines as follows:
 OFRG =
 (pin 21 Measured voltage)-(pin 22. Measured voltage) (mV)
 OFBG =
 (pin 23 Measured voltage)-(pin 22 Measured voltage) (mV)

R(C) R cutoff characteristics

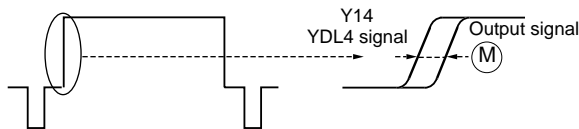
G(C) G cutoff characteristics

B(C) B cutoff characteristics

1. Measure DC voltage of output at pins 21,22 and 23 when R(C), G(C) and B(C) data are maximum and minimum respectively. The DC voltage at blanking part should be measured.
2. R(C), G(C) and B(C) are defined as follows:
 R(C), G(C), and B(C) =
 (Voltage at data max.) - (Voltage at data min.) (V)

DLF DL fine delay

1. Input SGA to VI IN.
2. Measure the time lag (absolute value) between signal YDL4 and output signal at pins 21,22 and 23.



Measure the time lag at the center point of rise

Ccon1 Color control characteristics 1

Ccon2 Color control characteristics 2

1. Input SGE to -R IN (pin 45).
2. Measure output amplitude at pins 21,22 and 23 under each condition.

VMF Video mute characteristics

1. Input SGF to VI IN.
2. Measure output amplitude of the element of 4.43MHz when the mute switch is on and off. (VMFon, VMFoff)
3. VMF is defined as follows:

$$VMF = 20 \log \frac{TRF_{on} (V_{P-P})}{TRF_{off} (V_{P-P})} \text{ (dB)}$$

MTXB Matrix characteristics 1

MTXG Matrix characteristics 2

1. Input SGE to -B IN (pin 44).
2. Measure output amplitude at pins 22 and 23.
 (P23 = MTXB, P22 = MTXG)

MTXR Matrix characteristics 3

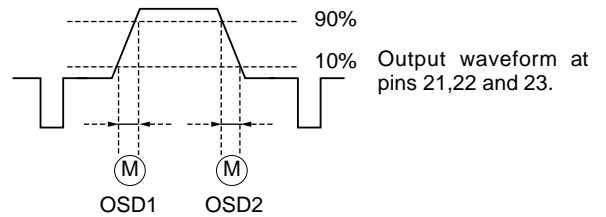
MTXG1 Matrix characteristics 4

1. Input SGE to -R IN (pin 45).
2. Measure output amplitude at pins 21 and 22.
 (P21 = MTXR, P22 = MTXG1)

OSD1 OSD speed characteristics 1

OSD2 OSD speed characteristics 2

1. Input SGD to FB, ER, EG and EB.
2. Measure rise time and fall time of the signal of output at pins 21,22 and 23. Measurement points should be higher than the pedestal level and blanking part should not be measured.



GYmax1 Contrast control characteristics 3

GYmin1 Contrast control characteristics 4

1. Input SGA to VI IN.
2. Measure output amplitude at pins 21,22 and 23 when 2.9V and 0V are externally applied to pin 26.

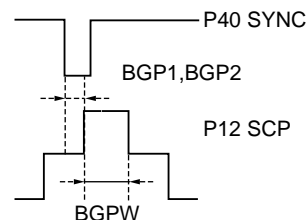
ISS Sync separation input sensitivity current

Make current flow out from pin 40 and measure the flow current when the burst gate pulse is not found at pin 12.

BGP1 BGP timing 1

BGP2 BGP timing 2

BGPW BGP pulse width



FH Horizontal free run frequency

Measure the output frequency at pin 13 when no signal is input.

FPH1 Horizontal pull-in range 1

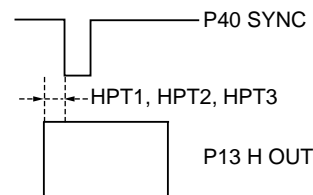
FPH2 Horizontal pull-in range 2

Change the frequency of SGc and measure the frequency at the moment when the output signal at pin 13 and the input signal at pin 40 are pulled in. The horizontal pull-in range is measured by comparing with the horizontal free run frequency.

HPT1 Horizontal pulse timing 1

HPT2 Horizontal pulse timing 2

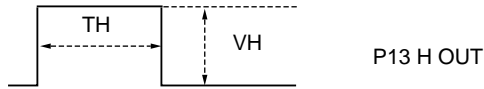
HPT3 Horizontal pulse timing 3



PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

TH Horizontal pulse width

VH Horizontal pulse amplitude



HSTO Horizontal stop operation

Confirm that the horizontal output is high when the horizontal stop switch is on.

AFCG AFG gain operation

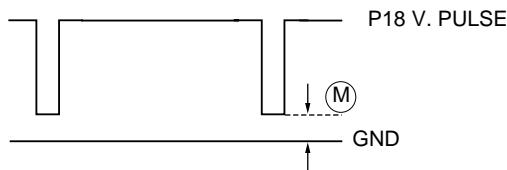
1. Measure AFCOn which is the output amplitude of pin 16 when AFC switch is on and AFCoff which is that when the switch is off.
2. AFCG is defined as follows:

$$AFCG = 20 \log \frac{AFC_{on} (V_{P-P})}{AFC_{off} (V_{P-P})} \text{ (dB)}$$

FV Vertical free run frequency

Measure the output frequency at pin 18 when no signal is input.

VVL Minimum vertical output voltage



CoinL Minimum coincidence detection voltage

Measure the output DC voltage at pin 28 when no signal is input.

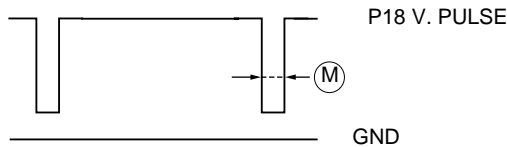
SW Service SW operation

Measure the output DC voltage at pin 18 when the service switch is on.

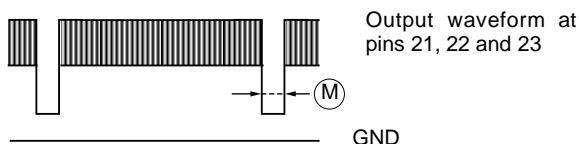
FPV Vertical pull-in range

Decrease the frequency of SGd and measure the frequency when output waveform at pin 18 is pulled in.

VVL Vertical pulse width



VBLKW Vertical BLK width



AVER1 50/60 confirmation 1

AVER2 50/60 confirmation 2

AVER3 50/60 confirmation 3

AVER4 50/60 confirmation 4

Confirm that the frequency of output at pin 18 is the same at each input frequency (pull-in state). Also, confirm the state of the bus write mode (D7).

WVSS Minimum sync detection width

Reduce the width of signal SGd and measure the width of input signal when the output waveform at pin 18 disappears.

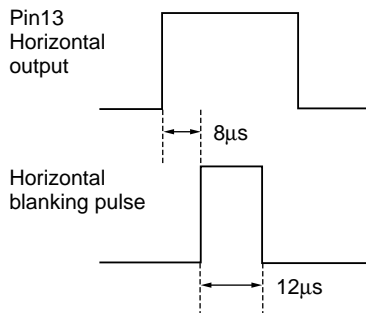
PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

INPUT SIGNAL

VIF/SIF

SG. No.	Input signal (Value at pin terminal is 50Ω)
SG. 1	$f_0 = 38.9\text{MHz}$, 90dBμ, $f_m = 20\text{KHz}$, AM77.8%
SG. 2	$f_0 = 38.9\text{MHz}$, 90dBμ, $f_m = 50\text{KHz}$, AM77.8%
SG. 3	$f_0 = 38.9\text{MHz}$, 80dBμ, CW
SG. 4	$f_1 = 45.75\text{MHz}$, 90dBμ, CW $f_2 = 44\pm 5\text{MHz}$, 90dBμ, CW } Mixed signal
SG. 5	$f_0 = 38.9\text{MHz}$, Variable, $f_m = 20\text{KHz}$, AM77.8%
SG. 6	$f_0 = 38.9\text{MHz}$, $f_m = 20\text{KHz}$, AM16%, Level variable
SG. 7	$f_0 = 38.9\text{MHz}$, 80dBμ, CW
SG. 8	$f_0 = 38.9\text{MHz}$, 110dBμ, CW
SG. 9	$f_0 = 38.9 \pm 5\text{MHz}$, 90dBμ, CW
SG. 10	$f_0 = 37.9\text{MHz}$, 90dBμ, CW
SG. 11	$f_0 = 39.9\text{MHz}$, 90dBμ, CW
SG. 12	$f_1 = 38.9\text{MHz}$, 90dBμ, CW $f_2 = 34.47\text{MHz}$, 80dBμ, CW $f_3 = 33.4\text{MHz}$, 80dBμ, CW } Mixed signal
SG. 13	$f_0 = 38.9\text{MHz}$, Standard 10-step modulation, Sync ratio:28.6%, AM = 87.5% video modulation, Sync chip level 90dBμ
SG. 14	$f_0 = 38.9\text{MHz}$, 93dBμ, CW
SG. 15	$f_0 = 38.9\text{MHz}$, 73dBμ, CW
SG. 16	$f_0 = 4.5\text{MHz}$, 100dBμ, $f_m = 400\text{Hz}$, FM±25KHz dev
SG. 17	$f_0 = 5.5\text{MHz}$, 100dBμ, $f_m = 400\text{Hz}$, FM±50KHz dev
SG. 18	$f_0 = 6.0\text{MHz}$, 100dBμ, $f_m = 400\text{Hz}$, FM±50KHz dev
SG. 19	$f_0 = 6.5\text{MHz}$, 100dBμ, $f_m = 400\text{Hz}$, FM±50KHz dev
SG. 20	$f_0 = 6.0\text{MHz}$, 100dBμ, $f_m = 400\text{Hz}$, AM30%
SG. 21	$f_0 = 6.0\text{MHz}$, 100dBμ, CW

Note 1: The timing and pulse width of the horizontal blanking pulse should be as shown in the following figure by adjusting the variable resistor of the single shot multi vibrator.

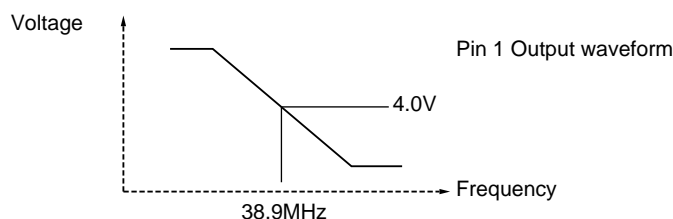


The variable resistor at pin 15 of the TTL IC, M74LS221P, is used to fix the timing at 8μs and that at pin 7 is used to fix the pulse width at 12μs.

Coil adjustment

VCO coil

1. Set the test conditions as shown in the parameter V14.
2. Input CW ($f_0=38.9\text{MHz}$, $V_i=90\text{dB}\mu$) to input pin A.
3. Set the DC voltage at pin 1 (AFT OUT) to 1/2Vcc (4.0V) by adjusting VCO coil.

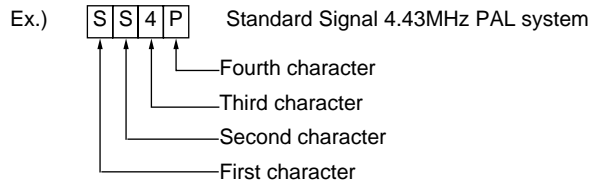


Note) VCO coil should always be adjusted as above before using this IC.

PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

INPUT SIGNAL PARAMETERS INCLUDING INPUT SIGNALS

1. Input signal name is four alphanumeric characters.



First character: Standard=S, Nonstandard=V (Modified parts should be specified.)

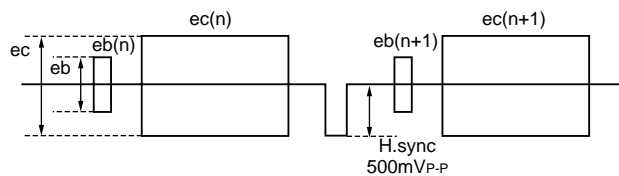
Second character: Meaning of signal

Third character: Frequency of burst and chroma
4(4.433619MHz), 3(3.579545MHz) (In case of "S", SECAM standard signal is applied.)

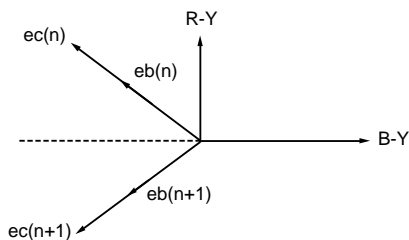
Fourth character: Color system
N(NTSC), P(PAL)

2. Structure of input color signal

The following figure shows the structure of color signal.

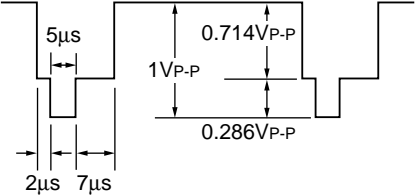
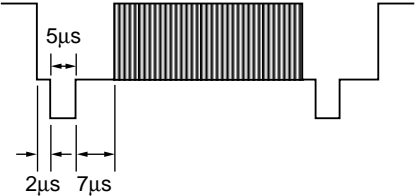
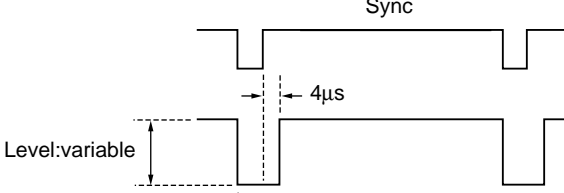
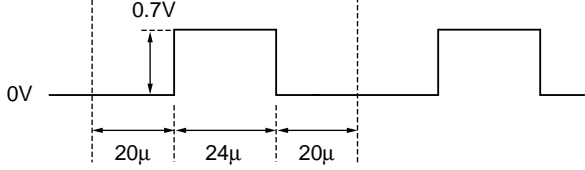

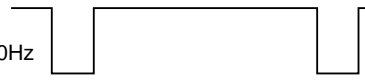
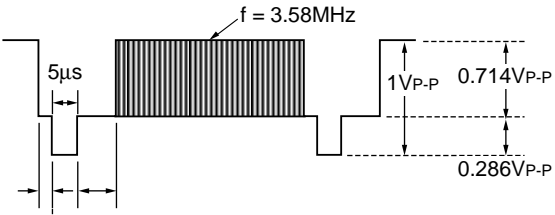
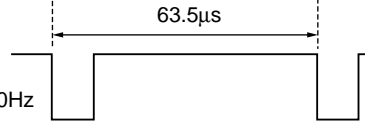


1. When S (standard) is used as the first character, the standard color bar signal of each system is applied. H.sync should be added for input clamp. (The frequency of H.sync is fixed according to the fourth character. P:50Hz, N:60Hz)
2. Amplitude and frequency of burst are represented as eb. In case of standard signal, the amplitude is 285mVp-p and the frequency is shown by the third character.
3. Amplitude and frequency of chroma are represented as ec. In case of standard signal, the amplitude is 570mVp-p and the frequency is shown by the third character.
4. The following figure shows the phase of a PAL system signal.



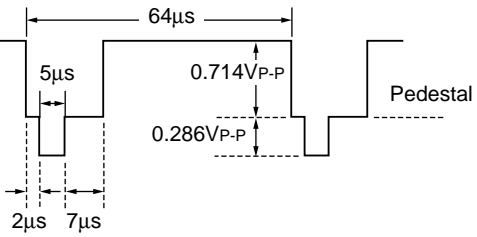
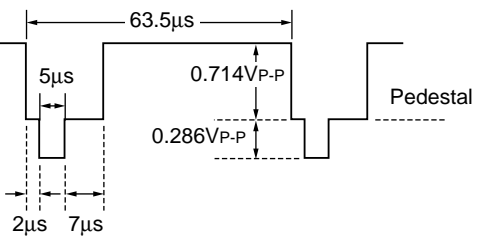

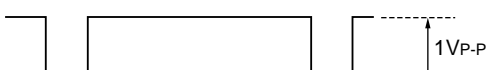
PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

VIDEO/INTERFACE

SG. No.	Input signal (Value at pin terminal is 50Ω)	
SG. A	<p>PAL system PAL system APL 100% standard video signal should be input as sync separation input as shown in the figure. The vertical signal should be interlaced at 50Hz.</p>	
SG. B	<p>The frequency and amplitude of signal Lumi can be changed by signal SGA. The typical amplitude is 0.714mVp-p.</p>	
SG. C		
SG. D		
SG. E		
SG. 50	<p>Level:variable typ = 0.3Vp-p H = 15.625KHz, V = 50Hz</p>	 <p>Standard PAL SYNC</p>
SG. F		
SG. 60	<p>NTSC system Level:variable typ = 0.3Vp-p H = 15.734KHz, V = 60Hz</p>	 <p>Standard NTSC SYNC</p>

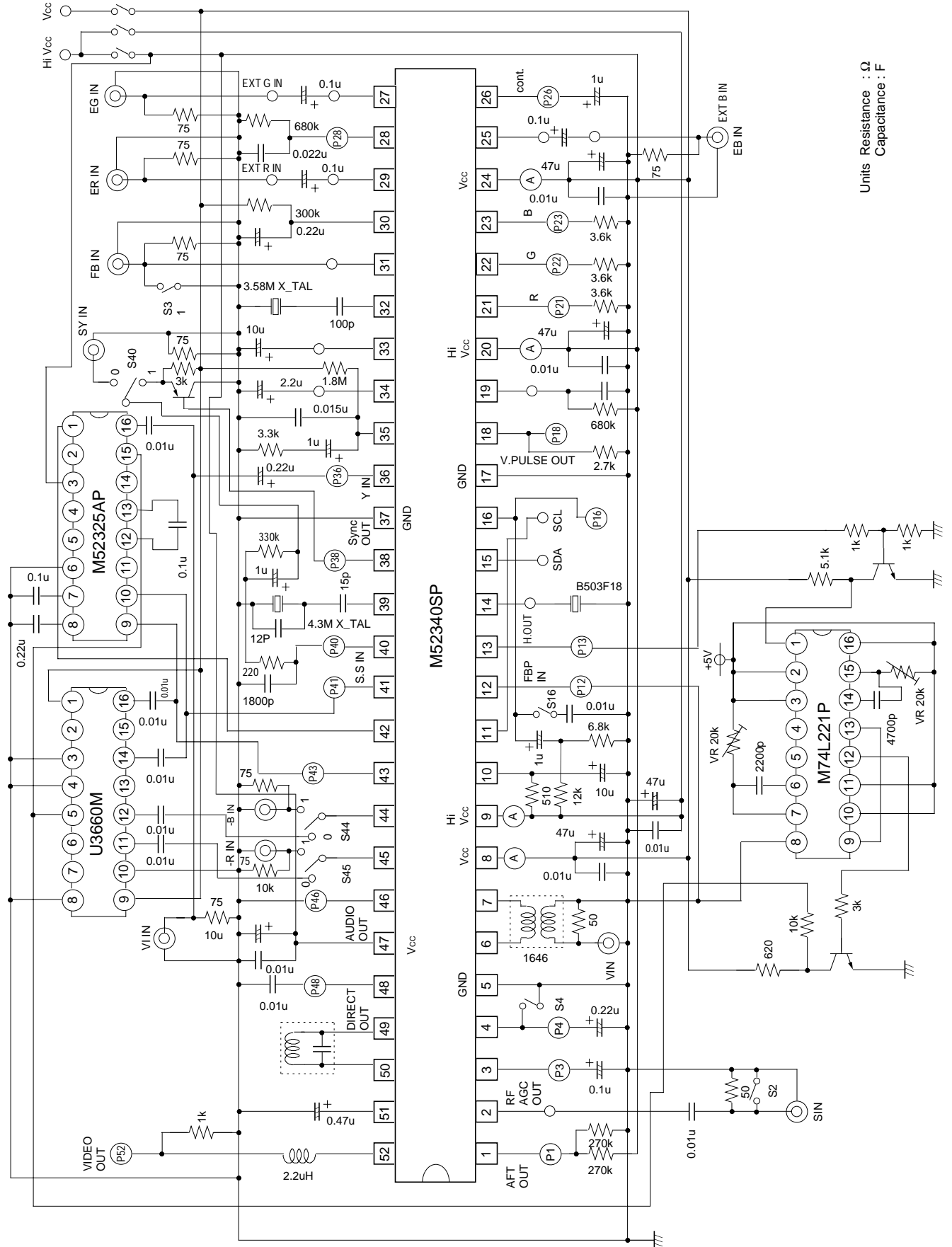
PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DEFLECTION

SG. No.	Input signal (Value at pin terminal is 50Ω)	
SG. a	<p>The input signal should be PAL system APL-variable video signal. Vertical signal should be interlaced at 50Hz.</p>	
SG. b	<p>The input signal should be NTSC APL-variable video signal. Vertical signal should be interlaced at 60Hz.</p>	
SG. c	<p>Duty 90% Frequency:variable Level:variable (Typ. : 1VP-P)</p> 	
SG. d	<p>Duty 95% Frequency:variable Level:variable (Typ. : 1VP-P) Duty : variable (Typ. : 95%)</p> 	

PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

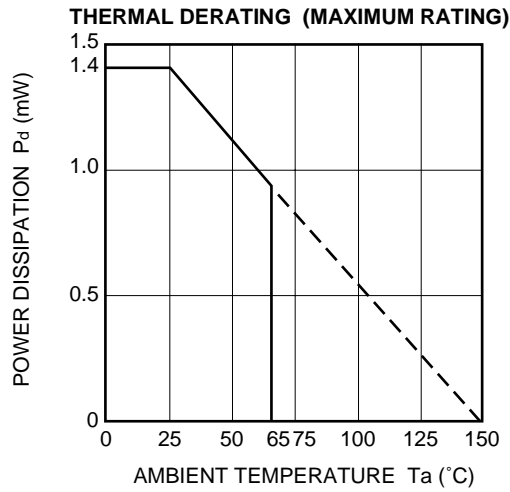
TEST CIRCUIT



Units Resistance : Ω
Capacitance : F

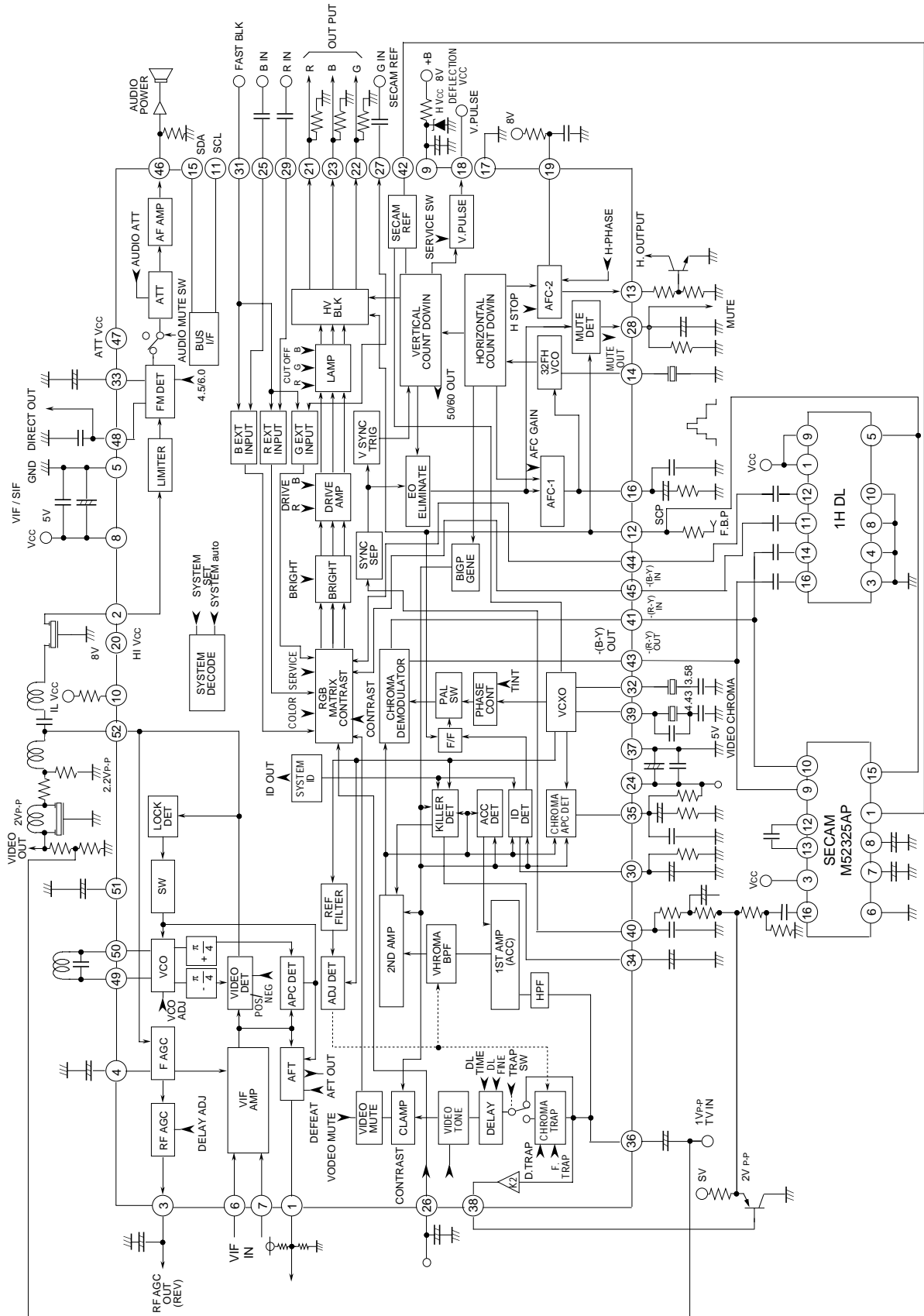
PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

TYPICAL CHARACTERISTICS



PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

APPLICATION EXAMPLE



PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN

Pin No.	Name	Description	Peripheral circuit of pin	DC voltage
①	AFT OUT		<p>The diagram shows a differential amplifier circuit. The output node is connected to a 1k resistor and a diode clamp consisting of two diodes connected in series to ground. The other side of the diodes is connected to ground.</p>	4.0V
②	LIMITER IN		<p>The diagram shows a complex circuit with two transistors. The input node is connected to a 5.6k resistor and a 20pF capacitor. The output node is connected to a 100 resistor and a 30k resistor. There is also a 10pF capacitor connected to ground.</p>	3.0V
③	RE AGC OUT		<p>The diagram shows a differential amplifier circuit. The output node is connected to a 50 resistor and a diode clamp consisting of two diodes connected in series to ground. The other side of the diodes is connected to ground.</p>	7.5V to 0.5V
④	IF AGC FILTER		<p>The diagram shows a differential amplifier circuit. The output node is connected to a 1k resistor and a diode clamp consisting of two diodes connected in series to ground. The other side of the diodes is connected to ground.</p>	4.5V to 2.5V
⑤	VIF GND		<p>A simple horizontal line representing a ground connection.</p>	

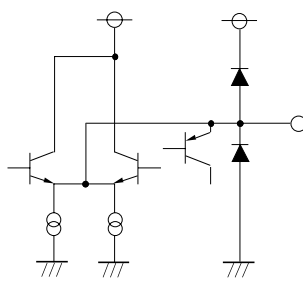
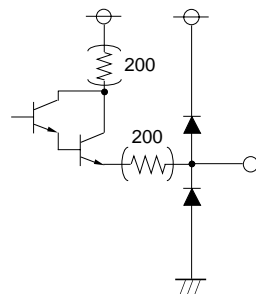
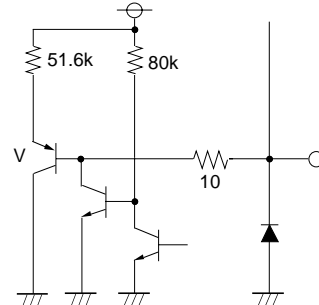
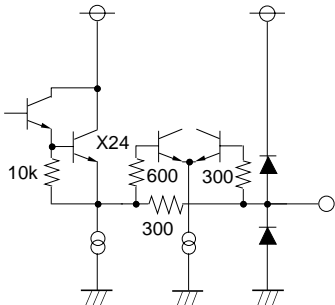
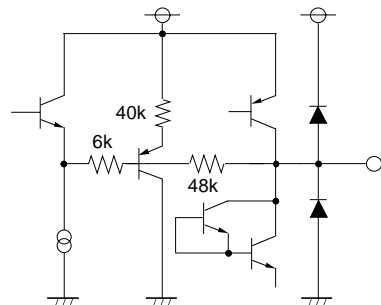
PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Description	Peripheral circuit of pin	DC voltage
⑥ ⑦	VIF IN			1.5V
⑧	VIF Vcc	Power supply for VIF	_____	5.0V
⑨	H Vcc	Power supply for all circuits in the deflection block	_____	8.0V
⑩	IIL Vcc	Power supply for I ² C bus IIL	_____	1.5V
⑪	SCL	I ² C bus clock input		5V to 0V

PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Description	Peripheral circuit of pin	DC voltage
⑫	SCP OUT	Sandcastle pulse output		5V to 0V
⑬	H OUT	MAX 4mA Horizontal frequency pulse output		4V to 0V
⑮	SDA	I ² C bus data input		5V to 0V
⑭	H OSC	CSB-503 F18 is used.		3.1V
⑯	AFC 1 FILTER			5.5V

PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Description	Peripheral circuit of pin	DC voltage
⑰	GND	Power supply for R/G/B output	_____	
⑱	V pulse	Open emitter input		2.5V
⑲	AFC 2 FILTER			
⑳	Hi Vcc	Power supply for R/G/B output	_____	8V
㉑ ㉒ ㉓	B OUT G OUT R OUT	MAX 4mA Primary-color (R, G and B) signal output pin		2.9V TYP
㉔	VCD Vcc	Power supply for video chroma	_____	5V

PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Description	Peripheral circuit of pin	DC voltage
<p>②⑤</p> <p>②⑦</p> <p>②⑨</p>	<p>B IN</p> <p>G IN</p> <p>R IN</p>	External R/G/B input pin		
②⑥	CONTRAST	Pin to adjust contrast externally		
②⑧	COINCIDENCE	Sync detection pin Sync → Hi Async → Lo		7.5V to 0.5V
③①	KILLER FILTER			
③①	FAST BLK			0V

PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Description	Peripheral circuit of pin	DC voltage
③②	3.58MHz X-tal	Pin used to connect an oscillator (3.58MHz)		0V
③③	AUDIO BYPASS			2.5V
③④	ID Filter			2.3V
③⑤	CHROMA APC FILTER			3.3V
③⑥	TV IN (Y IN)			2.3V

PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Description	Peripheral circuit of pin	DC voltage
③⑦	VCD GND		_____	
③⑧	V(Y) SW OUT	Pin to output 6dB amplifier		1.75V
③⑨	X-TAL 4.43MHz	Pin used to connect an oscillator (4.43MHz)		3.2V
④①	SYNC SEP IN	Emitter input		5.7V
④① ④③	-(B-Y) OUT -(R-Y) OUT			2.3V

PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Description	Peripheral circuit of pin	DC voltage
④②	SECAM REF			4.4V to 1.3V
④④ ④⑤	-(B-Y) IN -(R-Y) IN			3.0V
④⑥	AUDIO OUT			3.2V
④⑦	AUDIO Vcc			8.0V
④⑧	FM DIRECT OUT			3.0V

PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Description	Peripheral circuit of pin	DC voltage
<p>④⑨</p> <p>⑤⑩</p>	VCO			4.0V
⑤①	VIDEO APC FILTER			2.9V
⑤②	VIDEO OUT			2.2V or 5.7V

PAL/NTSC SYSTEM SHINGLE-CHIP COLOR TV SIGNAL PROCESSOR

[DATA list]

Data No.	Data									Data No.	Data								
	D7	D6	D5	D4	D3	D2	D1	D0	Decimal		D7	D6	D5	D4	D3	D2	D1	D0	Decimal
A0	0	0	0	0	0	0	0	0	0	C3	0	0	0	0	1	1	0	0	12
A1	0	0	0	0	0	0	0	1	1	C4	0	0	0	1	1	0	0	0	24
A2	0	0	0	0	0	0	1	0	2	C5	0	0	1	1	0	0	0	0	48
A3	0	0	0	0	0	1	0	0	4	C6	0	1	1	0	0	0	0	0	96
A4	0	0	0	0	1	0	0	0	8	C7	0	0	0	0	1	1	1	0	14
A5	0	0	0	1	0	0	0	0	16	C8	0	0	0	1	1	1	0	0	28
A6	0	0	1	0	0	0	1	0	32	C9	0	0	1	1	1	0	0	0	56
A7	0	1	0	0	0	0	0	1	64	D0	0	1	1	1	0	0	0	0	112
A8	1	0	0	0	0	0	0	0	128	D1	0	0	0	1	1	1	1	0	30
A9	0	0	0	0	0	0	1	1	3	D2	0	0	1	1	1	1	0	0	60
B0	0	0	0	0	0	1	0	1	5	D3	0	1	1	1	1	0	0	0	120
B1	0	0	0	0	1	0	0	1	9	D4	0	0	0	0	1	0	1	0	10
B2	0	0	0	1	0	0	0	1	17	D5	0	0	0	1	0	1	0	0	20
B3	0	0	1	0	0	0	0	1	33	D6	0	0	1	0	1	0	0	0	40
B4	0	1	0	0	0	0	0	1	65	D7	0	1	0	1	0	0	0	0	80
B5	1	0	0	0	0	0	0	1	129	D8	0	0	0	1	0	0	1	0	18
B6	0	0	0	0	0	1	1	1	7	D9	0	0	1	0	0	1	0	0	36
B7	0	0	0	0	1	1	1	1	15	E0	0	0	1	0	0	1	1	0	38
B8	0	0	0	1	1	1	1	1	31	E1	0	0	1	0	0	0	1	0	34
B9	0	0	1	1	1	1	1	1	63	E2	0	0	1	0	0	0	1	1	35
C0	0	1	1	1	1	1	1	1	127	E3	0	1	0	0	0	1	1	0	69
C1	1	1	1	1	1	1	1	1	255	E4	0	0	1	1	0	0	1	1	51
C2	0	0	0	0	0	1	1	0	6	E5	0	0	1	1	0	0	1	0	50
E7	0	0	1	1	0	1	1	0	54	E6	0	1	0	0	0	1	0	0	68
E8	0	0	1	0	0	1	0	1	37	E9	0	0	1	0	0	1	1	1	39

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Datasheets for electronics components.