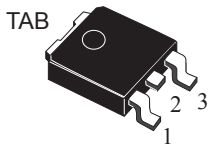
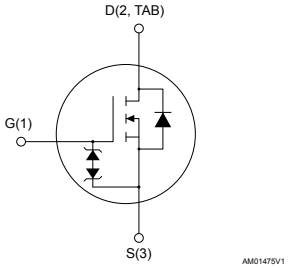
N-channel 620 V, 0.95 Ω typ., 5.5 A MDmesh™ K3 Power MOSFET in DPAK package



DPAK



Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STD6N62K3	620 V	1.2 Ω	5.5 A	90 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

This MDmesh™ K3 Power MOSFET is the result of improvements applied to STMicroelectronics' MDmesh™ technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

Product status
STD6N62K3

Product summary	
Order code	STD6N62K3
Marking	6N62K3
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	620	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	5.5	A
I_D	Drain current (continuous) at T_C = 100 °C	3	A
I_{DM} (1)	Drain current (pulsed)	22	A
P_{TOT}	Total dissipation at T_C = 25 °C	90	W
I_{AR} (2)	Avalanche current, repetitive or not-repetitive	5.5	A
E_{AS} (3)	Single pulse avalanche energy	140	mJ
ESD	Gate-source human body model (R = 1.5 kΩ, C = 100 pF)	2.5	kV
dv/dt (4)	Peak diode recovery voltage slope	12	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Pulse width limited by safe operating area.*
2. *Pulse width limited by Tj max.*
3. *Starting Tj = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.*
4. *I_{SD} ≤ 5.5 A, di/dt ≤ 400 A/µs, V_{DD} = 80% $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.39	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	50	°C/W

1. *When mounted on 1inch² FR-4 board, 2 oz Cu.*

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 3. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	620			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 620 V			0.8	µA
		V_{GS} = 0 V, V_{DS} = 620 V T_C = 125 °C (1)			50	µA
I_{GSS}	Gate body leakage current	V_{GS} = ±20 V, V_{DS} = 0 V			± 9	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2.8 A		0.95	1.2	Ω

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	875	-	pF
C_{oss}	Output capacitance			100		
C_{rss}	Reverse transfer capacitance			17		
$C_{o(er)}$ (1)	Equivalent output capacitance energy related	V_{GS} = 0 V, V_{DS} = 0 to 480 V	-	28	-	pF
$C_{o(tr)}$ (2)	Equivalent output capacitance time related			63		
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	3.5	-	Ω
Q_g	Total gate charge	V_{DD} = 496 V, I_D = 5.5 A, V_{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	34	-	nC
Q_{gs}	Gate-source charge			4		
Q_{gd}	Gate-drain charge			22		

1. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
2. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 310 V, I_D = 2.75 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	22	-	ns
t_r	Rise time			12		
$t_{d(off)}$	Turn-off delay time			49		
t_f	Fall time			20		

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5.5	A
I_{SDM} (1)	Source-drain current (pulsed)				27	
V_{SD} (2)	Forward on voltage	I_{SD} = 5.5 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 5.5 A, di/dt = 100 A/µs	-	290		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)		1.9		µC
I_{RRM}	Reverse recovery current			13.5		A
t_{rr}	Reverse recovery time	I_{SD} = 5.5 A, di/dt = 100 A/µs	-	335		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_j = 150 °C		2.4		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)		14.5		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

Table 7. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_D = 0 A, I_{GS} = ±1 mA	±30	-		V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics curves

Figure 1. Safe operating area

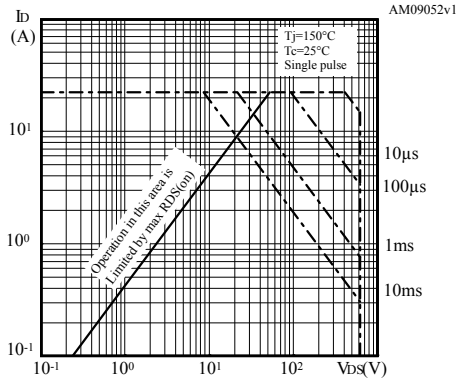


Figure 2. Thermal impedance

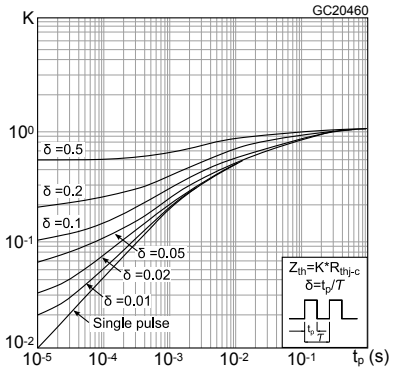


Figure 3. Output characteristics

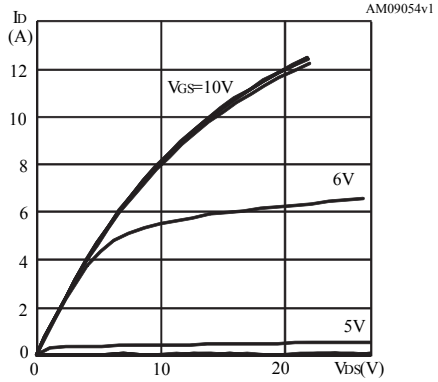


Figure 4. Transfer characteristics

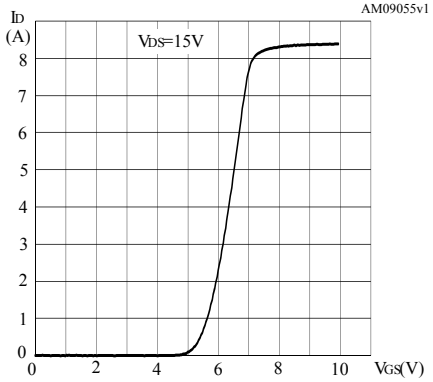


Figure 5. Gate charge vs gate-source voltage

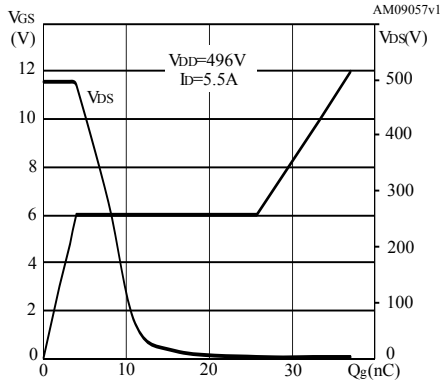


Figure 6. Static drain-source on resistance

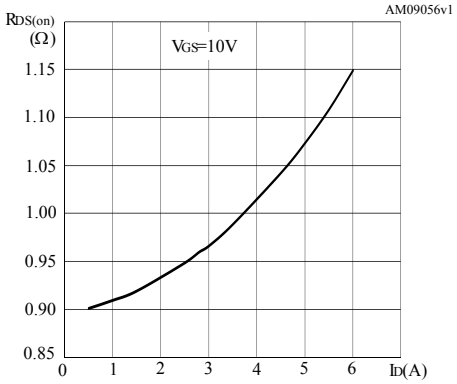


Figure 7. Capacitance variations

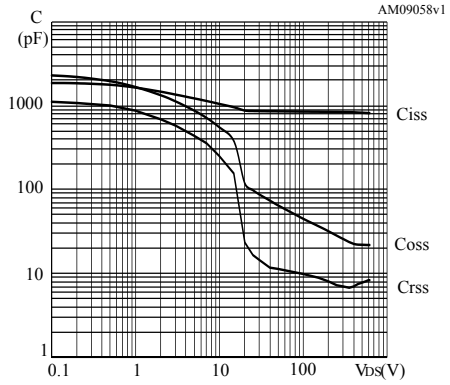


Figure 8. Output capacitance stored energy

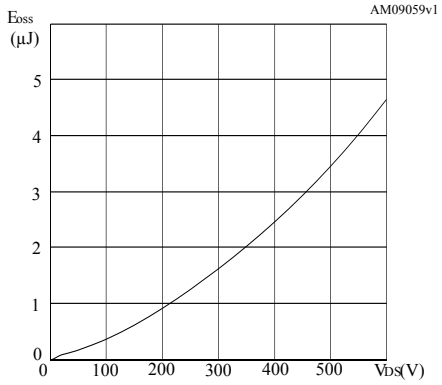


Figure 9. Normalized gate threshold voltage vs temperature

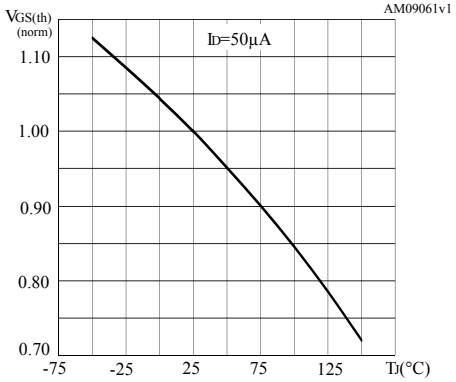


Figure 10. Normalized on resistance vs temperature

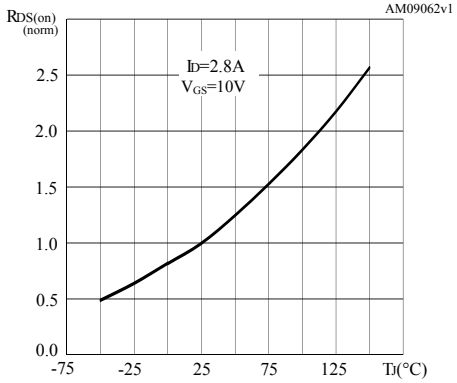


Figure 11. Normalized B_{VDSS} vs temperature

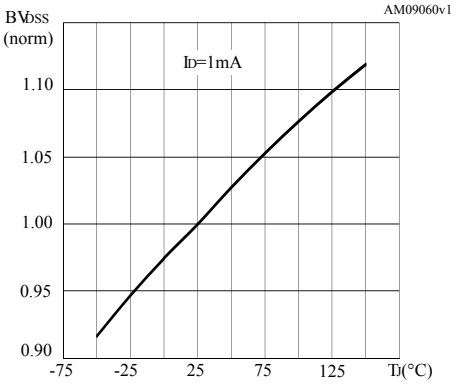


Figure 12. Source-drain diode forward characteristics

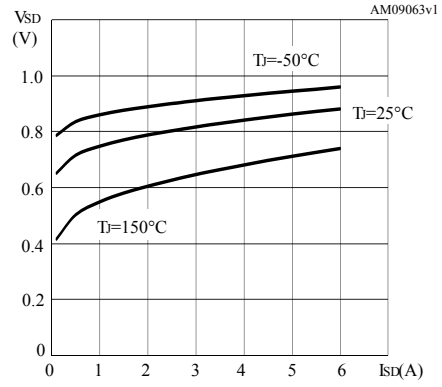
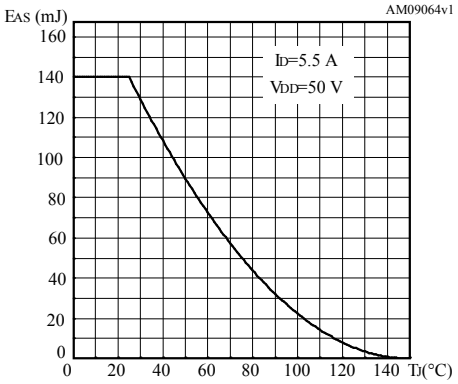


Figure 13. **Maximum avalanche energy vs temperature**



3 Test circuits

Figure 14. Test circuit for resistive load switching times

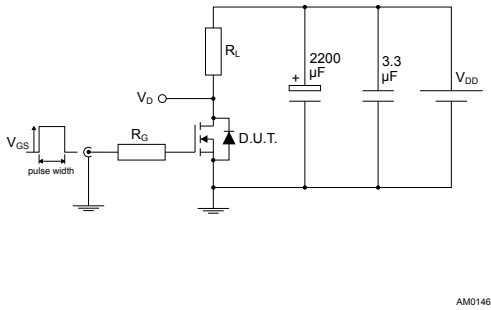


Figure 15. Test circuit for gate charge behavior

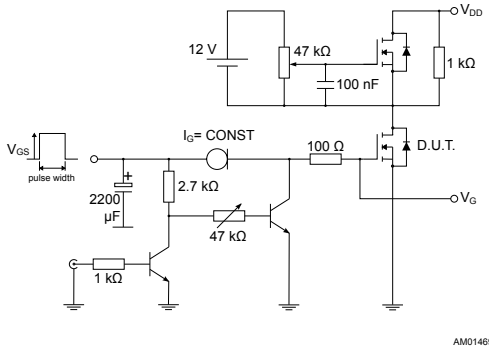


Figure 16. Test circuit for inductive load switching and diode recovery times

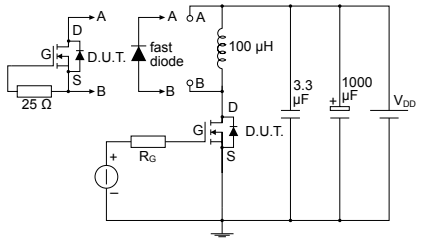


Figure 17. Unclamped inductive load test circuit

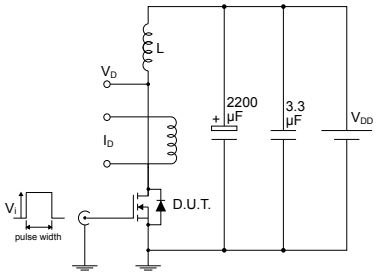


Figure 18. Unclamped inductive waveform

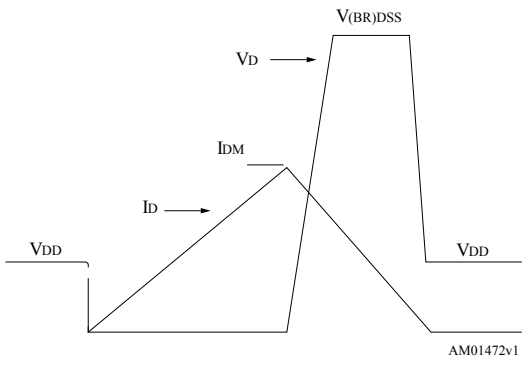
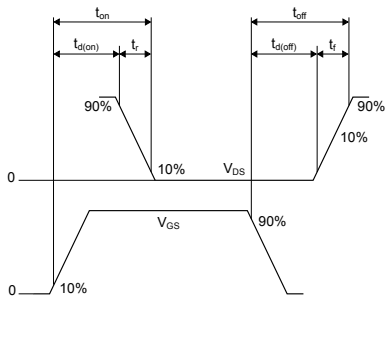


Figure 19. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 20. **DPAK (TO-252) type A2 package outline**

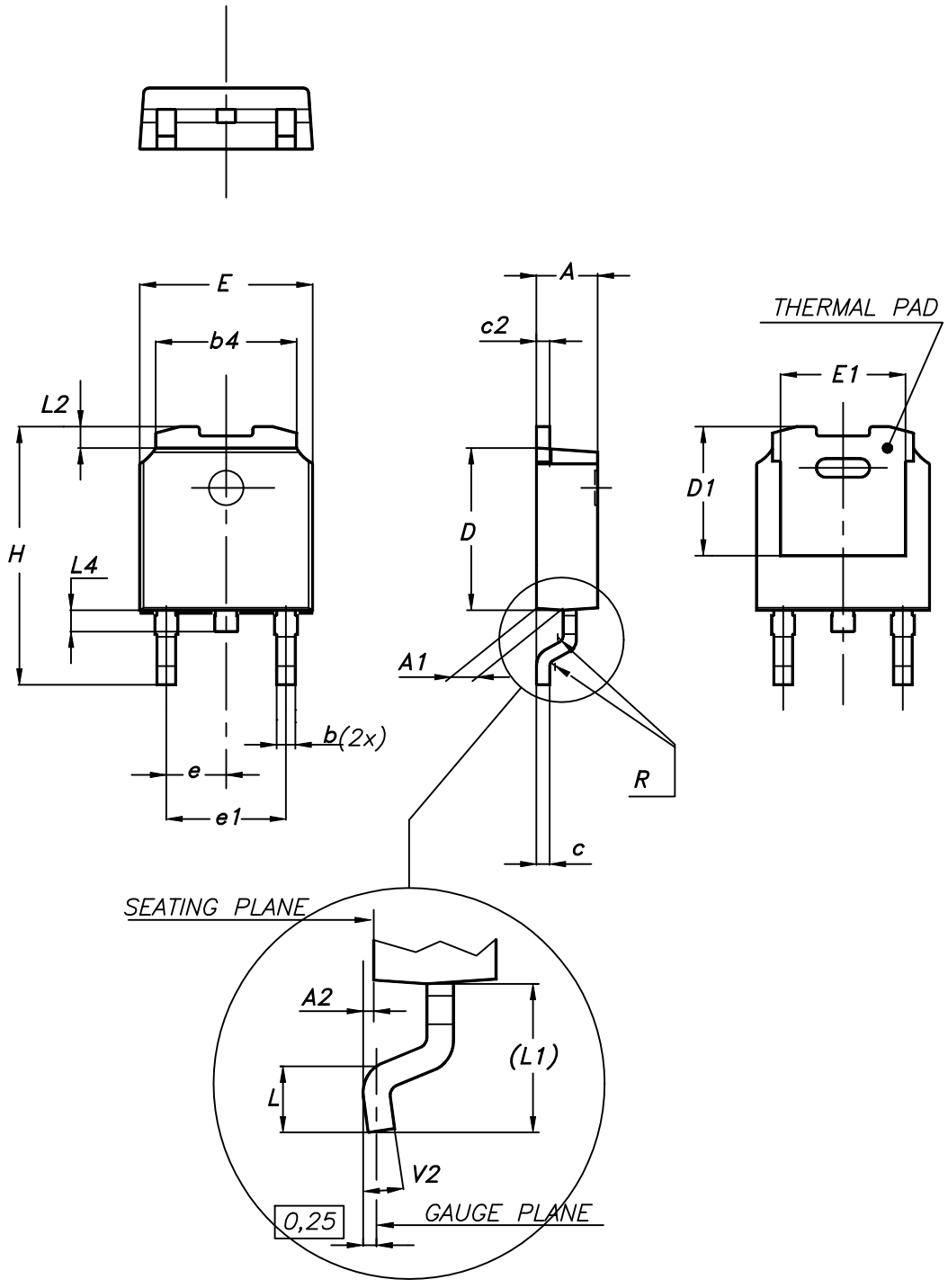


Table 8. **DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C2 package information

Figure 21. **DPAK (TO-252) type C2 package outline**

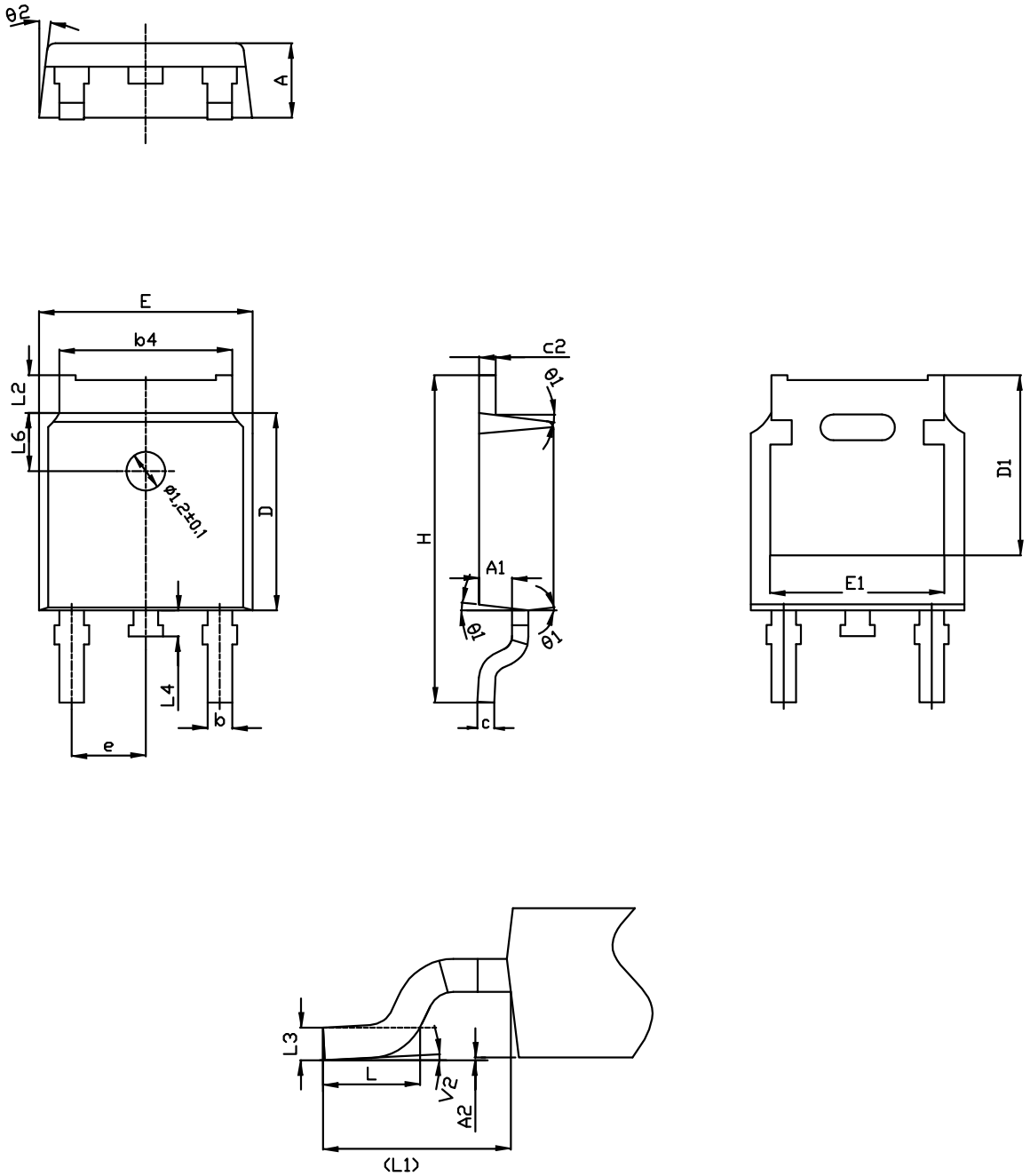


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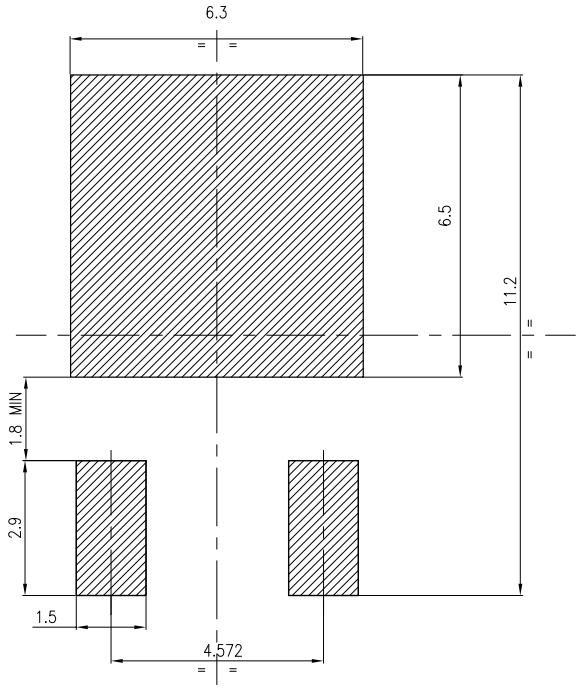
Table 9. **DPAK (TO-252) type C2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
E	6.50	6.60	6.70
E1	5.20		5.50
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1		2.90 REF	
L2	0.90		1.25
L3		0.51 BSC	
L4	0.60	0.80	1.00
L6		1.80 BSC	
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Figure 22. **DPAK (TO-252) recommended footprint (dimensions are in mm)**



4.3 DPAK (TO-252) packing information

Figure 23. **DPAK (TO-252) tape outline**

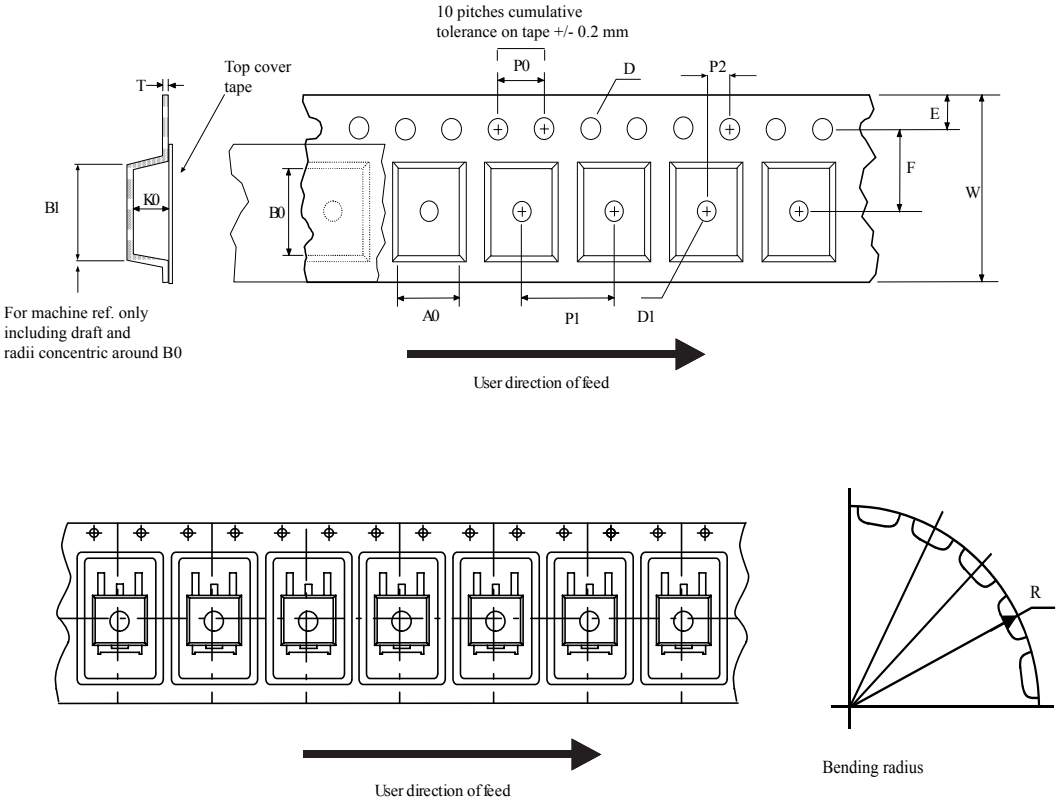


Figure 24. **DPAK (TO-252) reel outline**

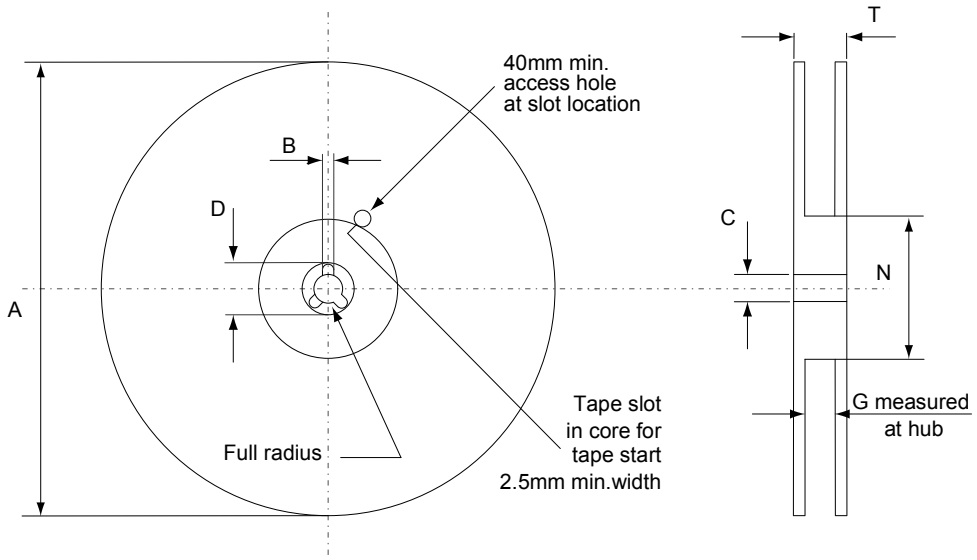


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Table 10. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 11. **Document revision history**

Date	Revision	Changes
21-Dec-2011	1	First release.
10-Apr-2018	2	The part number STB6N62K3 has been moved to a separate datasheet. Removed maturity status indication from cover page. The document status is production data. Updated title and features in cover page. Updated Section 1 Electrical ratings, Section 2 Electrical characteristics, Section 2.1 Electrical characteristics curves and Section 4 Package information. Minor text changes.

Contents

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