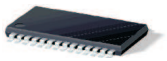


Typical Size
6.4 mm x 9.7 mm



# 24 V, EIGHT-CHANNEL DIGITAL-INPUT SERIALIZER

## FEATURES

- **Eight Sensor Inputs**
  - **High Input Voltage up to 30 V**
  - **Selectable Debounce Filters From 0 ms to 3 ms**
  - **Adjustable Current Limits From 0.2 mA to 5.2 mA**
  - **Field Inputs and Supply Lines Protected to 15-kV HBM**
- **Output Drivers for External Status LEDs**
- **Cascadable for More Inputs in Multiples of Eight**
- **SPI-Compatible Interface**
- **Regulated 5-V Output for External Digital Isolator**
- **Over-Temperature and Low-Supply Voltage Indicator**

## APPLICATIONS

- **Sensor Inputs for Industrial Automation and Process Control**
  - **IEC61131-2 Type 1, 2, or 3 Switches**
  - **EN60947-5-2 Proximity Switches**
- **High Channel Count Digital Input Modules for PC and PLC Systems**
- **Decentralized I/O Modules**

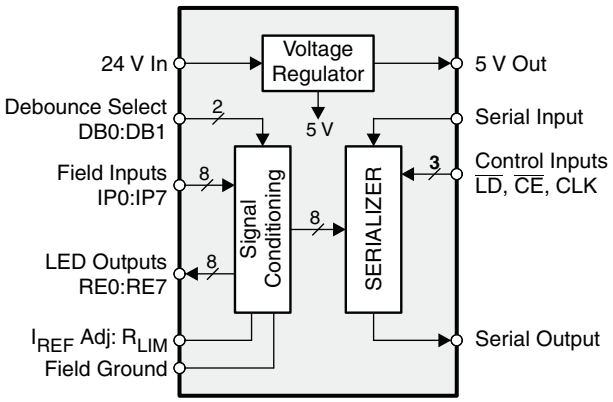
## DESCRIPTION

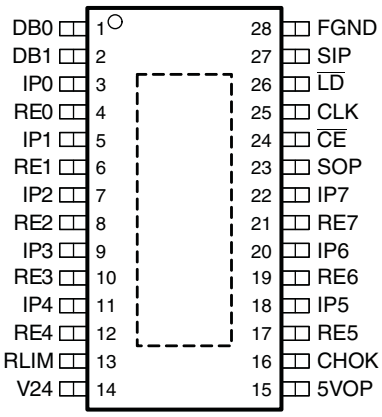
The SN65HVS880 is a 24-V, eight-channel, digital-input serializer for high-channel density digital input modules of PC and PLC based systems in industrial automation. In combination with galvanic isolators the device completes the interface between the 24-V sensor outputs of the field-side and the low-voltage controller inputs at the control-side. Input signals provided by EN60947-5-2 compliant 2- and 3-wire proximity switches are current-limited and then validated by internal debounce filters. The input switching characteristic is in accordance with IEC61131-2 for Type 1, 2, and 3 sensor switches.

Upon the application of load and clock signals, input data is latched in parallel into the shift register and afterwards clocked out serially via a subsequent isolator into a serial PLC input.

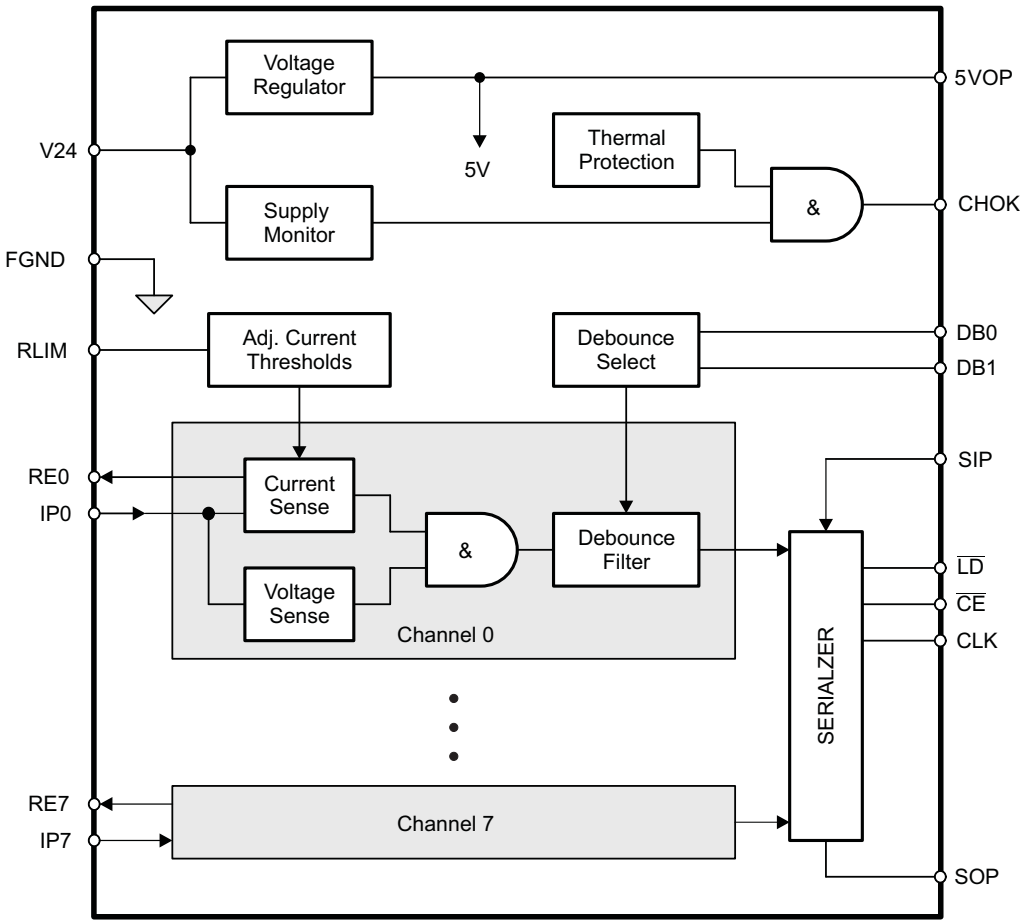
Cascading of multiple SN65HVS880 is possible by connecting the serial output of the leading device with the serial input of the following device, enabling the design of high-channel count input modules. Input status is indicated via 3-mA constant current LED outputs. An external precision resistor is required to set the internal reference current. The integrated voltage regulator provides a 5-V output to supply low-power isolators. An on-chip temperature sensor together with an internal supply voltage monitor provides a chip-okay (CHOK) indication.

The SN65HVS880 comes in a 28-pin PWP PowerPAD™ package allowing for efficient heat dissipation. The device is specified for operation at temperatures from –40°C to 85°C.




## FUNCTIONAL BLOCK DIAGRAM



## TERMINAL FUNCTIONS

| TERMINAL | | DESCRIPTION |
|---|---|---|
| PIN NO. | NAME | |
| 1, 2 | DB0, DB1 | Debounce select inputs |
| 3, 5, 7, 9, 11, 18, 20, 22 | IPx | Input channel x |
| 4, 6, 8, 10, 12, 17, 19, 21 | REx | Return path x (LED drive) |
| 13 | RLIM | Current limiting resistor |
| 14 | V24 | 24 VDC field supply |
| 15 | 5VOP | 5 V output to supply low-power isolators |
| 16 | CHOK | Chip okay indicator output |
| 23 | SOP | Serial data output |
| 24 | $\overline{CE}$ | Clock enable input |
| 25 | CLK | Serial clock input |
| 26 | $\overline{LD}$ | Load pulse input |
| 27 | SIP | Serial data input |
| 28 | FGND | Field ground |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

| | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| V24 | Field power input | | V24 | –0.3 | 35 | V |
| $V_{IPx}$ | Field digital inputs | | IPx | –0.3 | 35 | V |
| $V_{ID}$ | Voltage at any logic input | | DB0, DB1, CLK, SIP, $\overline{CE}$, $\overline{LD}$ | –0.5 | 6 | V |
| $I_O$ | Output current | | CHOK, SOP | | ±8 | mA |
| $V_{ESD}$ | Electrostatic discharge | Human-Body Model(1) | All pins | | ±4 | kV |
| | | | IPx,V24 | | ±15 | |
| | | Charged-Device Model(2) | All pins | | ±1 | kV |
| | | Machine Model(3) | All pins | | ±100 | V |
| $P_{TOT}$ | Continuous total power dissipation | See Thermal Characteristics table | | | | |
| $T_J$ | Junction temperature | | | | 170 | °C |

(1) JEDEC Standard 22, Method A114-A.
(2) JEDEC Standard 22, Method C101
(3) JEDEC Standard 22, Method A115-A

## THERMAL CHARACTERISTICS

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-air thermal resistance | High-K thermal resistance | | 35 | | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance | | | 15 | | °C/W |
| $\theta_{JC}$ | Junction-to-case thermal resistance | | | 4.27 | | °C/W |
| PD | Device power dissipation | $I_{LOAD}$ = 50 mA, $R_{IN}$ = 0, IPO–IP7 = V24 = 30 V, RE7 = FGND, $f_{CLK}$ = 100 MHz, $I_{IP-LIM}$ and $I_{CC}$ = worst case with $R_{LIM}$ = 25 kΩ | | | 2591 | mW |

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{24}$ | Field supply voltage | 18 | 24 | 30 | V |
| $V_{IPL}$ | Field input low-state input voltage(1) | 0 | | 6 | V |
| $V_{IPH}$ | Field input high-state input voltage(1) | 10 | | 30 | V |
| $V_{IL}$ | Logic low-state input voltage | 0 | | 0.8 | V |
| $V_{IH}$ | Logic high-state input voltage | 2 | | 5.5 | V |
| $R_{LIM}$ | Current limiter resistor | 17 | 25 | 500 | kΩ |
| $f_{IP}$ | Input data rate(2) | 0 | | 1 | Mbps |
| $T_J$ | | | | 150 | °C |
| $T_A$ | | –40 | | 85 | °C |

(1) Field input voltages correspond to an input resistor of $R_{IN}$ = 1.2 kΩ
(2) Maximum data rate corresponds to 0 ms debounce time, (DB0 = open, DB1 = FGND), and $R_{IN}$ = 0 Ω

## ELECTRICAL CHARACTERISTICS

all voltages measured against FGND unless otherwise stated, see Figure 12

| SYMBOL | PARAMETER | TERMINAL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{TH-(IP)}$ | Low-level device input threshold voltage | IP0–IP7 | 18 V< V24 < 30 V, $R_{IN}$ = 0 Ω | 4 | 4.3 | | V |
| $V_{TH+(IP)}$ | High-level device input threshold voltage | | | | 5.2 | 5.5 | V |
| $V_{HYS(IP)}$ | Device input hysteresis | | | | 0.9 | | V |
| $V_{TH-(IN)}$ | Low-level field input threshold voltage | measured at field side of $R_{IN}$ | 18 V < V24 < 30 V, $R_{IN}$ = 1.2 kΩ ± 5%, $R_{LIM}$ = 25 kΩ | 6 | 8.4 | | V |
| $V_{TH+(IN)}$ | High-level field input threshold voltage | | | | 9.4 | 10 | V |
| $V_{HYS(IN)}$ | Field input hysteresis | | | | 1 | | V |
| $V_{TH-(V24)}$ | Low-level V24-monitor threshold voltage | V24 | | 15 | 16.05 | | V |
| $V_{TH+(V24)}$ | High-level V24-monitor threshold voltage | | | | 16.8 | 18 | V |
| $V_{HYS(V24)}$ | V24-monitor hysteresis | | | | 0.75 | | V |
| $R_{IP}$ | Input resistance | IP0–IP7 | 3 V < $V_{IPx}$ < 6 V, $R_{IN}$ = 1.2 kΩ ± 5%, $R_{LIM}$ = 25 kΩ | 1.4 | 1.83 | 2.3 | kΩ |
| $I_{IP-LIM}$ | Input current limit | | 10 V < $V_{IPx}$ < 30 V, $R_{LIM}$ = 25 kΩ | 3.15 | 3.6 | 4 | mA |
| $V_{OL}$ | Logic low-level output voltage | SOP, CHOK | $I_{OL}$ = 20 µA | | | 0.4 | V |
| $V_{OH}$ | Logic high-level output voltage | | $I_{OH}$ = –20 µA | 4 | | | V |
| $I_{IL}$ | Logic input leakage current | DB0, DB1, SIP, LD, CE, CLK | | –50 | | 50 | µA |
| $I_{RE-on}$ | RE on-state current | RE0–RE7 | $R_{LIM}$ = 25 kΩ, $RE_X$ = FGND | 2.8 | 3.15 | 3.5 | mA |
| $I_{CC(V24)}$ | Supply current | V24 | IP0 to IP7 = V24, 5VOP = open, $RE_X$ = FGND, All logic inputs open | | | 8.7 | mA |
| $V_{O(5V)}$ | Linear regulator output voltage | 5VOP | 18 V < V24 < 30 V, no load | 4.5 | 5 | 5.5 | V |
| | | | 18 V < V24 < 30 V, $I_L$ = 50 mA | 4.5 | 5 | 5.5 | |
| $I_{LIM(5V)}$ | Linear regulator output current limit | | | | 115 | | mA |
| $\Delta V_5/\Delta V_{24}$ | Line regulation | 5VOP, V24 | 18 V < V24 < 30 V, $I_L$ = 5 mA | | | 2 | mV/V |
| $t_{DB}$ | Debounce times of input channels | IP0–IP7 | DB0 = open, DB1 = FGND | | 0 | | ms |
| | | | DB0 = FGND, DB1 = open | | 1 | | |
| | | | DB0 = DB1 = open | | 3 | | |
| $t_{DB-HL}$ | Voltage monitor debounce time after V24 < 15 V (CHOK turns low) | V24, CHOK | | | 1 | | ms |
| $t_{DB-LH}$ | Voltage monitor debounce time after V24 > 18 V (CHOK turns high) | | | | 6 | | ms |
| $T_{OVER}$ | Over-temperature indication | | | | 150 | | °C |
| $T_{SHDN}$ | Shutdown temperature | | | | 170 | | °C |

## TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

| SYMBOL | PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{W1}$ | CLK pulse width | See Figure 6 | 4 | | | ns |
| $t_{W2}$ | $\overline{LD}$ pulse width | See Figure 4 | 6 | | | ns |
| $t_{SU1}$ | SIP to CLK setup time | See Figure 7 | 4 | | | ns |
| $t_{H1}$ | SIP to CLK hold time | See Figure 7 | 2 | | | ns |
| $t_{SU2}$ | Falling edge to rising edge ($\overline{CE}$ to CLK) setup time | See Figure 8 | 4 | | | ns |
| $t_{REC}$ | $\overline{LD}$ to CLK recovery time | See Figure 5 | 2 | | | ns |
| $f_{CLK}$ | Clock pulse frequency | See Figure 6 | DC | | 100 | MHz |

## SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH1}$, $t_{PHL1}$ | CLK to SOP | $C_L$ = 15 pF, see Figure 6 | | | 10 | ns |
| $t_{PLH2}$, $t_{PHL2}$ | $\overline{LD}$ to SOP | $C_L$ = 15 pF, see Figure 4 | | | 14 | ns |
| $t_r$, $t_f$ | Rise and fall times | $C_L$ = 15 pF, see Figure 6 | | | 5 | ns |

## INPUT CHARACTERISTICS

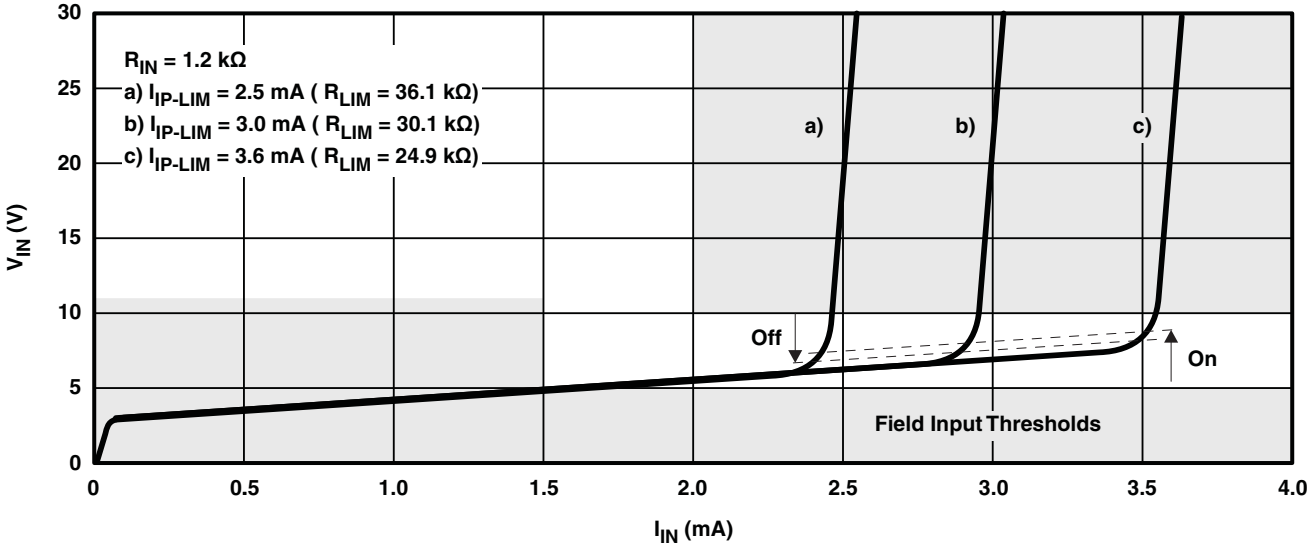



**Figure 1. Typical Input Characteristics**

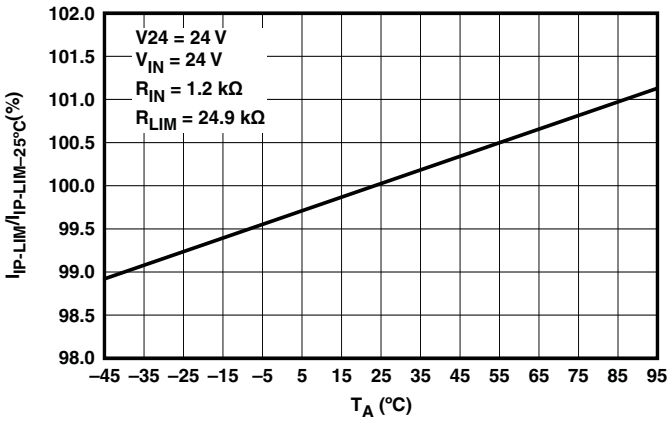



**Figure 2. Typical Current Limiter Variation vs Ambient Temperature**

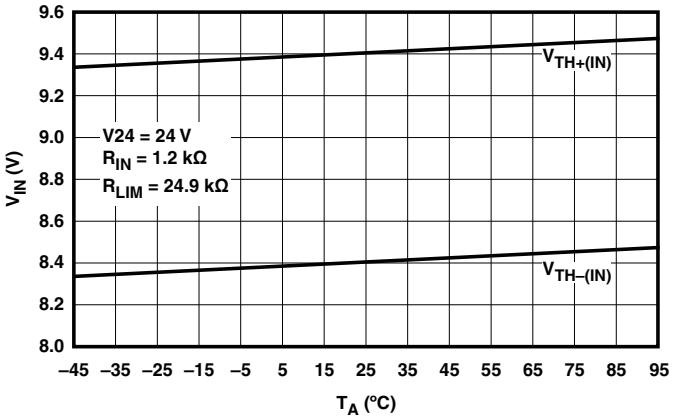



**Figure 3. Typical Limiter Threshold Voltage Variation vs Ambient Temperature**

## PARAMETER MEASUREMENT INFORMATION

### Waveforms

For the complete serial interface timing, refer to Figure 21.

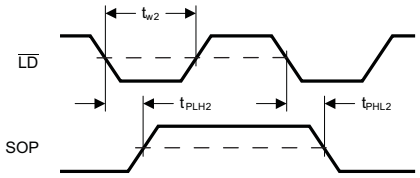



**Figure 4. Parallel – Load Mode**

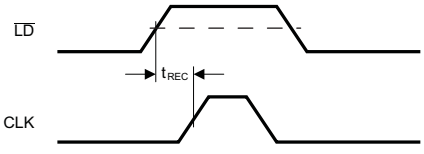



**Figure 5. Serial – Shift Mode**

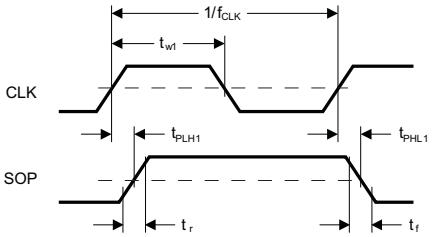



**Figure 6. Serial – Shift Mode**

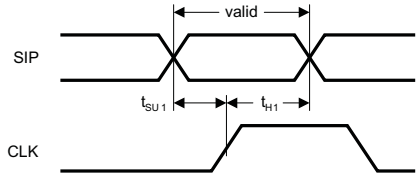



**Figure 7. Serial – Shift Mode**

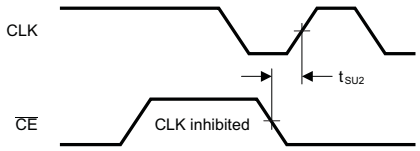



**Figure 8. Serial – Shift Clock Inhibit Mode**

## VOLTAGE REGULATOR PERFORMANCE CHARACTERISTICS

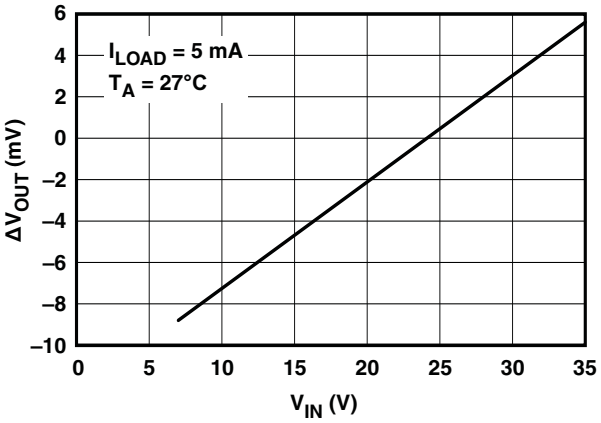



Figure 9. Line Regulation

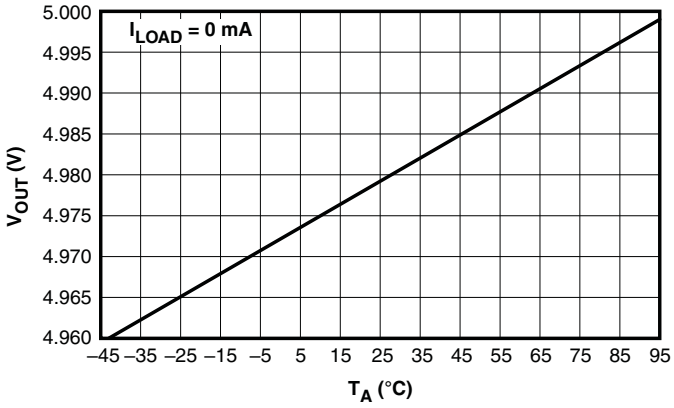



Figure 10. Output Voltage vs Ambient Temperature

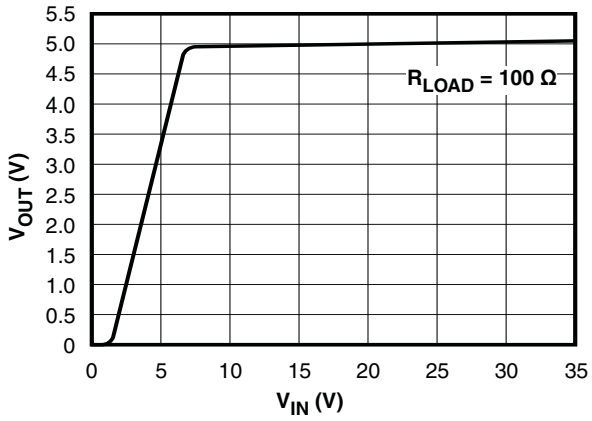



Figure 11. Output Voltage vs Input Voltage

## SIGNAL CONVENTIONS

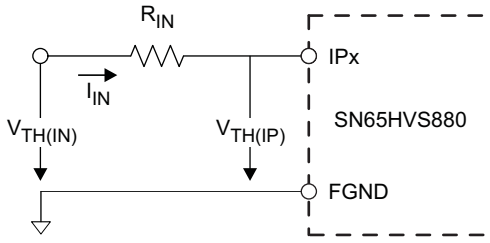



Figure 12. On/Off Threshold Voltage Measurements

## DEVICE INFORMATION

### Digital Inputs

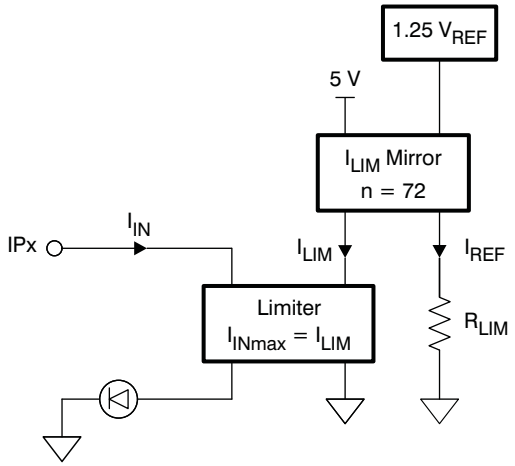



**Figure 13. Digital Input Stage**

Each digital input operates as a controlled current sink limiting the input current to a maximum value of $I_{LIM}$. The current limit is derived from the reference current via $I_{LIM} = n \times I_{REF}$, and $I_{REF}$ is determined by $I_{REF} = V_{REF}/R_{LIM}$. Thus, changing the current limit requires the change of $R_{LIM}$ to a different value via: $R_{LIM} = n \times V_{REF}/I_{LIM}$.

Inserting the actual values for n and $V_{REF}$ gives: $R_{LIM} = 90\ V / I_{LIM}$.

While the device is specified for a current limit of **3.6 mA**, (via $R_{LIM}$ = 25 kΩ), it is easy to lower the current limit to further reduce the power consumption. For example, for a current limit of **2.5 mA** simply calculate:

$$R_{LIM} = \frac{90\ V}{I_{LIM}} = \frac{90\ V}{2.5\ mA} = 36\ k\Omega$$

### Debounce Filter

The HVS880 applies a simple analog/digital filtering technique to remove unintended signal transitions due to contact bounce or other mechanical effects. Any new input (either low or high) must be present for the duration of the selected debounce time to be latched into the shift register as a valid state.

The logic signal levels at the control inputs, DB0 and DB1 of the internal Debounce-Select logic determine the different debounce times listed in the following truth table.

**Table 1. Debounce Times**

| DB1 | DB0 | FUNCTION |
|---|---|---|
| Open | Open | 3 ms delay |
| Open | FGND | 1 ms delay |
| FGND | Open | 0 ms delay (Filter bypassed) |
| FGND | FGND | Reserved |

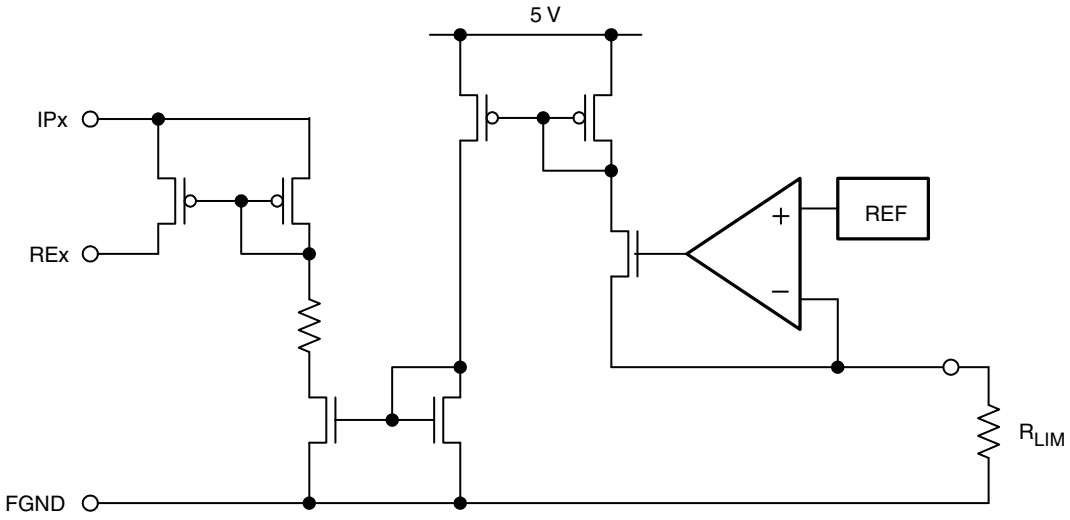



**Figure 14. Equivalent Input Diagram**

## Shift Register

The conversion from parallel input to serial output data is performed by an eight-channel, parallel-in serial-out shift register. Parallel-in access is provided by the internal inputs, PIP0–PIP7, that are enabled by a low level at the load input ($\overline{LD}$). When clocked, the latched input data shift towards the serial output (SOP). The shift register also provides a clock-enable function.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while $\overline{LD}$ is held high and the clock enable ($\overline{CE}$) input is held low. Parallel loading is inhibited when $\overline{LD}$ is held high. The parallel inputs to the register are enabled while $\overline{LD}$ is low independently of the levels of the CLK, $\overline{CE}$, or serial (SIP) inputs.

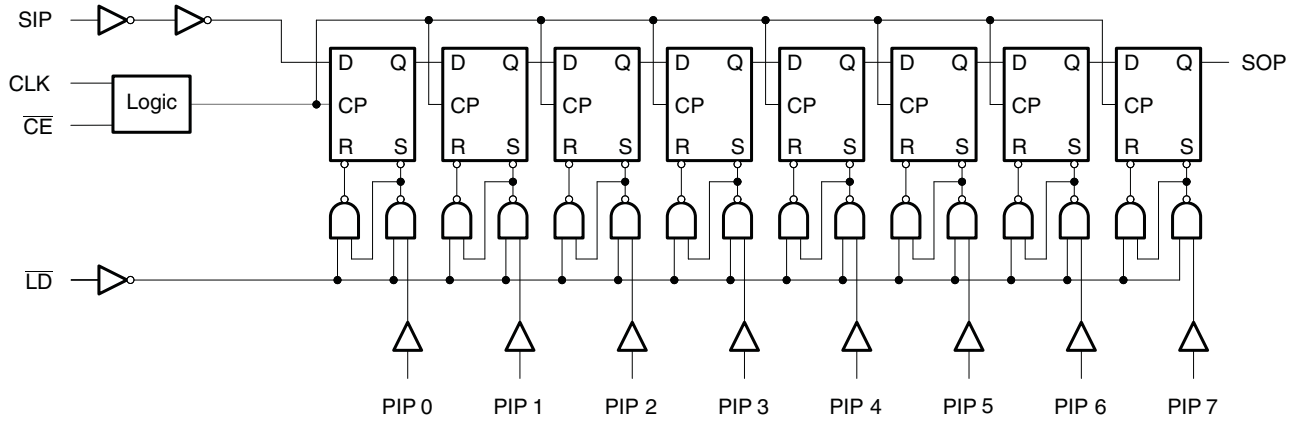



**Figure 15. Shift Register Logic Structure**

**Table 2. Function Table**

| INPUTS | | | FUNCTION |
|---|---|---|---|
| $\overline{LD}$ | CLK | $\overline{CE}$ | |
| L | X | X | Parallel load |
| H | X | H | No change |
| H | ↑ | L | Shift(1) |

(1) Shift = content of each internal register shifts towards serial outputs. Data at SIP is shifted into first register.

## Voltage Regulator

The on-chip linear voltage regulator provides a 5 V supply to the internal- and external circuitry, such as digital isolators, with an output drive capability of 50 mA and a typical current limit of 115 mA. The regulator accepts input voltages from 30 V down to 10 V. Because the regulator output is intended to supply external digital isolator circuits proper output voltage decoupling is required. For best results connect a 1 µF and a 0.1 µF ceramic capacitor as close as possible to the 5VOP-output. For longer traces between the SN65HVS880 and isolators of the ISO72xx family use additional 0.1 µF and 10 pF capacitors next to the isolator supply pins. Make sure, however, that the total load capacitance does not exceed 4.7 µF.

For good stability the voltage regulator requires a minimum load current, $I_{L\text{-}MIN}$. Ensure that under any operating condition the ratio of the minimum load current in mA to the total load capacitance in µF is larger than 1:

$$\frac{I_{L\text{-}MIN}}{C_L} > \frac{1\ mA}{1\ \mu F}$$

## Supply Voltage Monitor

The integrated supply voltage monitor senses the supply voltage of the SN65HVS880 at the V24-pin. If this voltage drops below 15 V but stays within the regulator's operating range, i.e., 15 V > V24 > 10 V, the output CHOK goes low 1 ms later. When the supply voltage returns to 24 V, the CHOK output turns logic high after 6 ms. Should the supply voltage drop below 10 V, the device ceases operation. Upon the supply returning to above 18 V, the CHOK output turns high again after 6 ms.

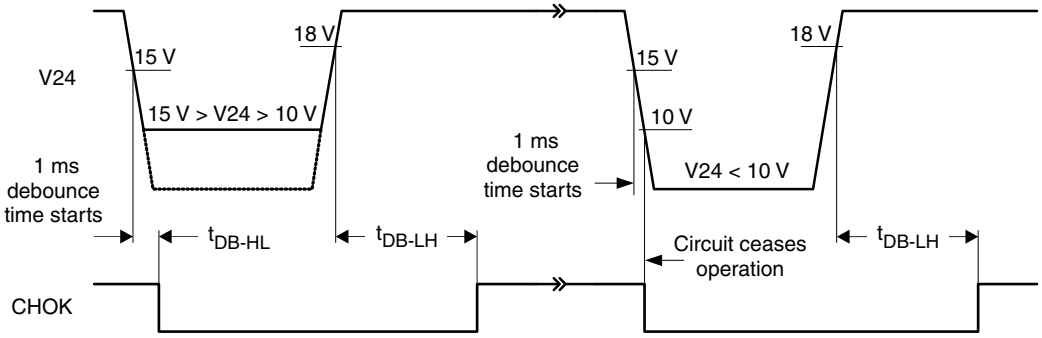



**Figure 16. CHOK Output Timing as a Function of Supply Voltage Drop at V24**

## Temperature Sensor

An on-chip temperature sensor monitors the device temperature and signals a fault condition if the device becomes too hot. A first trip point exists at 150°C. If the junction temperature exceeds this trip point, the sensor output, being active low, presents a low to the input of the AND gate forcing the CHOK output to go low. If the junction temperature continues to rise, passing a second trip point at 170°C, all device outputs assume tri-state.

## Chip Okay (CHOK) Output

The CHOK output is the Boolean AND-function of the two, active-low fault conditions: temperature failure and supply failure. As such CHOK is a device health indicator, assuming logic high in the absence of any fault condition. If either one of the two or both fault conditions occur, CHOK becomes logic low.

A special condition occurs, however, when the chip temperature exceeds the second temperature trip point due to an output short. Then the CHOK output buffer becomes tri-state, thus separating the buffer from the external circuitry. An internal 100 kΩ pulldown resistor, connecting the CHOK-pin to ground, is used as a “cooling down” resistor, which continues to provide a logic low level to the external circuitry.

## APPLICATION INFORMATION

### System-Level EMC

The SN65HVS880 must operate reliably in harsh industrial environments. At a system level, the device is tested according to several international electromagnetic compatibility (EMC) standards.

In addition to the device internal ESD structures, external protection circuitry, such as the one in Figure 17, is needed to absorb as much energy from burst- and surge-transients as possible.

| | |
|---|---|
| $D_{TS}$ | 39V Transient Voltage Suppressor. SM15T39CA |
| $D_{RP}$ | Super Rectifier. BYM10-1000, or General Purpose rectifier. 1N4007 |
| $D_Z$ | 33 V – 36 V fast Zener Diode, Z2SMB36 |
| $R_S$ | 56 Ω, 1/3 W MELF Resistor |
| $R_{IN}$ | 1.2 kΩ, 1/4 W MELF Resistor |
| $C_{IN}$ | 22 nF, 60 V Ceramic Capacitor |
| $C_{HV}$ | 4.7 nF, 2 kV Ceramic Capacitor |
| $C_C$ | n x 220 nF, 60 V Ceramic Capacitors |
| $C_B$ | 1 µF - 10 µF, 60 V Ceramic Capacitor |

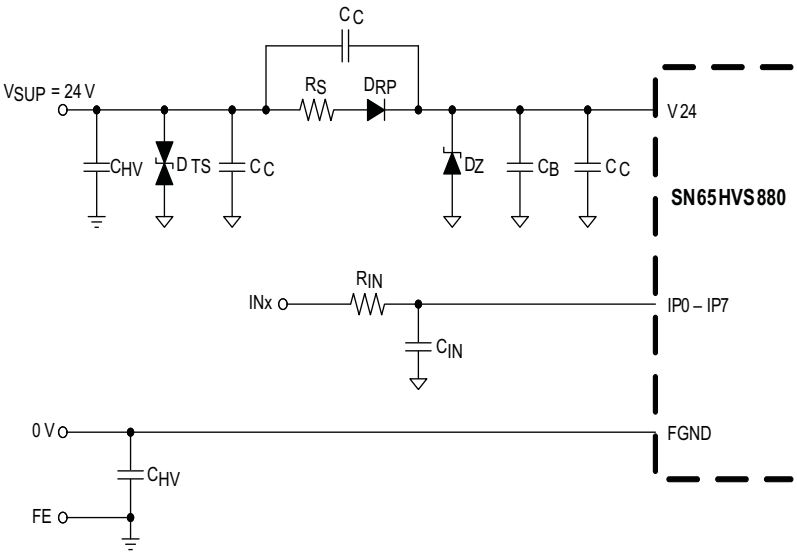



**Figure 17. Typical EMC Protection Circuitry for Supply and Signal Inputs**

### Input Channel Switching Characteristics

The input stage of the HVS880 is so designed, that for an input resistor $R_{IN}$ = 1.2 kΩ the trip point for signalling an ON-condition is at 9.4 V at 3.6 mA. This trip point satisfies the switching requirements of IEC61131-2 Type 1 and Type 3 switches.

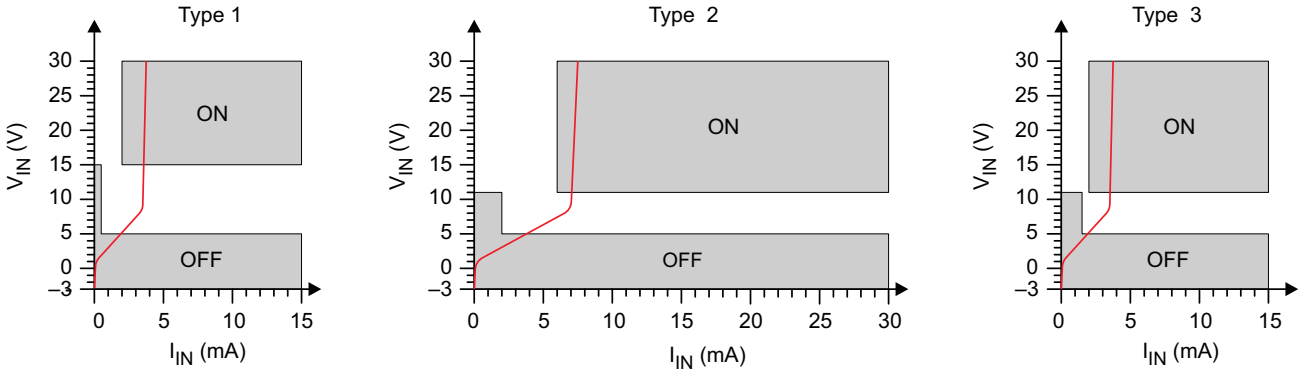



**Figure 18. Switching Characteristics for IEC61131-2 Type 1, 2, and 3 Proximity Switches**

For a Type 2 switch application, two inputs are connected in parallel. The current limiters then add to a total maximum current of 7.2 mA. While the return-path (RE-pin), of one input might be used to drive an indicator LED, the RE-pin of the other input channel should be connected to ground (FGND).

Paralleling input channels reduces the number of available input channels from an octal Type 1 or Type 3 input to a quad Type 2 input device. Note, that in this configuration output data of an input channel is represented by two shift register bits.

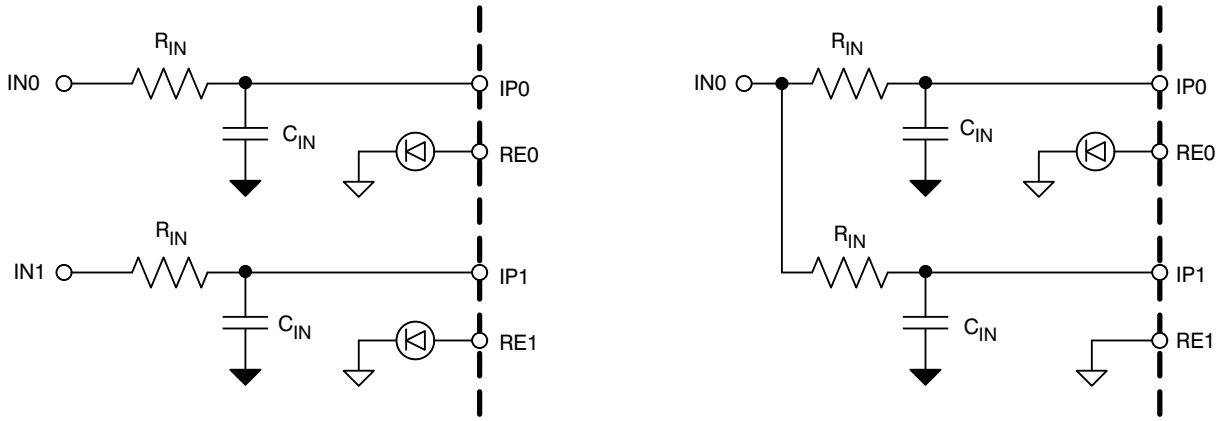



**Figure 19. Paralleling Two Type 1 or Type 3 Inputs Into One Type 2 Input**

## Digital Interface Timing

The digital interface of the SN65HVS880 is SPI compatible and interfaces, isolated or non-isolated, to a wide variety of standard micro controllers.

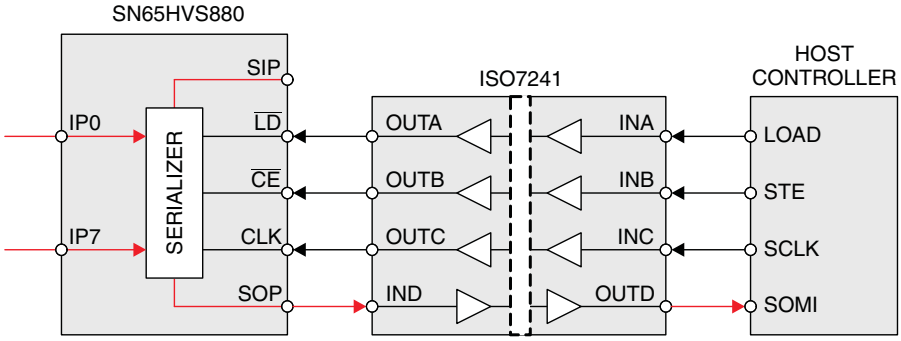



**Figure 20. Simple Isolation of the Shift Register Interface**

Upon a low-level at the load input, $\overline{LD}$, the information of the field inputs, IP0 to IP7 is latched into the shift register. Taking /LD high again blocks the parallel inputs of the shift register from the field inputs. A low-level at the clock-enable input, $\overline{CE}$, enables the clock signal, CLK, to serially shift the data to the serial output, SOP. Data is clocked at the rising edge of CLK. Thus after eight consecutive clock cycles all field input data have been clocked out of the shift register and the information of the serial input, SIP, appears at the serial output, SOP.

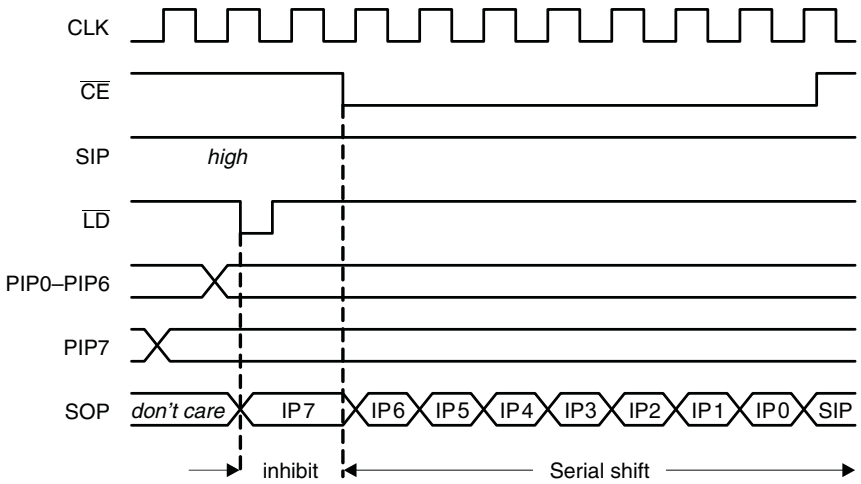



**Figure 21. Interface Timing for Parallel-Load and Serial-Shift Operation of the Shift Register**

## Cascading for High Channel Count Input Modules

Designing high-channel count modules require cascading multiple SN65HVS880 devices. Simply connect the serial output (SOP) of a leading device with the serial input (SIP) of a following device without changing the processor interface.

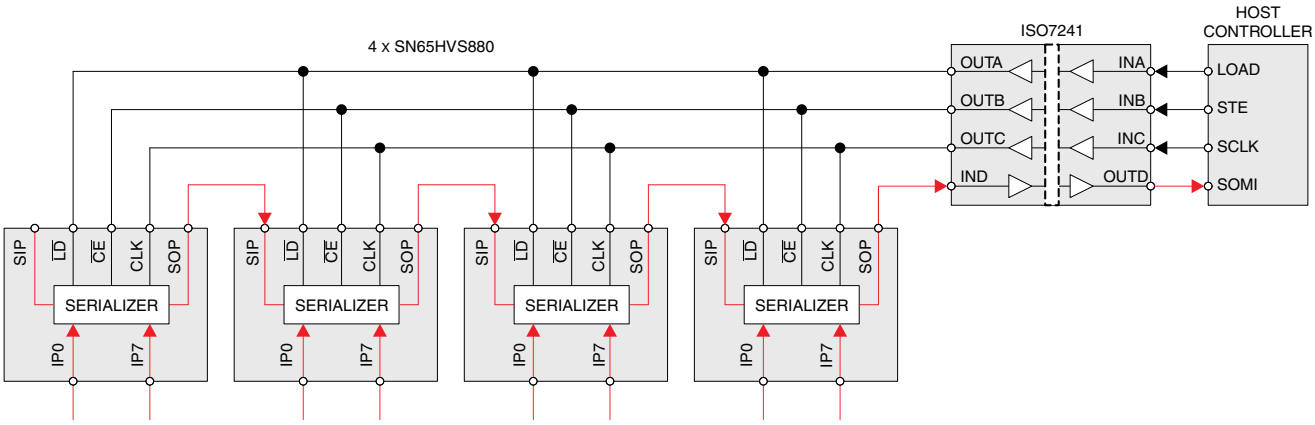



**Figure 22. Cascading Four SN65HVS880 for a 32-Channel Input Module**

## Typical Digital Input Module Application

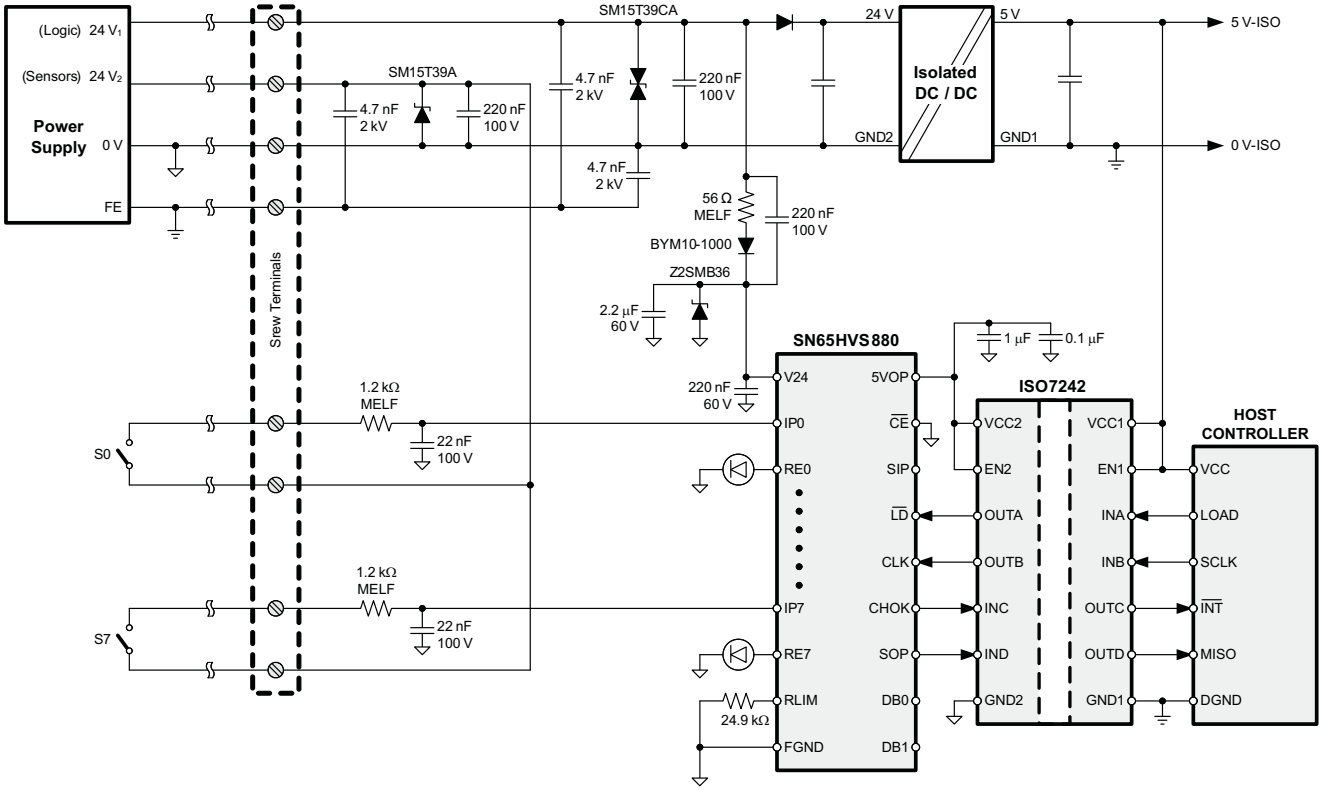



**Figure 23. Typical Digital Input Module Application**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65HVS880PWP | ACTIVE | HTSSOP | PWP | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | HVS880 | Samples |
| SN65HVS880PWPR | ACTIVE | HTSSOP | PWP | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | HVS880 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

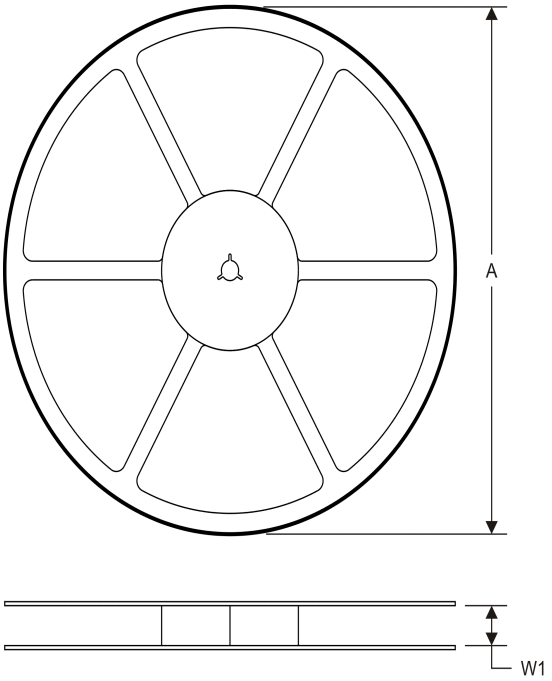
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

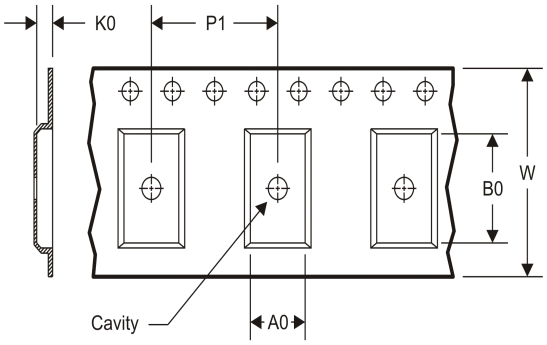
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



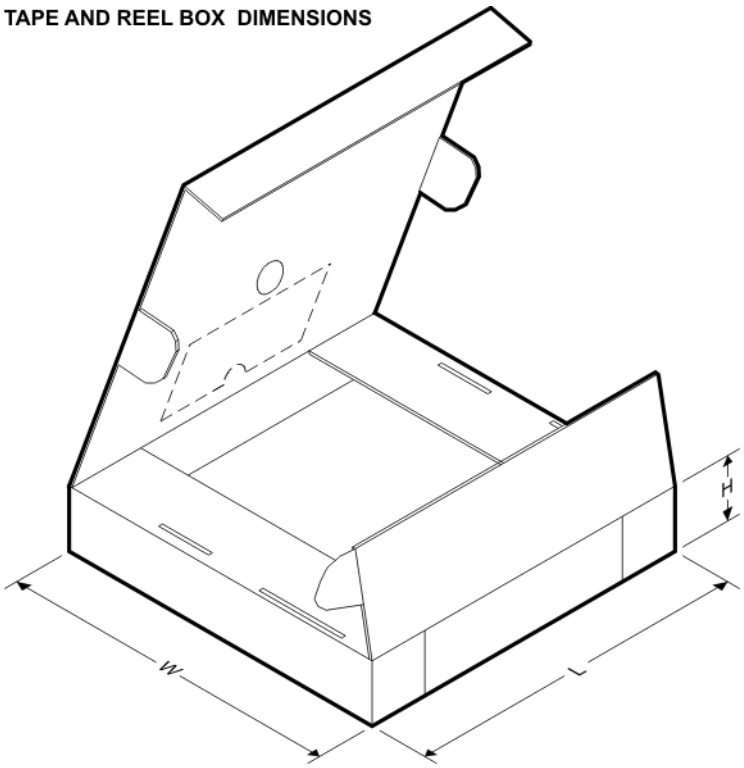

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65HVS880PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |

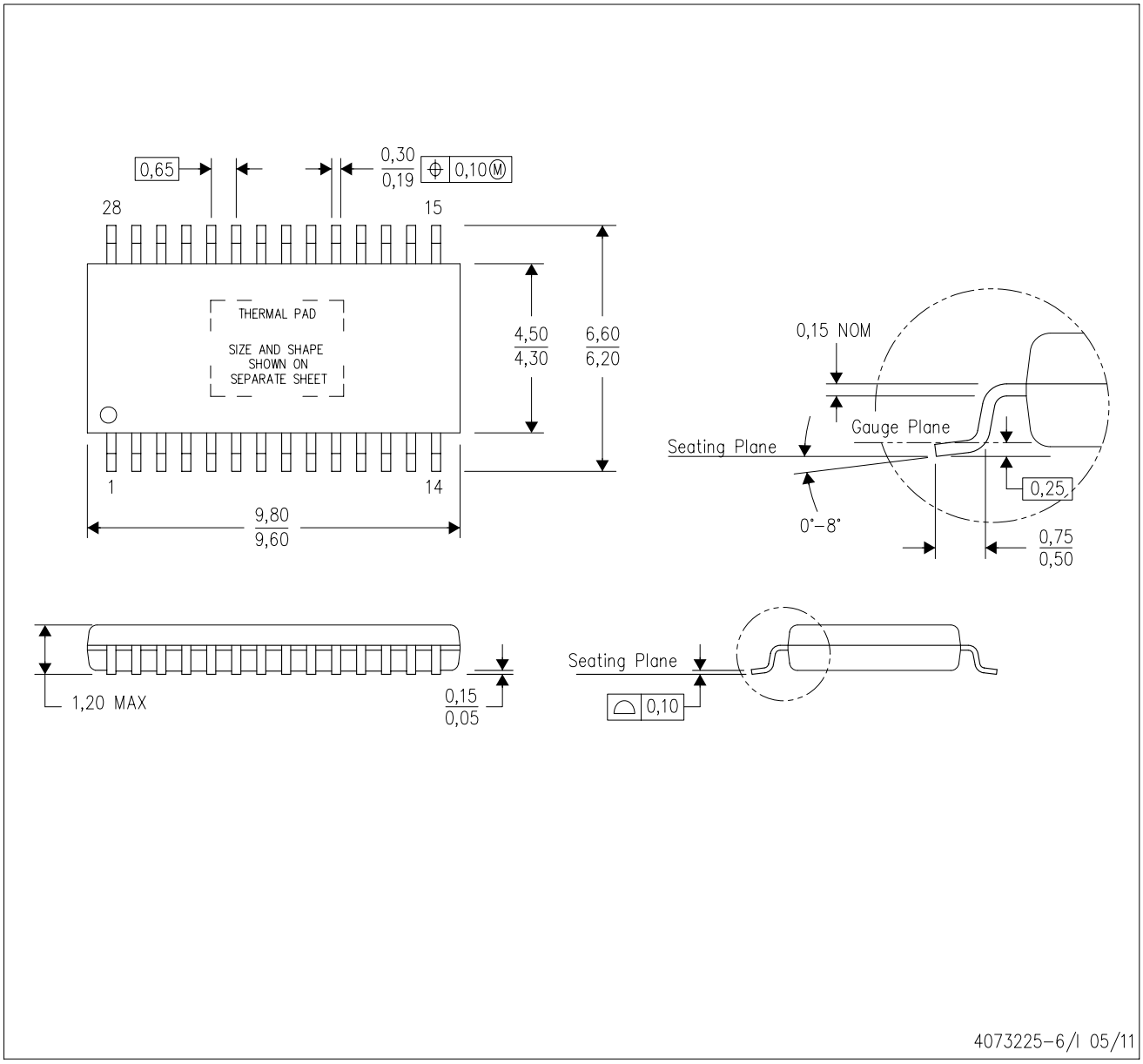
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65HVS880PWPR | HTSSOP | PWP | 28 | 2000 | 367.0 | 367.0 | 38.0 |

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

**PowerPAD is a trademark of Texas Instruments.**

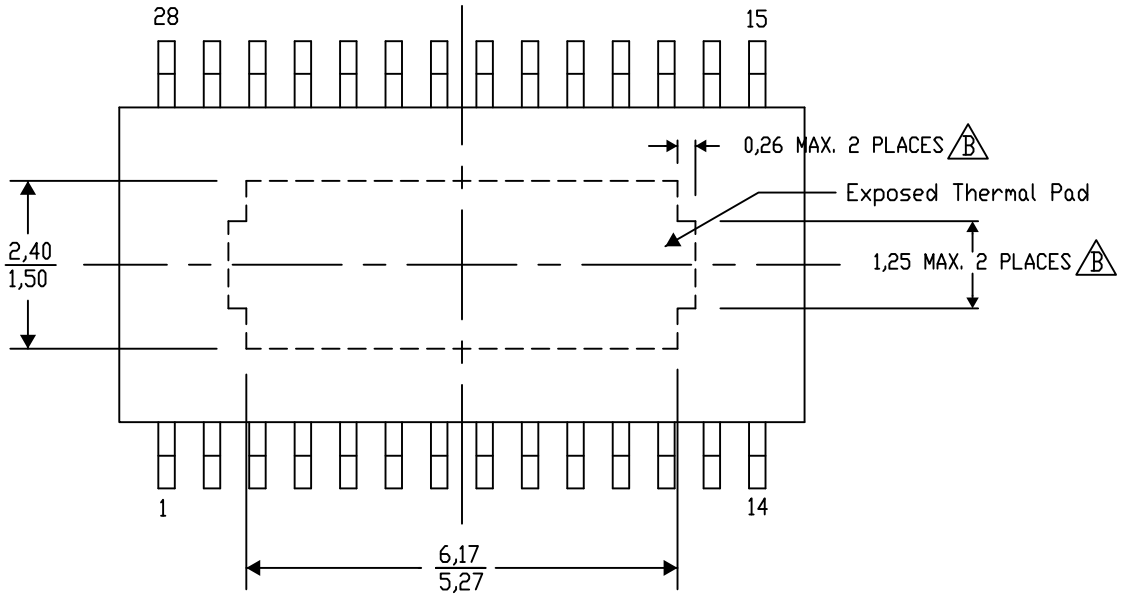
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

4206332–33/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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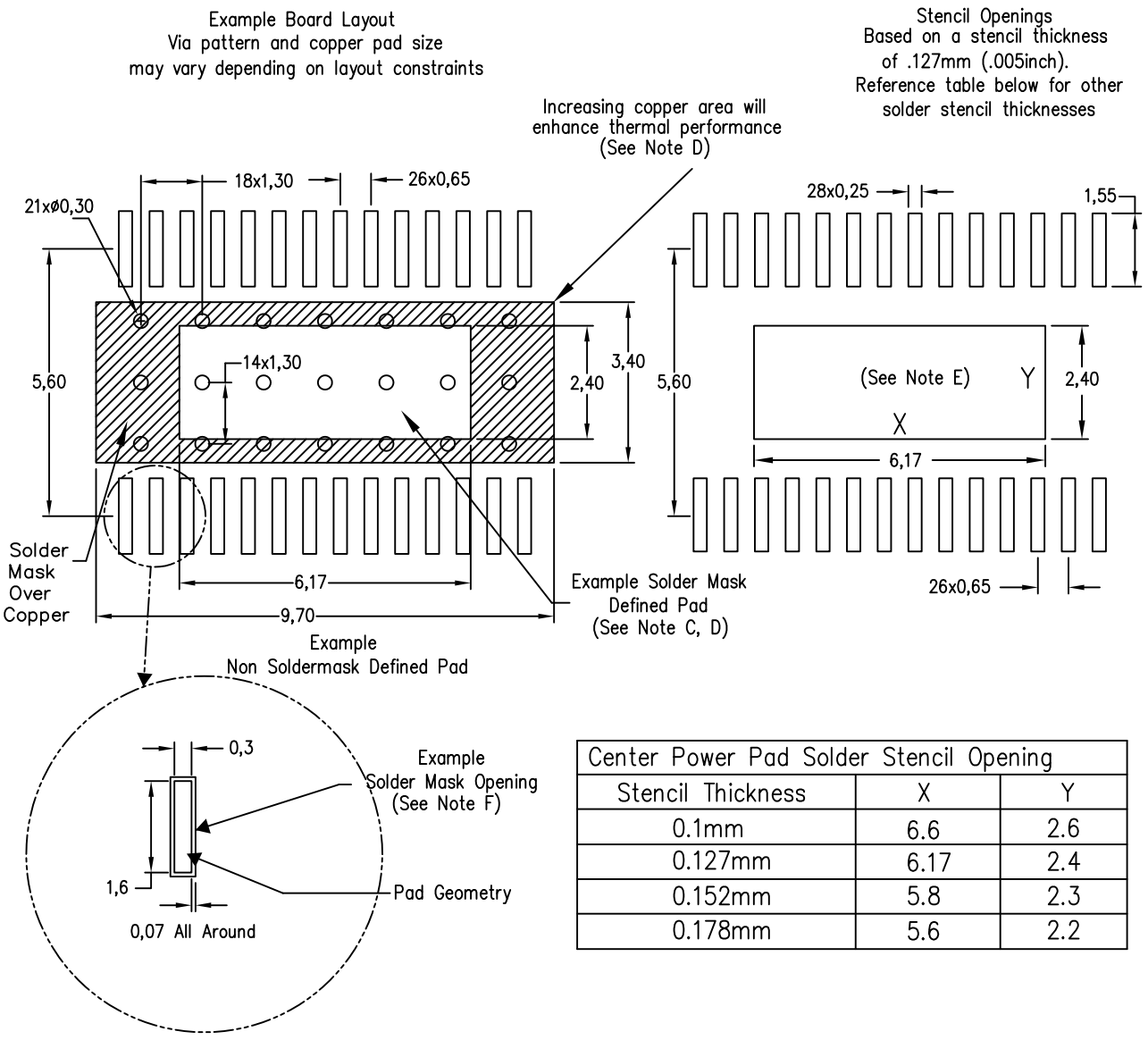
## PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 6.6 | 2.6 |
| 0.127mm | 6.17 | 2.4 |
| 0.152mm | 5.8 | 2.3 |
| 0.178mm | 5.6 | 2.2 |

4207609–19/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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