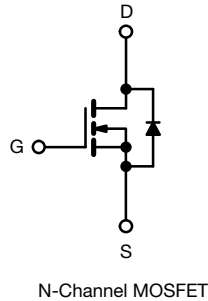


## E Series Power MOSFET

**TO-220 FULLPAK**


### FEATURES

- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	700	
$R_{DS(on)}$ max. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V	0.38
$Q_g$ max. (nC)	70	
$Q_{gs}$ (nC)	9	
$Q_{gd}$ (nC)	16	
Configuration	Single	

### ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free and Halogen-free	SiHF12N65E-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)


PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	650	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current ( $T_J = 150$ °C) <sup>e</sup>	$V_{GS}$ at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	28	
Linear Derating Factor		0.26	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	226	mJ
Maximum Power Dissipation	$P_D$	33	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	°C
Drain-Source Voltage Slope	$dV/dt$	$T_J = 125$ °C	37
Reverse Diode $dV/dt$ <sup>d</sup>		28	
Soldering Recommendations (Peak temperature) <sup>c</sup>	For 10 s	300	°C
Mounting Torque	M3 screw	0.6	Nm

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 4$  A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C.
- Limited by maximum junction temperature.



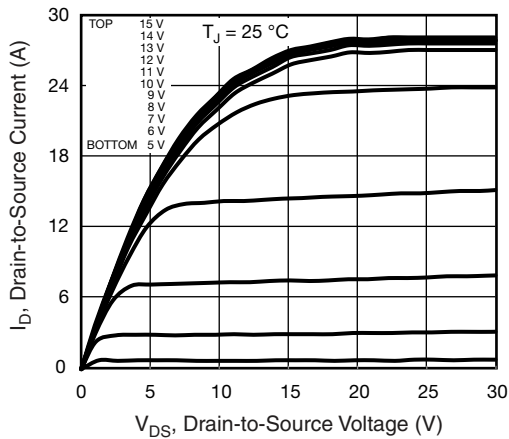
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-	65	°C/W
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	3.8	

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		650	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.78	-	V/°C
Gate-Source Threshold Voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2	-	4	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
		V <sub>GS</sub> = ± 30 V		-	-	± 1	μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 650 V, V <sub>GS</sub> = 0 V		-	-	1	μA
		V <sub>DS</sub> = 520 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	10	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 6 A	-	0.33	0.38	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 6 A		-	3.5	-	S
<b>Dynamic</b>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, f = 1 MHz		-	1224	-	pF
Output Capacitance	C <sub>oss</sub>			-	65	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	4	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	C <sub>o(er)</sub>			-	50	-	
Effective Output Capacitance, Time Related <sup>b</sup>	C <sub>o(tr)</sub>	V <sub>DS</sub> = 0 V to 520 V, V <sub>GS</sub> = 0 V		-	160	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 6 A, V <sub>DS</sub> = 520 V	-	35	70	nC
Gate-Source Charge	Q <sub>gs</sub>			-	9	-	
Gate-Drain Charge	Q <sub>gd</sub>			-	16	-	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 520 V, I <sub>D</sub> = 6 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 9.1 Ω		-	16	32	ns
Rise Time	t <sub>r</sub>			-	19	38	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	35	70	
Fall Time	t <sub>f</sub>			-	18	36	
Gate Input Resistance	R <sub>g</sub>	f = 1 MHz, open drain		-	0.81	-	Ω
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	12	A
Pulsed Diode Forward Current	I <sub>SM</sub>			-	-	28	
Diode Forward Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 6 A, V <sub>GS</sub> = 0 V		-	1.0	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 6 A, di/dt = 100 A/μs, V <sub>R</sub> = 25 V		-	309	618	ns
Reverse Recovery Charge	Q <sub>rr</sub>			-	3.8	7.6	μC
Reverse Recovery Current	I <sub>RRM</sub>			-	21	-	A

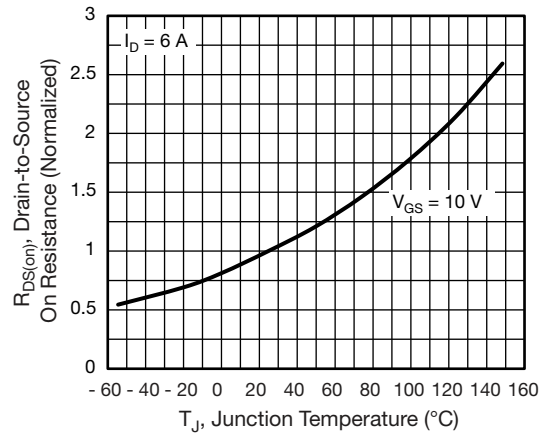
**Notes**

- a. C<sub>oss(er)</sub> is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DSS</sub>.
- b. C<sub>oss(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DSS</sub>.

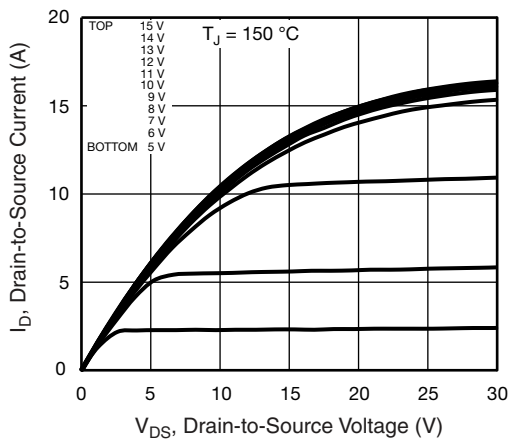
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



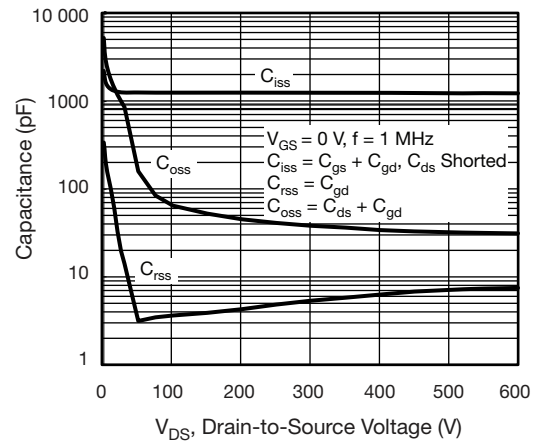
**Fig. 1 - Typical Output Characteristics**



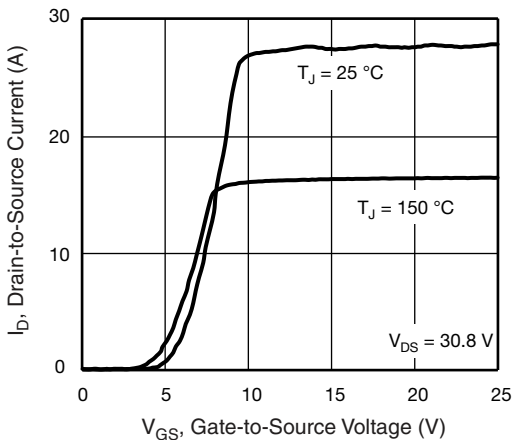
**Fig. 4 - Normalized On-Resistance vs. Temperature**



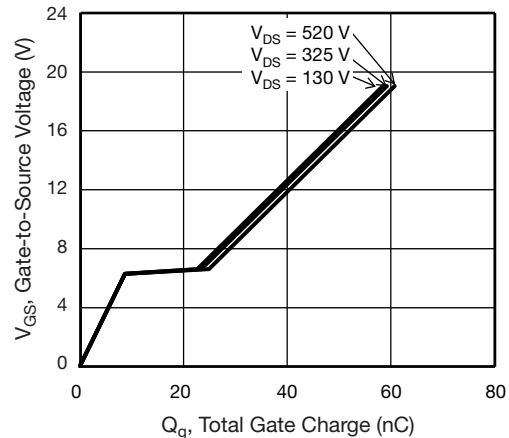
**Fig. 2 - Typical Output Characteristics**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

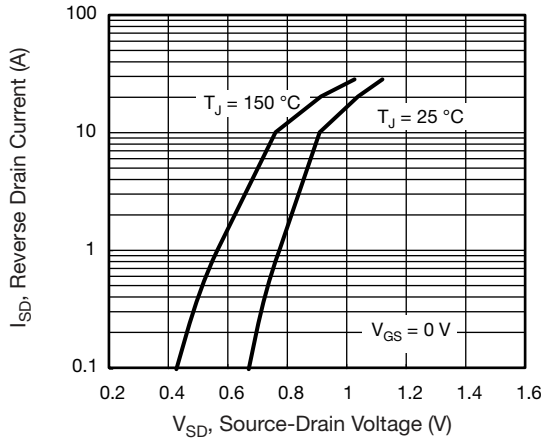


Fig. 7 - Typical Source-Drain Diode Forward Voltage

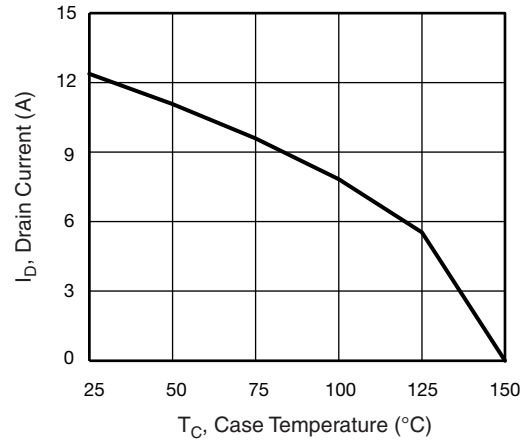


Fig. 9 - Maximum Drain Current vs. Case Temperature

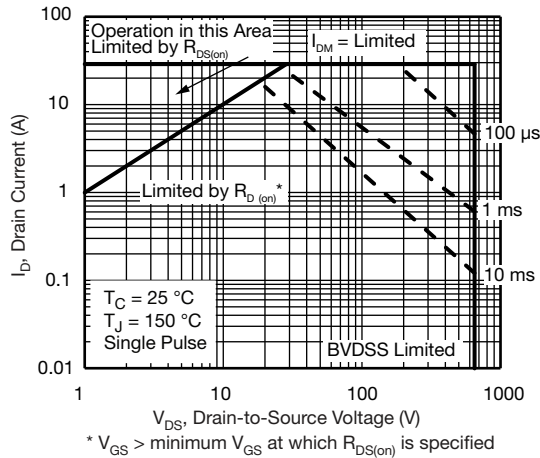


Fig. 8 - Maximum Safe Operating Area

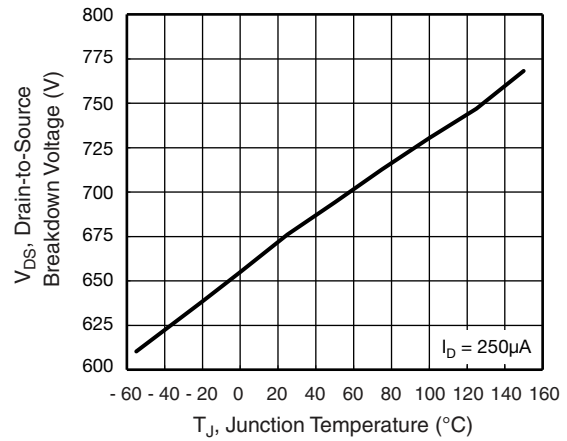


Fig. 10 - Temperature vs. Drain-to-Source Voltage

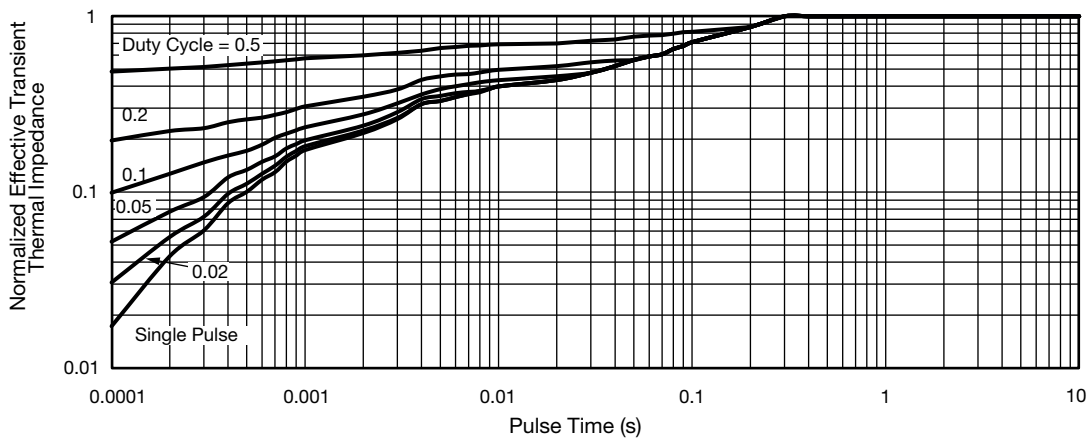


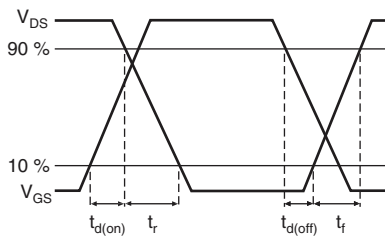
Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case



**Fig. 12 - Switching Time Test Circuit**



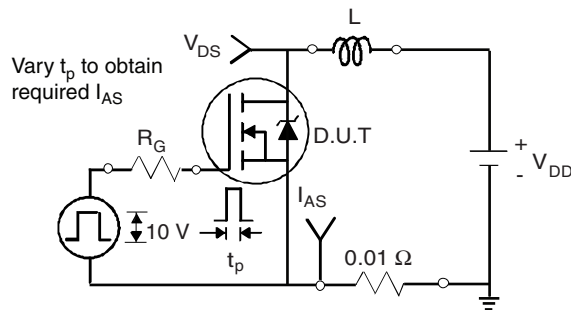
**Fig. 16 - Basic Gate Charge Waveform**



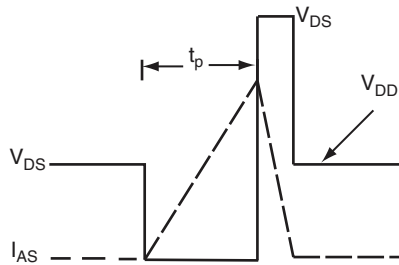
**Fig. 13 - Switching Time Waveforms**



**Fig. 17 - Gate Charge Test Circuit**



**Fig. 14 - Unclamped Inductive Test Circuit**



**Fig. 15 - Unclamped Inductive Waveforms**



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 18 - For N-Channel**

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