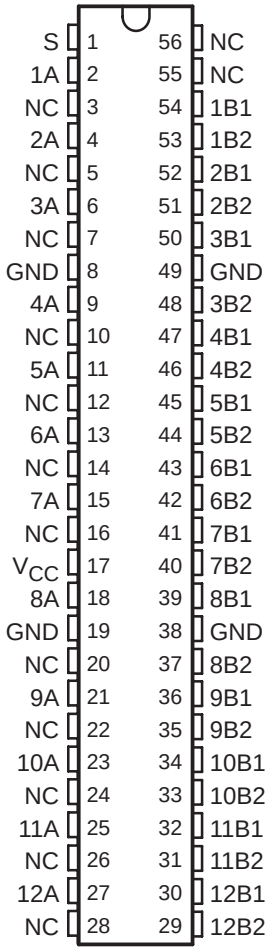
- **Member of the Texas Instruments Widebus™ Family**
- **4-Ω Switch Connection Between Two Ports**
- **Rail-to-Rail Switching on Data I/O Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Make-Before-Break Feature**
- **Internal 500-Ω Pulldown Resistors to Ground**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The SN74CBTLV16292 is a 12-bit 1-of-2 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1, and R_{INT} is connected to port B2. When S is high, port A is connected to port B2, and R_{INT} is connected to port B1.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

ORDERING INFORMATION

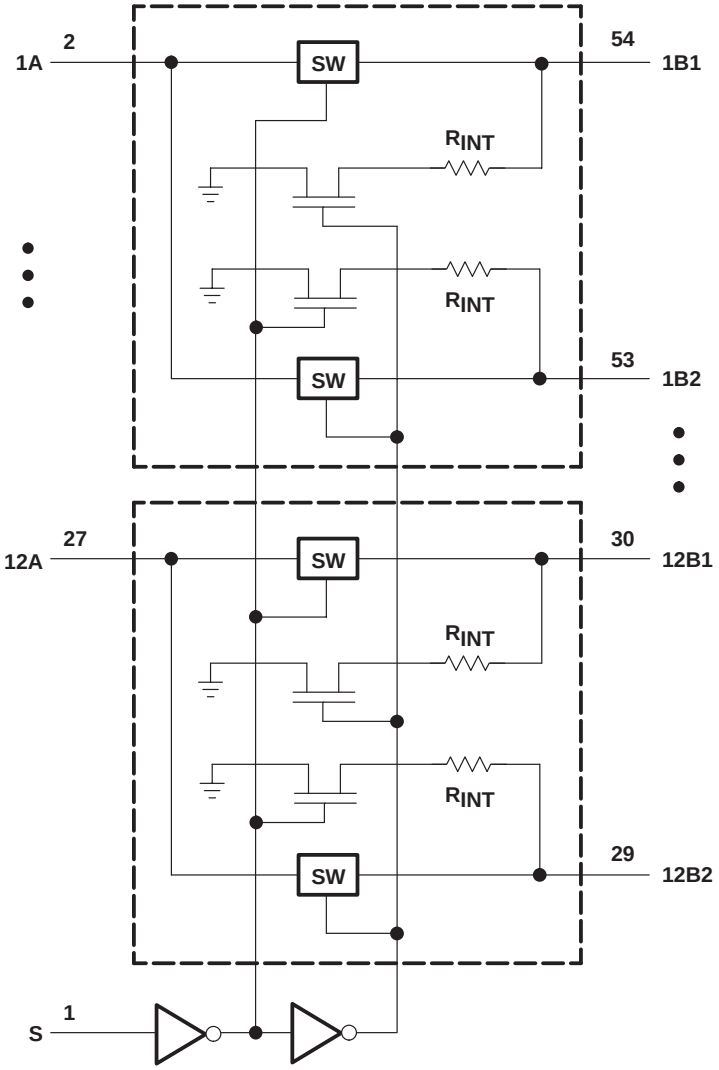
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBTLV16292DL	CBTLV16292
		Tape and reel	SN74CBTLV16292DLR	
	TSSOP − DGG	Tape and reel	SN74CBTLV16292GR	CBTLV16292
	TVSOP − DGV	Tape and reel	SN74CBTLV16292VR	CN292

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

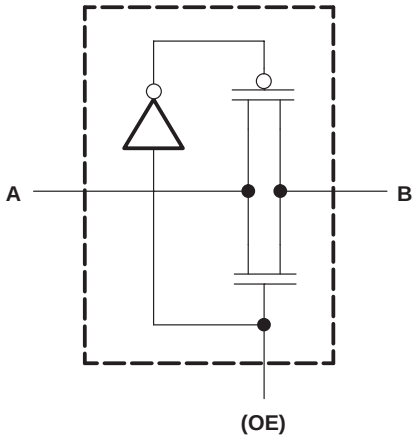
FUNCTION TABLE

INPUT S	FUNCTION
L	A port = B1 port R_{INT} = B2 port
H	A port = B2 port R_{INT} = B1 port

logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 4.6 V
Continuous channel current . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . −50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . . 64°C/W
DGV package . . . . . 48°C/W
DL package . . . . . 56°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±1	μA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				10	μA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND			10	μA
ΔI_{CC}‡	Control input	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	μA
C_i	Control input	V_I = 3.3 V or 0				3.5		pF
C_{io}	A or B port	V_O = 3.3 V or 0				22.5		pF
r_{on}§		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		5	8	Ω
				I_I = 24 mA		5	8	
			V_I = 1.7 V,	I_I = 15 mA		11	40	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		3	7	
				I_I = 24 mA		3	7	
			V_I = 2.4 V,	I_I = 15 mA		7	15	

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.15		0.25	ns
t_{pd}#	S	A	2.5	7.1	2.5	6.7	ns
t_{en}	S	B	1	5.6	1	5	ns
t_{dis}	S	B	1	5	1	4.5	ns

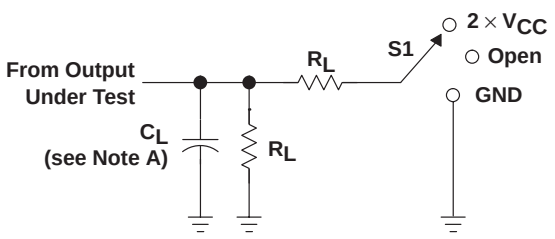
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
# This propagation delay was measured by observing the change of voltage on the A output introduced by static levels equal to 3-V or 0 for 3.3 V ± 0.3 V or V_{CC} or 0 for 2.5 V ± 0.2 V on B1 and B2 to achieve the desired transition.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	DESCRIPTION	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_{mbb}‖	Make-before-break time	0	2	0	2	ns

‖ The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.

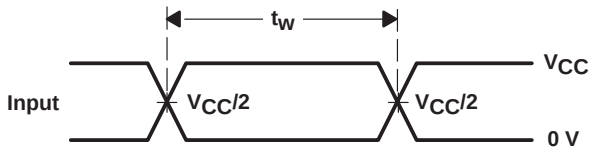
PARAMETER MEASUREMENT INFORMATION



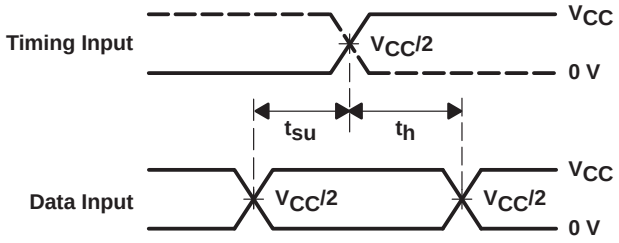
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

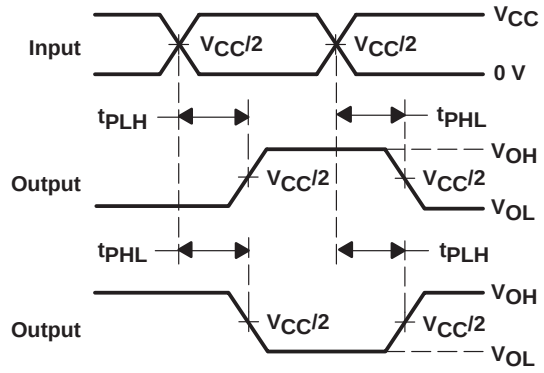
V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V



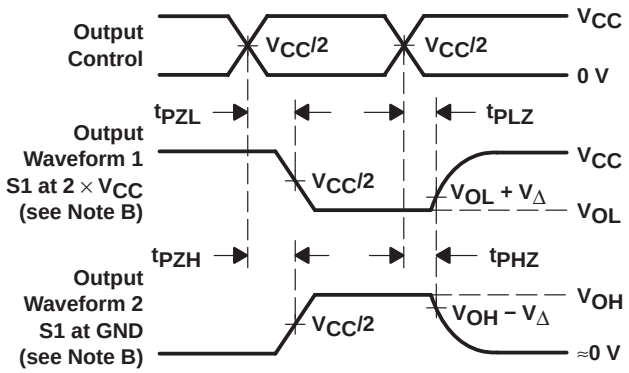
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBTLV16292DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV16292	Samples
SN74CBTLV16292DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV16292	Samples
SN74CBTLV16292GR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV16292	Samples
SN74CBTLV16292VR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CN292	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

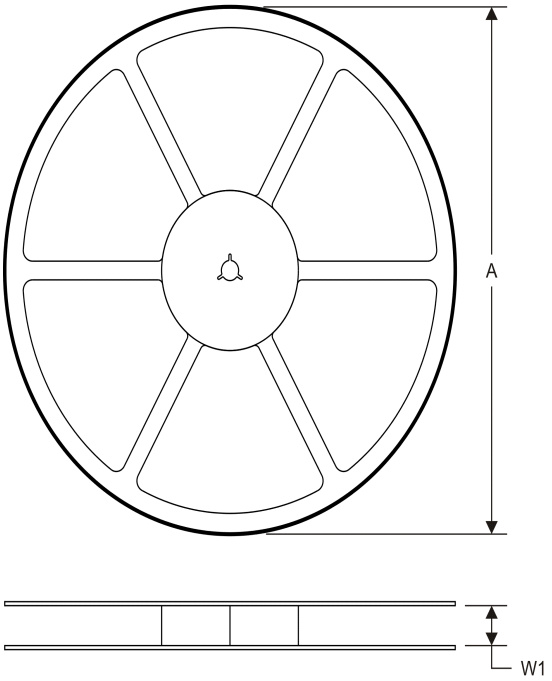
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

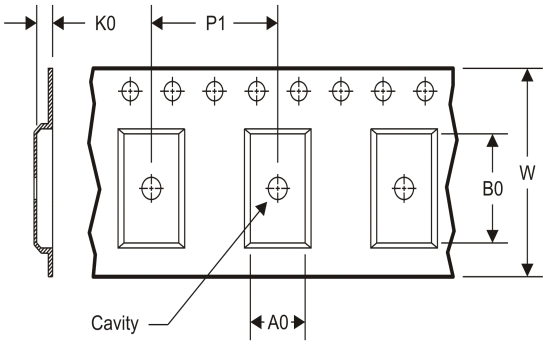
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



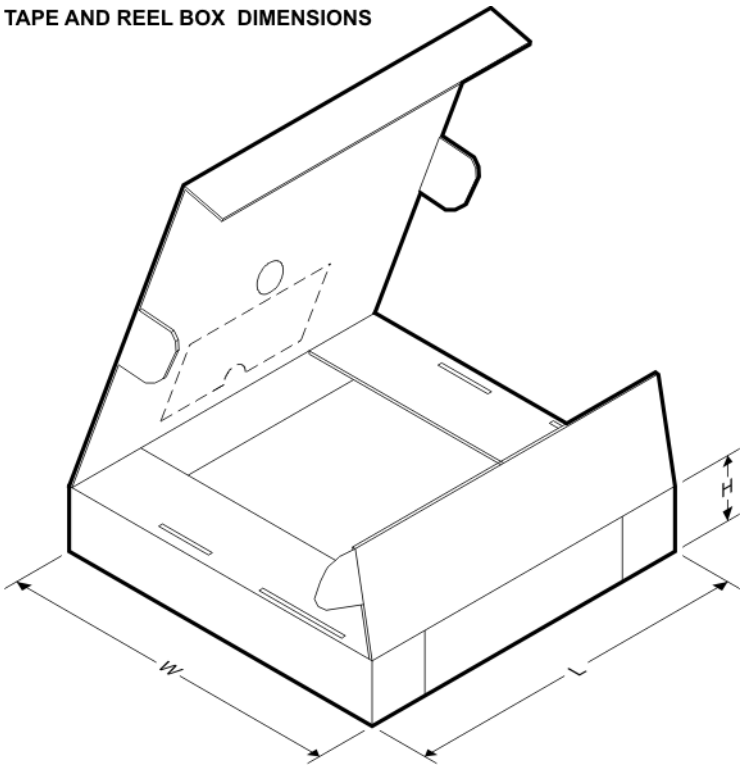
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTLV16292DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN74CBTLV16292GR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74CBTLV16292VR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

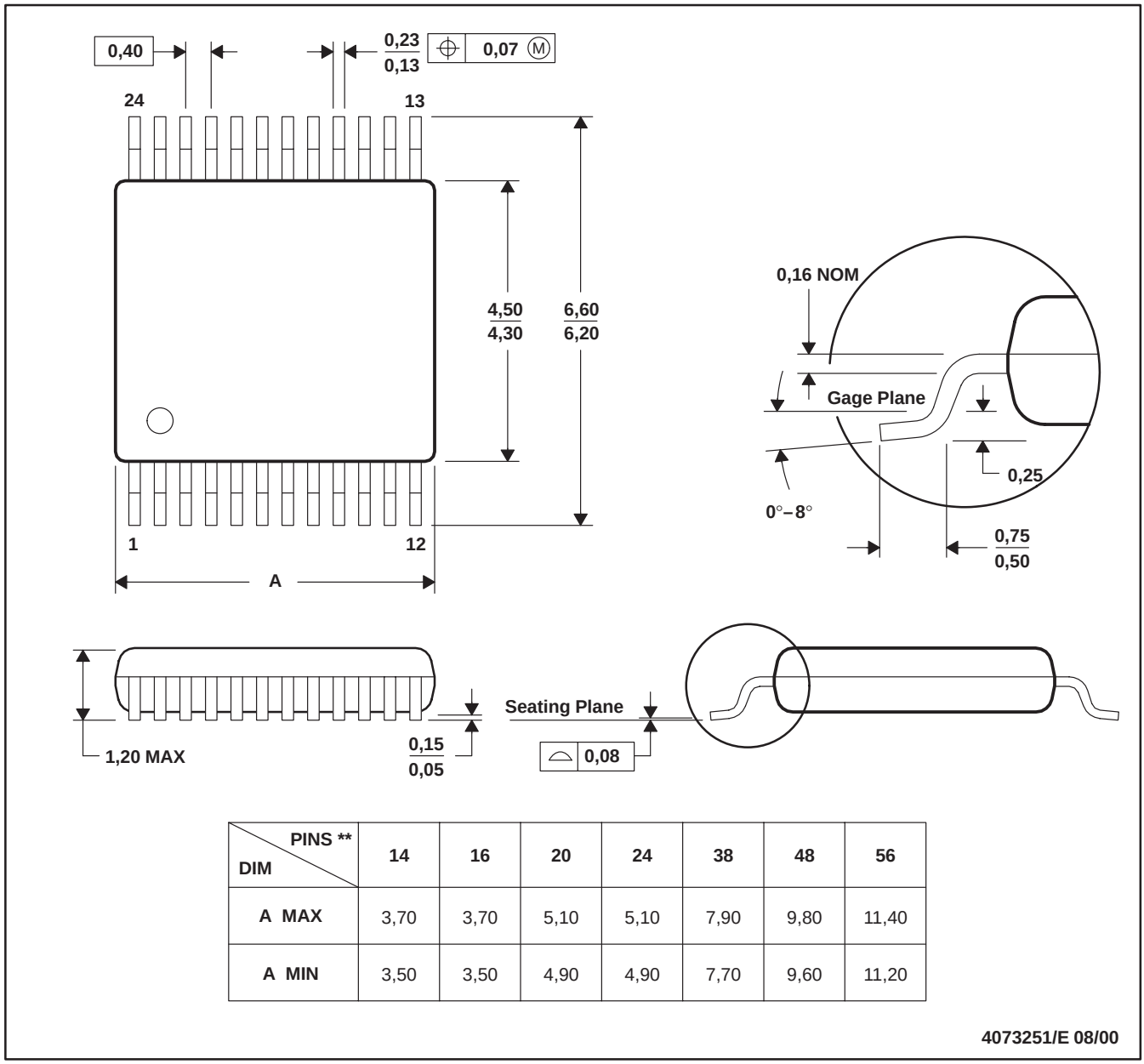


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTLV16292DLR	SSOP	DL	56	1000	367.0	367.0	55.0
SN74CBTLV16292GR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74CBTLV16292VR	TVSOP	DGV	56	2000	367.0	367.0	45.0

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

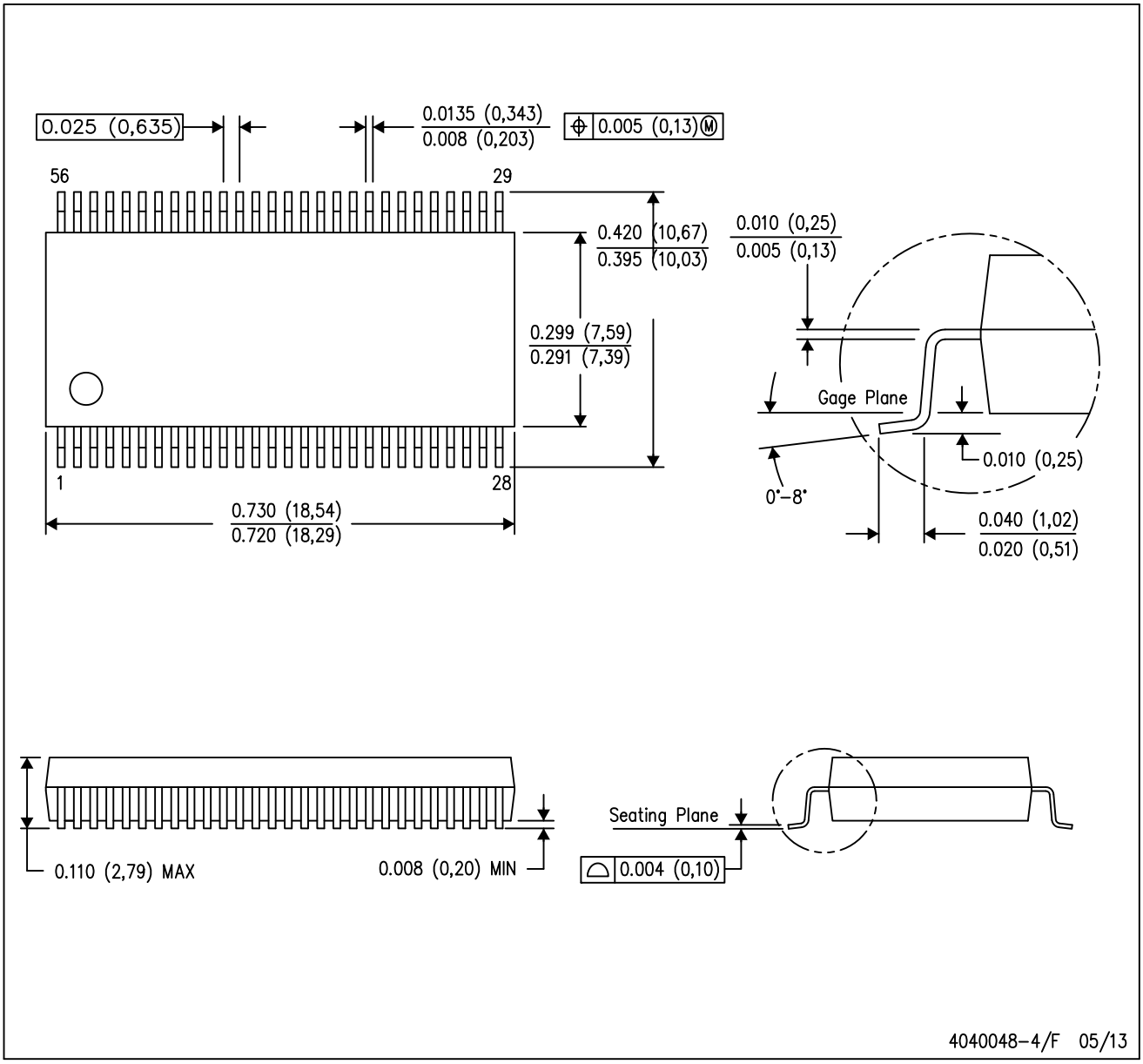


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

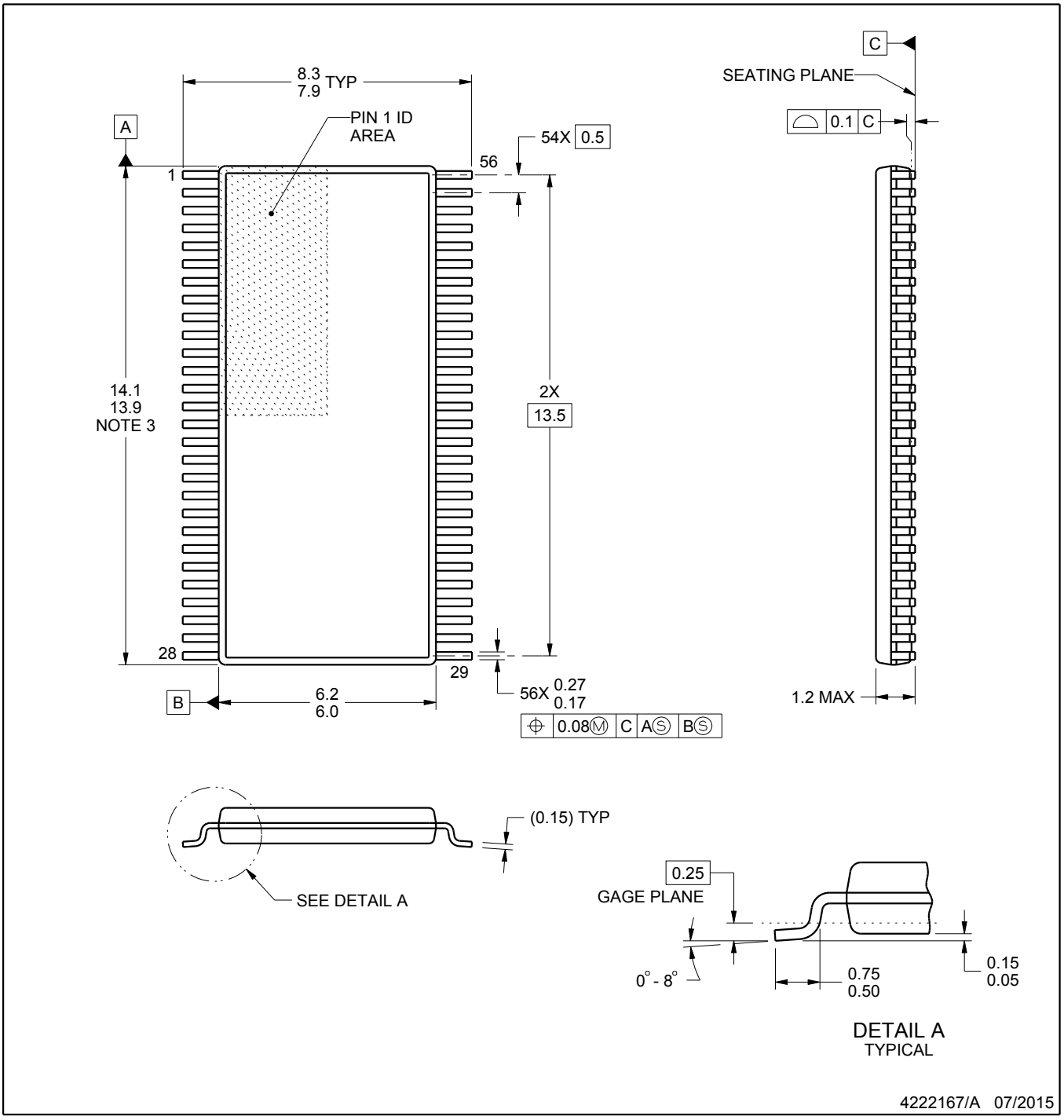
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DGG0056A

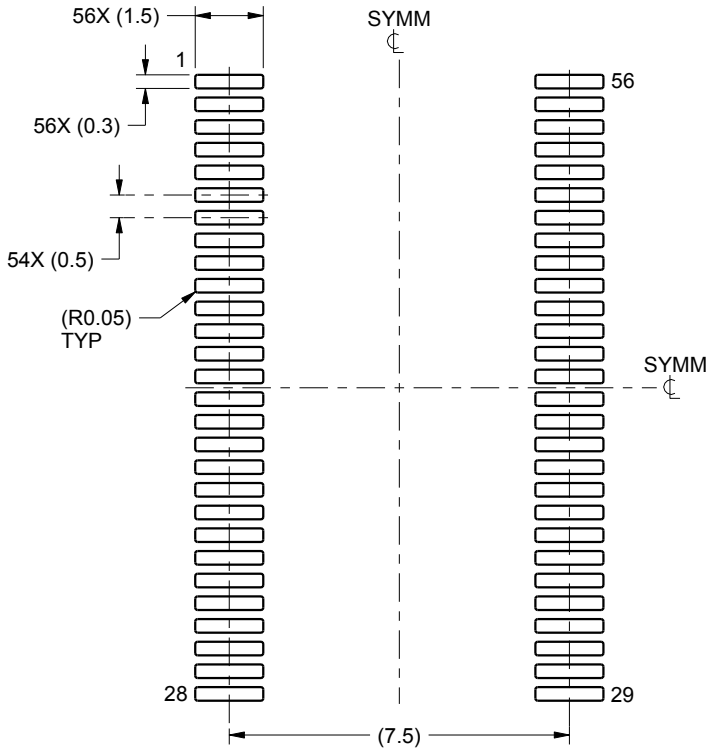
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

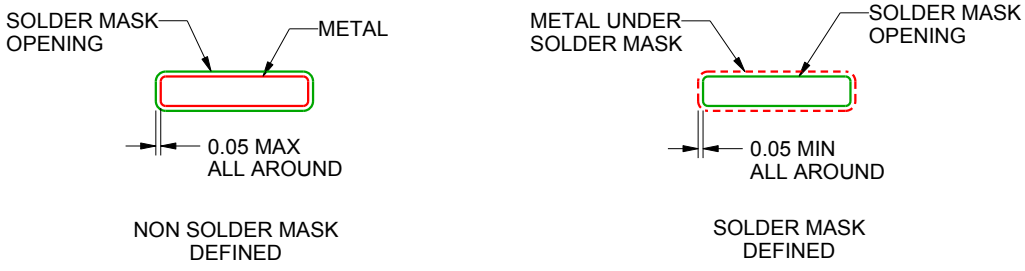


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

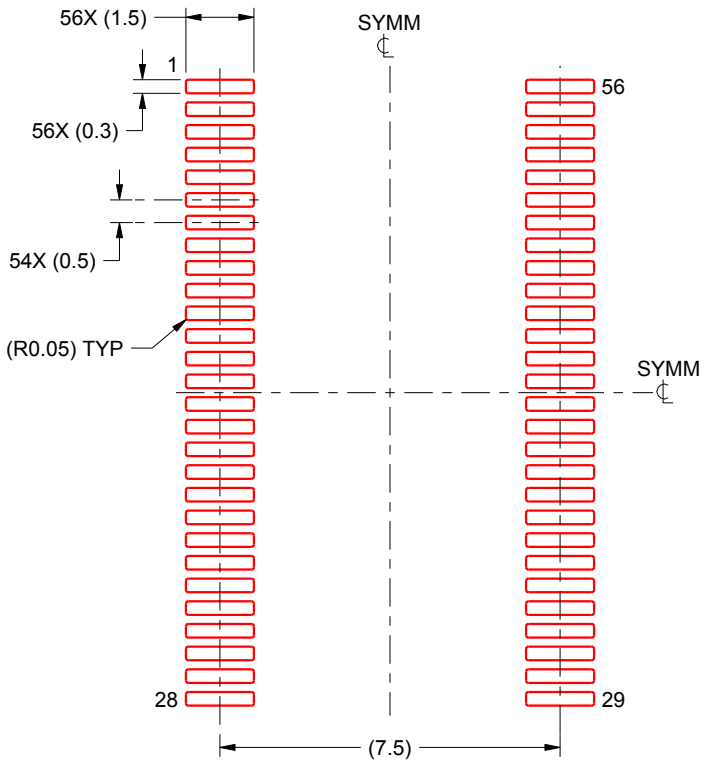


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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