TEXAS INSTRUMENTS

bq29700

SLUSBU9 – MARCH 2014

bq29700 Cost-Effective Voltage and Current Protection Integrated Circuit for Single-Cell Li-Ion/Li-Polymer Batteries

ECCN: EAR99

1 Features

- Input Voltage Range Pack+: VSS – 0.3 V to 12 V
- FET Drive:
  - CHG and DSG FET Drive Output
- Voltage Sensing Across External FETs for Overcurrent Protection (OCP) Is Within ± 5 mV (Typical)
- Fault Detection
  - Overcharge Detection (OVP)
  - Over-Discharge Detection (UVP)
  - Charge Overcurrent Detection (OCC)
  - Discharge Overcurrent Detection (OCD)
  - Load Short-Circuit Detection (SCP)
- Zero Voltage Charging for Depleted Battery
- Factory Programmed Fault Protection Thresholds
  - Fault Detection Voltage Thresholds
  - Fault Trigger Timers
  - Fault Recovery Timers
- Modes of Operation Without Battery Charger Enabled
  - NORMAL Mode I_{CC} = 4 µA
  - Shutdown Iq = 100 nA
- Operating Temperature Range T_A = –40°C to 85°C
- Package:
  - 6-Pin DSE (1.5 mm × 1.5 mm × 0.75 mm)

2 Applications

- Tablet PC
- Mobile Handset
- Handheld Data Terminals

3 Description

The bq29700 battery cell protection device provides an accurate monitor and trigger threshold for overcurrent protection during high discharge/charge current operation or battery overcharge conditions.

The bq29700 device provides the protection functions for Li-Ion/Li-Polymer cells, and monitors across the external power FETs for protection due to high charge or discharge currents. In addition, there is overcharge and depleted battery monitoring and protection. These features are implemented with low current consumption in NORMAL mode operation.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
bq29700DSE	WSON (6)	1.5 mm × 1.5 mm

4 Simplified Schematic
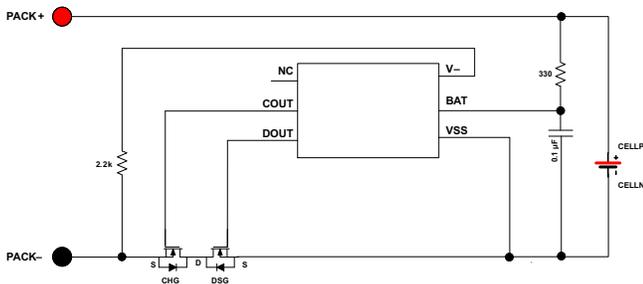
OCD Detection Accuracy Versus Temperature

Table of Contents

5 Revision History

DATE	REVISION	NOTES
March 2014	*	Initial Release

Product Folder Links: *bq29700*

6 Terminal Configuration and Functions

(DSE) 6 TERMINAL

NC	1		6	V–
COUT	2		5	BAT
DOUT	3		4	VSS
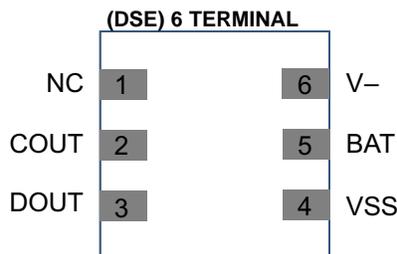
Terminal Functions

Terminal Number	Terminal Label	Type	Description
1	NC	NC	No Connection (electrically open, do *not* connect to BAT or VSS)
2	COUT	O	Gate Drive Output for Charge FET
3	DOUT	O	Gate Drive Output for Discharge FET
4	VSS	P	Ground terminal
5	BAT	P	VDD terminal
6	V–	I/O	Input terminal for charger negative voltage

6.1 Terminal Descriptions

6.1.1 Supply Input: BAT

This terminal is the input supply for the device and is connected to the positive terminal of the battery pack. There is a 0.1-µF input capacitor to ground for filtering noise.

6.1.2 Cell Negative Connection: VSS

This terminal is an input to the device for cell negative ground reference. Internal circuits associated with cell voltage measurements and overcurrent protection input to differential amplifier for either Vds sensing or external sense resistor sensing will be referenced to this node.

6.1.3 Voltage Sense Node: V–

This is a sense node used for measuring several fault detection conditions, such as overcurrent charging or overcurrent discharging configured as Vds sensing for protection. This input, in conjunction with VSS terminal, forms the differential measurement for the stated fault detection conditions. A 2.2-k resistor is connected between this input terminal and Pack– terminal of the system in the application.

6.1.4 Discharge FET Gate Drive Output: DOUT

This terminal is an output to control the discharge FET. The output is driven from an internal circuitry connected to the BAT supply. This output will transition from high to low when a fault is detected, and requires the DSG FET to turn OFF. A high impedance resistor of 5 MΩ is connected from DOUT to VSS for gate capacitance discharge when the FET is turned OFF.

6.1.5 Charge FET Gate Drive Output: COUT

This terminal is an output to control the charge FET. The output is driven from an internal circuitry connected to the BAT supply. This output transitions from high to low when a fault is detected, and requires the CHG FET to turn OFF. A high impedance resistor of 5 MΩ is connected from COUT to Pack– for gate capacitance discharge when FET is turned OFF.

Submit Documentation Feedback   3

ECCN: EAR99

TEXAS
INSTRUMENTS

bq29700

SLUSBU9 –MARCH 2014

www.ti.com

7   Specifications

7.1   Absolute Maximum Ratings[(1)]

		MIN	MAX	UNIT
Supply Control/Input	Input Voltage: BAT	−0.3	12	V
	V− Terminal (Pack−)	BAT − 28	BAT + 0.3	V
FET Drive and Protection	DOUT (Discharge FET Output), GDSG (Discharge FET Gate Drive)	VSS − 0.3	BAT + 0.3	V
	COUT (Charge FET Output), GCHG (Charge FET Gate Drive)	BAT − 28	BAT + 0.3	V
	Operating Temperature: T_{FUNC}	−40	85	°C

(1)   Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2   Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage Temperature Range	−55	150	°C
V_{ESD}[(1)]	Human Body Model (HBM) ESD stress voltage[(2)]	−2	2	kV
	Charged Device Model (CDM) ESD stress voltage[(3)]	−500	500	V

(1)   Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2)   Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Terminals listed as 1000 V may have higher performance.
(3)   Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Terminals listed as 250 V may have higher performance.

7.3   Recommended Operating Conditions[(1)]

		MIN	MAX	UNIT
Supply Control/Input	Positive Input Voltage: BAT	−0.3	8	V
	Negative Input Voltage: V−	BAT − 25	BAT	V
FET Drive and Protection	Discharge FET Control: DOUT	VSS	BAT	V
	Charge FET Control: COUT	BAT − 25	BAT	V
Temperature Ratings	Operating Temperature: T_{Amb}	−40	85	°C
	Storage Temperature: T_S	−55	150	°C
	Lead Temperature (Soldering 10 s)		300	°C
	Thermal Resistance Junction to Ambient, θ_{JA}[(1)]		250	°C/W

(1)   For more information about traditional and new thermal metrics, see the IC package Thermal Metrics application report, SPRA953.

7.4 Thermal Information

	THERMAL METRIC[1]	DSE (12 Terminals)	UNITS
$R_{\theta JA,\ High\ K}$	Junction-to-ambient thermal resistance[2]	190.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance[3]	94.9	
$R_{\theta JB}$	Junction-to-board thermal resistance[4]	149.3	
ψ_{JT}	Junction-to-top characterization parameter[5]	6.4	
ψ_{JB}	Junction-to-board characterization parameter[6]	152.8	
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance[7]	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 DC Characteristics

Typical Values stated where T_A = 25°C and BAT = 3.6 V. Min/Max values stated where T_A = –40°C to 85°C, and BAT = 3.0 V to 4.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION						
V_{BAT}	Device Operating Range	BAT – VSS	1.5		8	V
		BAT – V–	1.5		28	
I_{NORMAL}	Current Consumption in NORMAL Mode	BAT = 3.8 V, V– = 0 V		4	5.5	µA
I_{Power_down}	Current Consumption in Power Down Mode	BAT = V– = 1.5 V			0.1	µA
FET OUTPUT, DOUT and COUT						
V_{OL}	Charge FET Low Output	I_{OL} = 30 µA, BAT = 3.8 V		0.4	0.5	V
V_{OH}	Charge FET High Output	I_{OH} = –30 µA, BAT = 3.8 V	3.4	3.7		V
V_{OL}	Discharge FET Low Output	I_{OL} = 30 µA, BAT = 2.0 V		0.2	0.5	V
V_{OH}	Discharge FET High Output	I_{OH} = –30 µA, BAT = 3.8 V	3.4	3.7		V
PULL UP INTERNAL RESISTANCE ON V–						
$R_{V–D}$	Resistance between V– and VBAT	V_{BAT} = 1.8 V, V– = 0 V	100	300	550	kΩ
CURRENT SINK ON V–						
$I_{V–S}$	Current sink on V– to VSS	V_{BAT} = 3.8V	8		24	µA
LOAD SHORT DETECTION ON V–						
V_{short}	Short detection voltage	V_{BAT} = 3.8V and R_{PackN} = 2.2 k		V_{BAT} – 1 V		V
0-V BATTERY CHARGE FUNCTION						
V_{0CHG}	0-V battery charging starter voltage	0-V battery charging function allowed	1.7			V
V_{0INH}	0-V battery charging inhibit voltage	0-V battery charging function disallowed			0.75	V

7.6 Programmable Fault Detection Thresholds

FUNCTION	RANGE	ACCURACY
Over-charge detection voltage (V_{OVP})	3.85 V to 4.6 V in 50-mV steps	±10 mV at T_A = 25°C ±20 mV at T_A = 0°C to 60°C
Overcharge release hysteresis voltage ($V_{OVP–Hys}$)	100 mV and (VSS – V–) > OCC (min) for release	±20 mV at T_A = 25°C
Over-discharge detection voltage (V_{UVP})	2.0 V to 2.80 V in 50 mV steps	±50 mV at T_A = 25°C

ECCN: EAR99

bq29700

SLUSBU9 –MARCH 2014

TEXAS
INSTRUMENTS

www.ti.com

Programmable Fault Detection Thresholds (continued)

FUNCTION	RANGE	ACCURACY
Over-discharge release hysteresis voltage ($V_{UVP+Hys}$)	100 mV and (BAT – V–) > 1 V for release	±50 mV at T_A = 25°C
Discharging overcurrent detection voltage (V_{OCD})	90 mV to 200 mV in 5-mV steps	±10 mV (Typ) at T_A = 25°C
		±15 mV at T_A = –40°C to 85°C
Release of V_{OCD}	Release when BAT – V– > 1 V	1 V (Typ)
Charging overcurrent detection voltage (V_{OCC})	–45 mV to –155 mV in 5-mV steps	±10 mV (Typ) at T_A = 25°C
		±15 mV at T_A = –40°C to 85°C
Release of V_{OCC}	Release when VSS – V ≥ OCC (min)	40 mV (Typ)
Short Circuit detection voltage (V_{SCC})	Select, 300 mV, 400 mV, 500 mV, and 600 mV	±100 mV at T_A = 25°C
Release of Short Circuit detection voltage (V_{SCCR})	Release when BAT – V ≥ 1 V	1 V (Typ)

7.7   Programmable Fault Detection Timer Ranges

FUNCTION	RANGE	ACCURACY
Over-charge (t_{OVPD}) detection delay time	Select from 0.25 s, 1.0 s, 1.25 s, 4.5 s	±20%
Over-discharge (t_{UVPD}) detection delay time	Select from 20 ms, 96 ms, 125 ms, 144 ms	±20%
Discharging overcurrent (t_{OCDD}) detection delay time	Select from 8 ms, 16 ms, 20 ms, 48 ms	±20%
Charging overcurrent (t_{OCCD}) detection delay time	Select from 4 ms, 6 ms, 8 ms, 16 ms	±20%
Short Circuit detection delay time (t_{SCCD})	250 µs fixed	±50%

Product Folder Links: *bq29700*

ECCN: EAR99

TEXAS
INSTRUMENTS

www.ti.com

bq29700

SLUSBU9 –MARCH 2014

8 Typical Characteristics

$V_{BAT} = 1.5$ V
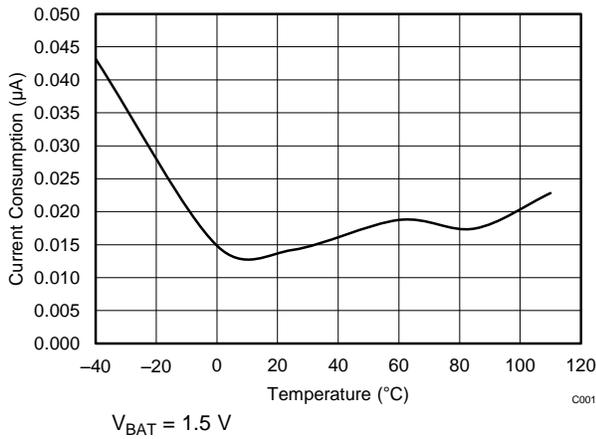
Figure 1. 1.5-V I_{BAT} Vs. Temperature

$V_{BAT} = 3.9$ V
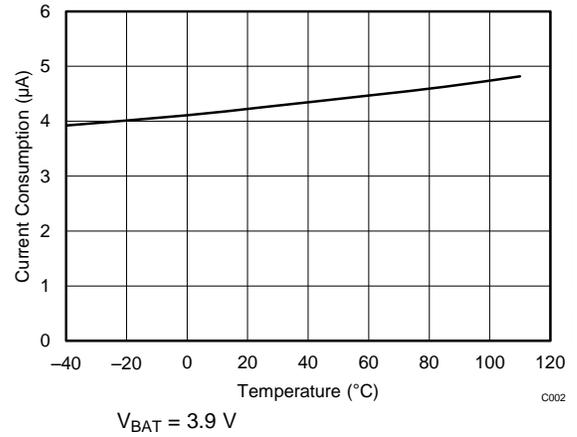
Figure 2. 3.9-V I_{BAT} Vs. Temperature

F_{OSC}, Setting = 1.255 kHz
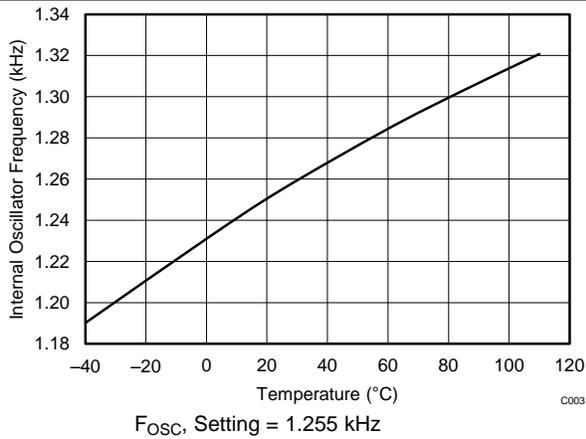
**Figure 3. Internal Oscillator Frequency Vs. Temperature**

V_{BAT}, Setting = 0 V
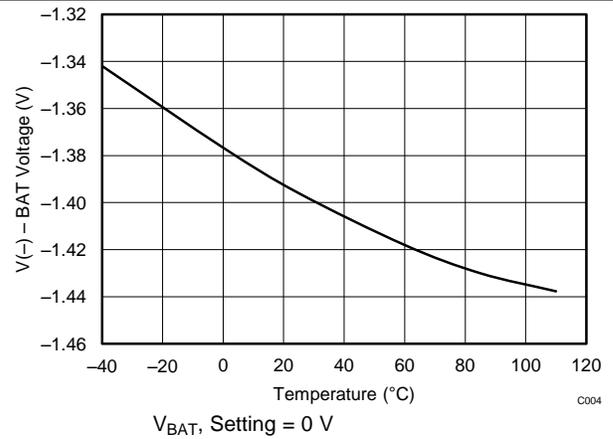
Figure 4. 0-V Charging Allowed Vs. Temperature
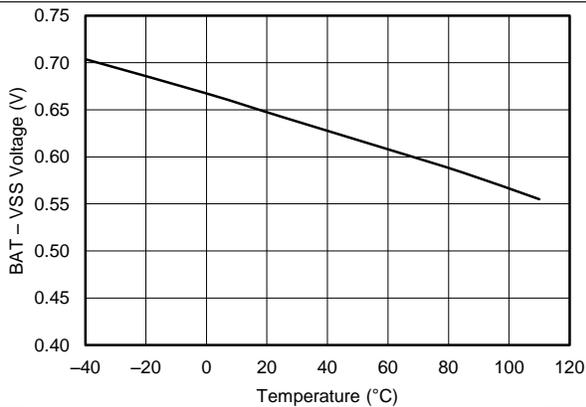
Figure 5. 0-V Charging Disallowed Vs. Temperature

OVP, Setting = 4.275 V
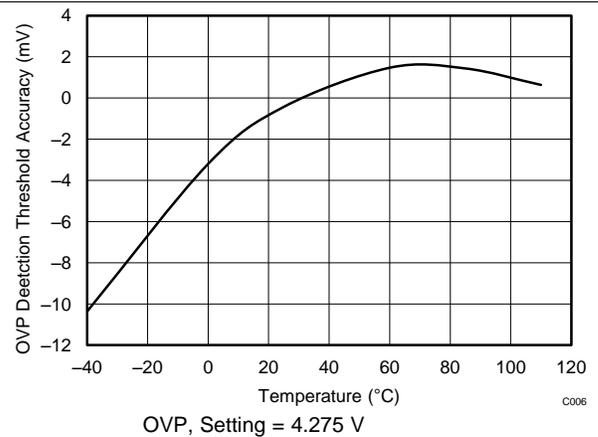
Figure 6. OVP Detection Accuracy Vs. Temperature

Typical Characteristics (continued)

t_{OVPD}, Setting = 1.25 s
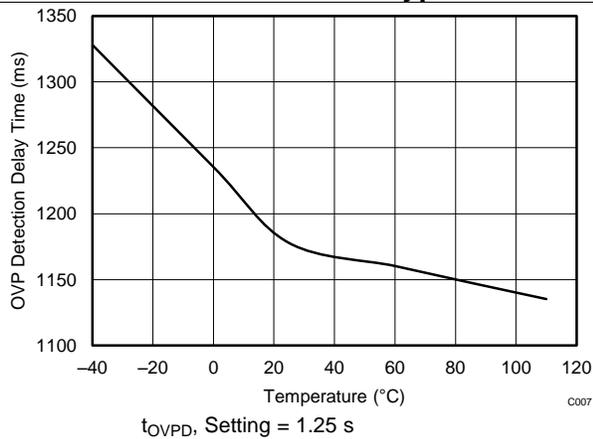
Figure 7. OVP Detection Dely Time Vs. Temperature

UVP, Setting = 2.800 V
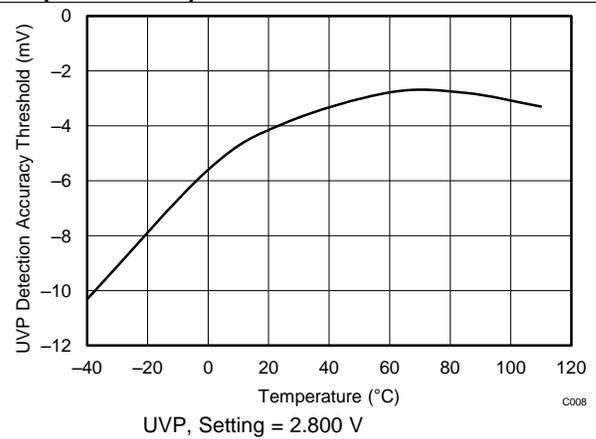
Figure 8. UVP Detection Accuracy Vs. Temperature

t_{UVPD}, Setting = 144 ms
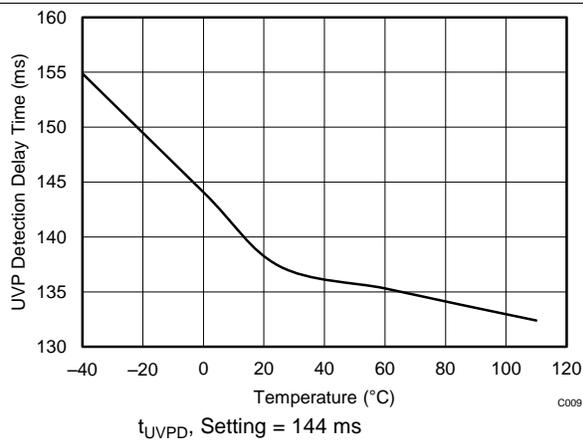
Figure 9. UVP Detection Delay Time Vs. Temperature

V_{OCC}, Setting = –100 mV
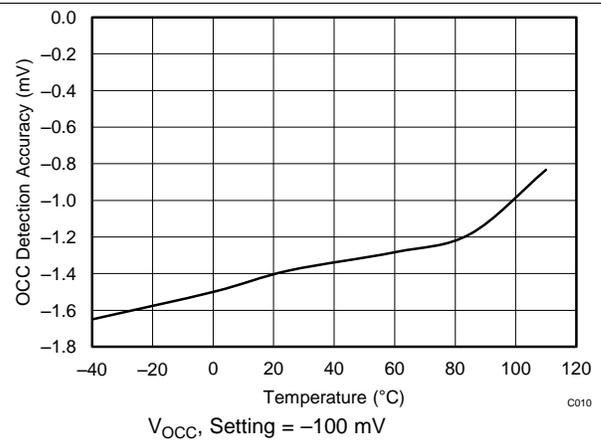
Figure 10. OCC Detection Accuracy Vs. Temperature

t_{OCCD}, Setting = 8 ms
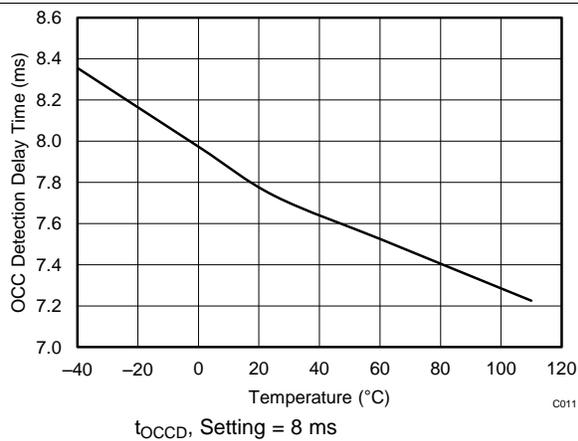
Figure 11. OCC Detection Delay Time Vs. Temperature

V_{OCD}, Setting = 100 mV
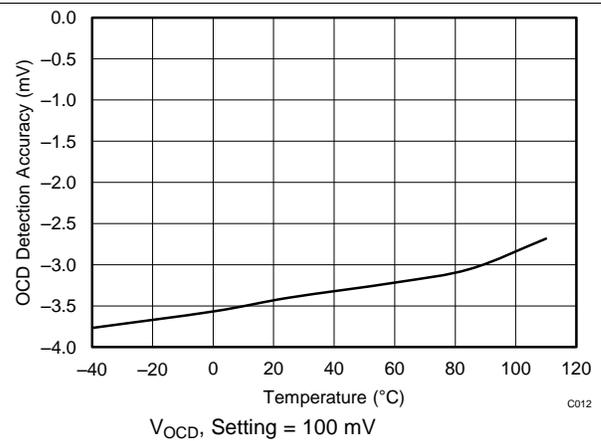
Figure 12. OCD Detection Accuracy Vs. Temperature

Product Folder Links: *bq29700*

Typical Characteristics (continued)

t_{UVPD}, Setting = 20 ms

Figure 13. OCD Detection Delay Time Vs. Temperature

V_{SCC}, Setting = 500 mV
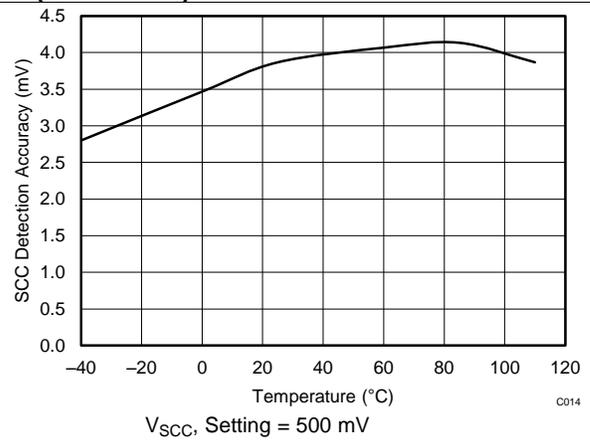
Figure 14. SCC Detection Accuracy Vs. Temperature
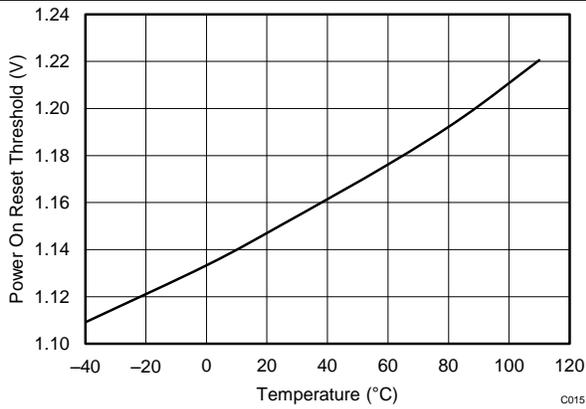
Figure 15. Power On Reset Vs. Temperature

V_{BAT}, Setting = 3.9 V
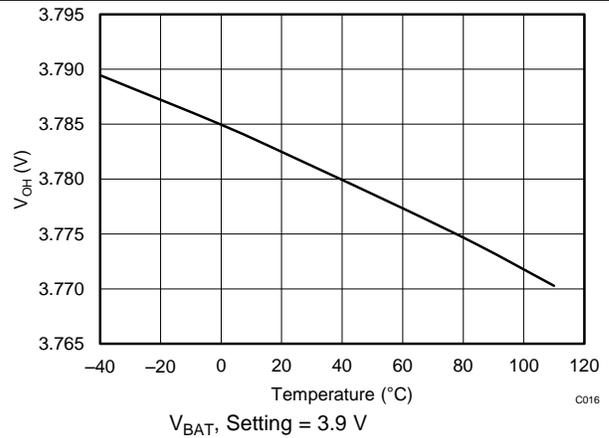
Figure 16. COUT Vs. Temperature with I_{oh} = – 30 µA

V_{BAT}, Setting = 3.9 V
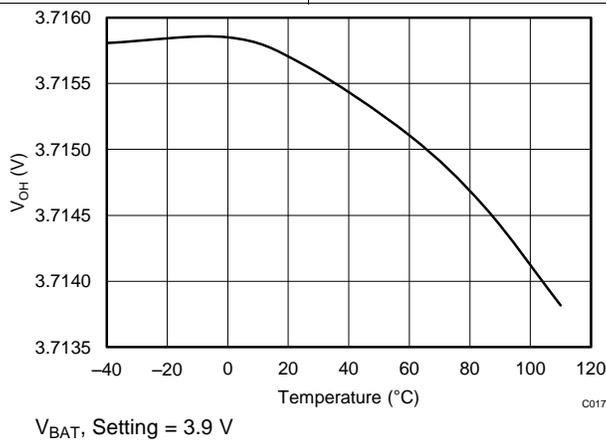
Figure 17. DOUT Vs. Temperature with I_{oh} = – 30 µA

Product Folder Links: *bq29700*

ECCN: EAR99

bq29700

SLUSBU9 –MARCH 2014

TEXAS
INSTRUMENTS

www.ti.com

9   Parameter Measurement Information

9.1   Timing Charts
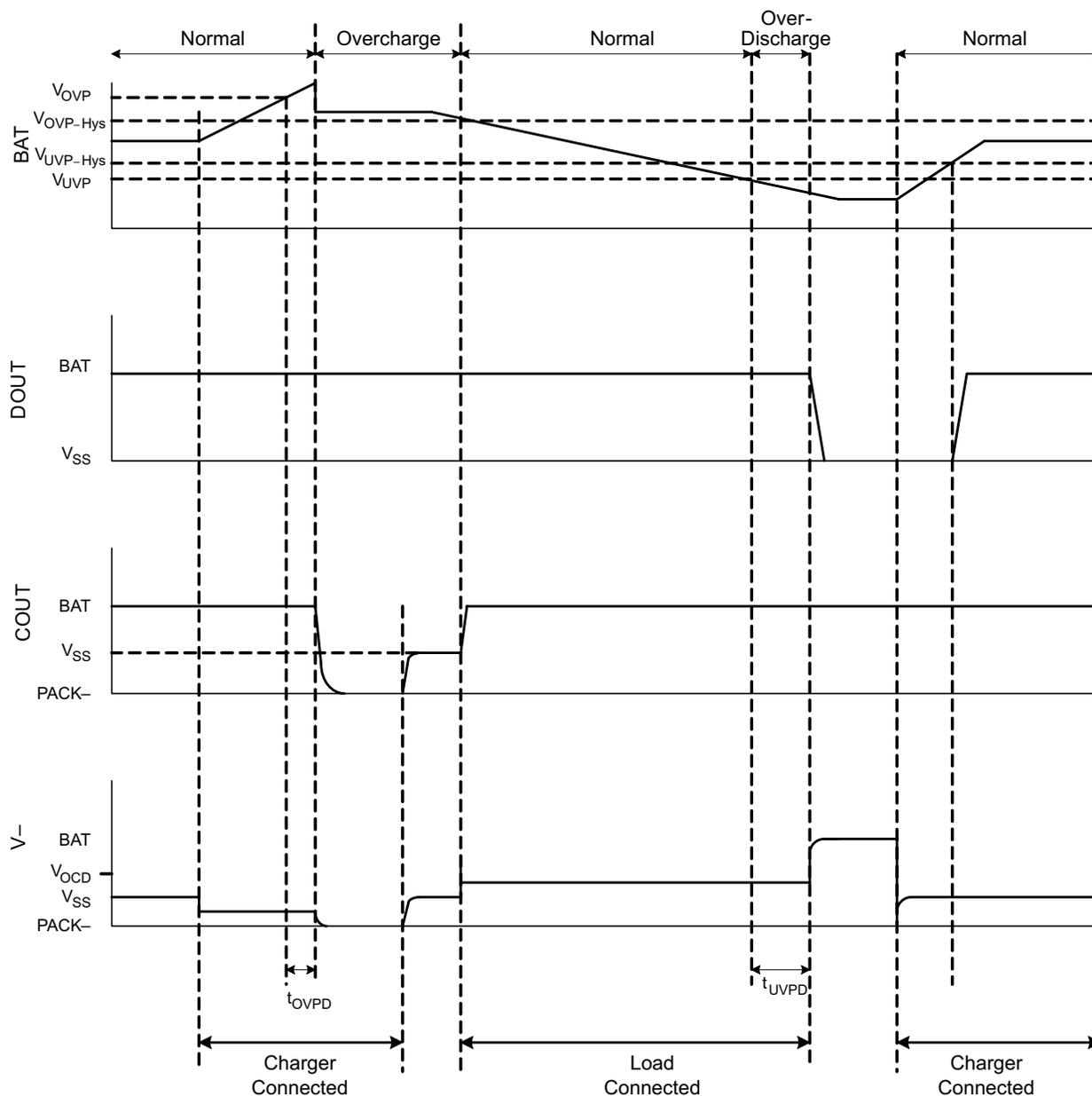
Figure 18.   1. Overcharge Detection, Over-Discharge Detection

Timing Charts (continued)
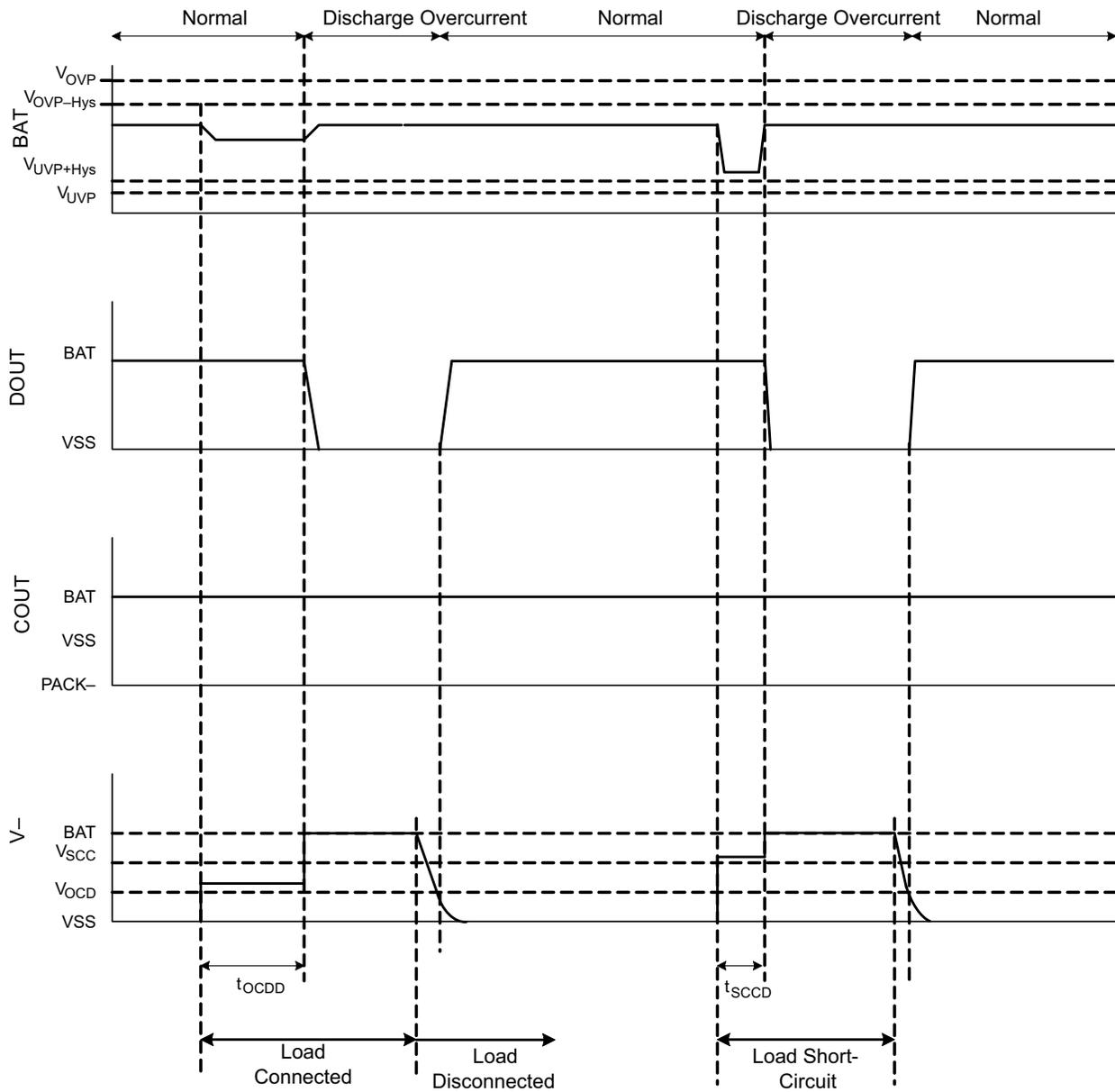
Figure 19. Discharge Overcurrent Detection

9.2 Test Circuits

The following tests are referenced as follows: The COUT and DOUT outputs are "H," which are higher than the threshold voltage of the external logic level FETs and regarded as ON state. Conversely, "L" is less than the turn ON threshold for external NMOS FETs and regarded as OFF state. The COUT terminal is with respect to V−, and the DOUT terminal is with respect to VSS.

1. ***Overcharge detection voltage and overcharge release voltage (Test Circuit 1):***

   The overcharge detection voltage (V_{OVP}) is measured between the BAT and VSS terminals, respectively. Once V1 is increased, the over-detection is triggered, and the delay timer expires, the COUT terminal transitions from a high to low state and then reduces the V1 voltage to check for the overcharge hysteresis parameter ($V_{OVP-Hys}$). This delta voltage between overcharge detection voltages (V_{OVP}) and the overcharge release occurs when the CHG FET drive output goes from low to high.

2. ***Over-discharge detection voltage and over-discharge release voltage (Test Circuit 2):***

   Over-discharge detection (V_{UVP}) is defined as the voltage between BAT and VSS at which the DSG drive output goes from high to low by reducing the V1 voltage. V1 is set to 3.5 V and gradually reduced while V2 is set to 0 V. The over-discharge release voltage is defined as the voltage between BAT and VSS at which the DOUT drive output transition from low to high when V1 voltage is gradually increased from a V_{UVP} condition. The overcharge hysteresis voltage is defined as the delta voltage between V_{UVP} and the instance at which the DOUT output drive goes from low to high.

3. ***Discharge overcurrent detection voltage (Test Circuit 2):***

   The discharge overcurrent detection voltage (V_{OCD}) is measured between V− and VSS terminals and triggered when the V2 voltage is increased above V_{OCD} threshold with respect to VSS. This delta voltage once satisfied will trigger an internal timer t_{OCDD} before the DOUT output drive transitions from high to low.

4. ***Load short circuit detection voltage (Test Circuit 2):***

   Load short-circuit detection voltage (V_{SCC}) is measured between V− and VSS terminals and triggered when the V2 voltage is increased above V_{SCC} threshold with respect to VSS within 10 µs. This delta voltage, once satisfied, triggers an internal timer t_{SCCD} before the DOUT output drive transitions from high to low.

5. ***Charge overcurrent detection voltage (Test Circuit 2):***

   The charge overcurrent detection voltage (V_{OCC}) is measured between VSS and V− terminals and triggered when the V2 voltage is increased above V_{OCC} threshold with respect to V−. This delta voltage, once satisfied,l triggers an internal timer t_{OCDD} before the COUT output drive transitions from high to low.

6. ***Operating current consumption (Test Circuit 2):***

   The operating current consumption $I_{BNORMAL}$ is the current measured going into the BAT terminal under the following conditions: V1 = 3.9 V and V2 = 0 V.

7. ***Power down current consumption (Test Circuit 2):***

   The operating current consumption I_{Power_down} is the current measured going into the BAT terminal under the following conditions: V1 = 1.5 V and V2 = 1.5 V.

8. ***Resistance between V− and BAT terminal (Test Circuit 3):***

   Measure the resistance (R_{V_D}) between V− and BAT terminals by setting the following conditions: V1 = 1.8 V and V2 = 0 V.

9. ***Current sink between V− and VSS (Test Circuit 3):***

   Measure the current sink $I_{V−S}$ between V− and VSS terminals by setting the following condition: V1 = 4 V.

10. ***COUT current source when activated High (Test Circuit 4):***

    Measure I_{COUT} current source on the COUT terminal by setting the following conditions: V1 = 3.9 V, V2 = 0 V and V3 = 3.4 V.

11. ***COUT current sink when activated Low (Test Circuit 4):***

    Measure I_{COUT} current sink on COUT terminal by setting the following conditions: V1 = 4.5 V, V2 = 0 V and V3 = 0.5 V.

Test Circuits (continued)

12. ***DOUT current source when activated High (Test Circuit 4):***

Measure I_{DOUT} current source on DOUT terminal by setting the following conditions: V1 = 3.9 V, V2 = 0 V and V3 = 3.4 V.

13. ***DOUT current sink when activated Low (Test Circuit 4):***

Measure I_{DOUT} current sink on DOUT terminal by setting the following conditions: V1 = 2.0 V, V2 = 0 V and V3 = 0.4 V.

14. ***Overcharge detection delay (Test Circuit 5):***

The overcharge detection delay time t_{OVPD} is the time delay before the COUT drive output transitions from high to low once the voltage on V1 exceeds the V_{OVP} threshold. Set V2 = 0 V and then increase V1 until BAT input exceeds the V_{OVP} threshold and to check the time for when COUT goes from high to low.

15. ***Over-discharge detection delay (Test Circuit 5):***

The over-discharge detection delay time t_{UVPD} is the time delay before the DOUT drive output transitions from high to low once the voltage on V1 decreases to V_{UVP} threshold. Set V2 = 0 V and then decrease V1 until BAT input reduces to the V_{UVP} threshold and to check the time of when DOUT goes from high to low.

16. ***Discharge overcurrent detection delay (Test Circuit 5):***

The discharge overcurrent detection delay time t_{OCDD} is the time for DOUT drive output to transition from high to low after the voltage on V2 is increased from 0 V to 0.35 V, with V1 = 3.5 V and V2 starts from 0 V and increases to trigger threshold.

17. ***Load short circuit detection delay (Test Circuit 5):***

The load short-circuit detection delay time t_{SCCD} is the time for DOUT drive output to transition from high to low after the voltage on V2 is increased from 0 V to V1 − 1 V, with V1 = 3.5 V and V2 starts from 0 V and increases to trigger threshold.

18. ***Charge overcurrent detection delay (Test Circuit 5):***

The charge overcurrent detection delay time t_{OCCD} is the time for COUT drive output to transition from high to low after the voltage on V2 is decreased from 0 V to –0.3 V, with V1 = 3.5 V and V2 starts from 0 V and decreases to trigger threshold.

19. ***0-V battery charge starting charger voltage (Test Circuit 2):***

The 0-V charge for start charging voltage V_{0CHA} is defined as the voltage between BAT and V– terminals at which COUT goes high when voltage on V2 is gradually decreased from a condition of V1 = V2 = 0 V.

20. ***0-V battery charge inhibition battery voltage (Test Circuit 2):***

The 0-V charge inhibit for charger voltage V_{0INH} is defined as the voltage between BAT and VSS terminals at which COUT should go low as V1 is gradually decreased from V1 = 2 V and V2 = –4 V.

## 9.3 Test Circuit Diagrams
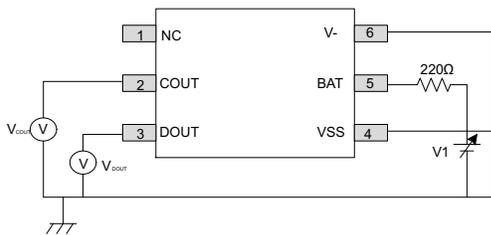
**Figure 20. Test Circuit 1**
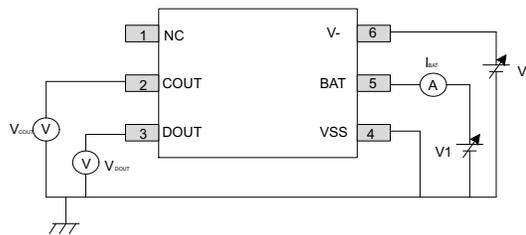
Figure 21. Test Circuit 2
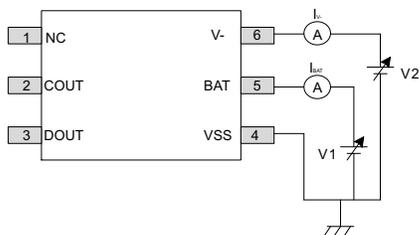
Figure 22. Test Circuit 3
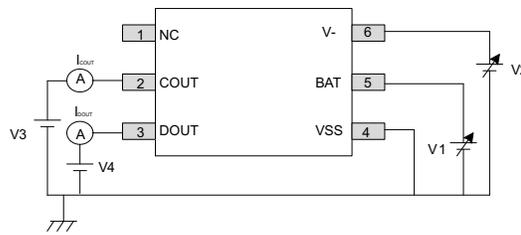
Figure 23. Test Circuit 4
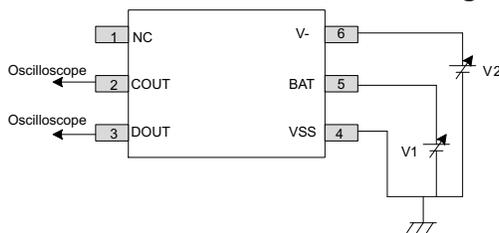
**Figure 24. Test Circuit 5**

10 Detailed Description

10.1 Overview

This bq297xy device is a primary protector for a single-cell Li-Ion/Li-Polymer battery pack. The device uses a minimum number of external components to protect for overcurrent conditions due to high discharge/charge currents in the application. In addition, it monitors and helps to protect against battery pack overcharging or depletion of energy in the pack. The bq297xy device is capable of having an input voltage of 8 V from a charging adapter and can tolerate a voltage of BAT – 25 V across the two input terminals. In the condition when a fault is triggered, there are timer delays before the appropriate action is taken to turn OFF either the CHG or DSG FETs. There is also a timer delay for the recovery period once the threshold for recovery condition is satisfied. These parameters are fixed once they are programmed. There is also a feature called zero voltage charging that enables depleted cells to be charged to a acceptable level before the battery pack can be used for normal operation. Zero voltage charging is allowed if the charger voltage is above 1.7 V.

10.2 Functional Block Diagram
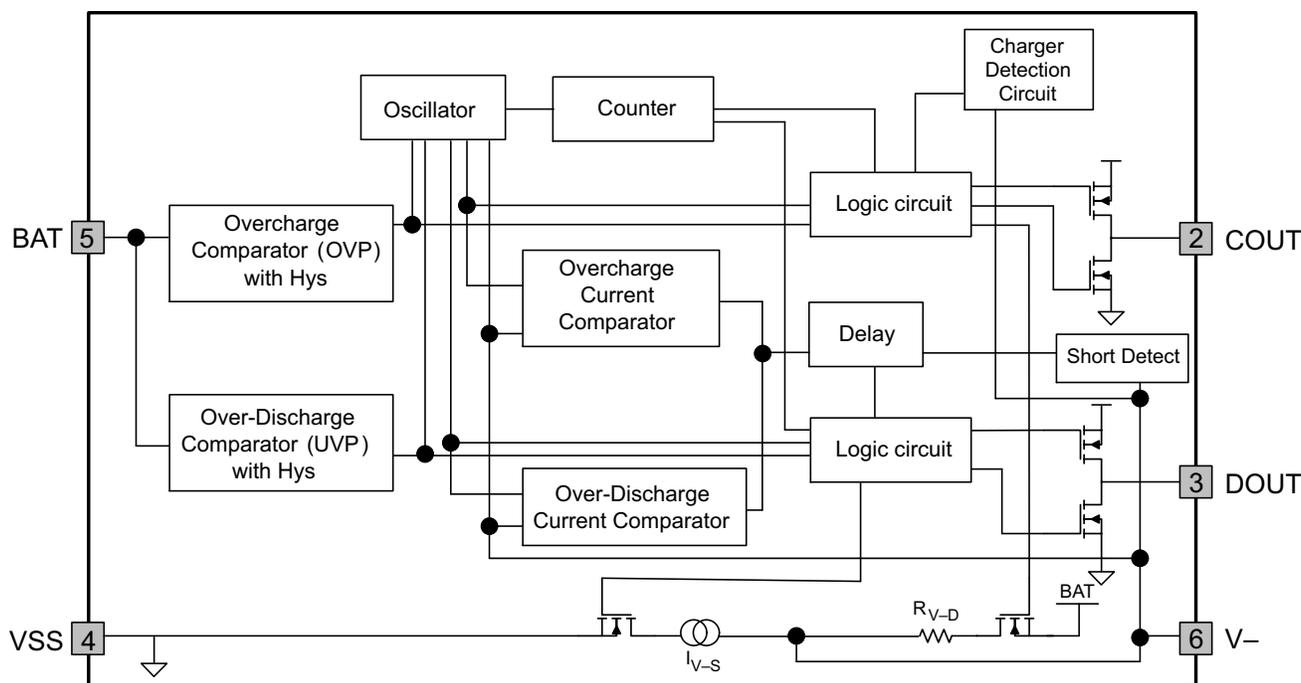
10.3 Feature Description

The bq297xy family of devices measures voltage drops across several input terminals for monitoring and detection of the following faults: OCC, OCD, OVP, and UVP. An internal oscillator initiates a timer to the fixed delays associated with each parameter once the fault is triggered. Once the timer expires due to a fault condition, the appropriate FET drive output (COUT or DOUT) is activated to turn OFF the external FET. The same method is applicable for the recovery feature once the system fault is removed and the recovery parameter is satisfied, then the recovery timer is initiated. If there are no reoccurrences of this fault during this period, the appropriate gate drive is activated to turn ON the appropriate external FET.

10.4 Device Functional Modes

10.4.1 Normal Operation

This device monitors the voltage of the battery connected between BAT terminal and VSS terminal and the differential voltage between V– terminal and VSS terminal to control charging and discharging. The system is operating in NORMAL mode when the battery voltage range is between the over-discharge detection threshold (V_{UVP}) and the overcharge detection threshold (V_{OVP}), and the V– terminal voltage is within the range for charge overcurrent threshold (V_{OCC}) to over-discharge current threshold (V_{OCD}) when measured with respect to VSS. If these conditions are satisfied, the device turns ON the drive for COUT and DOUT FET control.

CAUTION

When the battery is connected for the first time, the discharging circuit may not be enabled. In this case, short the V– terminal to the VSS terminal.

Alternatively, connect the charger between the Pack+ and Pack– terminals in the system.

10.4.2 Overcharge Status

This mode is detected when the battery voltage measured is higher than the overcharge detection threshold (V_{OVP}) during charging. If this condition exists for a period greater than the overcharge detection delay (t_{OVPD}) or longer, the COUT output signal is driven low to turn OFF the charging FET to prevent any further charging of the battery.

The overcharge condition is released if one of the following conditions occurs:

- If the V– terminal is higher than the overcharge detection voltage (V_{OCC_Min}), the device releases the overcharge status when the battery voltage drops below the overcharge release voltage ($V_{OVP-Hys}$).
- If the V– terminal is higher than or equal to the over-discharge detection voltage (V_{OCD}), the device releases the overcharge status when the battery voltage drops below the overcharge detection voltage (V_{OVP}).

The discharge is initiated by connecting a load after the overcharge detection. The V– terminal rises to a voltage greater than VSS due to the parasitic diode of the charge FET conducting to support the load. If the V– terminal voltage is higher than or equal to the discharge overcurrent detection threshold (V_{OCD}), the overcurrent condition status is released only if the battery voltage drops lower than or equal to the overcharge detection voltage (V_{OVP}).

CAUTION

1. If the battery is overcharged to a level greater than overcharge detection (V_{OVP}) and the battery voltage does *not* drop below the overcharge detection voltage (V_{OVP}) with a heavy load connected, the discharge overcurrent and load short-circuit detection features do *not* function until the battery voltage drops below the overcharge detection voltage (V_{OVP}). The internal impedance of a battery is in the order of tens of mΩ, so application of a heavy load on the output should allow the battery voltage to drop immediately, enabling discharge overcurrent detection and load short-circuit detection features after an overcharge release delay.

2. When a charger is connected after an overcharge detection, the overcharge status does *not* release even if the battery voltage drops below the overcharge release threshold. The overcharge status is released when the V– terminal voltage exceeds the overcurrent detection voltage (V_{OCD}) by removing the charger.

Device Functional Modes (continued)

10.4.3 Over-Discharge Status

If the battery voltage drops below the over-discharge detection voltage (V_{UVP}) for a time greater than (t_{UVPD}) the discharge control output, DOUT is switched to a low state and the discharge FET is turned OFF to prevent further discharging of the battery. This is referred to as an over-discharge detection status. In this condition, the V– terminal is internally pulled up to BAT by the resistor $R_{V–D}$. When this occurs, the voltage difference between V– and BAT terminals is 1.3 V or lower, and the current consumption of the device is reduced to power-down level $I_{STANDBY}$. The current sink $I_{V–S}$ is not active in power-down state or over-discharge state. The power-down state is released when a charger is connected and the voltage delta between V– and BAT terminals is greater than 1.3 V.

If a charger is connected to a battery in over-discharge state and the voltage detected at the V– is lower than –0.7 V, the device releases the over-discharge state and allows the DOUT terminal to go high and turn ON the discharge FET once the battery voltage exceeds over-discharge detection voltage (V_{UVP}).

If a charger is connected to a battery in over-discharge state and the voltage detected at the V– is higher than –0.7 V, the device releases the over-discharge state and allows the DOUT terminal to go high and turn ON the discharge FET once the battery voltage exceeds over-discharge detection release hysteresis voltage ($V_{UVP +Hys}$).

10.4.4 Discharge Overcurrent Status (Discharge Overcurrent, Load Short-Circuit)

When a battery is in normal operation and the V– terminal is equal to or higher than the discharge overcurrent threshold for a time greater than the discharge overcurrent detection delay, the DOUT terminal is pulled low to turn OFF the discharge FET and prevent further discharge of the battery. This is known as the discharge overcurrent status. In the discharge overcurrent status, the V– and VSS terminals are connected by a constant current sink $I_{V–S}$. When this occurs and a load is connected, the V– terminal is at BAT potential. If the load is disconnected, the V– terminal goes to VSS (BAT/2) potential.

This device detects the status when the impedance between Pack+ and Pack– (see Figure 2) increases and is equal to the impedance that enables the voltage at the V– terminal to return to BAT – 1 V or lower. The discharge overcurrent status is restored to the normal status.

Alternatively, by connecting the charger to the system, the device returns to normal status from discharge overcurrent detection status, because the voltage at the V– terminal drops to BAT – 1 V or lower.

The resistance $R_{V–D}$ between V– and BAT is not connected in the discharge overcurrent detection status.

10.4.5 Charge Overcurrent Status

When a battery is in normal operation status and the voltage at V– terminal is lower than the charge overcurrent detection due to high charge current for a time greater than charge overcurrent detection delay, the COUT terminal is pulled low to turn OFF the charge FET and prevent further charging to continue. This is known as charge overcurrent status.

The device is restored to normal status from charge overcurrent status when the voltage at the V– terminal returns to charge overcurrent detection voltage or higher by removing the charger from the system.

The charge overcurrent detection feature does *not* work in the over-discharge status.

The resistance $R_{V–D}$ between V– and BAT and the current sink $I_{V–S}$ is not connected in the charge overcurrent status.

10.4.6 0-V Charging Function (Available)

This feature enables recharging a connected battery that has very low voltage due to self-discharge. When the 0-V battery charge starting charger voltage V_{0CHG} or higher voltage is applied to Pack+ and Pack– connections by the charger, the COUT terminal gate drive is fixed by the BAT terminal voltage.

Once the voltage between the gate and the source of the charging FET becomes equal to or greater than the turn ON voltage due to the charger voltage, the charging FET is ON and the battery is charged with current flow through the charging FET and the internal parasitic diode of the discharging FET. Once the battery voltage is equal to or higher than the over-discharge release voltage, the device enters normal status.

Device Functional Modes (continued)

CAUTION

1. Some battery providers do not recommend charging a depleted (self-discharged) battery. Consult the battery supplier to determine whether to have the 0-V battery charger function.

2. The 0-V battery charge feature has a higher priority than the charge overcurrent detection function. In this case, the 0-V charging will be allowed and the battery charges forcibly, which results in charge overcurrent detection being disabled if the battery voltage is lower than the over-discharge detection voltage.

10.4.7 0-V Charging Function (Unavailable)

This feature inhibits recharging a battery that has an internal short circuit of a 0-V battery. If the battery voltage is below the charge inhibit voltage V_{0INH} or lower, the charge FET control gate is fixed to the Pack– voltage to inhibit charging. When battery is equal to V_{0INH} or higher, charging can be performed.

CAUTION

Some battery providers do not recommend charging a depleted (self-discharged) battery. Consult the battery supplier to determine whether to enable or inhibit the 0-V battery charger function.

10.4.8 Delay Circuit

The detection delay timers are based from an internal clock with a frequency of 10 kHz.
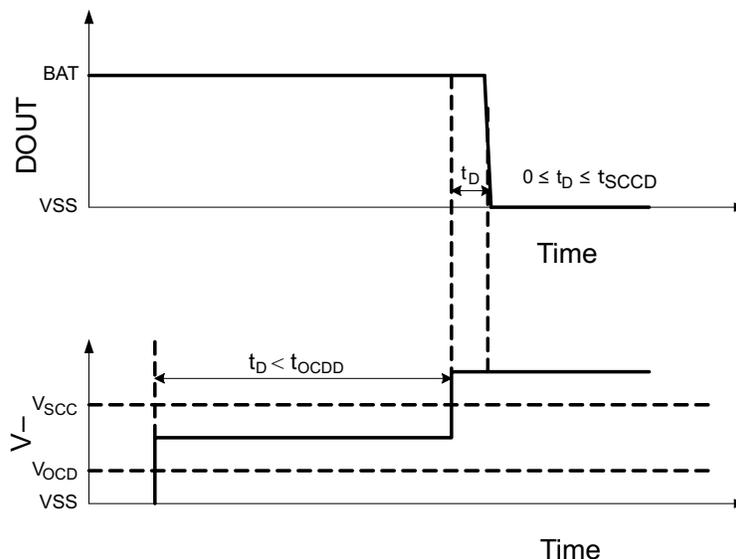
If the over-discharge current is detected, but remains below the over-discharge short circuit detection threshold, the over-discharge detection conditions must be valid for a time greater than or equal to over-discharge current delay t_{OCCD} time before the DOUT goes low to turn OFF the discharge FET. However, during any time the discharge overcurrent detection exceeds the short circuit detection threshold for a time greater than or equal to load circuit detection delay t_{SCCD}, the DOUT terminal goes low in a faster delay for protection.

11 Applications and Implementation

11.1 Application Information

The bq297xy devices are a family of primary protectors used for protection of the battery pack in the application. The application drives two low-side NMOS FETs that are controlled to provide energy to the system loads or interrupt the power in the event of a fault condition.

11.2 Typical Application
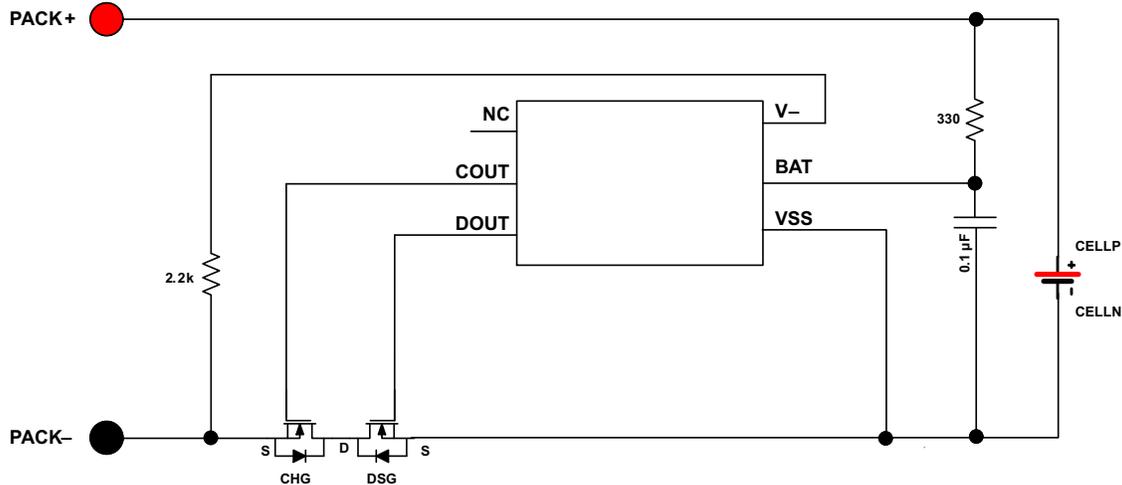
NOTE: The 5-M resistor for an external gate-source is optional.

Figure 25. Typical Application Schematic, bq297xy

11.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE at Ta = 25C
Input voltage range	4.5 V to 7 V
Maximum operating discharge current	7A
Maximum Charge Current for battery pack	4.5A
Overvoltage Protection (OVP)	4.275 V
Overvoltage detection delay timer	1.2 s
Overvoltage Protection (OVP) release voltage	4.175
Undervoltage Protection (UVP)	2.8 V
Undervoltage detection delay timer	150 ms
Undervoltage Protection (UVP) release voltage	3.1 V
Charge Overcurrent detection (OCC) voltage	−70 mV
Charge Overcurrent Detection (OCC) delay timer	9 ms
Discharge Overcurrent Detection (OCD) voltage	100 mV
Discharge Overcurrent Detection (OCD) delay timer	18 ms
Load Short Circuit Detection SCC) voltage, BAT to −V ≤ threshold	500 mV
Load Short Circuit Detection (SCC) delay timer	250 μs
Load Short Circuit release voltage, BAT to −V ≥ Threshold	1 V

ECCN: EAR99

bq29700

SLUSBU9 – MARCH 2014

TEXAS
INSTRUMENTS

www.ti.com

11.2.2 Detailed Design Procedure

> **NOTE**
> The external FET selection is important to ensure the battery pack protection is sufficient and complies to the requirements of the system.

- FET Selection: Because the maximum desired discharge current is 7A, ensure that the Discharge Overcurrent circuit does *not* trigger until the discharge current is above this value.
- The total resistance tolerated across the two external FETs (CHG + DSG) should be 100 mV/7A = 14.3 mΩ.
- Based on the information of the total ON resistance of the two switches, determine what would be the Charge Overcurrent Detection threshold, 14.3 mΩ × 4.5A = 65 mV. Selecting a device with a 70-mV trigger threshold for Charge Overcurrent trigger is acceptable.
- The total Rds ON should factor in any worst-case parameter based on the FET ON resistance, de-rating due to temperature effects and minimum required operation, and the associated gate drive (Vgs). Therefore, the FET choice should meet the following criteria:
  Vdss = 25 V
  Each FET Rds ON = 7.5 mΩ at Tj = 25°C and Vgs = 3.5 V
- Imax > 50 A to allow for short Circuit Current condition for 350 μs (max delay timer). The only limiting factor during this condition is Pack Voltage/(Cell Resistance + (2 × FET_RdsON) + Trace Resistance).
- Use the CSD16406Q3 FET for the application.
- An RC filter is required on the BAT for noise, and enables the device to operate during sharp negative transients. The 330-Ω resistor also limits the current during a reverse connection on the system.
- It is recommended to place a high impedance 5-MΩ across the gate source of each external FET to deplete any charge on the gate-source capacitance.

11.2.3 Application Performance Plots
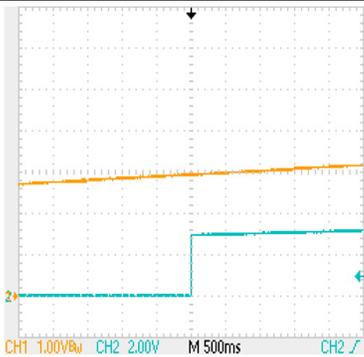
Orange Line (Channel 1) = Power Up Ramp on BAT Terminal

Turquoise Line (Channel 2) = DOUT Gate Drive Output

DOUT goes from low to high when UVP Recovery = UVP Set Threshold +100 mV

Figure 26. UVP Recovery
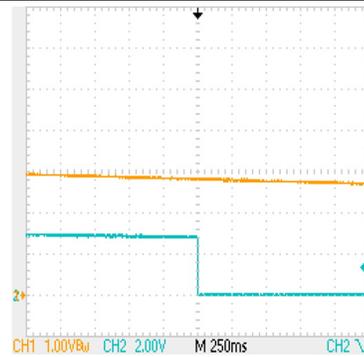
Orange Line (Channel 1) = Power Down Ramp on BAT Terminal

Turquoise Line (Channel 2) = DOUT Date Drive Output

DOUT goes from high to low when UVP threshold = UVP set Threshold + set delay time

Figure 27. UVP Set Condition
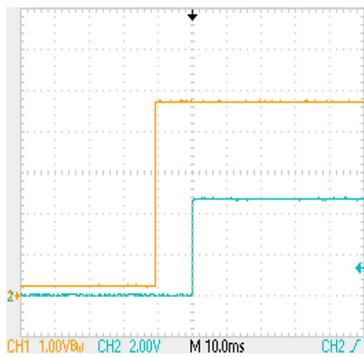
Orange Line (Channel 1) = Power Up Ramp on BAT Terminal

Turquoise Line (Channel 2) = DOUT Gate Drive Output

Figure 28. Initial Power Up, DOUT
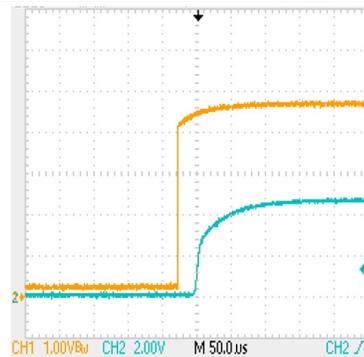
Orange Line (Channel 1) = Power Up Ramp on BAT Terminal

Turquoise Line (Channel 2) = COUT Gate Drive Output

Figure 29. Initial Power Up, COUT
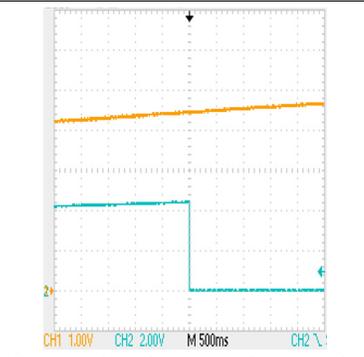
Orange Line (Channel 1) = Power Up Ramp on BAT Terminal

Turquoise Line (Channel 2) = COUT Gate Drive Output

COUT goes from high to low when OVP threshold = OVP set Threshold + set delay time

Figure 30. OVP Set Condition
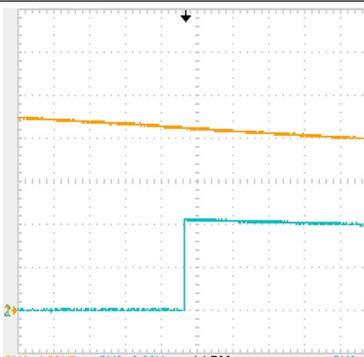

Orange Line (Channel 1) = Decrease Voltage on BAT terminal

Turquoise Line (Channel 2) = COUT Gate Drive Output

COUT goes from low to high when OVP Recovery = OVP Set Threshold −100 mV

Figure 31. OVP Recovery Condition

Product Folder Links: *bq29700*

12   Power Supply Recommendations

The recommended power supply for this device is a maximum 8-V operation on the BAT input terminal.

13   Layout

13.1   Layout Guidelines

The following are the recommended layout guidelines:

1. Ensure the external power FETs are adequately compensated for heat dissipation with sufficient thermal heat spreader based on worst-case power delivery.
2. The connection between the two external power FETs should be very close to ensure there is not an additional drop for fault sensing.
3. The input RC filter on the BAT terminal should be close to the terminal of the IC.

13.2   Layout Example
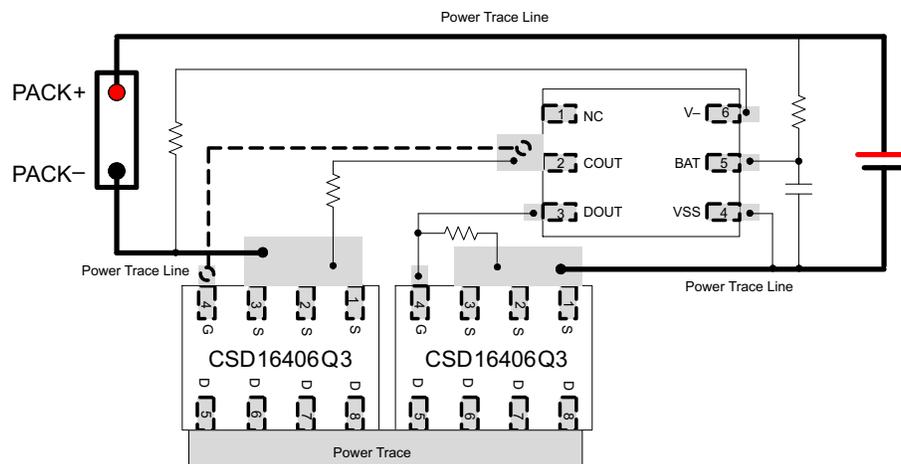
Via connects between two layers

Figure 32. bq297xy Board Layout

14 Device and Documentation Support

14.1 Trademarks

All trademarks are the property of their respective owners.

14.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.3 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from Disclosing party under this Agreement, or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

14.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ29700DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85		Samples
BQ29700DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
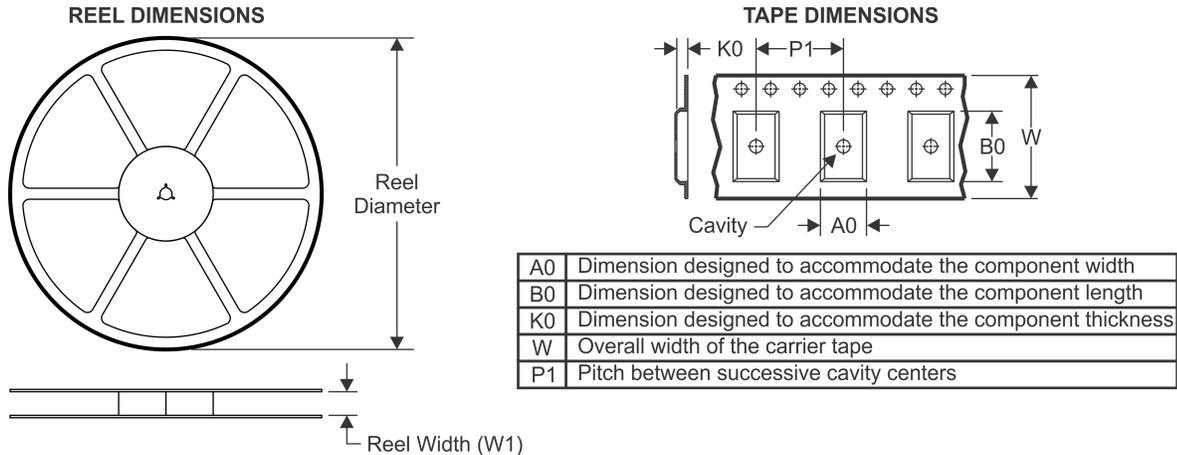
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
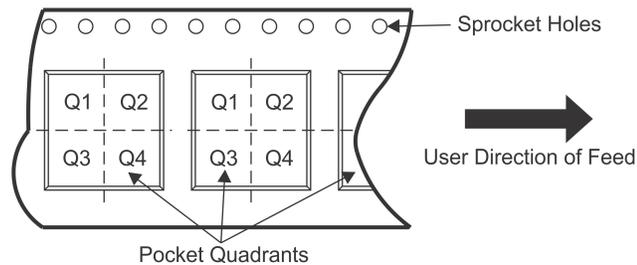
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29700DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29700DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2

PACKAGE MATERIALS INFORMATION

TEXAS INSTRUMENTS

TAPE AND REEL BOX DIMENSIONS
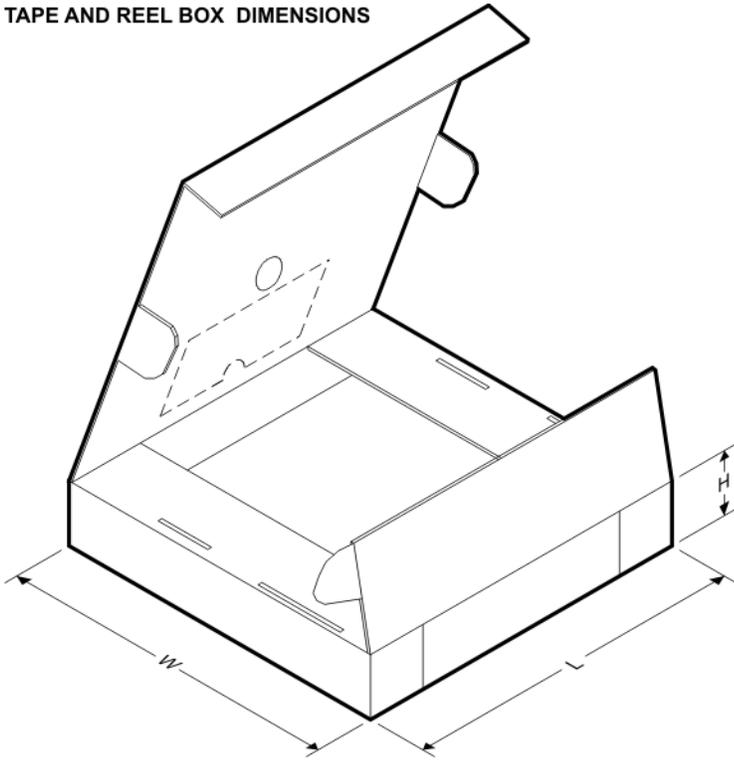
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29700DSER	WSON	DSE	6	3000	210.0	185.0	35.0
BQ29700DSET	WSON	DSE	6	250	210.0	185.0	35.0

DSE (S−PDSO−N6)   PLASTIC SMALL OUTLINE

B

1,55 / 1,45

1,55 / 1,45

PIN 1 INDEX AREA

A

0.80 / 0,70

⌓ 0.08

0,20 REF.

C

SEATING PLANE

0,05 / 0,00

4X ⎣0,50⎦

1   2   3

0,70 / 0,50

5X 0,60 / 0,40

6   5   4

6X 0.30 / 0,20   ⊕ 0.10Ⓜ C A B
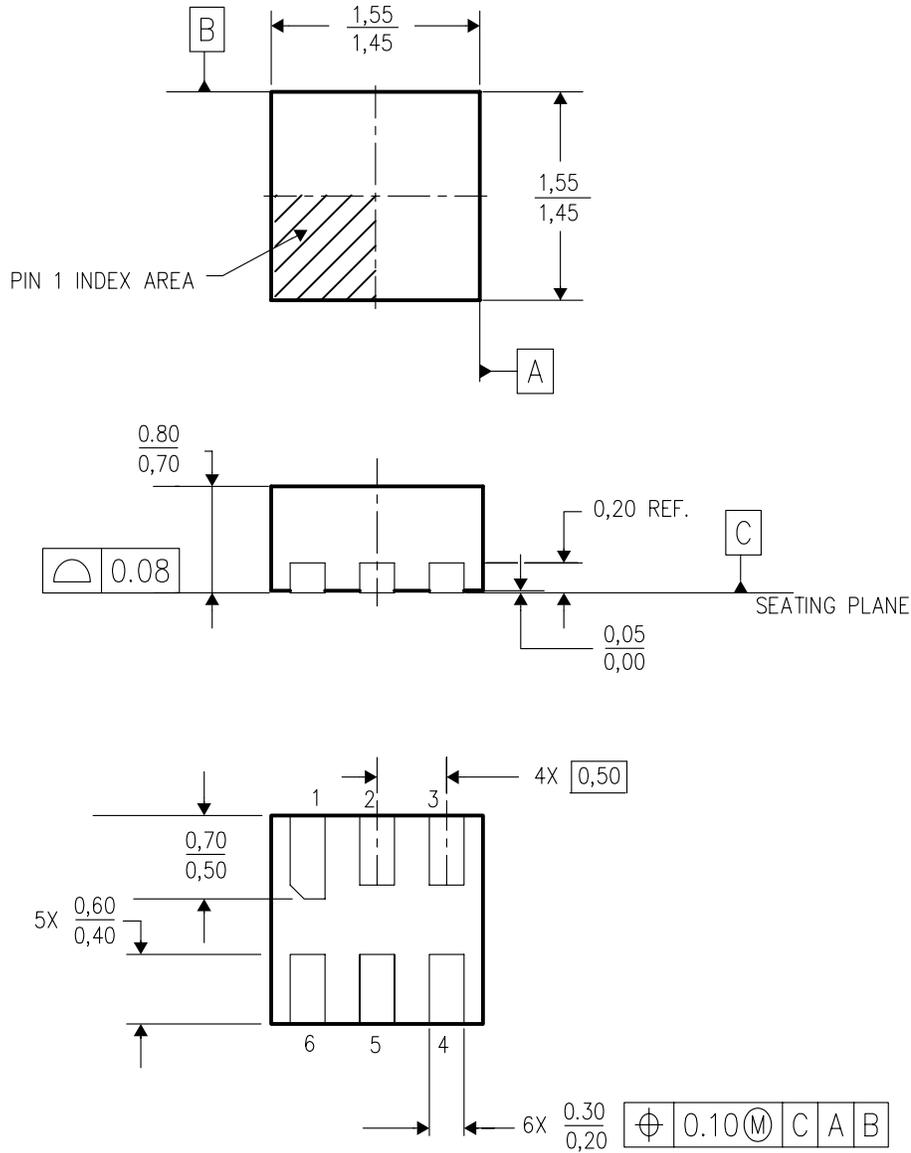
4207810/A 03/06

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Small Outline No−Lead (SON) package configuration.
         D.   This package is lead−free.

DSE (S−PWSON−N6)   PLASTIC SMALL OUTLINE NO−LEAD
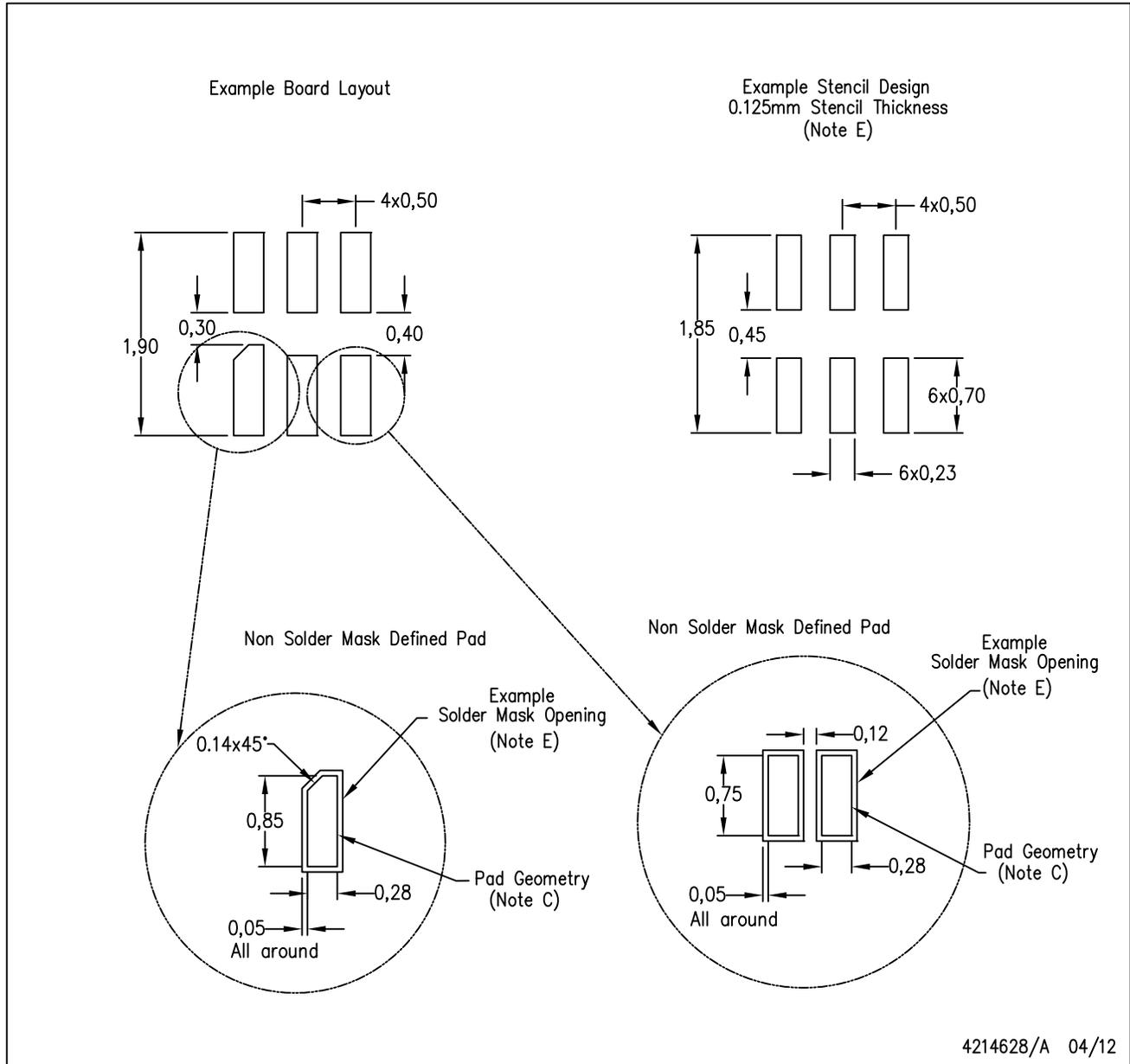
Example Board Layout

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

4x0,50

4x0,50

1,90

0,30   0,40

1,85   0,45

6x0,70

6x0,23

Non Solder Mask Defined Pad

Non Solder Mask Defined Pad

Example
Solder Mask Opening
(Note E)

Example
Solder Mask Opening
(Note E)

0.14x45°

0,85

0,12

0,75

Pad Geometry
(Note C)

0,28

Pad Geometry
(Note C)

0,05
All around

0,28

0,05
All around

4214628/A 04/12

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.

        D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        E. Customers should contact their board fabrication site for solder mask tolerances.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2014, Texas Instruments Incorporated