MULTI-INNO TECHNOLOGY CO., LTD.

OLED MODULE SPECIFICATION

Model : MI12864NO-W

Revision	1.0
Engineering	
Date	
Our Reference	

Address : Room 10J,Xin HaoFang Building, No.188 Shennan Road, Nanshan Drstrict, ShenZhen,China.
Tel : (86-755)2643 9937
Fax : (86-755)8613 4241
Email : sales@multi-inno.com
Web : http://www.multi-inno.com

REVISION RECORD

REV NO.	REV DATE	CONTENTS	REMARKS
1.0	2011-11-28	First Release	preliminary

CONTENTS

■ PHYSICAL DATA

No.	Items:	Specification:	Unit
1	Diagonal Size	2.4	Inch
2	Display Mode	Passive Matrix OLED	-
3	Resolution	128x64	Pixel
4	Active Area	55.01(W) x 27.49(H)	mm
5	Outline Dimension	60.5 (W) x 37.0(H)x2.03(D)	mm
6	Dot Pitch	0.43 (W) x 0.43 (H)	mm
7	Dot Size	0.4 (W) x 0.4 (H)	mm
8	Driver IC	SSD1305Z	-
9	Color	White	-
11	Interface	8-bit 8080,8-bit 6800,SPI,I2C	-
12	Aperture Rate	86	%
13	Weight	9.05 ±10%	g
14	Duty	1/64	-

■ ABSOLUTE MAXIMUM RATINGS

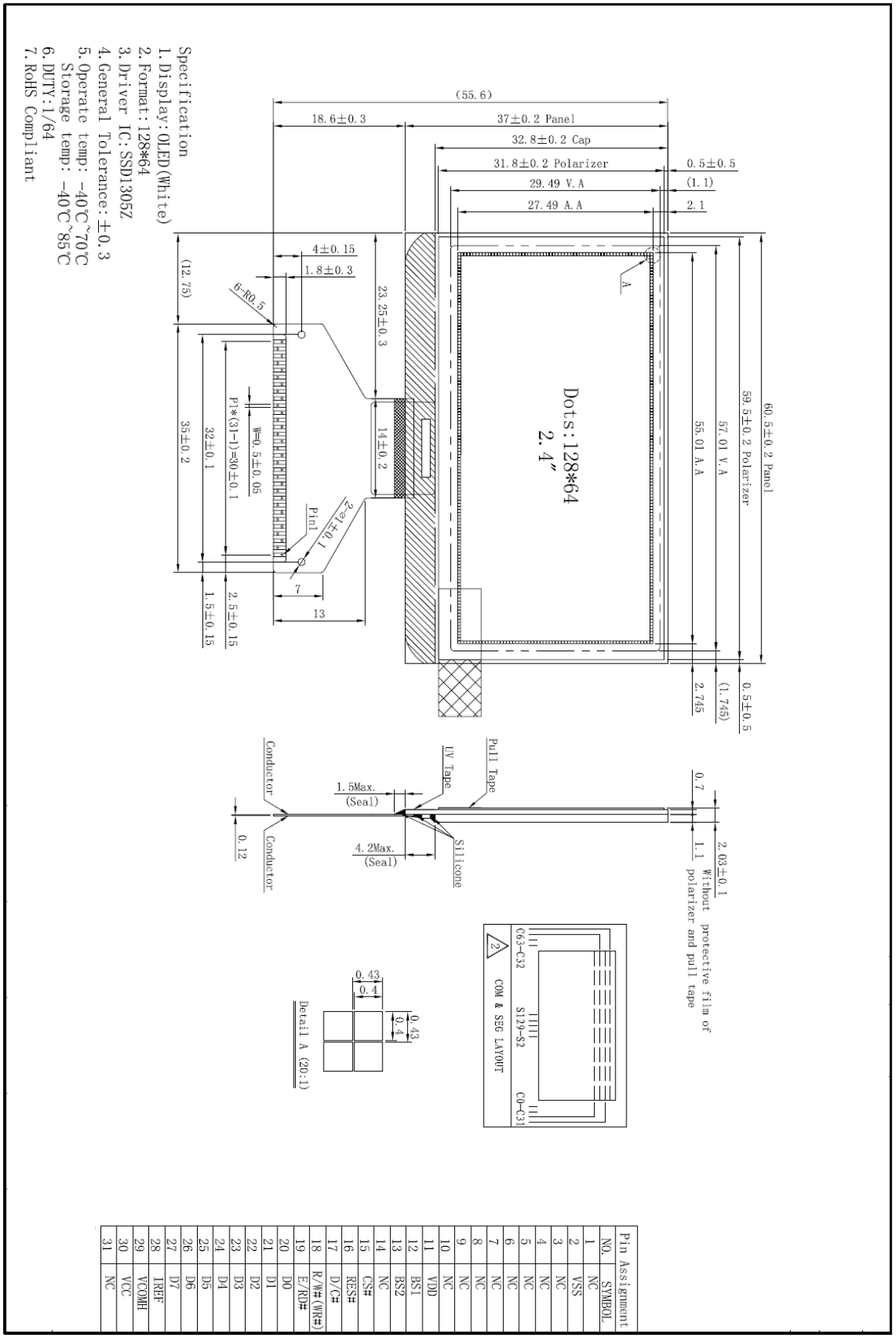
Unless otherwise specified, V_{SS} = 0V (Ta = 25℃)

ITEM	SYMBOL	MIN	MAX	UNIT	REMARK
Logic supply voltage	VDD	-0.3	+4.0	V	IC maximum rating
OLED Operating voltage	VCC	0	+16	V	IC maximum rating
Operating Temp.	Top	-40	+70	℃	-
Storage Temp	Tstg	-40	+85	℃	-

Note (1): All of the voltages are on the basis of “VSS = 0V”.

Note (2): Permanent breakage of module may occur if the module is used beyond the maximum rating. The module can be normal operated under the conditions according to Section 8 “Electrical Characteristics”. Malfunctioning of the module may occur and the reliability of the module may deteriorate if the module is used beyond the conditions.

■ EXTERNAL DIMENSIONS



Pin Assignment		
NO.	SYMBOL	
1	NC	
2	VSS	
3	NC	
4	NC	
5	NC	
6	NC	
7	NC	
8	NC	
9	NC	
10	NC	
11	VDD	
12	BS1	
13	BS2	
14	NC	
15	CS#	
16	RES#	
17	D/C#	
18	R/W# (WR#)	
19	E/RD#	
20	D0	
21	D1	
22	D2	
23	D3	
24	D4	
25	D5	
26	D6	
27	D7	
28	IREF	
29	VCOMH	
30	VCC	
31	NC	

■ ELECTRICAL CHARACTERISTICS

DC Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Logic Supply Voltage	VDD	22±3°C, 55±15%R.H	2.4	3.0	3.5	V
OLED Driver Supply Voltage	VCC	22±3°C, 55±15%R.H	12.5	13	13.5	V
High-level Input Voltage	V_{IH}	-	0.8×VDD	-	-	V
Low-level Input Voltage	V_{IL}	-	-	-	0.2×VDD	V
High-level Output Voltage	V_{OH}	-	0.9×VDD	-	-	V
Low-level Output Voltage	V_{OL}	-	-	-	0.1×VDD	V

Note : The VCC input must be kept in a stable value; ripple and noise are not allowed.

Electro-optical Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Normal Mode Brightness	L_{br}	All pixels ON(1)	40	60	-	cd/m^2
ICC Sleep mode Current	ICC,SLEEP	VDD=2.4V~3.5V, VCC=7V~15V Display OFF,No panel attached	-	-	10	uA
IDD Sleep mode Current	IDD,SLEEP	VDD=2.4V~3.5V, VCC=7V~15V Display OFF,No panel attached	-	-	10	uA
Normal Mode Power Consumption	Pt	All pixels ON(1)	-	380	455	mW
C.I.E(White)	(x)	x,y(CIE1931)	0.26	0.30	0.34	-
	(y)		0.29	0.33	0.37	-
Dark Room Contrast	CR	-	≥2000:1	-	-	-
Response Time	-	-	-	10	-	μ s
View Angle	-	-	≥160	-	-	Degree

Note(1): Normal Mode test conditions are as follows:

- Driving voltage : 13V
- Contrast setting : 0xb0
- Frame rate : 85Hz
- Duty setting : 1/64

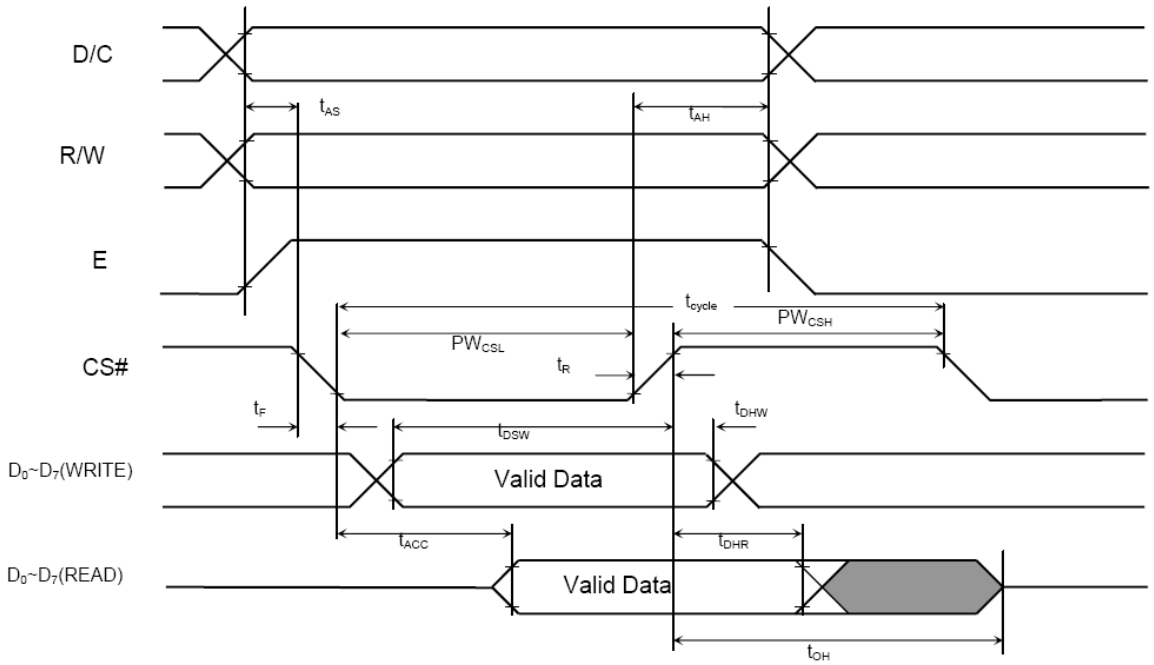
◆AC Characteristics

(1)6800-Series MPU Parallel Interface Timing Characteristics

(VDD - VSS = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

6800-series MCU parallel interface characteristics



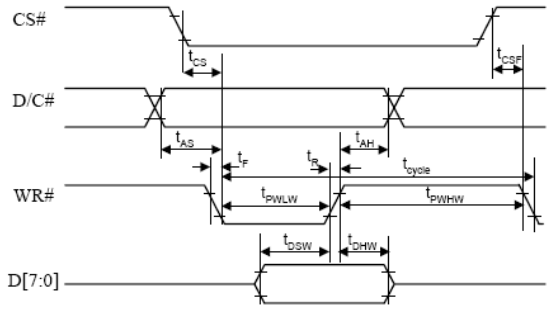
(2)8080-Series MPU Parallel Interface Timing Characteristics

(VDD - VSS = 2.4V to 3.5V, TA = 25°C)

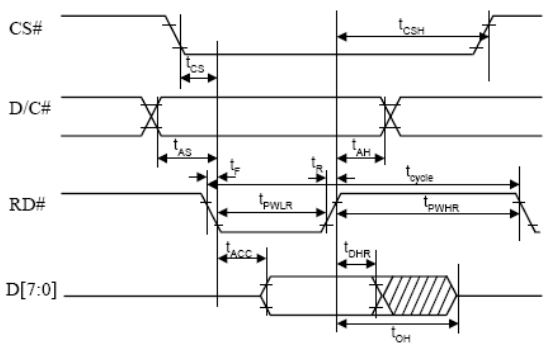
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series parallel interface characteristics (Form 1)

Write cycle (Form 1)

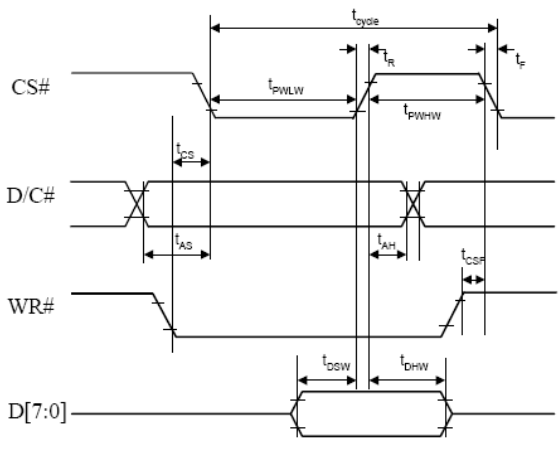


Read cycle (Form 1)

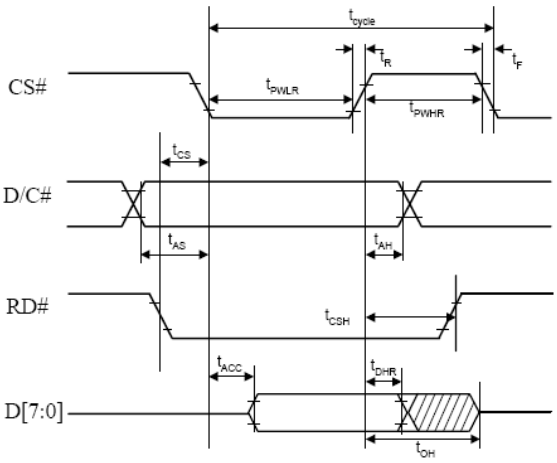


8080-series parallel interface characteristics (Form 2)

Write cycle (Form 2)



Read cycle (Form 2)

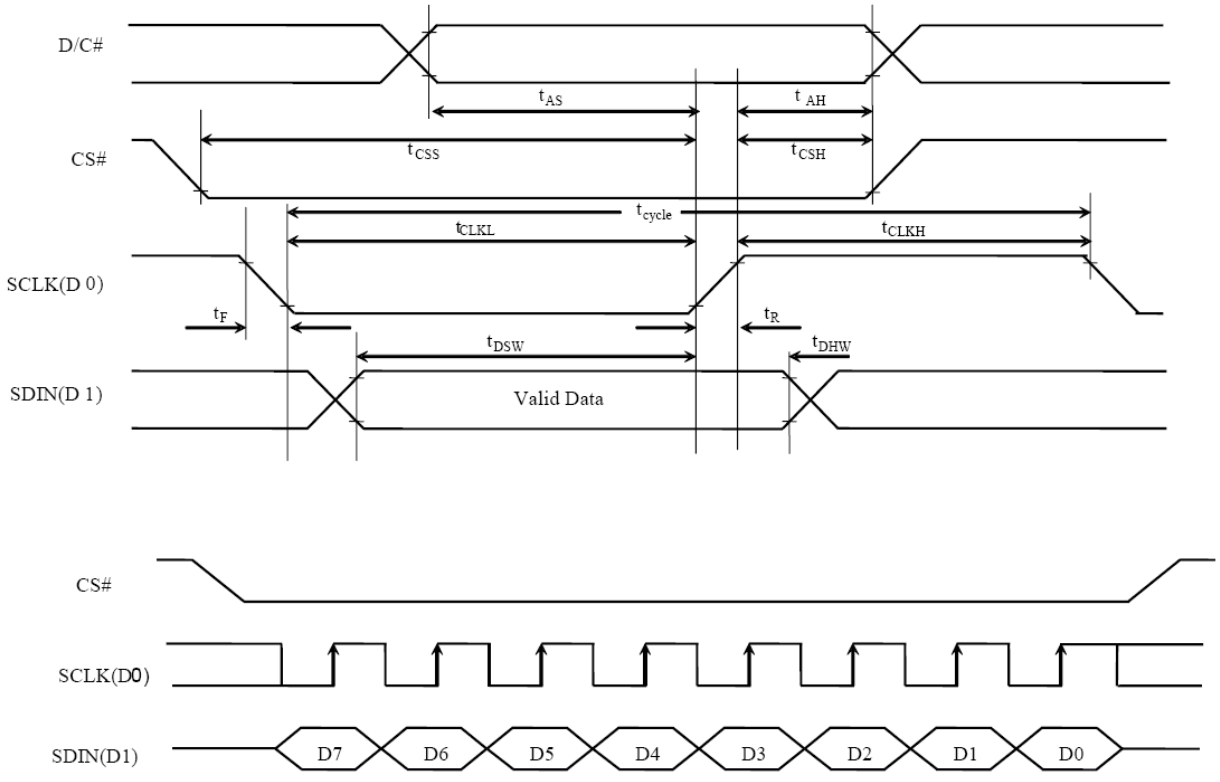


(3)Serial Interface Timing Characteristics

(VDD - VSS = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Serial interface characteristics

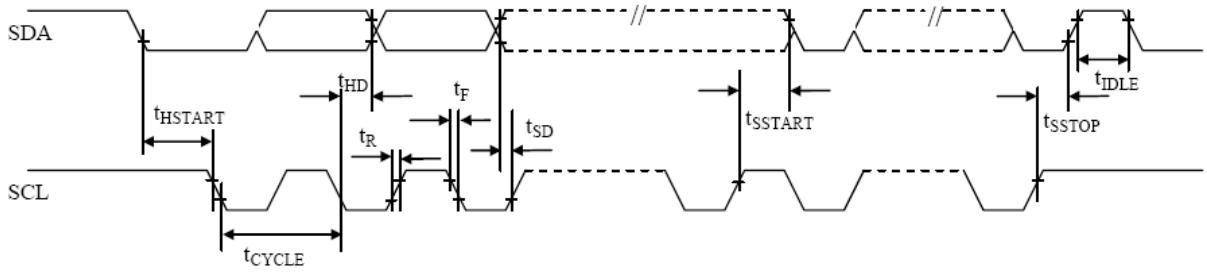


(4) I^2C interface Timing Characteristics

(VDD - VSS = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

I^2C interface Timing characteristics

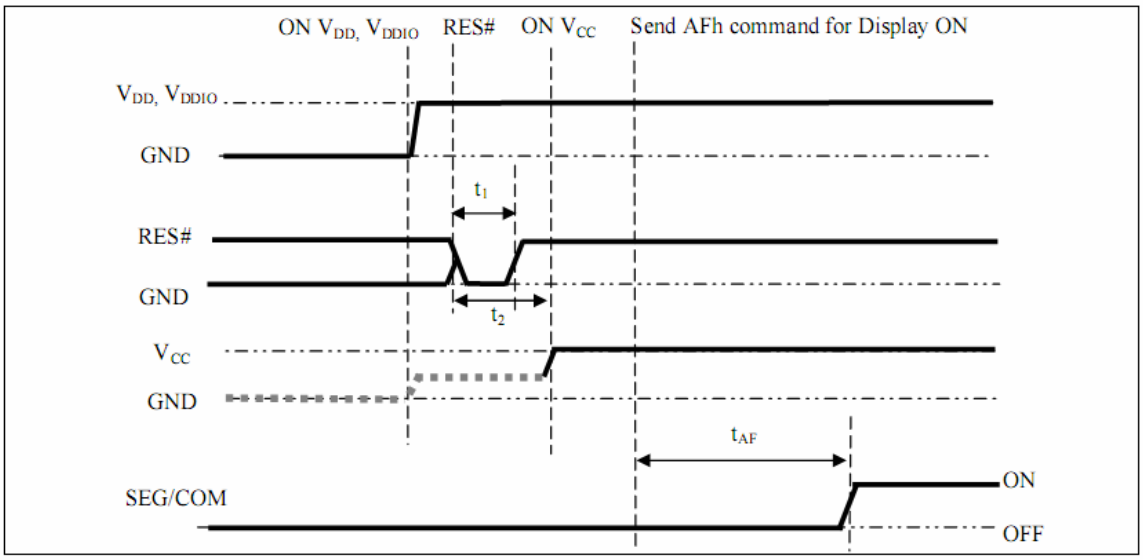


■ FUNCTIONAL SPECIFICATION AND APPLICATION CIRCUIT

1.1 Power ON and Power OFF Sequence

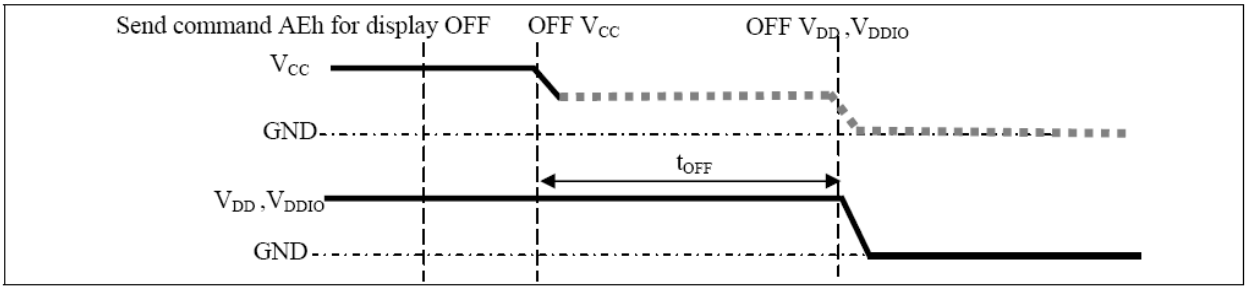
Power ON Sequence:

1. Power ON V_{DD},V_{DDIO}
2. After V_{DD}, V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 3us (t_1)[4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}[1].
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t_{AF}).



Power OFF Sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}[1],[2],[3].
3. Wait for t_{OFF}. Power OFF V_{DD}, V_{DDIO}. (where Minimum t_{OFF}=0ms[5], Typical t_{OFF}=100ms)



Note:

(1)Since an ESD protection circuit is connected between V_{DD}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD}, V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.

(2) V_{CC} should be kept float (disable) when it is OFF.

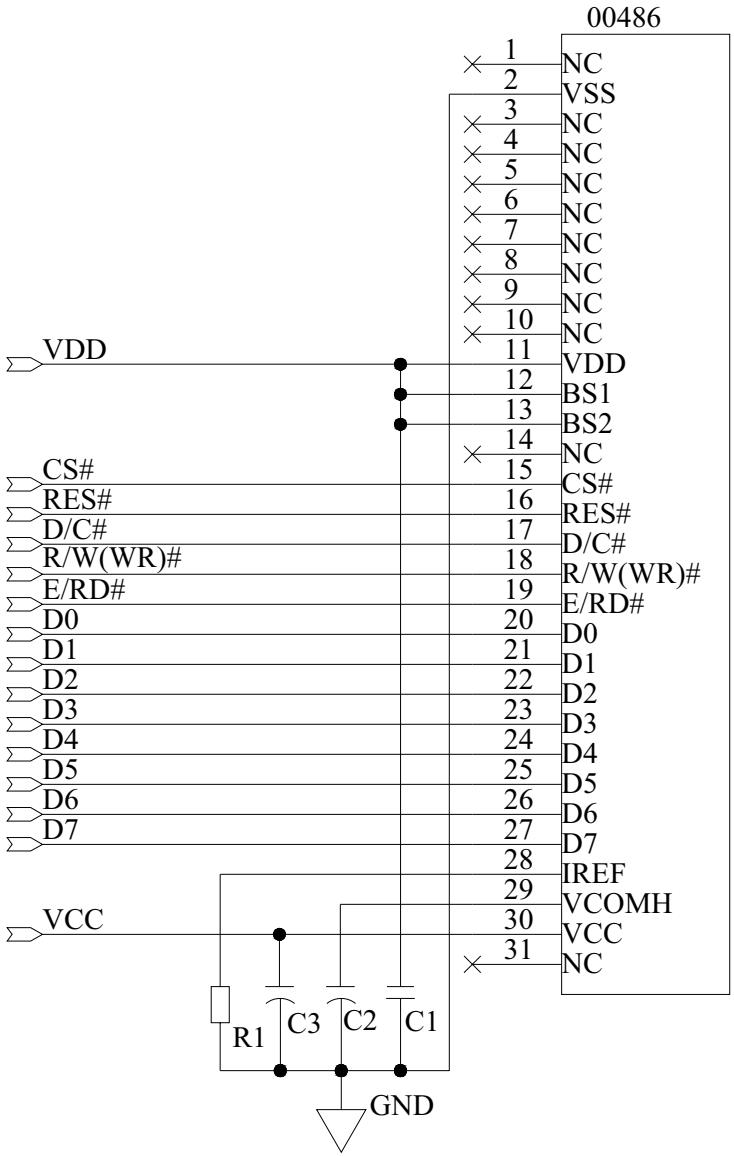
(3) Power Pins(V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.

(4) The register values are reset after t_1.

(5) V_{DD} should not be Power OFF before V_{CC} Power OFF

1.2 Application Circuit

(1).The configuration for 8-bit 8080-parallel interface mode, external VCC is shown in the following diagram.



Pin connected to MCU interface: D[0:7], E/RD#, R/W(WR)#, D/C#, CS#, RES#

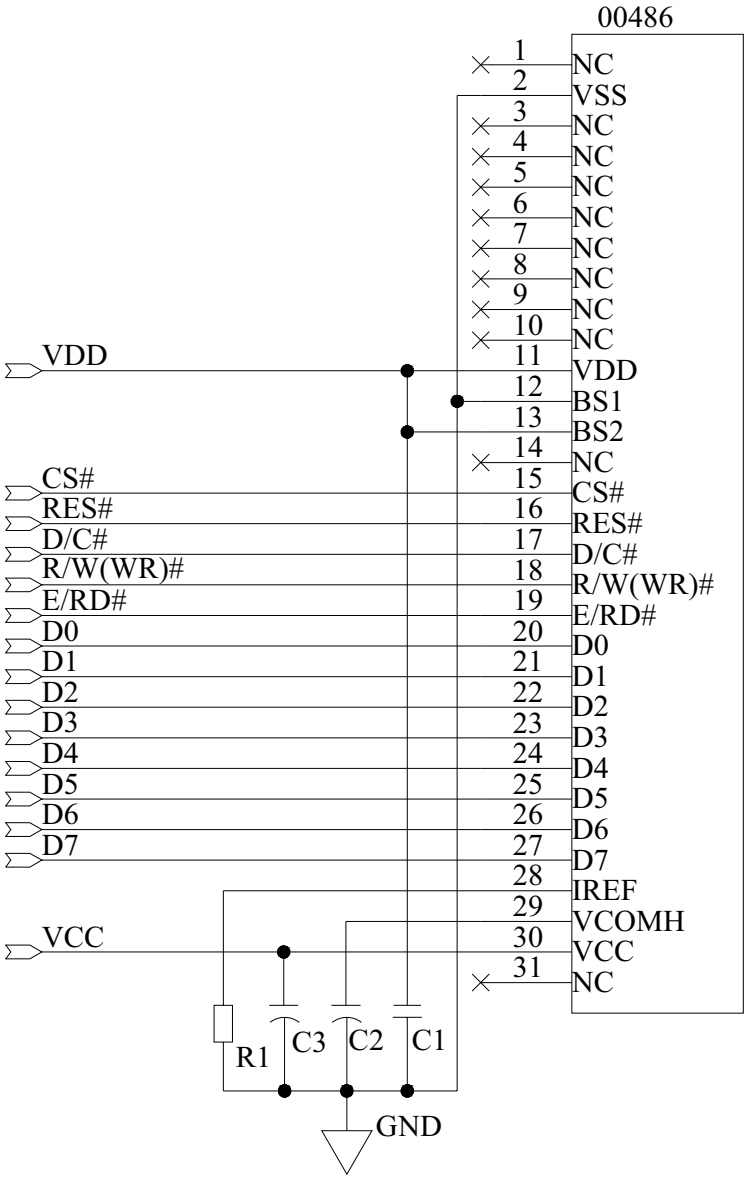
Recommended components:

C1: 0.1uF-0603-X7R±10%.ROHS

C2, C3: 4.7μF/25V.ROHS (Tantalum Capacitors)

R1: 910K ohm 0603 1/10W +/-5%.ROHS

(2).The configuration for 8-bit 6800-parallel interface mode, external VCC is shown in the following diagram.



Pin connected to MCU interface: D[0:7], E/RD#, R/W(WR)#, D/C#, CS#, RES#

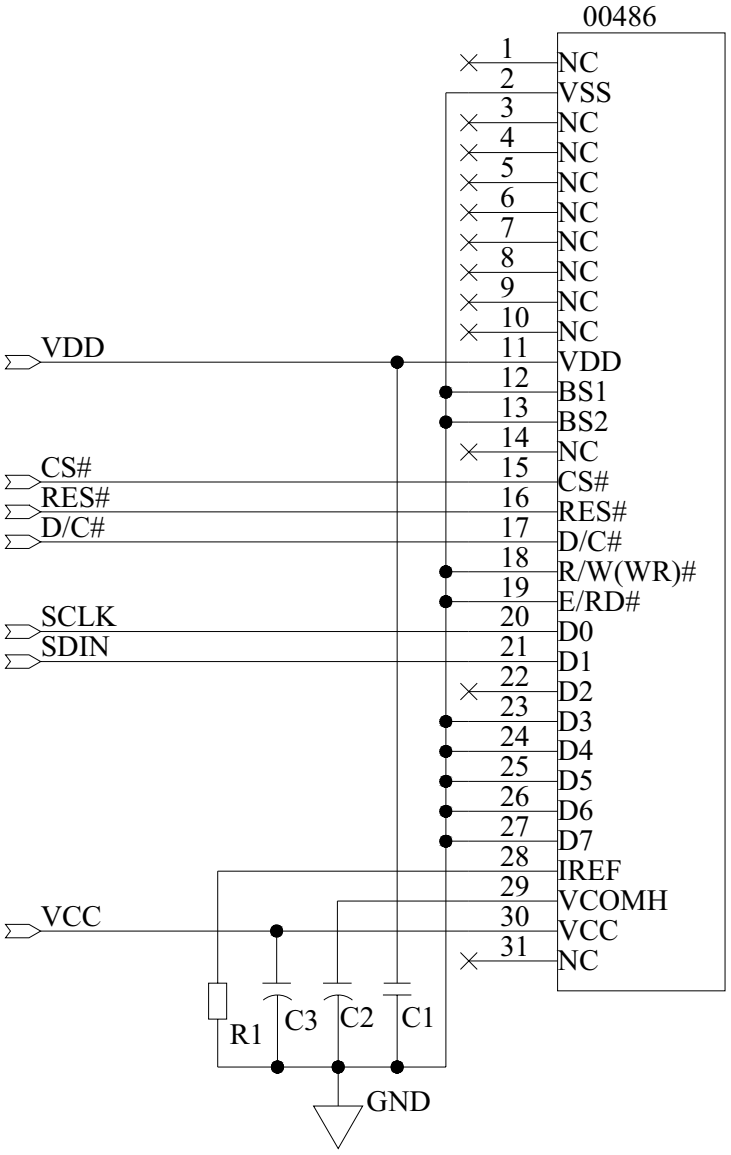
Recommended components:

C1: 0.1uF-0603-X7R±10%.ROHS

C2, C3: 4.7μF/25V.ROHS (Tantalum Capacitors)

R1: 910K ohm 0603 1/10W +/-5%.ROHS

(3).The configuration for SPI interface mode,
external VCC is shown in the following diagram.



Pin connected to MCU interface:SCLK,SDIN, D/C#, CS#, RES#

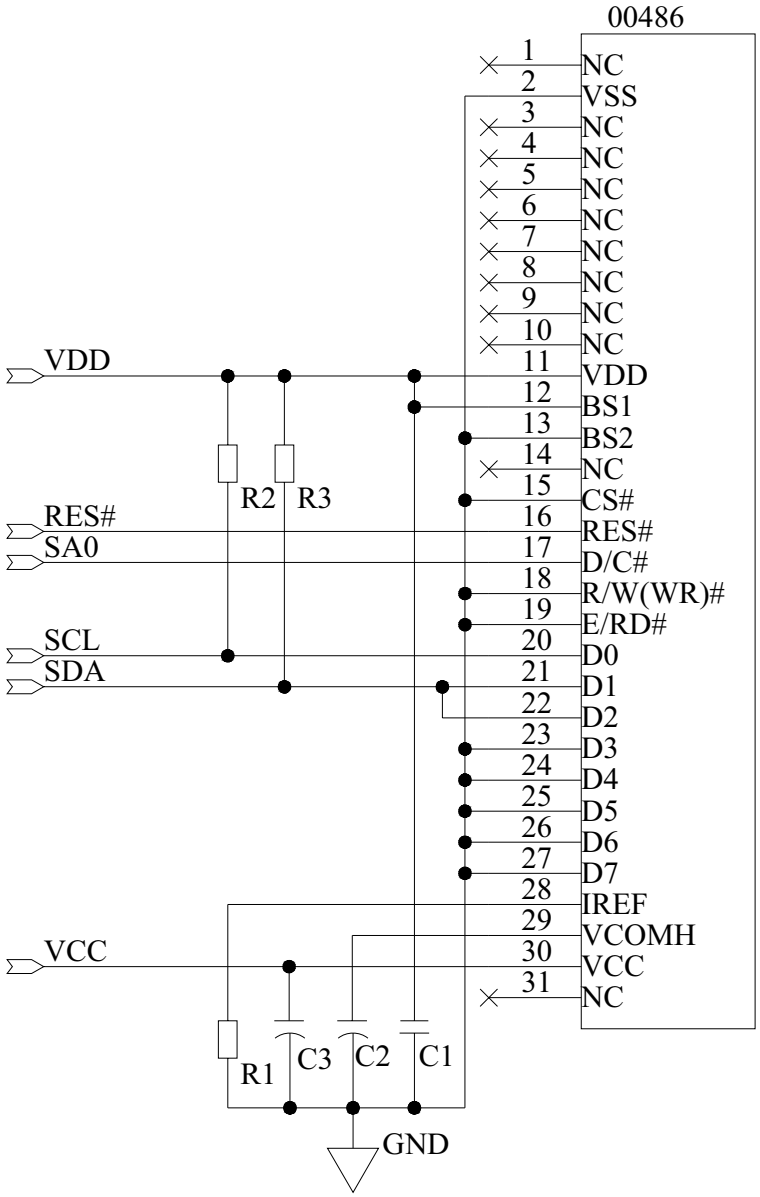
Recommended components:

C1: 0.1uF-0603-X7R±10%.ROHS

C2, C3: 4.7μF/25V.ROHS (Tantalum Capacitors)

R1: 910K ohm 0603 1/10W +/-5%.ROHS

(4).The configuration for I²C interface mode,
external VCC is shown in the following diagram.



Pin connected to MCU interface:, RES#,SA0,SCL,SDA

Component:

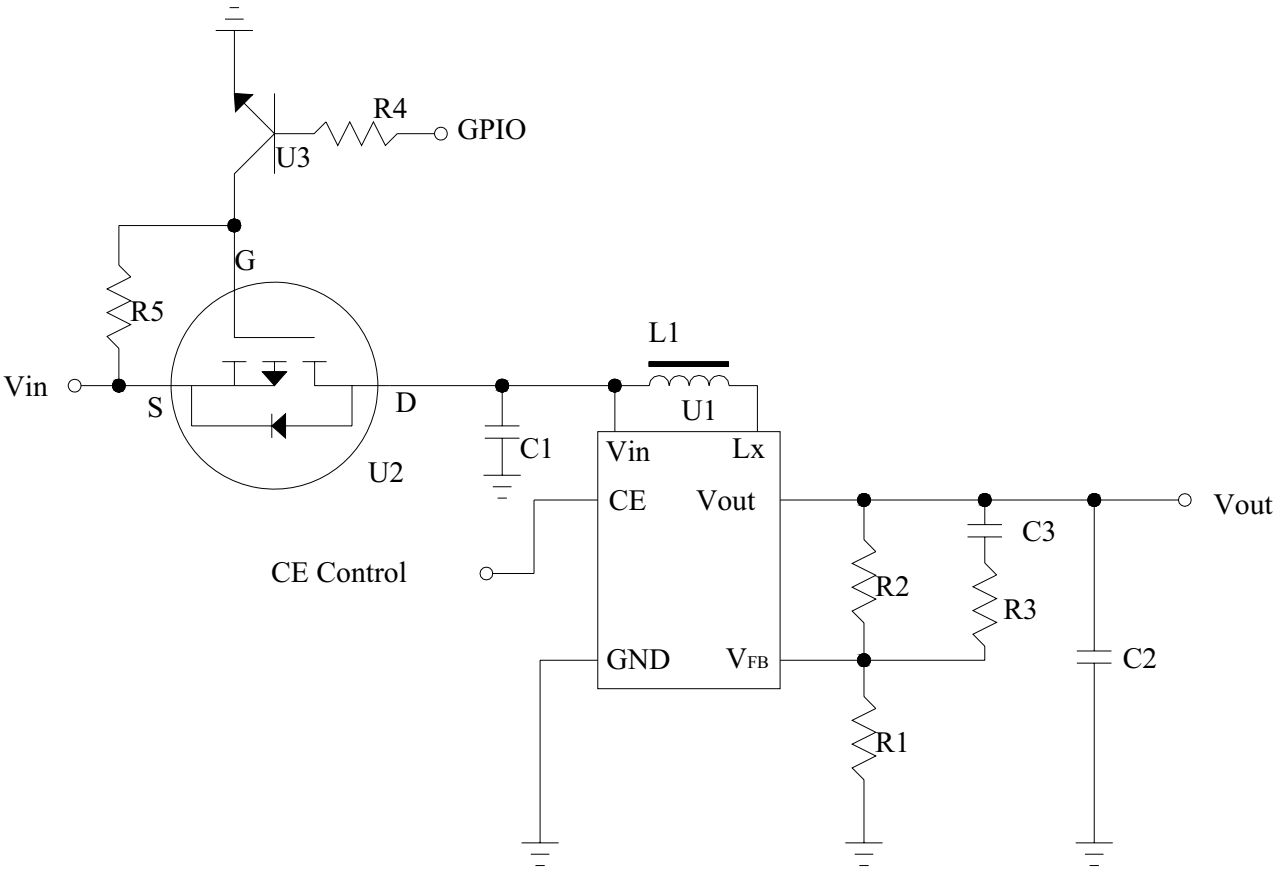
C1: 0.1uF-0603-X7R±10%.ROHS

C2, C3: 4.7μF/25V.ROHS (Tantalum Capacitors)

R1: 910K ohm 0603 1/10W +/-5%.ROHS

R2,R3: 10K ohm 0603 1/10W +/-5%.ROHS

1.3 External DC-DC application circuit



Recommend component

The C1	: 1 uF-0603-X7R±10%.ROHS
The C2	: 1 uF-0603-X7R±10%.ROHS
The C3	: 220pF-0603-X7R±10%.ROHS
The R1	: 0603 1/10W +/-5% 10Kohm.ROHS
The R2	: 0603 1/10W +/-5% 120Kohm.ROHS
The R3	: 0603 1/10W +/-5% 2Kohm.ROHS
The R4	: 0603 1/10W +/-5% 1Kohm.ROHS
The R5	: 0603 1/10W +/-5% 10Kohm.ROHS
The L1	: 22uH
The U1	: R1200
The U2	: FDN338N
The U3	: 8050

1.4 Display Control Instruction

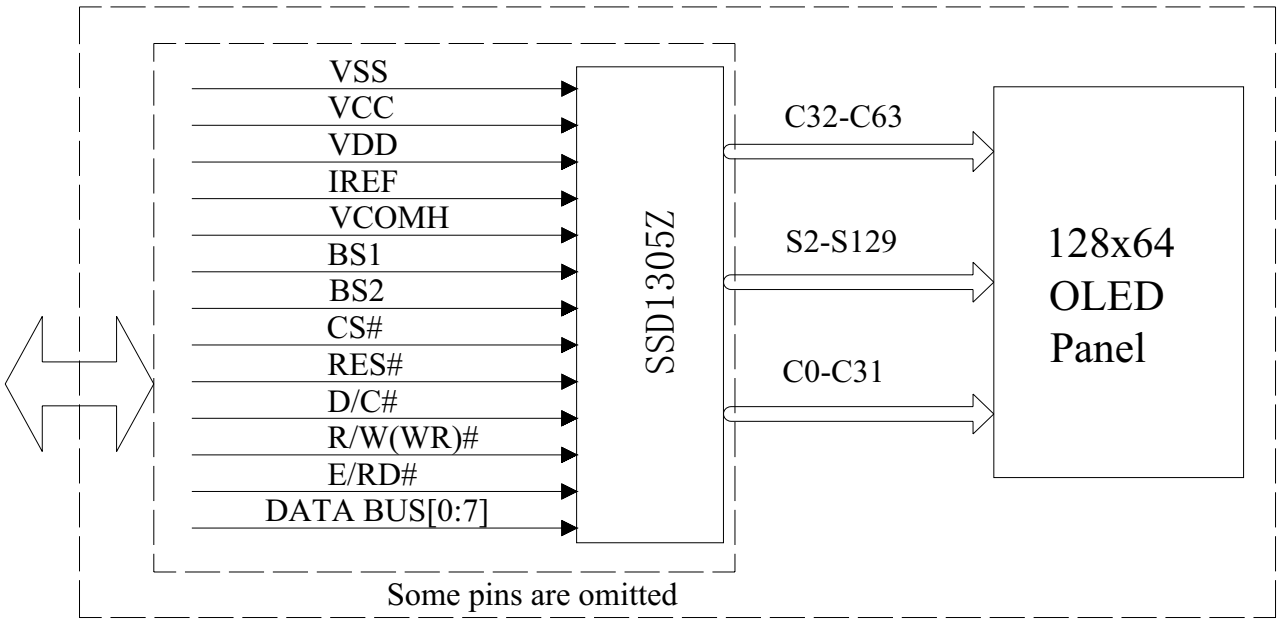
Refer to SSD1305 IC Specification.

1.5 Recommended Software Initialization

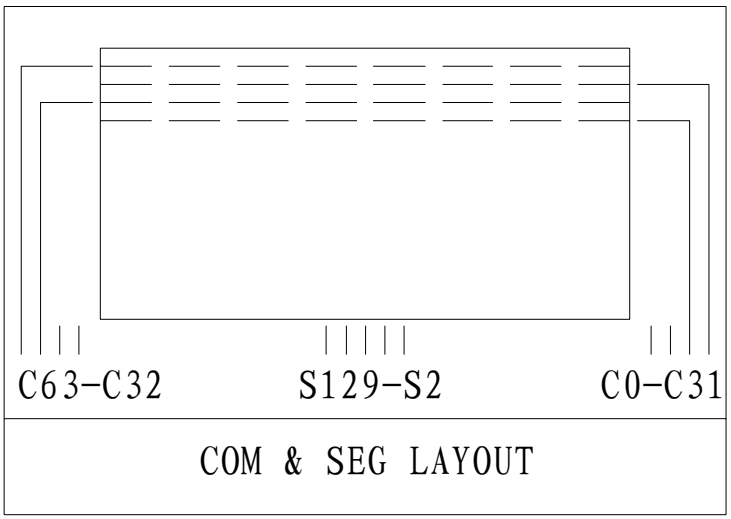
```
void Init_SSD1305()
{
    Write_Command(0xae);
    Write_Command(0xa1);      //segment remap
    Write_Command(0xda);      //common pads hardware: alternative
    Write_Command(0x12);
    Write_Command(0xc8);      //common output scan direction:com63~com0
    Write_Command(0xa8);      //multiplex ration mode:63
    Write_Command(0x3f);
    Write_Command(0xd5);      //display divide ratio/osc. freq. mode
    Write_Command(0x50);      //Osc. Freq:320kHz,DivideRation:1
    Write_Command(0x81);      //contrast control
    Write_Command(0xb0);      //
    Write_Command(0xd9);      //set pre-charge period
    Write_Command(0xf1);      //set period 1:1;period 2:15
    Write_Command(0x20);      //Set Memory Addressing Mode
    Write_Command(0x02);      //page addressing mode
    Write_Command(0xdb);      //VCOM deselect level mode
    Write_Command(0x3c);      //set Vvcomh=0.83*Vcc
    Write_Command(0xad);      //master configuration
    Write_Command(0x8e);      //external VCC supply
    Write_Command(0xa4);      //out follows RAM content
    Write_Command(0xa6);      //set normal display
    Write_Command(0xaf);
}
```

■ INTERFACE PIN CONNECTIONS

1.1 Function Block Diagram



1.2 Panel Layout Diagram



2 Module Interface

<table>
<tr><th>PIN NO.</th><th>PIN NAME</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>NC</td><td>No Connection.</td></tr>
<tr><td>2</td><td>VSS</td><td>Ground.</td></tr>
<tr><td>3~10</td><td>NC</td><td>No Connection.</td></tr>
<tr><td>11</td><td>VDD</td><td>Power supply pin for core logic operation.</td></tr>
<tr><td>12</td><td>BS1</td><td rowspan="2">MCU bus interface selection pins.
<table>
<tr><th>Pin Name</th><th>I²C Interface</th><th>6800-parallel interface (8 bit)</th><th>8080-parallel interface (8 bit)</th><th>Serial interface</th></tr>
<tr><td>BS1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>BS2</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>13</td><td>BS2</td></tr>
<tr><td>14</td><td>NC</td><td>No Connection.</td></tr>
<tr><td>15</td><td>CS#</td><td>Chip Select, active low. In I²C mode, this pin should be connected to VSS.</td></tr>
<tr><td>16</td><td>RES#</td><td>Reset, active low.</td></tr>
<tr><td>17</td><td>D/C#</td><td>H:Data; L :Command.In I²C mode, this pin acts as SA0 for slave address selection.</td></tr>
<tr><td>18</td><td>R/W#(WR#)</td><td>8080: Write; 6800: Read/Write select pin; SPI or I²C:connected to VSS.</td></tr>
<tr><td>19</td><td>E/RD#</td><td>8080: Read; 6800: Read/Write enable pin; SPI or I²C:connected to VSS.</td></tr>
<tr><td>20~27</td><td>D0~D7</td><td>Data bus.
<table>
<tr><th>Pin Name / Bus Interface</th><th colspan="8">Data/Command Interface</th></tr>
<tr><th></th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>8-bit 8080</td><td colspan="8">D[7:0]</td></tr>
<tr><td>8-bit 6800</td><td colspan="8">D[7:0]</td></tr>
<tr><td>SPI</td><td colspan="5">Tie LOW</td><td>NC</td><td>SDIN</td><td>SCLK</td></tr>
<tr><td>I²C</td><td colspan="5">Tie LOW</td><td>SDA_{OUT}</td><td>SDA_{IN}</td><td>SCL</td></tr>
</table></td></tr>
<tr><td>28</td><td>IREF</td><td>This is a segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10uA.</td></tr>
<tr><td>29</td><td>VCOMH</td><td>The pin for COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.</td></tr>
<tr><td>30</td><td>VCC</td><td>Power supply for panel driving voltage.</td></tr>
<tr><td>31</td><td>NC</td><td>No Connection.</td></tr>
</table>

■ RELIABILITY TESTS

<table>
<tr><th colspan="2">Item</th><th>Condition</th><th>Criterion</th></tr>
<tr><td colspan="2">High Temperature Storage (HTS)</td><td>85±2℃, 240 hours</td><td rowspan="6">1. After testing, the function test is ok.
2. After testing, no addition to the defect.
3. After testing, the change of luminance should be within +/- 50% of initial value.
4. After testing, the change for the mono and area color must be within (+/-0.02, +/- 0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates.
5. After testing, the change of total current consumption should be within +/- 50% of initial value.</td></tr>
<tr><td colspan="2">High Temperature Operating (HTO)</td><td>70±2℃, 240 hours</td></tr>
<tr><td colspan="2">Low Temperature Storage (LTS)</td><td>-40±2℃, 240 hours</td></tr>
<tr><td colspan="2">Low Temperature Operating (LTO)</td><td>-40±2℃, 240 hours</td></tr>
<tr><td colspan="2">High Temperature / High Humidity Storage (HTHHS)</td><td>60±3℃, 90%±3%RH, 240 hours</td></tr>
<tr><td colspan="2">Thermal Shock (Non-operation) (TS)</td><td>-40±2℃ ~ 25℃ ~ 85±2℃
(30min) (5min) (30min)
10cycles</td></tr>
<tr><td>Vibration (Packing)</td><td>10~55~10Hz,amplitude 1.5mm, 1 hour for each direction x, y, z</td><td colspan="2" rowspan="2">1. One box for each test.
2. No addition to the cosmetic and the electrical defects.</td></tr>
<tr><td>Drop (Packing)</td><td>Height : 1 m, each time for 6 sides, 3 edges, 1 angle</td></tr>
</table>

Note： 1) For each reliability test, the sample quantity is 3, and only for one test item.
2) The HTHHS test is requested the Pure Water(Resistance＞10MΩ).

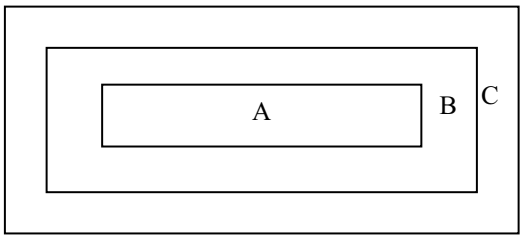
■OUTGOING QUALITY CONTROL SPECIFICATION

◆Standard

According to GB/T2828.1-2003/ISO 2859-1： 1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

◆Definition

1 Major defect : The defect that greatly affect the usability of product.
2 Minor defect : The other defects, such as cosmetic defects, etc.
3 Definition of inspection zone:



Zone A: Active Area

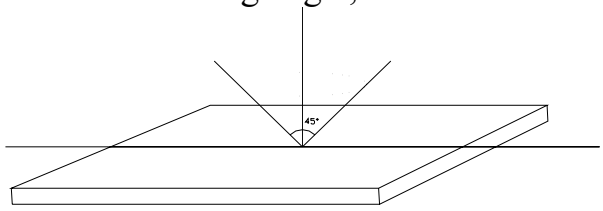
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer`s product.

◆Inspection Methods

1 The general inspection : under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45º viewing angle, under 25±5℃.



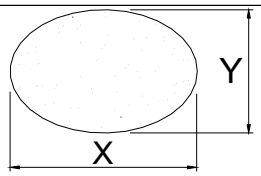
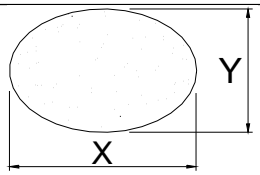
2 The luminance and color coordinate inspection : By PR705 or BM-7 or the equal equipments, in the dark room, under 25±5℃.

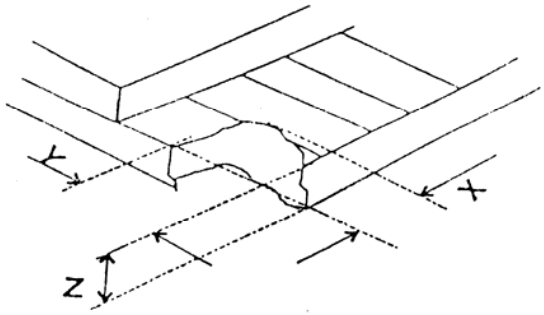
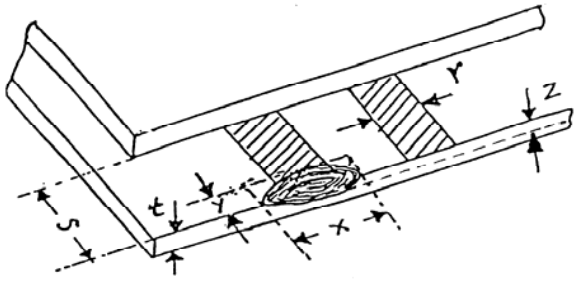
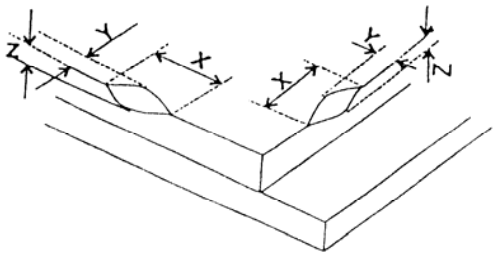
◆Inspection Criteria

1 Major defect : AQL= 0.65

Item	Criterion
Function Defect	1. No display or abnormal display is not accepted
	2. Open or short is not accepted.
	3. Power consumption exceeding the spec is not accepted.
Outline Dimension	Outline dimension exceeding the spec is not accepted.
Glass Crack	Glass crack tends to enlarge is not accepted.

2 Minor Defect : AQL= 1.5

<table>
<tr><td>Item</td><td colspan="4">Criterion</td></tr>
<tr><td rowspan="6">Spot Defect (dimming and lighting spot)</td><td colspan="2" rowspan="2">Size (mm)</td><td colspan="2">Accepted Qty</td></tr>
<tr><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4">  </td><td>Φ≦0.10</td><td colspan="2">Ignored</td></tr>
<tr><td>0.10＜Φ≦0.15</td><td>3</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.15＜Φ≦0. 20</td><td>1</td></tr>
<tr><td>0.20＜Φ</td><td>0</td></tr>
<tr><td colspan="4">Note : Φ= (x + y) / 2</td></tr>
<tr><td rowspan="5">Line Defect (dimming and lighting line)</td><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.03</td><td colspan="2">Ignored</td></tr>
<tr><td>L≦3.0</td><td>0.03＜W≦0.05</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>L≦2.0</td><td>0.05＜W≦0.08</td><td>1</td></tr>
<tr><td>/</td><td>0.08＜W</td><td>As spot defect</td></tr>
<tr><td colspan="5">Remarks: The total of spot defect and line defect shall not exceed 4 pcs.</td></tr>
<tr><td>Polarizer Stain</td><td colspan="4">Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.</td></tr>
<tr><td rowspan="7">Polarizer Scratch</td><td colspan="4">1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.</td></tr>
<tr><td colspan="4">2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :</td></tr>
<tr><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.03</td><td colspan="2">Ignore</td></tr>
<tr><td>5.0＜L≦10.0</td><td>0.03＜W≦0.05</td><td>2</td><td rowspan="3">Ignore</td></tr>
<tr><td>L≦5.0</td><td>0.05＜W≦0.08</td><td>1</td></tr>
<tr><td>/</td><td>0.08＜W</td><td>0</td></tr>
<tr><td rowspan="5">Polarizer Air Bubble</td><td colspan="2">Size</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4">  </td><td>Φ≦0.20</td><td colspan="2">Ignored</td></tr>
<tr><td>0.20＜Φ≦0.50</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.50＜Φ≦0.80</td><td>1</td></tr>
<tr><td>0.80＜Φ</td><td>0</td></tr>
</table>

<table>
<tr><td rowspan="4">Glass Defect (Glass Chiped)</td><td>1. On the corner
 
(mm)
<table><tr><td>x</td><td>≤ 2.0</td></tr><tr><td>y</td><td>≤ S</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>2. On the bonding edge
 
(mm)
<table><tr><td>x</td><td>≤ a / 2</td></tr><tr><td>y</td><td>≤ s / 3</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>3. On the other edges
 
(mm)
<table><tr><td>x</td><td>≤ a / 5</td></tr><tr><td>y</td><td>≤ 1.0</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>Note: t: glass thickness ; s: pad width ; a: the length of the edge</td></tr>
<tr><td>TCP Defect</td><td>Crack, deep fold and deep pressure mark on the TCP are not accepted</td></tr>
<tr><td>Pixel Size</td><td>The tolerance of display pixel dimension should be within ±20% of the spec</td></tr>
<tr><td>Luminance</td><td>Refer to the spec or the reference sample</td></tr>
<tr><td>Color</td><td>Refer to the spec or the reference sample</td></tr>
</table>

■ CAUTIONS IN USING OLED MODULE

◆Precautions For Handling OLED Module:

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
   i. Avoid drop from high, avoid excessive impact and pressure.
   ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
   iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
   iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
   v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
   vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
   i. Be sure to ground the body when handling the OLED Modules.
   ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
   iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
   iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
   v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
   vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrade the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence: $V_{DD} \rightarrow V_{PP}$, and power off sequence: $V_{PP} \rightarrow V_{DD}$.
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module’ s life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and Datasheet of IC controller, otherwise something wrong may be seen.

13.When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆Precautions For Soldering OLED Module:

1. Soldering temperature : 260°C ± 10°C.
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

◆ Precautions For Storing OLED Module:

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between 0°C and 30°C , the relative humidity not over 60%.

◆ Limited Warranty

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) Multi-Inno will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with Multi-Inno OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to Multi-Inno within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of Multi-Inno is limited to repair and/or replacement on the terms above. Multi-Inno will not be responsible for any subsequent or consequential events.

◆Return OLED Module Under Warranty:

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.