UCC2822x Interleaved Dual PWM Controller With Programmable Max Duty Cycle

1 Features

- 2-MHz High-Frequency Oscillator With 1-MHz Operation Per Channel
- Matched Internal Slope Compensation Circuits
- Programmable Maximum Duty Cycle Clamp 60% to 90% Per Channel
- Peak Current Mode Control With Cycle-by-Cycle Current Limit
- Current Sense Discharge Transistor for Improved Noise Immunity
- Accurate Line Undervoltage and Overvoltage Sense With Programmable Hysteresis
- Opto-Coupler Interface
- 110-V Internal Start-Up JFET (UCC28221)
- Operates From 12-V Supply (UCC28220)
- Programmable Soft Start

2 Applications

- High Output Current (50-A to 100-A) Converters
- Maximum Power Density Designs
- High-Efficiency 48-V Input With Low Output Ripple Converters
- High-Power Offline, Telecom, and Datacom Power Supplies

3 Description

The UCC28220 and UCC28221 are a family of BiCMOS interleaved dual channel PWM controllers. Peak current mode control is used to ensure current sharing between the two channels. A precise maximum duty cycle clamp can be set to any value between 60% and 90% duty cycle per channel.

The UCC28220 has an UVLO turnon threshold of 10 V for use in 12-V supplies while UCC28221 has a turnon threshold of 13 V for systems needing wider UVLO hysteresis. Both have 8-V turnoff thresholds.

Additional features include a programmable internal slope compensation with a special circuit which is used to ensure exactly the same slope is added to each channel and a high-voltage 110-V internal JFET for easier start-up for the wider hysteresis UCC28221 version.

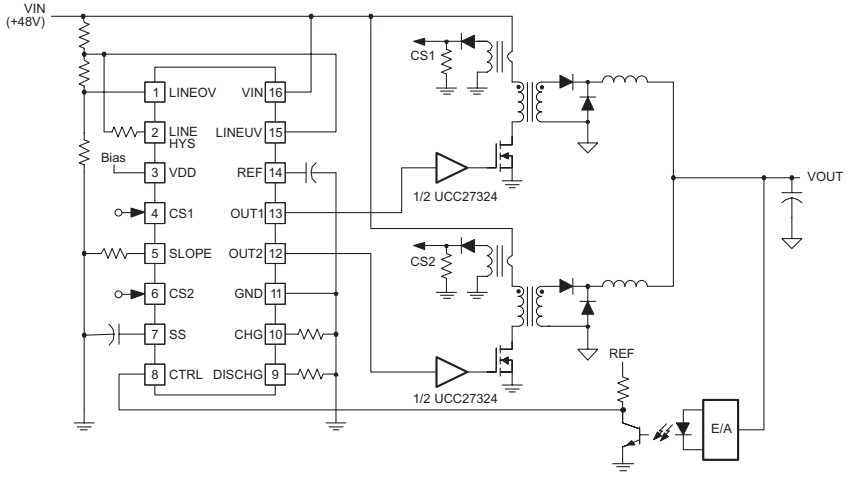
The UCC28220 is available in both 16-pin SOIC and low-profile TSSOP packages. The UCC28221 also comes in 16-pin SOIC package and a slightly larger 20-pin TSSOP package to allow for high-voltage pin spacing to meet UL1950 creepage clearance safety requirements.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC28220, UCC28221	SOIC (16)	9.00 mm × 3.90 mm
	TSSOP (16)	5.00 mm × 4.40 mm
UCC28221	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



Pin 16 is a no connect (NC) on UCC28220 which does not include the JFET option.

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4 Revision History

Changes from Revision F (September 2016) to Revision G **Page**

- Deleted Control Loop Compensation section. ... 19
- Deleted Current Loop section. ... 19
- Deleted Voltage Loop ($T_{V(S)}$) section ... 19

Changes from Revision E (March 2009) to Revision F **Page**

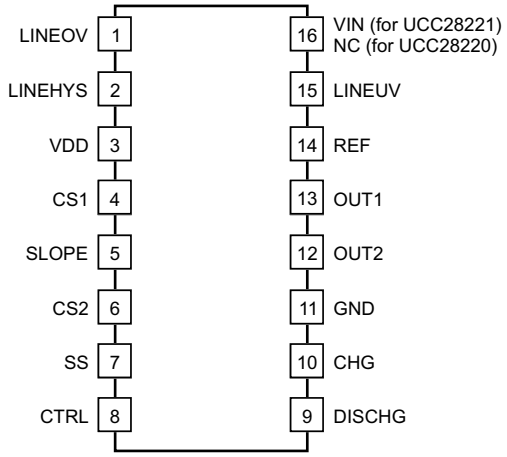
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table; see POA at the end of the data sheet ... 3
- Added *Thermal Information* table ... 5

5 Device Comparison Table

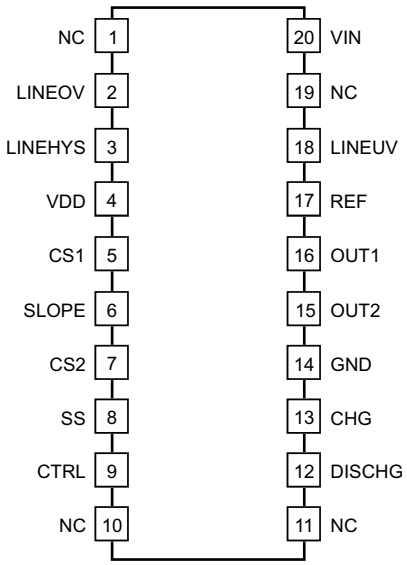
DEVICE	DESCRIPTION	PACKAGE OPTION
UCC2732x	Dual 4-A High Speed Low Side MOSFET Drivers	SOIC (8), PowerPAD MSOP (8), PDIP (8)
UCC2742x	Dual 4-A High Speed Low Side MOSFET Drivers with Enable	SOIC (8), PowerPAD MSOP (8), PDIP (8)
TPS281x	Dual 2.4-A High Speed Low Side MOSFET Drivers	SOIC (8), TSSOP (8), PDIP (8)
UC371x	Dual 2.4-A High Speed Low Side MOSFET Drivers	SOIC (8), PowerSOIC (14), PDIP (8)

6 Pin Configuration and Functions

D or PW Package
16-Pin SOIC or TSSOP
Top View



PW Package
20-Pin TSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC, TSSOP (16)	TSSOP (20)		
CHG	10	13	I	Sets oscillator charge current: A resistor from this pin to GND sets up the charging current of the internal C_T capacitor used in the oscillator. This resistor, in conjunction with the resistor on the DISCHG pin is used to set up the operating frequency and maximum duty cycle. Under normal operation the dc voltage on this pin is 2.5 V.
CS1	4	5	I	Channel 1 current sense input: These 2 pins are the current sense inputs to the device. The signals are internally level shifted by 0.5 V before the signal gets to the PWM comparator. Internally the slope compensation ramp is added to this signal. The linear operating range on this input is 0 to 1.5 V. Also, this pin gets pulled to ground each time its respective output goes low (that is: OUT1 and OUT2).
CS2	6	7	I	Channel 2 current sense input: These 2 pins are the current sense inputs to the device. The signals are internally level shifted by 0.5 V before the signal gets to the PWM comparator. Internally the slope compensation ramp is added to this signal. The linear operating range on this input is 0 to 1.5 V. Also, this pin gets pulled to ground each time its respective output goes low (that is: OUT1 and OUT2).
CTRL	8	9	I	Feedback control input:

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	SOIC, TSSOP (16)	TSSOP (20)		
DISCHG	9	12	I	Sets oscillator discharge current: A resistor from this pin to GND sets up the discharge current of the internal C_T capacitor used in the oscillator. This resistor, in conjunction with the resistor on the CHG pin is used to set up the operating frequency and maximum duty cycle. Under normal operation the dc voltage on this pin is 2.5 V.
GND	11	14	—	Device ground
LINEHYS	2	3	I	Sets line comparator hysteresis: This pin is controlled by both the LINEOV and LINEUV pins. It is used to control the hysteresis values for both the over and under voltage line detectors.
LINEOV	1	2	I	Input for line over voltage comparator: This pin is connected to a comparator and used to monitor the line voltage for an over voltage condition. The typical threshold is 1.26 V.
LINEUV	15	18	I	Input for line under voltage comparator: This pin is connected to a comparator and used to monitor the line voltage for an under voltage condition. The typical threshold is 1.26 V.
N/C	16	1, 10, 11, 19	—	No connection
OUT1	13	16	O	PWM output from channel 1: These output buffers are intended to interface with high current MOSFET drivers. The output drive capability is approximately 33 mA and has an output impedance of 100 Ω. The outputs swing between GND and REF.
OUT2	12	15	O	PWM output from channel 2: These output buffers are intended to interface with high current MOSFET drivers. The output drive capability is approximately 33 mA and has an output impedance of 100 Ω. The outputs swing between GND and REF.
REF	14	17	O	Reference voltage output: REF is a 3.3-V output used primarily as a source for the output buffers and other internal circuits. It is protected from accidental shorts to ground. For improved noise immunity, TI recommends the reference pin be bypassed with a minimum of 0.1 µF of capacitance to GND.
SLOPE	5	6	I	Sets slope compensation: This pin sets up a current used for the slope compensation ramp. A resistor to ground sets up a current, which is internally divided by 25 and then applied to an internal 10-pF capacitor. Under normal operation th dc voltage on this pin is 2.5 V.
SS	7	8	I	Soft-start input: A capacitor to ground sets up the soft-start time for the open loop soft-start function. The source and sink current from this pin is equal to 3/7th of the oscillator charge current set by the resistor on the CHG pin. The soft start capacitor is held low during UVLO and during a Line OV or UV condition. Once an OV or UV fault occurs, the soft-start capacitor is discharged by a current equal to its charging current. The capacitor does NOT quickly discharge during faults. In this way, the controller has the ability to recover quickly from very short line transients. This pin can also be used as an Enable/Disable function.
VDD	3	4	I	Device supply input: This is used to supply power to the device, monitoring this pin is a the UVLO circuit. This is used to insure glitch-free startup operation. Until VDD reaches its UVLO threshold, it remains in a low power mode, drawing approximately 150 µA of current and forcing pins, SS, CS1, CS2, OUT1, and OUT2 to logic 0 states. If the VDD falls below 8 V after reaching turnon, it goes back into this low power state. In the case of the UCC28221, the UVLO threshold is 13 V. It is 10 V for the UCC28220. Both versions have a turnoff threshold of 8 V.
VIN	—	20	I	High voltage start-up input: This pin has an internal high voltage JFET used for startup. The drain is connected to VIN, while its' source is connected to VDD. During startup, this JFET delivers 12 mA typically with a minimum of 4 mA to VDD, which in turn, charges up the VDD bypass capacitor. When VDD gets to 13 V, the JFET is turned off.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
High-voltage start-up input, V_{IN}			110	V
Supply voltage, V_{DD}			15	V
Output current (OUT1, OUT2) dc, $I_{OUT(dc)}$			±10	mA
OUT1/ OUT2 capacitive load			200	pF
REF output current, I_{REF}			10	mA
Current sense inputs, CS1, CS2		–1	2	V
Analog inputs (CHG, DISCHG, SLOPE, REF, CNTRL)		–0.3	3.6	V
Analog inputs (SS, LINEOV, LINEUV, LINEHYS)		–0.3	7	V
Power dissipation at T_A = 25°C	PW package		400	mW
	D package		650	
Junction operating temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	High-voltage start-up input	36	76	V
V_{DD}	Supply voltage	8.4	14.5	V

7.4 Thermal Information

THERMAL METRIC(1)		UCC28220, UCC28221		UCC28221	UNIT
		D (SOIC)	PW (TSSOP)	PW (TSSOP)	
		16 PINS	16 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	100.9	92.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.6	28.8	27.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.6	46.6	43.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.7	1.4	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.3	46	43.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

V_{DD} = 12 V, 0.1-µF capacitor from VDD to GND, 0.1-µF capacitor from REF to GND, F_{OSC} = 1 MHz, T_A = –40°C to 105°C, and $T_A = T_J$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERALL					
Operating VDD		8.4		14.5	V
Quiescent current	SS = 0 V, no switching, F_{OSC} = 1 MHz	1.5	3	4	mA
Operating current	Outputs switching, F_{OSC} = 1 MHz	1.6	3.5	6	mA
START-UP					
Startup current	UCC28220, VDD < (UVLO – 0.8)			200	µA
UVLO start threshold	UCC28220	9.5	10	10.5	V
	UCC28221	12.3	13	13.7	
UVLO stop threshold		7.6	8	8.4	V
UVLO hysteresis	UCC28220	1.8	2	2.2	V
	UCC28221	4.8	5	5.2	
JFET ON threshold	SS = 0, outputs not switching, VDD decreasing	9.5	10	10.5	V
	SS = 2 V, Cntrl = 2 V, output switching, VDD decreasing; same threshold as UVLO stop	7.6	8	8.4	
High voltage JFET current	VIN = 36 V to 76 V, VDD = 0 V	16	48	100	mA
	VIN = 36 V to 76 V, VDD = 10 V	4	16	40	
	VIN = 36 V to 76 V, VDD < UVLO	4	12	40	
JFET leakage	VIN = 36 V to 76 V, VDD = 14 V			100	µA
REFERENCE					
Output voltage	8 V < VDD < 14 V, ILOAD = 0 mA to –10 mA	3.15	3.3	3.45	V
Output current	Outputs not switching, CNTRL = 0 V	10			mA
Output short-circuit current	V_{REF} = 0 V	–40	–20	–10	mA
V_{REF} UVLO		2.55	3	3.25	V
SOFT START					
SS charge current	RCHG = 10.2 kΩ, SS = 0 V	–70	–100	–130	µA
SS discharge current	RCHG = 10.2 kΩ, SS = 2 V	70	100	130	µA
SS initial voltage	LINEOV = 2 V, LINEUV = 0 V	0.5	1	1.5	V
SS voltage at 0% dc	Point at which output starts switching	0.5	1.2	1.8	V
SS voltage ratio		75%	90%	100%	
SS max voltage	LINEOV = 0 V, LINEUV = 2 V	3	3.5	4	V
OSCILLATOR AND PWM					
Output frequency	RCHG = 10.2 kΩ, RDISCHG = 10.2 kΩ	450	500	550	kHz
Oscillator frequency	RCHG = 10.2 kΩ, RDISCHG = 10.2 kΩ	900	1000	1100	kHz
Output maximum duty cycle	RCHG = 10.2 kΩ, RDISCHG = 10.2 kΩ, measured at OUT1 and OUT2	73%	75%	77%	
CHG voltage		2	2.5	3	V
DSCHG voltage		2	2.5	3	V
SLOPE COMPENSATION					
Slope	RSLOPE = 75 kΩ, RCH = 66 kΩ, RDISCHG = 44 kΩ, Csx = 0 V to 0.5 V	140	200	260	mV/us
Channel matching	RSLOPE = 75 kΩ, Csx = 0 V		0%	10%	
CURRENT SENSE					
CS1, CS2 bias current	CS1 = 0, CS2 = 0	–500	0	500	nA
Prop delay CSx to OUTx	CSx input 0 V to 1.5 V step		40	85	ns
CS1, CS2 sink current	CSx = 2 V	2.3	4.5	7	mA

Electrical Characteristics (continued)

V_{DD} = 12 V, 0.1-µF capacitor from VDD to GND, 0.1-µF capacitor from REF to GND, F_{OSC} = 1 MHz, T_A = –40°C to 105°C, and $T_A = T_J$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CNTRL					
Resistor ratio(1)			0.6		
Ctrl input current	CTRL = 0 V and 3.3 V	–100	0	100	nA
Ctrl voltage at 0% dc	CSx = 0 V, point at which output starts switching (checks resistor ratio)	0.5	1.2	1.8	V
OUTPUT (OUT1, OUT2)					
Low level	I_{OUT} = 10 mA		0.4	1	V
High level	I_{OUT} = −10 mA, VREF – VOUT		0.4	1	V
Rise time	C_{LOAD} = 50 pF		10	20	ns
Fall time	C_{LOAD} = 50 pF		10	20	ns
LINE SENSE					
LINEOV threshold	T_A = 25°C	1.24	1.26	1.28	V
	T_A = –40°C to 105°C	1.235	1.26	1.285	
LINEUV threshold	T_A = 25°C	1.24	1.26	1.28	V
	T_A = –40°C to 105°C	1.235	1.26	1.285	
LINEHYST pullup voltage	LINEOV = 2 V, LINEUV = 2 V	3.1	3.25	3.4	V
LINEHYST off leakage	LINEOV = 0 V, LINEUV = 2 V	–500	0	500	nA
LINEHYS pullup resistance	I = –20 µA		100	500	Ω
LINEHYS pulldown resistance	I = 20 µA		100	500	Ω
LINEOV, LINEUV bias I	LINEOV = 1.25 V, LINEUV = 1.25 V	–500		500	nA

(1) Ensured by design. Not 100% tested in production.

7.6 Typical Characteristics

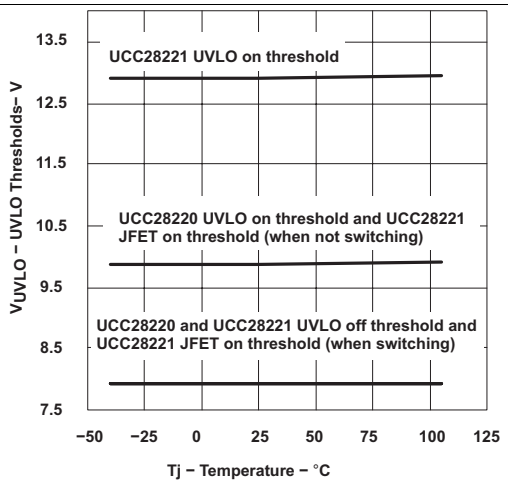


Figure 1. UVLO Thresholds vs Temperature

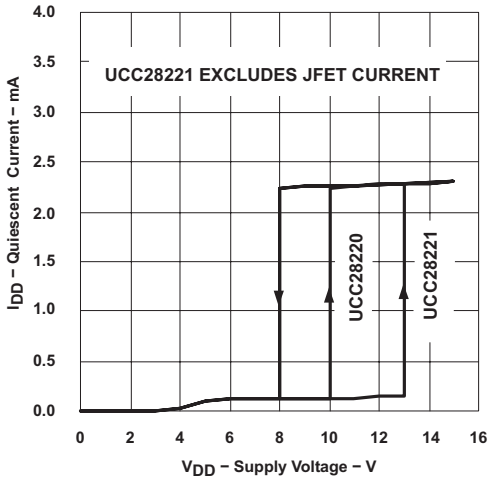


Figure 2. Quiescent Current vs Supply Voltage

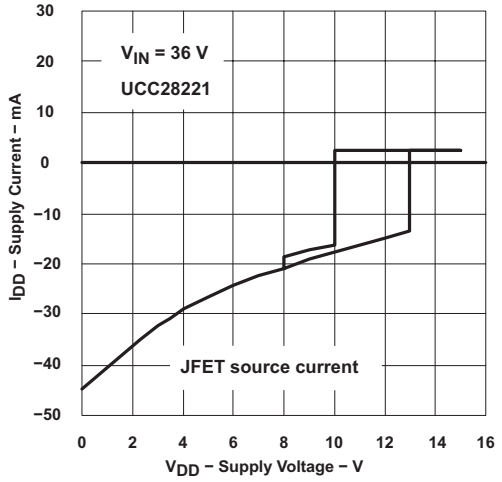


Figure 3. Supply Current vs Supply Voltage

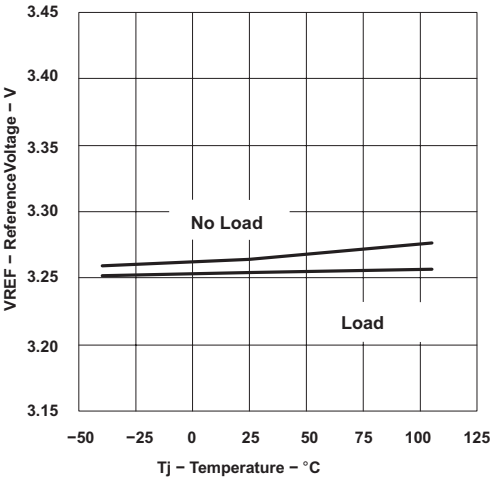


Figure 4. Reference Voltage vs Temperature

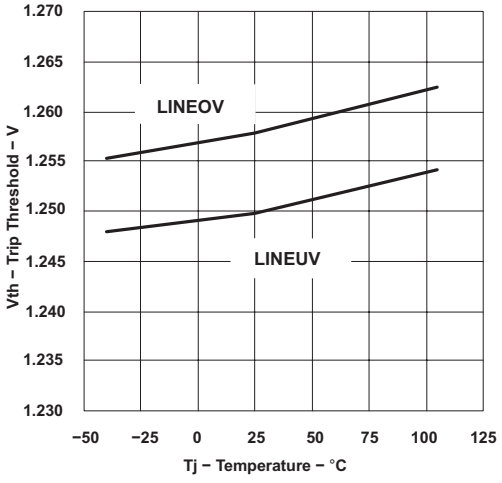


Figure 5. LINEOV and LINEUV Thresholds vs Temperature

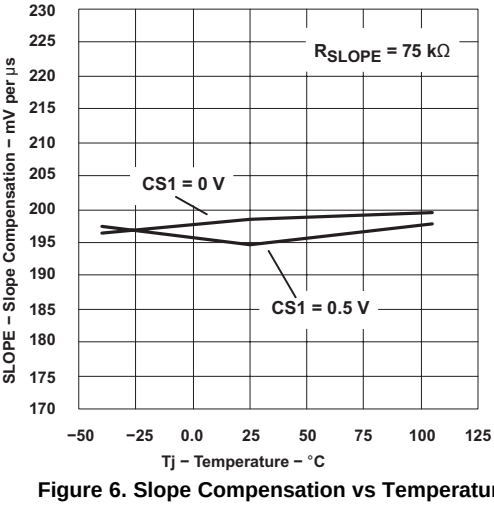


Figure 6. Slope Compensation vs Temperature

Typical Characteristics (continued)

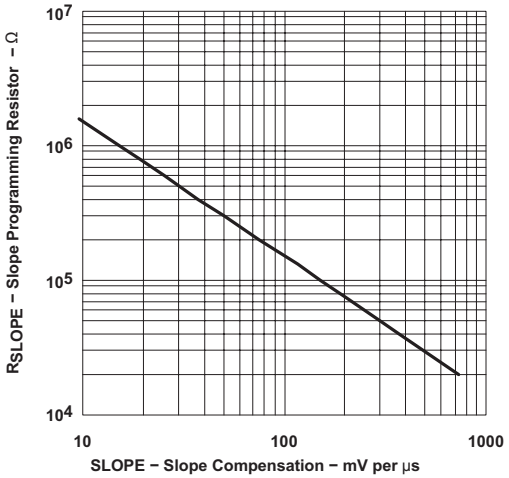


Figure 7. Programming Resistor vs Slope Compensation

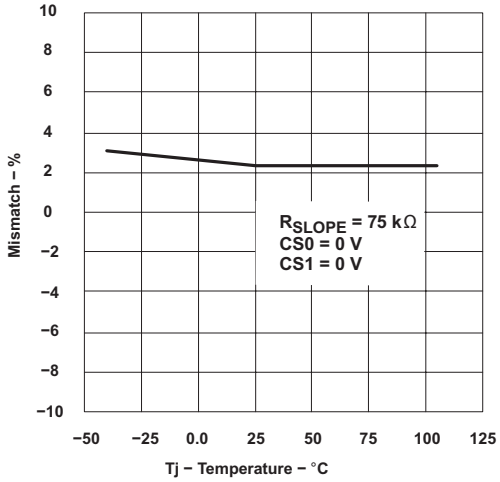
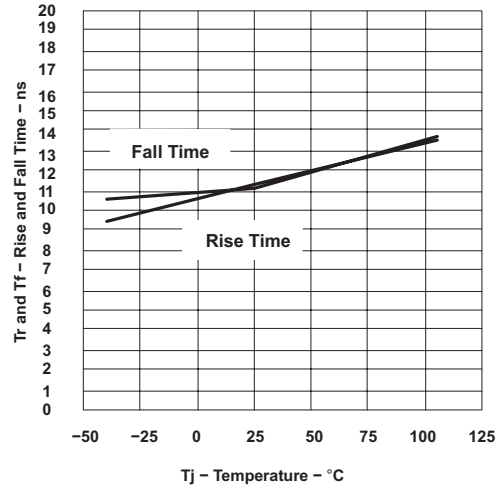


Figure 8. Channel1 and Channel2 Slope Matching vs Temperature



C_L = 50 pF

Figure 9. Rise and Fall Time vs Temperature

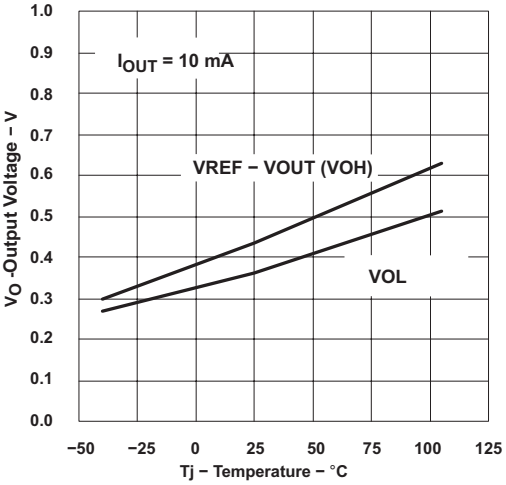


Figure 10. VOH and VOL vs Temperature

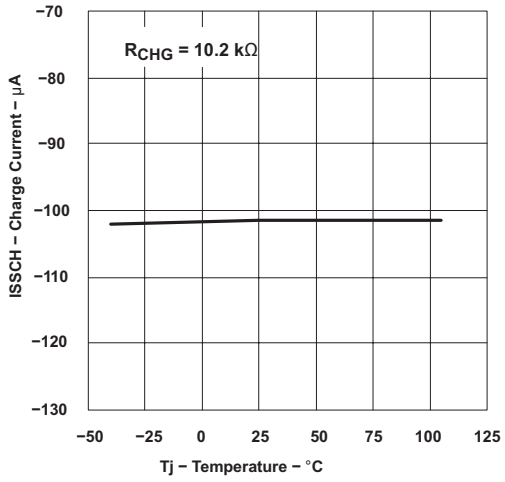


Figure 11. Soft-Start Charge Current vs Temperature

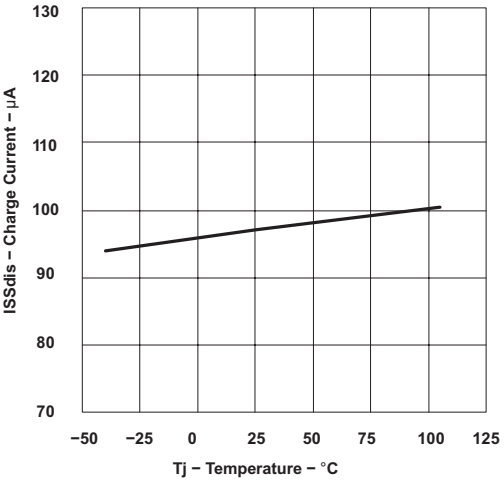


Figure 12. Soft-Start Discharge Current vs Temperature

Typical Characteristics (continued)

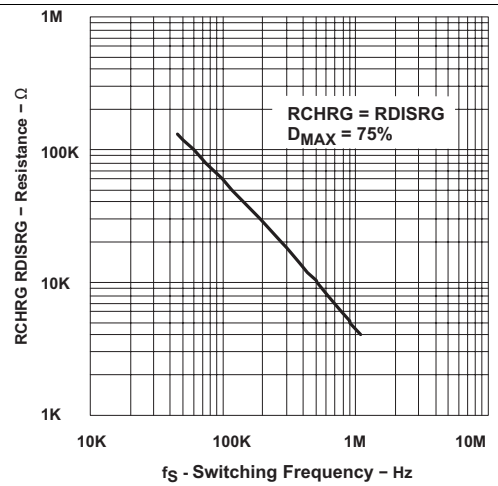


Figure 13. Programming Resistors vs Switching Frequency

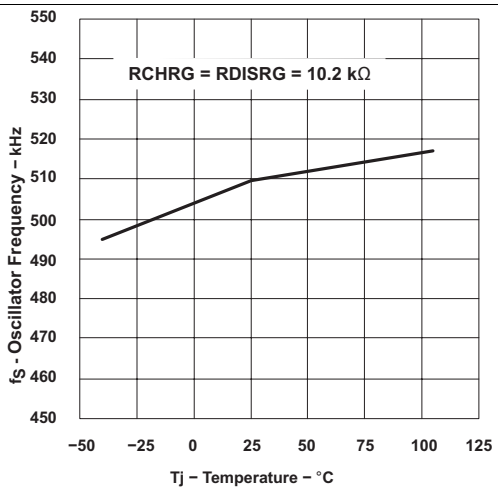


Figure 14. Oscillator Frequency vs Temperature

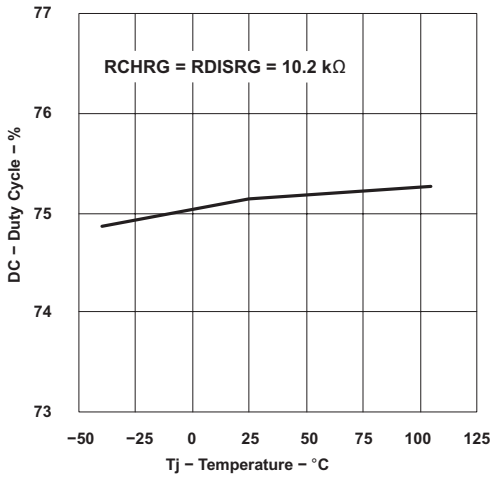


Figure 15. Programmable Max Duty Cycle vs Temperature

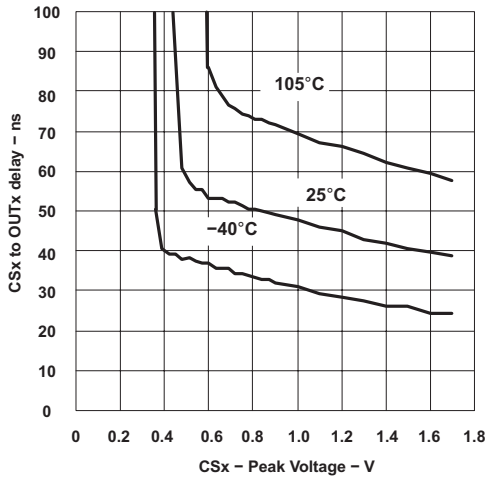


Figure 16. CSx to OUTx Delay vs CSx Peak Voltage

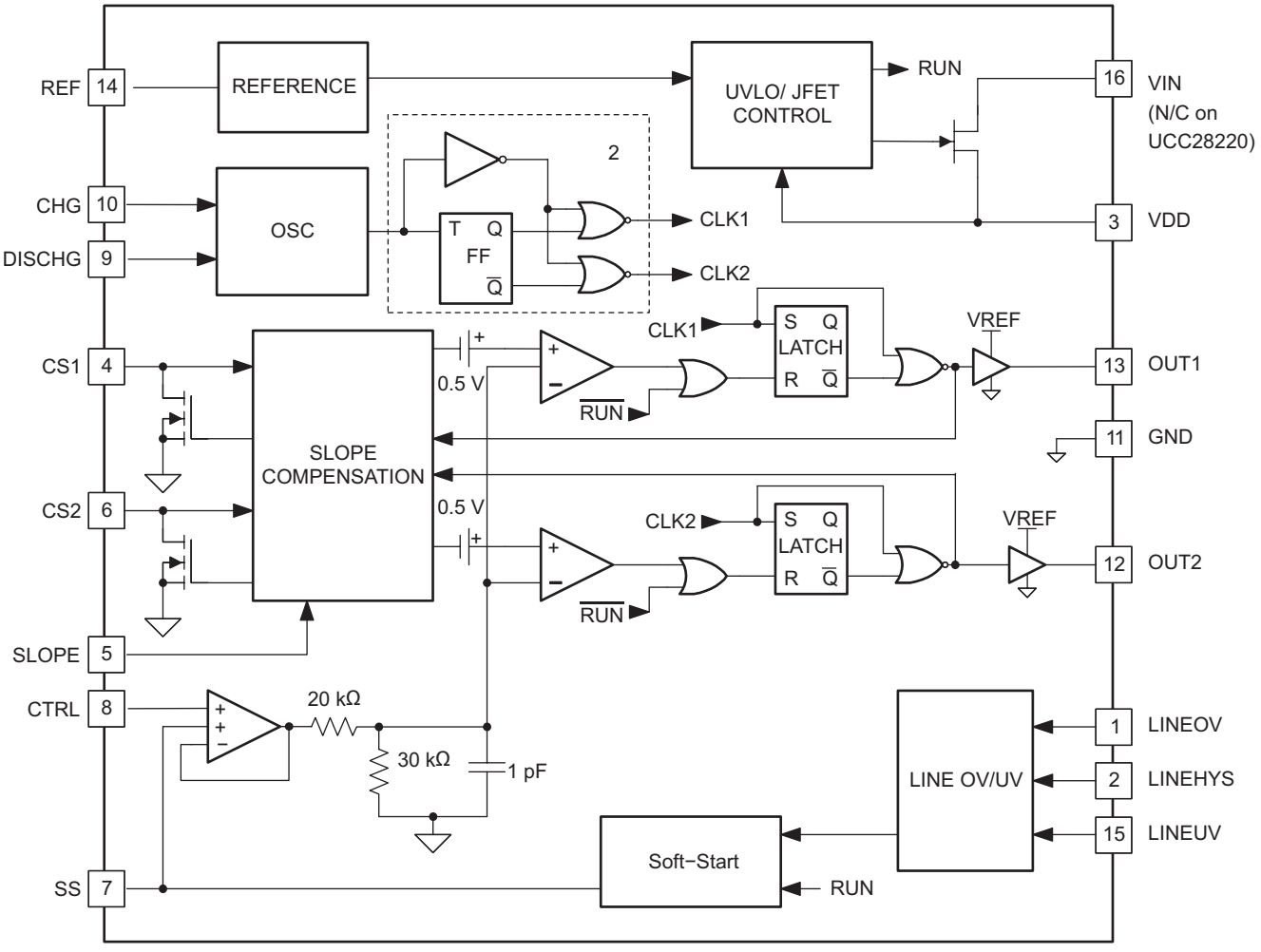
8 Detailed Description

8.1 Overview

The UCC2822x device is comprised of several housekeeping blocks as well as two slope compensated PWM channels that are interleaved. The circuit is intended to run from an external VDD supply voltage between 8 V and 14 V; however, the UCC28221 has the addition of a high-voltage start-up JFET with control circuitry which can be used for system start-up. Other functions contained in the device are supply UVLO, 3.3-V reference, accurate line OV and UV functions, a high-speed programmable oscillator for both frequency and duty cycle, programmable slope compensation, and programmable soft-start functions.

The UCC2822x is a primary side controller for a two-channel interleaved power converter. The device is compatible with forward or flyback converters as long as a duty cycle clamp between 60% and 90% is required. The active clamp forward and flyback converters as well as the RCD and resonant reset forward converters are therefore compatible with this device. To ensure the two channels share the total converter output current, current mode control with internal slope compensation is used. Slope compensation is user programmable through a dedicated pin and can be set over a 50:1 range, ensuring good small-signal stability over a wide range of applications.

8.2 Functional Block Diagram



Pinout for 16 pin option shown. See the 20-pin connection to UCC28221-PW in *Pin Configuration and Functions*.

8.3 Feature Description

8.3.1 VDD

Because the driver output impedance is high, the energy storage requirement on the VDD capacitor is low. For improved noise immunity, TI recommends that the VDD pin is bypassed with a minimum of 0.1-µF capacitance to GND. In most typical applications, the bias voltage for the MOSFET drivers is also used as the VDD supply voltage for the chip. It is beneficial to add a low valued resistor between the bulk storage capacitor of the driver and the VDD capacitor for the UCC2822x. By adding a resistor in series with the bias supply with the bias supply, any noise that is present on the bias supply is filtered out before getting to the VDD pin of the controller.

8.3.2 Reference

For improved noise immunity, TI recommends that the reference pin, REF, is bypassed with a minimum of 0.1-µF capacitance to GND.

8.3.3 Oscillator Operation and Maximum Duty Cycle Setpoint

The oscillator uses an internal capacitor to generate the time base for both PWM channels. The oscillator is programmable over a 200-kHz to 2-MHz frequency range with 20% to 80% maximum duty cycle range. Both the dead time and the frequency of the oscillator are divided by 2 to generate the PWM clock and off-time information for each of the outputs. In this way, a 20% oscillator duty cycle corresponds to a 60% maximum duty cycle at each output, where an 80% oscillator duty cycle yields a 90% duty cycle clamp at each output.

The design equations for the oscillator and maximum duty cycle setpoint are given in Equation 1 through Equation 4.

$$F_{OSC} = 2 \times F_{OUT} \tag{1}$$

$$D_{MAX(osc)} = 1 - 2 \times (1 - D_{MAX(out)}) \tag{2}$$

$$R_{CHG} = K_{OSC} \times \frac{D_{MAX(osc)}}{F_{OSC}} \tag{3}$$

$$R_{DISCHG} = K_{OSC} \times \frac{(1 - D_{MAX(osc)})}{F_{OSC}}$$

where

- K_{OSC} = 2.04 × 10^{10} (Ω/s)
- F_{OUT} = Switching frequency at the outputs of the chip (Hz)
- $D_{MAX(out)}$ = Maximum duty cycle limit at the outputs of the chip
- $D_{MAX(osc)}$ = Maximum duty cycle of the oscillator for the desired maximum duty cycle at the outputs
- F_{OSC} = Oscillator frequency for desired output frequency (Hz)
- R_{CHG} = External oscillator resistor which sets the charge current (Ω)
- R_{DISCHG} = External oscillator resistor which sets the discarge current (Ω) (4)

8.3.4 Soft Start

A current is forced out of the SS pin, equal to 3/7 of the current set by R_{CHG}, to provide a controlled ramp voltage. The current set by the R_{CHG} resistor is equal to 2.5 V divided by R_{CHG}. This ramp voltage overrides the commanded duty cycle on the CTRL pin, allowing a controlled start-up. Assuming the UCC288221 is biased on the primary side, the soft start must be quite quick to allow the secondary bias to be generated and the secondary side control can then take over. Once the soft-start time interval is complete, a closed-loop soft-start on the secondary side can be executed, such as Equation 5.

$$ISS = \frac{3}{7} \times \frac{2.5}{R_{CHG}}$$

where

- ISS = current which is sourced out of the SS pin during the soft-start time (A) (5)

Feature Description (continued)

8.3.5 Current Sense

The current sense signals CS1 and CS2 are level shifted by 0.5 V and have the slope compensation ramps added to them before being compared to the control voltage at the input of the PMW comparators. The amplitude of the current sense signal at full load must be selected such that it is very close to the maximum control voltage to limit the peak output current during short-circuit operation.

8.3.6 Output Drivers

The UCC2822x is intended to interface with the UCC2732x family of MOSFET drivers. As such, the output drive capability is low, effectively 100 Ω, and the driver output swing between GND and REF.

8.4 Device Functional Modes

8.4.1 Line Overvoltage and Undervoltage

Three pins are provided to turn off the output drivers and reset the soft-start capacitor when the converter input voltage is outside a prescribed range. The undervoltage setpoint and undervoltage hysteresis are accurately set through external resistors. The overvoltage set point is also accurately set through a resistor ratio, but the hysteresis is fixed by the same resistor that set the undervoltage hysteresis.

Figure 17 and Figure 18 show the detailed functional diagram and operation of the undervoltage lockout (UVLO) and overvoltage lockout (OVLO) features. Equation 6 through Equation 9 are for setting the thresholds define in Figure 18.

$$V1 = 1.26 \times \frac{R1}{(R2 + R3)} + 1.26 \tag{6}$$

$$V2 = 1.26 \times \frac{(R1 + Rx)}{Rx}, \text{ where } Rx = R4 \parallel (R2 + R3) \tag{7}$$

$$V4 = 1.26 \times \frac{(R1 + R2 + R3)}{R3} \tag{8}$$

$$V3 = V4 - 1.26 \times \left(\frac{R1}{R4} \right) \tag{9}$$

Device Functional Modes (continued)

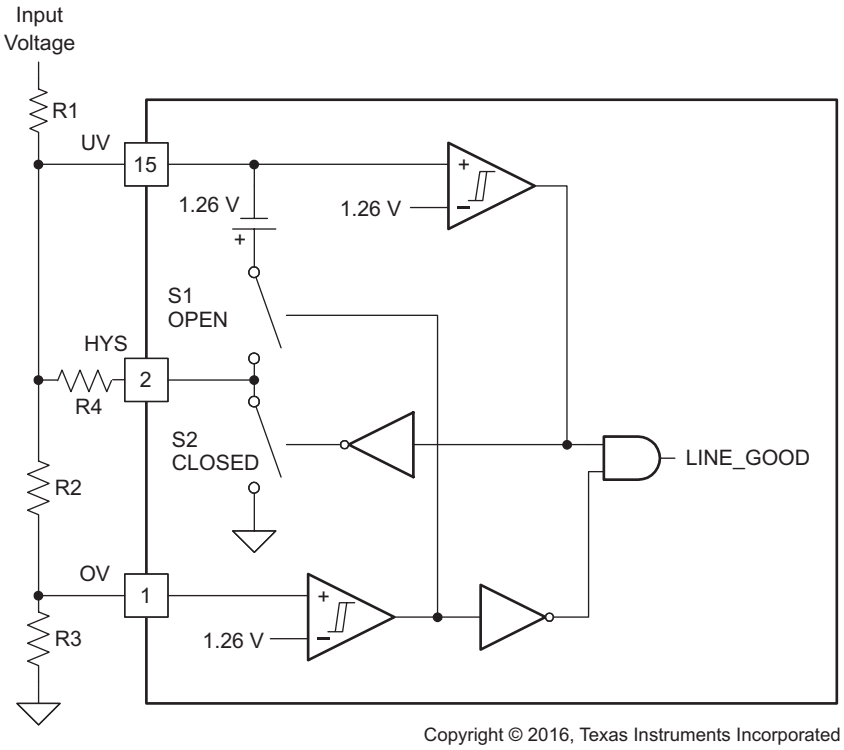


Figure 17. Line UVLO and OVLO Functional Diagram

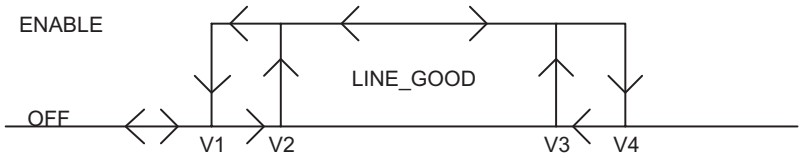


Figure 18. Line UVLO and OVLO Operation

The UVLO hysteresis and the OVLO hysteresis can be calculated as V2 – V1 and V4 – V3, respectively. By examining the design equations, it becomes apparent that the value of R4 sets the amount of hysteresis at both thresholds. By realizing this fact, the designer can then set the value of R4 based on the most critical hysteresis specification either at high line or at low line. In most designs the value of R4 is determined by the desired amount of hysteresis around the UVLO threshold. As an example, consider a telecom power supply with the following input UVLO and OVLO design specifications:

- V1 = 32 V
- V2 = 34 V
- V3 = 83 V
- V4 = 84.7 V

Then,

- R1 = 976 kΩ
- R2 = 24.9 kΩ
- R3 = 15 kΩ
- R4 = 604 kΩ

Device Functional Modes (continued)

8.4.2 Start-Up JFET Section

A 110-V start-up JFET is included to start the device from a wide range (36 V to 75 V) telecom input source. When VDD is lower than 13 V, the JFET is on, behaving as a current source charging the bias capacitors on VDD and supplying current to the device. In this way, the VDD bypass capacitors are charged to 13 V where the outputs start switching and the JFET is turned off. To enable a constant bias supply to the device during a pulse skipping condition, the JFET is turned back on whenever VDD decreases below 10 V and the outputs are not switching. Thus, the current from the JFET can overcome the internal bias currents, as long as the device is not actively switching the output drivers. See Figure 19 for a representation of the JFET and VDD operation. The OCC28220 does not contain an internal JFET and has a start-up threshold of 10 V which makes it capable of directly operating off a 12-V dc bus.

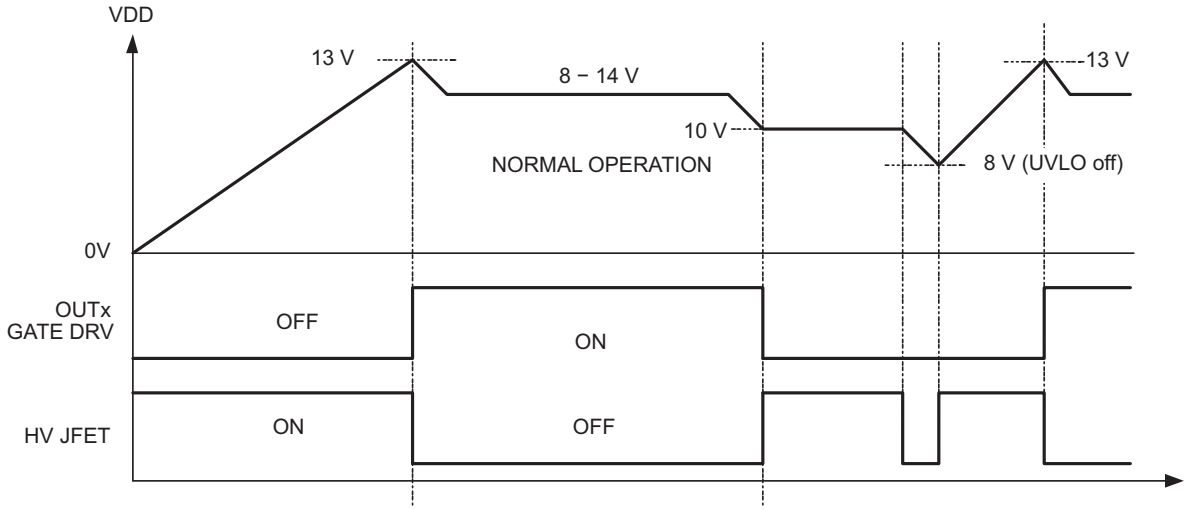


Figure 19. JFET Device Operation With VDD Voltage

8.4.3 Slope Compensation

The slope compensation circuit in the UCC2822x operates on a cycle-by-cycle basis. The two channels have separate slope compensation circuits. These are fabricated in precisely the same way so as current sharing is unaffected by the slope compensation circuit. For each channel, an internal capacitor is reset whenever that channel's output is off. At the beginning of the PMW cycle, a current is mirrored off the SLOPE pin into the capacitor, developing an independent ramp. Because the two channel's ramps start when the channel's output changes from a low to high state, the ramps are thus interleaved. These internal ramps are added to the voltages on the current sense pins, CS1 and CS2, and form an input to the PMW comparators.

Device Functional Modes (continued)

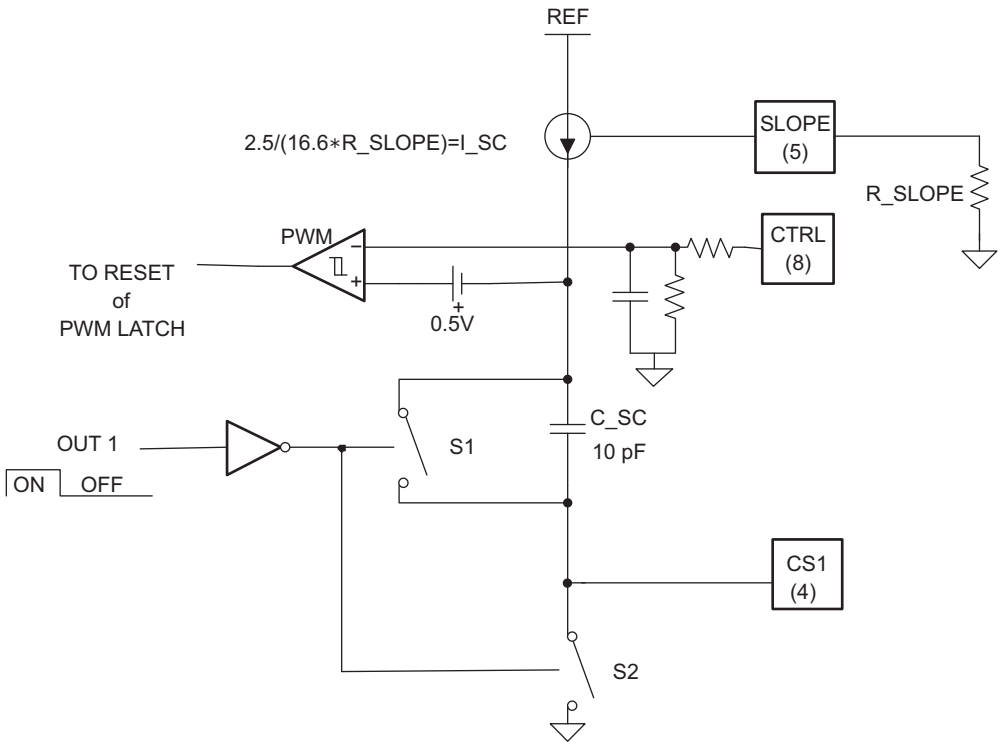


Figure 20. Slope Compensation Detail for Chanel 1. Duplicate Matched Circuitry Exists for Channel 2.

To ensure stability, the slope compensation circuit must add between 1/5 and 1 times the inductor downslope to each of the current sense signals before being applied to the input of the PWM comparator.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UCC28220 control device from Texas Instruments is used in a dual-interleaved, forward converter that enables the power supply designer to reduce output current ripple and reduce magnetic size per power stage allowing for improved transient response. The UCC28220 is a dual-interleaved PWM controller with programmable maximum duty cycle per channel up to 90% for interleaved forward and interleaved flyback designs.

9.2 Typical Application

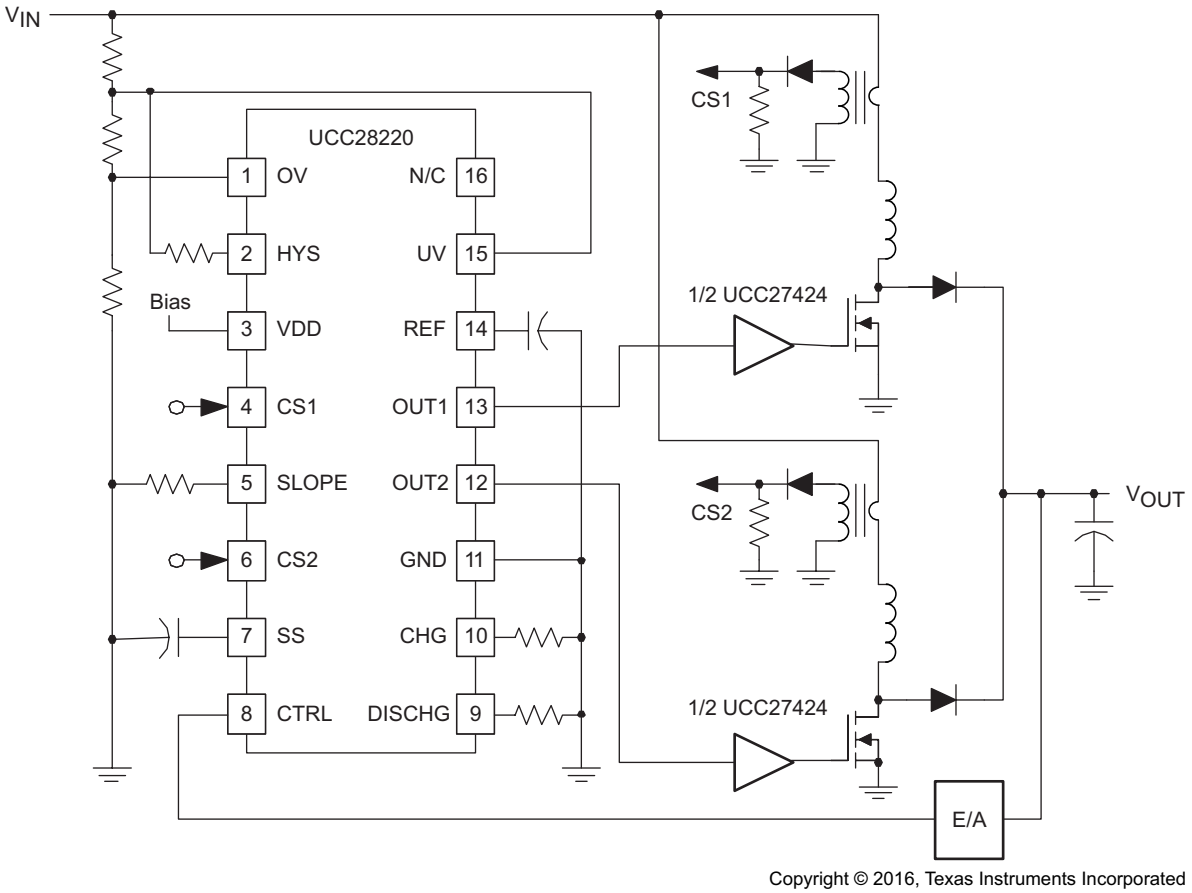


Figure 21. Interleaved Boost Application Circuit Using the UCC28220

Typical Application (continued)

9.2.1 Design Requirements

Table 1 lists the design parameters for the interleaved boost application circuit.

Table 1. Design Parameters

PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	85	110 or 230	265	V RMS
V_{OUT}	374	390	425	V
V_{RIPPLE}	—	—	30	V
Current THD at 350 W	—	—	10%	
PF at 350 W	0.95	—	—	
Full load efficiency	90%	—	—	
f_S	—	100	—	kHz
Holdup requirements, t_{HOLD}	—	—	20	ms
f_{LINE}	47	50	60	Hz

9.2.2 Detailed Design Procedure

9.2.2.1 Overvoltage Protection and Undervoltage Lockout

The OVP function and undervoltage lockout (UVLO) were handled by the UCC28220. It is a simple comparator that monitors the boost voltage. The OVP for this design was set to 425 V and UVLO was set to 108 V. The preregulator does not start switching until V_{OUT} reaches 108 V.

9.2.2.2 Peak Current Limit

Peak current limit is set by the maximum control voltage (V_C) at the input of the UCC28220's PWM comparator with Equation 10 through Equation 12. Where *a* is the current sense transformer turns ratio of T1 and T2. The peak current limit trip point was set for 130% of the nominal peak current to protect the boost FETs.

$$a = \frac{N_P}{N_S} = \frac{V_P}{V_S} = \frac{I_S}{I_P} = \frac{1}{50} \tag{10}$$

$$I_{PEAK} = \left(\frac{P_{OUT} \times \sqrt{2}}{2 \times v_{in(min)} \times \eta} + \frac{\Delta IL1}{2} \right) \times 1.3 \tag{11}$$

V_C = 1.8, V_{CTRL} was set to a maximum of 3 V to protect the UCC28220 CTRL pin.

$$R_{SENSE} = \frac{\frac{V_C - 0.5\ V}{2}}{I_{PEAK} \times a} \tag{12}$$

Equation 12 considers slope compensation that is added later.

The peak current of the FET during power up is 2 times I_{PEAK} under normal operation as calculated with Equation 13. This is due to the excessive slope compensation that is required for stability.

$$I_{PEAK(startup)} = 2 \times I_{PEAK} \tag{13}$$

9.2.2.3 Current Sense Transformer Reset Resistor (T1 and T2)

$$R_{RESET} = \frac{\frac{V_C - 0.5\ V}{2}}{I_{PEAK} \times \left(1 - D_{MIN(LL)}\right) \times a} \tag{14}$$

9.2.2.4 Oscillator and Maximum Duty Cycle Clamp

The UCC28220's oscillator and maximum duty cycle clamp are setup through resistor R_{CHG} and discharge. The desired duty cycle clamp (D_{MAX}) was set at 0.9 to stop the current sense transformers from saturating.

$$K_{OSC} = \left(2.04 \times 10^{10}\right)\frac{\Omega}{S} \quad (15)$$

Equation 15 is UCC28220's oscillator constant.

$$F_{OSC} = 2 \times f_S \quad (16)$$

Equation 16 is UCC28220's internal oscillator frequency.

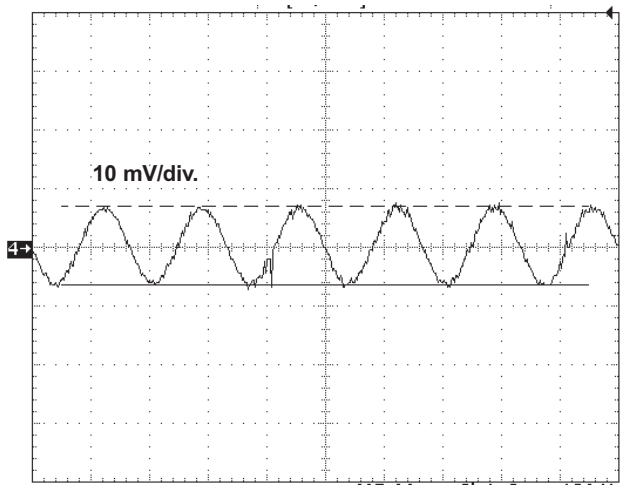
$$F_{OSC} = 2 \times f_S \quad (17)$$

Equation 17 is the internal duty cycle clamp.

$$D_{MAX(OSC)} = 1 - 2\left(1 - D_{MAX}\right) \quad (18)$$

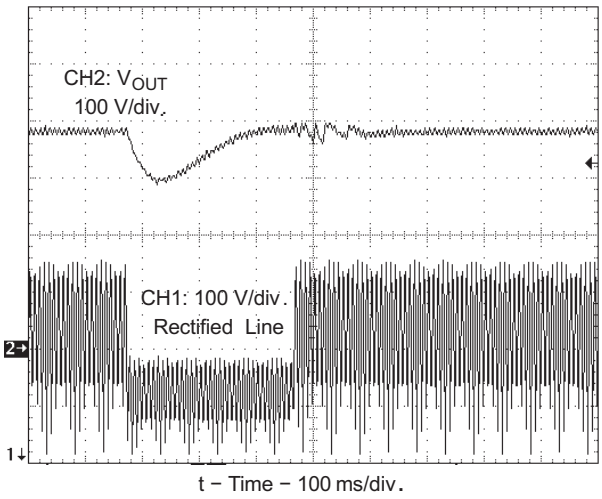
$$R_{DISCHG} = K_{OSC}\frac{\left(1 - D_{MAX(OSC)}\right)}{F_{OSC}} \quad (19)$$

9.2.3 Application Curves



P_{OUT} = 350 W

Figure 22. Output Ripple Voltage



Line transients at 350-W load
V_{IN} stepped from 240 V to 120 V to 240 V

Figure 23. Line Dropout at Full Load

10 Power Supply Recommendations

The VDD power terminal for the device requires the placement of electrolytic capacitor as energy storage capacitor. And requires the placement of low-ESR noise decoupling capacitance as directly as possible from the VDD terminal to the VSS terminal, ceramic capacitors with stable dielectric characteristics over temperature are recommended, such as X7R or better. TI recommends a 1-µF, 50-V e-capacitor.

11 Layout

11.1 Layout Guidelines

1. TI recommends placing a 1-µF ceramic decoupling capacitor as close as possible between the VDD terminal and GND, tracked directly to both terminals.
2. TI recommends placing a small, external filter capacitor on the CS1 and CS2 terminal. Track the filter capacitor as directly as possible from the CS to GND terminal.
3. Reduce the total surface area of traces on the CS net to a minimum.
4. Connect decoupling and noise filter capacitors, as well as sensing resistors directly to the GND terminal in a star-point fashion, ensuring that the current-carrying power tracks (such as the gate drive return) are track separately to avoid noise and ground-drops that could affect the analogue signal integrity.

11.2 Layout Example

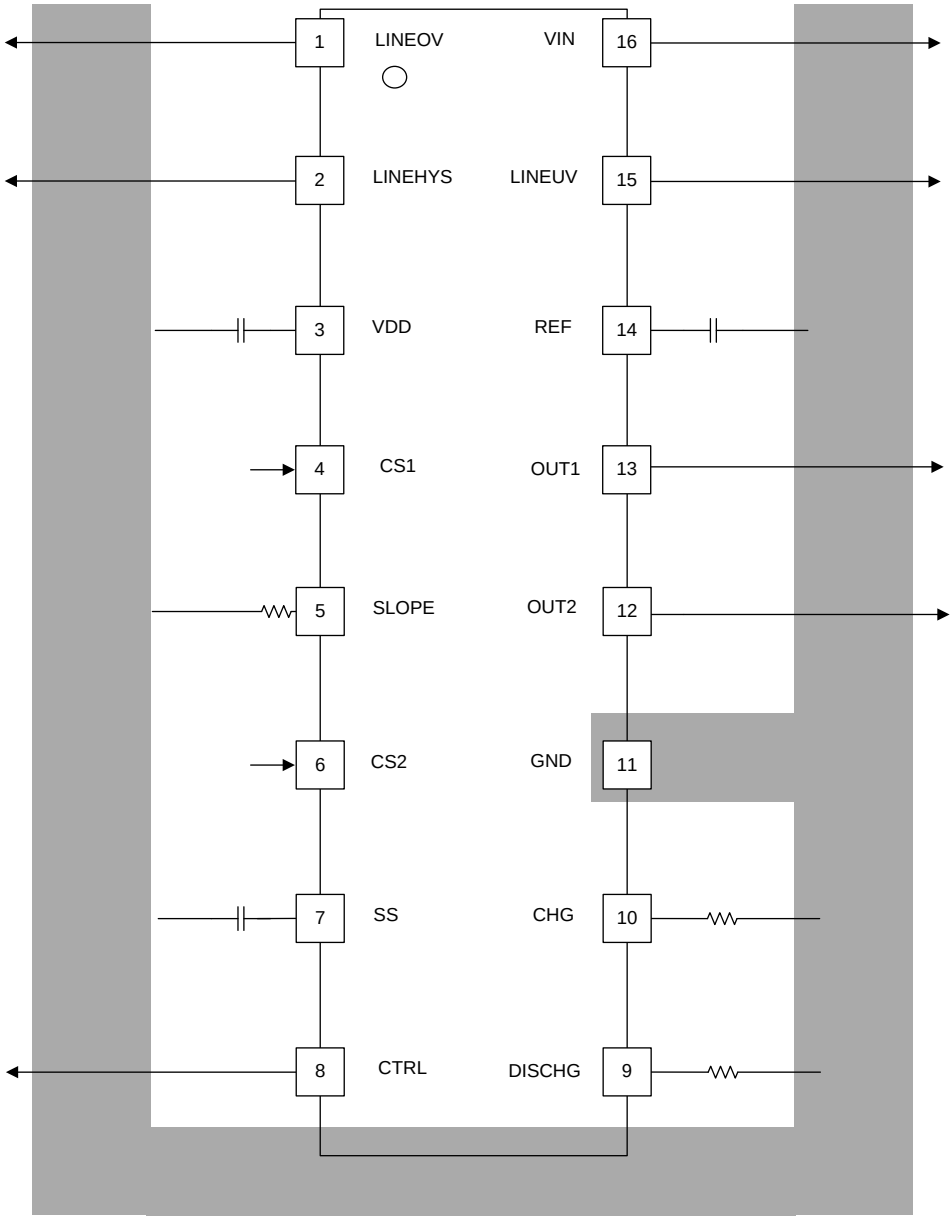


Figure 24. UCC28221 Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

An evaluation module and an associated user's guide are available. The UCC28221 is used in a two-channel interleaved Forward design converting from 36-V to 76-V dc input voltage to a regulated 12-V dc output. The power module has two isolated 100 W forward power stages operating at 500 kHz, which are operating 180 degrees out of phase with each other allowing for output current ripple cancellation and smaller magnetic design. This design also takes advantage of the UCC28221's on-board 110-V internal JFET start up circuit that removes the need of an external trickle charge resistor for boot strapping. This circuit turns off after auxiliary power is supplied to the device conserving power.

UCC28221 200-W Evaluation Module (EVM) (SLUU173)

For other related documentation see the following:

- *Unitrode - UC3854A/B and UC3855A-B Provide Power Limiting With Sinusoidal Input Current for PFC Front Ends* (SLUA196)
- *Advanced PFC/PWM Combination Controller With Trailing-Edge/Trailing-Edge Modulation* (SLUS608)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC28220	Click here	Click here	Click here	Click here	Click here
UCC28221	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28220D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28220	Samples
UCC28220DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28220	Samples
UCC28220DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28220	Samples
UCC28220PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28220	Samples
UCC28220PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28220	Samples
UCC28220PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28220	Samples
UCC28221D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28221	Samples
UCC28221DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28221	Samples
UCC28221PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28221	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC28220 :

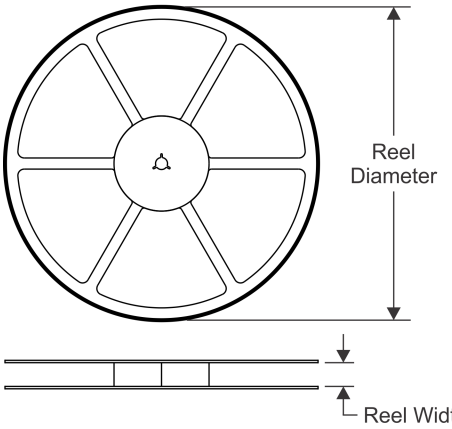
- Automotive: UCC28220-Q1

NOTE: Qualified Version Definitions:

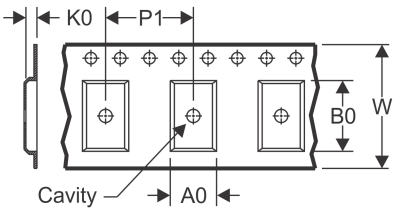
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

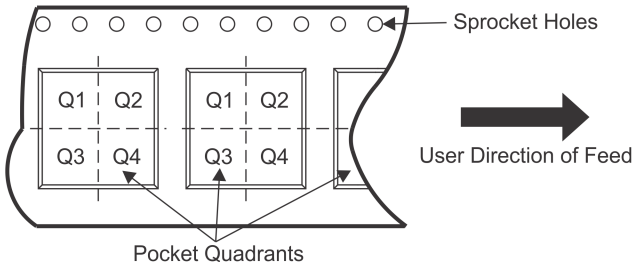


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

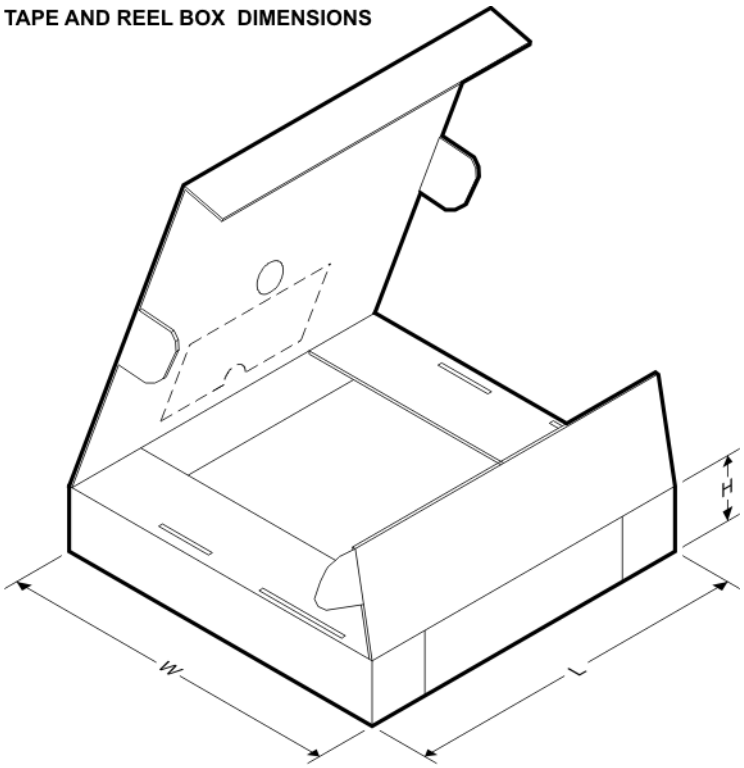
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28220DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC28220PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

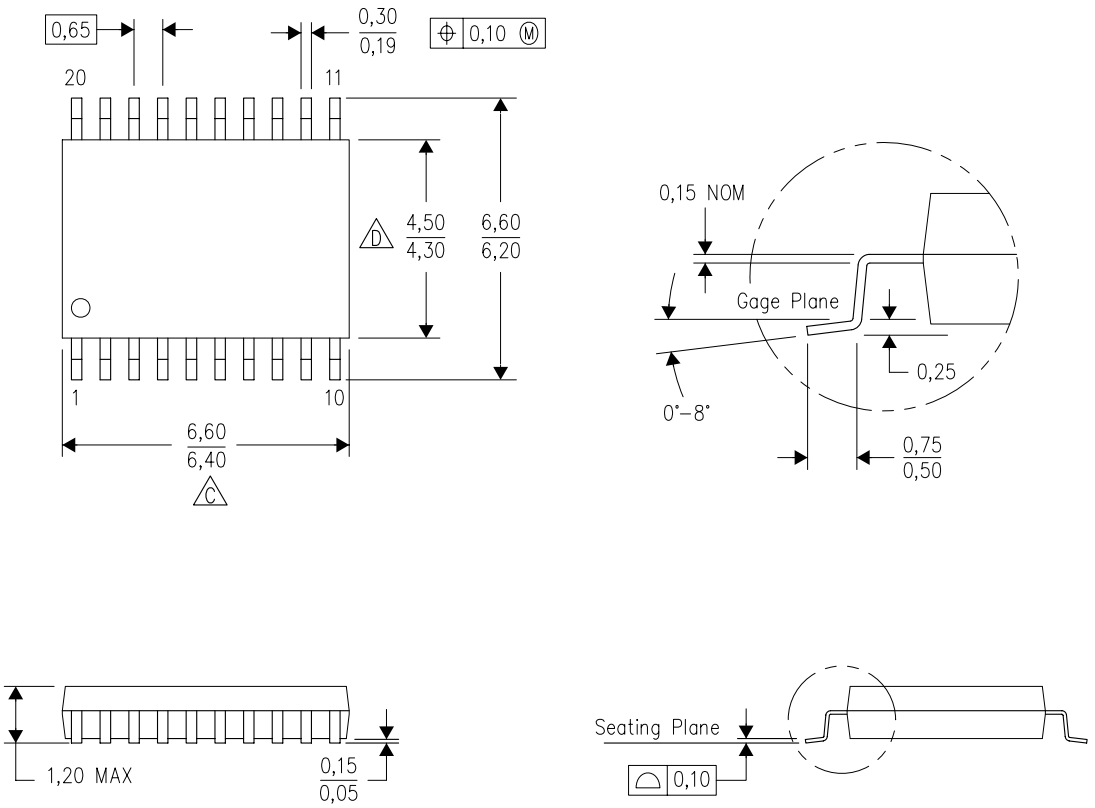
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28220DR	SOIC	D	16	2500	367.0	367.0	38.0
UCC28220PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

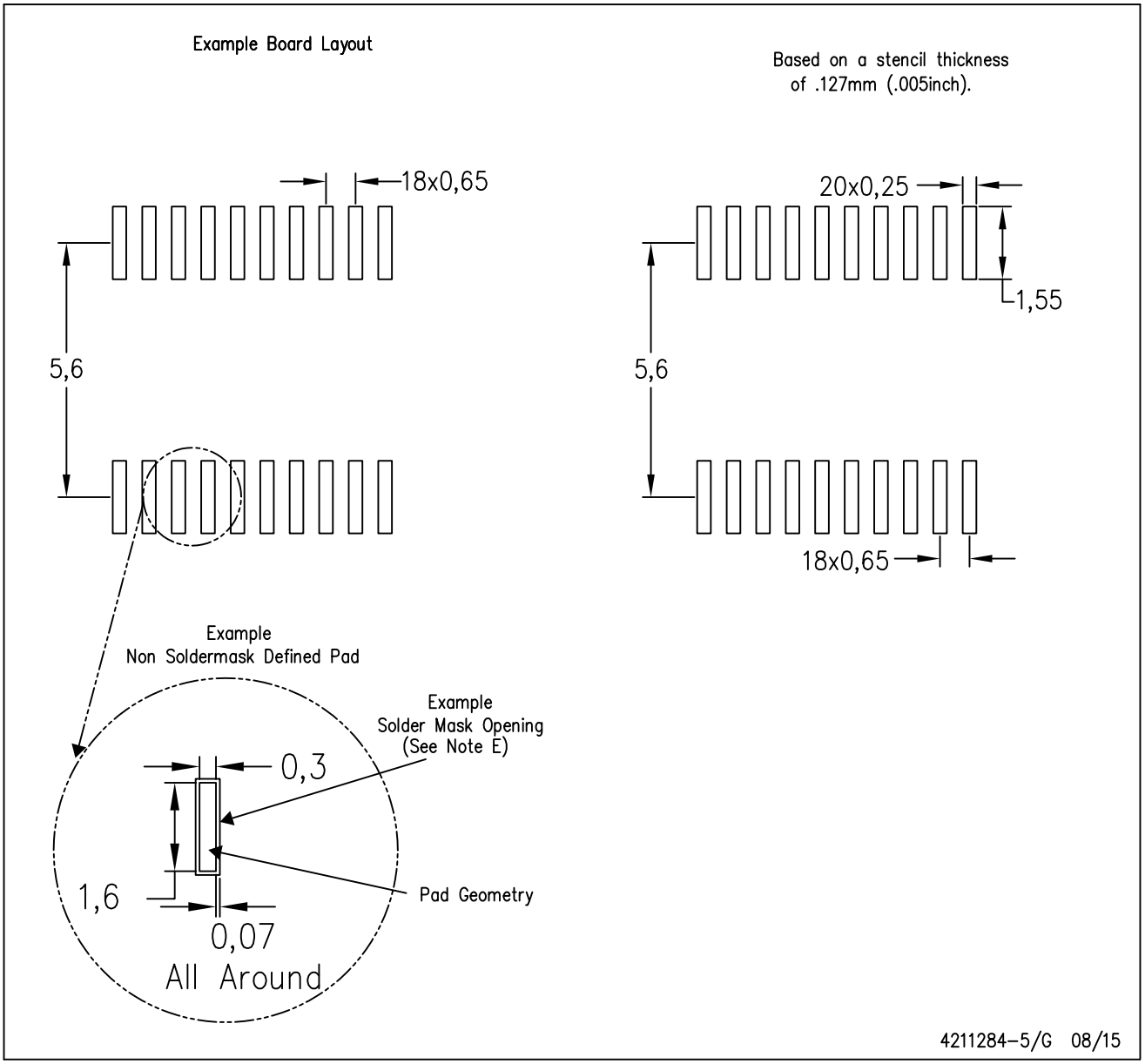
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

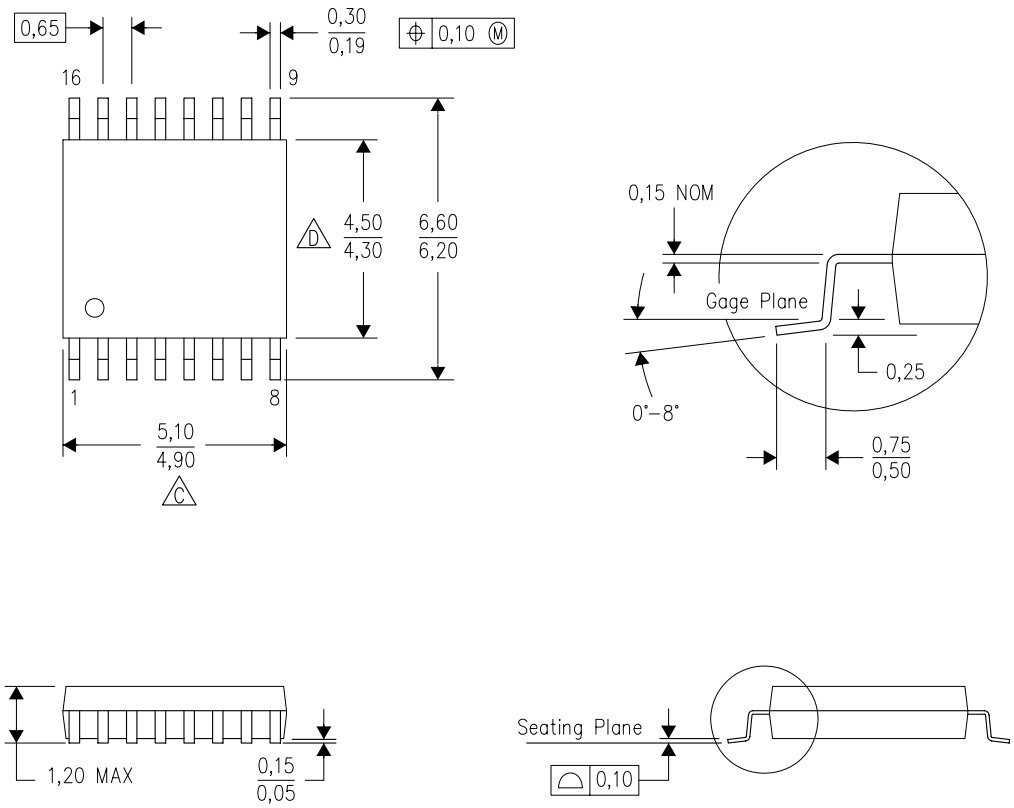
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

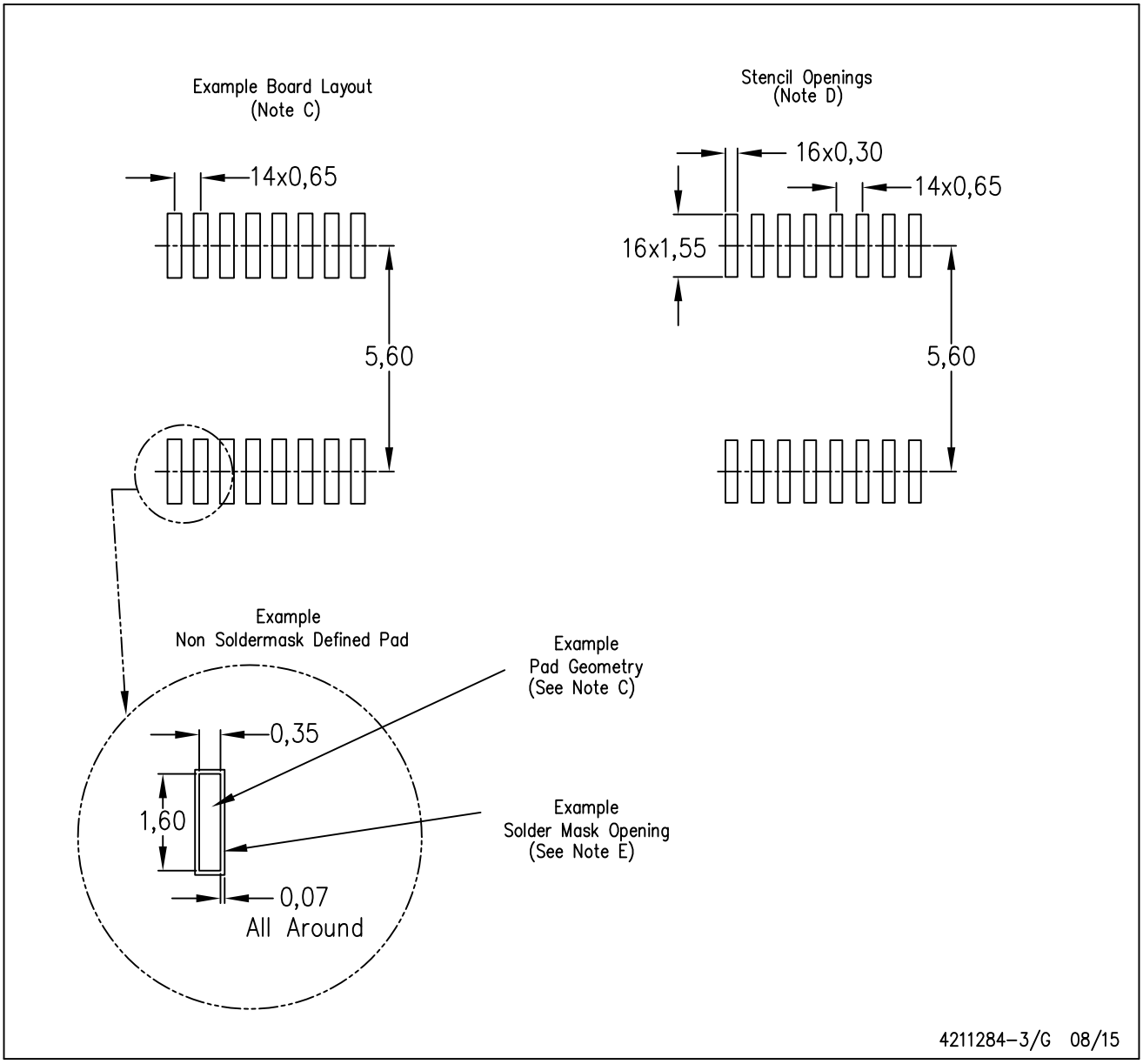
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

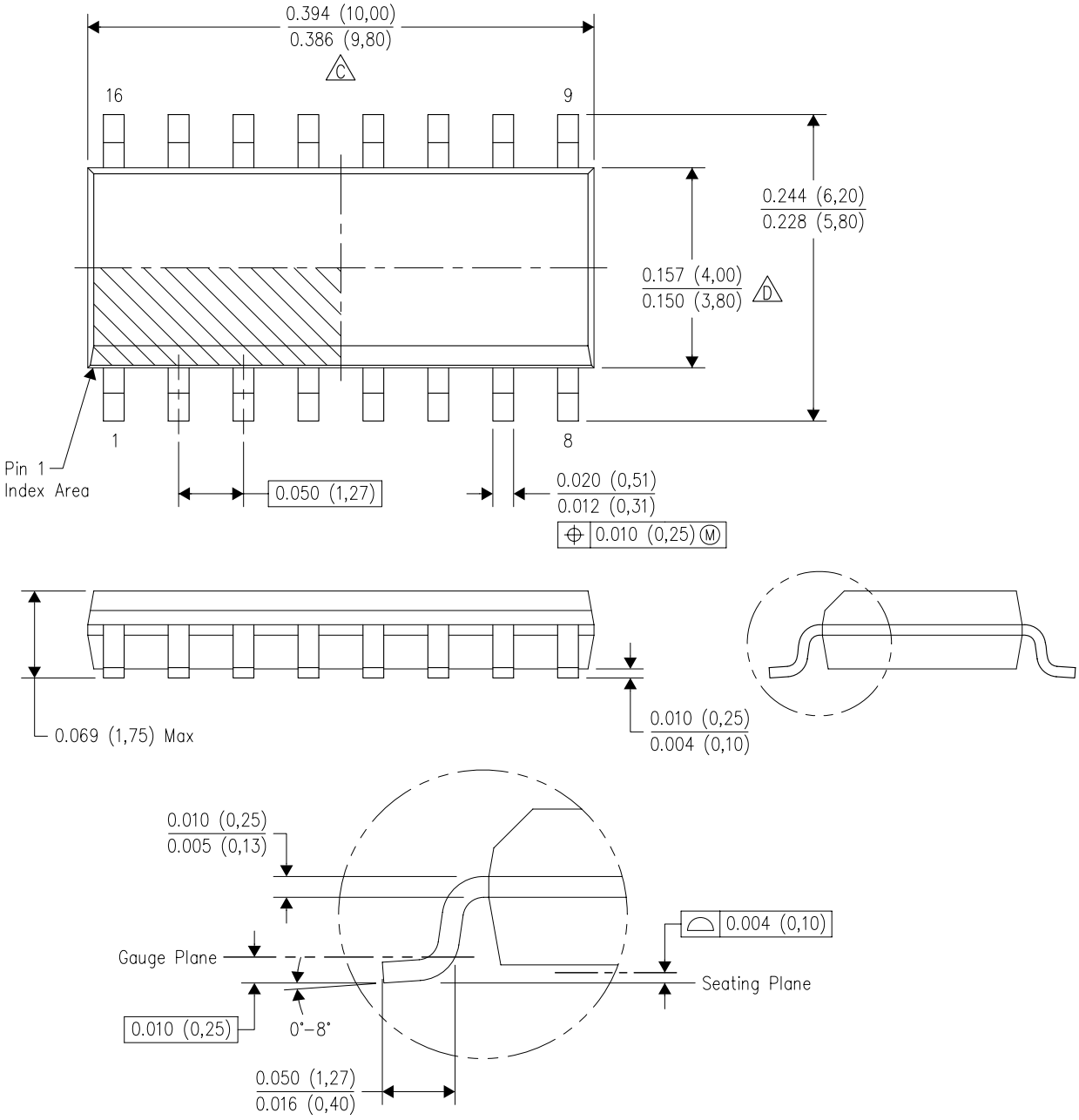
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



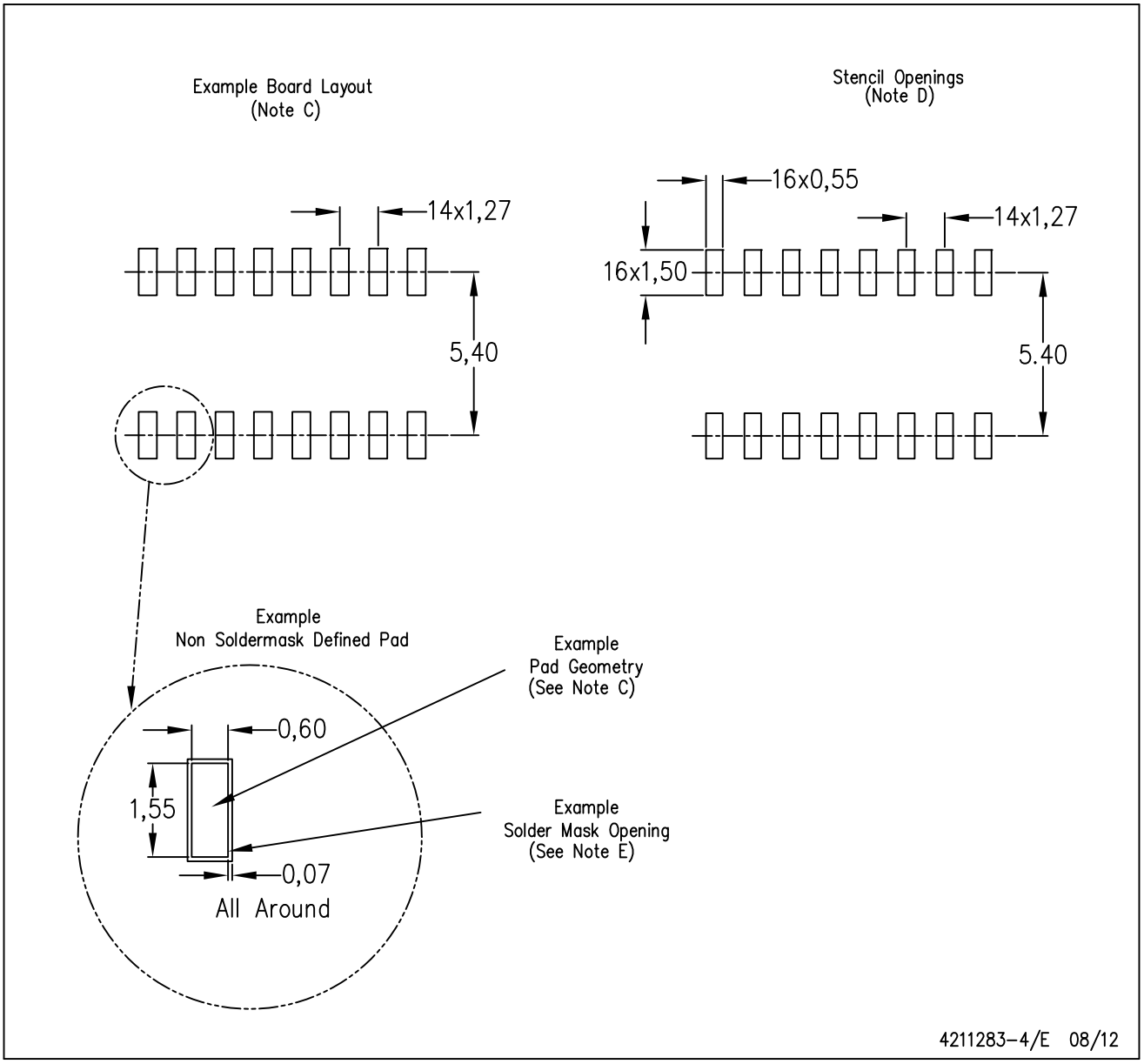
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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