DK_START_GW1N-LV9LQ144C6I5_V2.1

User Guide

DBUG399-1.0E, 08/17/2021

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Revision History

Date	Version	Description
08/17/2021	1.0E	Initial version published.

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1 About This Guide

1.1 Purpose

The DK_START_GW1N-LV9LQ144C6I5_V2.1 user manual consists of the following four parts:

1. A brief introduction to the features and hardware resources of the development board;
2. An introduction to the function, circuit, and pinout of each module;
3. Considerations for the use of development board;
4. An introduction to the usage of the FPGA development software.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. DS100, GW1N series of FPGA Products Data Sheet
2. UG103, GW1N series of FPGA Products Package and Pinout Manual
3. UG801, GW1N-9 Pinout
4. UG290, Gowin FPGA Products Programming and Configuration Guide
5. SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
SIP	System in Package
SDRAM	Synchronous Dynamic RAM
PSRAM	Pseudo static random access memory
CFU	Configurable Function Unit
CLS	Configurable Logic Slice
CRU	Configurable Routing Unit
LUT4	4-input Look-up Tables
LUT5	5-input Look-up Tables
LUT6	6-input Look-up Tables
LUT7	7-input Look-up Tables
LUT8	8-input Look-up Tables
REG	Register
ALU	Arithmetic Logic Unit
IOB	Input/Output Block
SSRAM	Shadow Static Random Access Memory
BSRAM	Block Static Random Access Memory
SP	Single Port
SDP	Semi Dual Port
DP	Dual Port
DSP	Digital Signal Processing
DQCE	Dynamic Quadrant Clock Enable
DCS	Dynamic Clock Selector
PLL	Phase-locked Loop
DLL	Delay-locked Loop
EQ144	EQFP144 package

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Introduction

2.1 Overview

Figure 2-1 DK_START_GW1N-LV9LQ144C6I5_V2.1 Development Board

The development board uses Gowin GW1N-9 FPGA devices. The GW1N series of FPGA products are the first generation of the Gowin LittleBee® family and it is an SIP chip. It has the characteristics of low power consumption, instant-start, low cost, non-volatility, high security, rich packages, convenient and flexible usage, etc., which can effectively reduce the learning cost and help users quickly enter the design and development field of programmable logic devices.

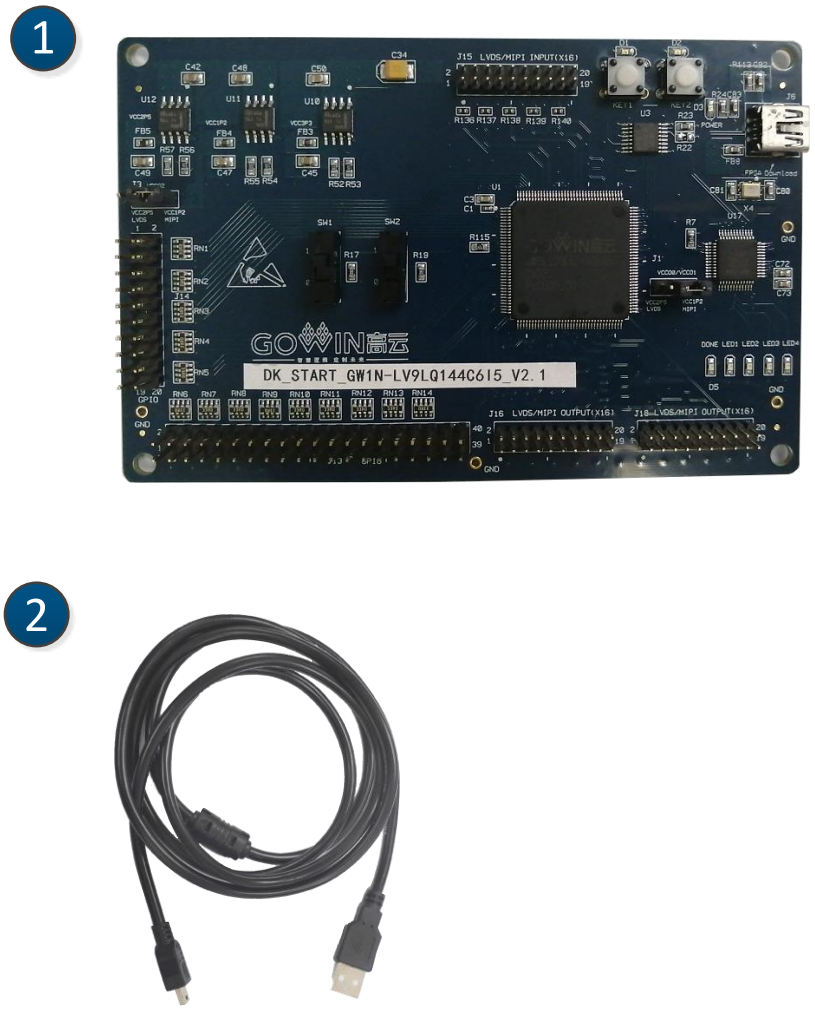
The development board offers abundant external interfaces, including MIPI/LVDS interfaces, GPIO interfaces, etc. There are also sliding switch, button switch, LED, clock, reset and other resources for developers or fans to learn to use.

2.2 Development Kit

A development board suite includes the following items:

- DK_START_GW1N-LV9LQ144C6I5_V2.1 development board
- USB Cable

Figure 2-2 A Development Kit

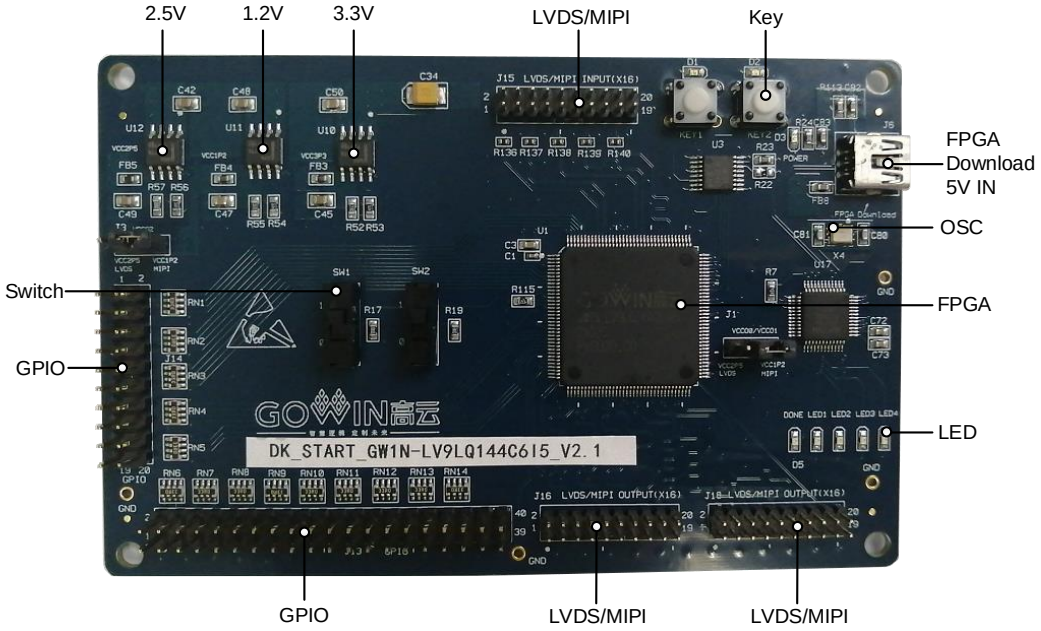


① DK_START_GW1N-LV9LQ144C6I5_V2.1 development board

② USB Cable

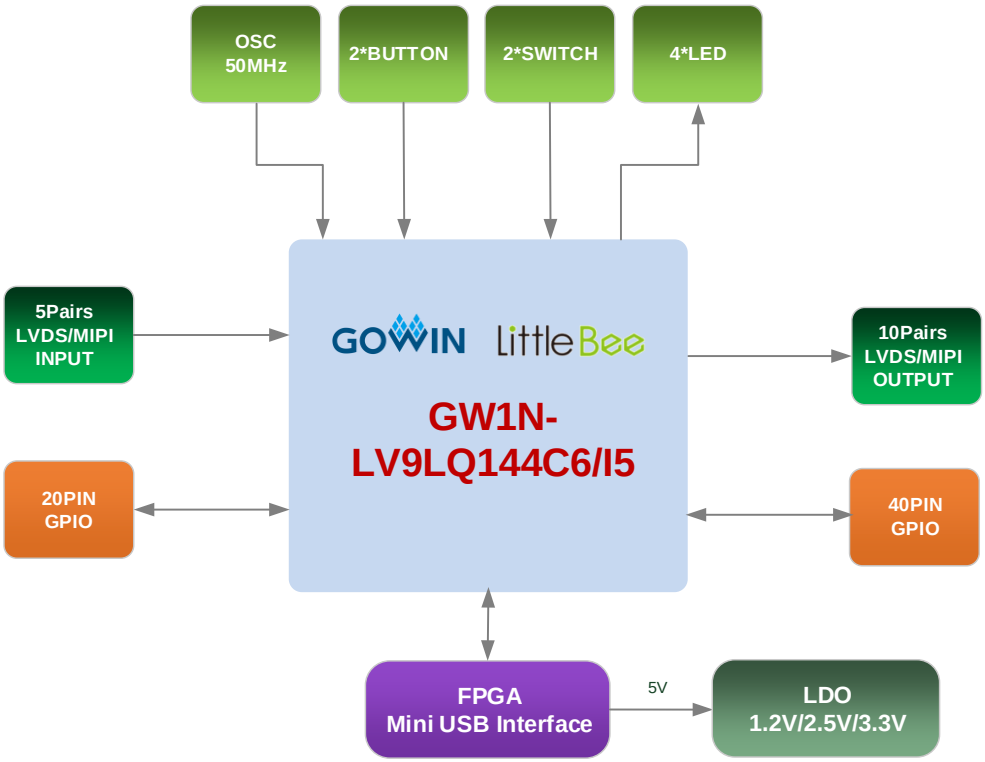
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Block Diagram

Figure 2-4 System Block Diagram



2.5 Features

The structure and features of the development board are as follows:

1. FPGA
   - LQFP144 package
   - Up to 120 user I/O
   - Embedded flash, data not easily lost if power down
   - Abundant LUT4 resources
   - Multiple modes and capacities of B-SRAM
2. FPGA Configuration Modes
   - JTAG
   - AUTO BOOT
3. Clock resource

   50MHz Clock Crystal Oscillator
4. Key switch and slide switch
   - Two key switches
   - Two slide switches
5. LED
   - One power indicator (green)
   - One DONE indicator (green)
   - Four LEDs (green)
6. Memory

   1Mbit embedded Flash
7. MIPI/LVDS

   5 pairs of MIPI/LVDS differential input; 10 pairs of MIPI/LVDS differential output
8. GPIO

   55 I/O expansion resources
9. LDO Power

   Supports 3.3 V, 2.5 V, and1.2V.

2.6 Development Board Description

Table 2-1 Development Board Description

No.	Name	Functional Description	Technical Condition	Note
1	FPGA	Core chip	–	–
2	Download	Support an USB interface; Support JTAG, AUTOBOOT	USB to JTAG chip integrated on board	–
3	Power Supply	3.3 V, 2.5V, and 1.2V output via LDO circuit	• Input power: 5V • Provide power for FPGA, download circuit and other circuits via 5V to 3.3V circuit; • Provide power for FPGA via 5V to 2.5V circuit; • Provide power for FPGA via 5V–1.2V circuit.	–
4	Switches	Available for testing	2	–
5	Key Switches	Available for testing	2	–
6	LED	Test indicator, DONE indicator, Power indicator	• Four Test indicators, green • One DONE indicator, green • One Power indicator, green	–
7	Crystal Oscillator	Provide 50MHz clock for FPGA	Package5032	–
8	Memory	Provides abundant Flash for design	1Mbit embedded Flash	–
9	GPIO	I/O for user to extend and test	55	–
10	MIPI/LVDS	MIPI/LVDS, used for testing	Five pairs of input, Ten pairs of output	–
11	Protection	USB interface: ESD protection	USB interface with ESD protection: ±15kV non-contact discharge and ± 8kV contact discharge;	–
12	Voltage	–	Input Voltage: 5V	–

No.	Name	Functional Description	Technical Condition	Note
13	Humidity	–	95%	–
14	Temperature	–	Operating range: –20°~70°	–

3 Development Board Circuit

3.1 FPGA Module

Overview

For the resources of GW1N series of FPGA Products, see DS100, *GW1N Series of FPGA Products Data Sheet*.

I/O BANK Introduction

For the I/O BANK, package, and pinout information, see UG103, *GW1N Series of FPGA Products Package and Pinout User Guide*.

3.2 Download

3.2.1 Overview

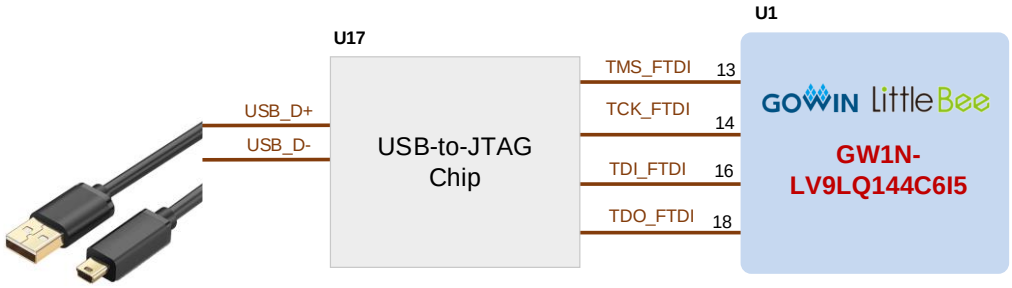
The development board provides an USB download interface. The bitstream file can be downloaded to the internal SRAM, or internal flash as needed.

Note!

- When downloaded to SRAM, the bitstream file will be lost if the device is powered down, and it will need to be downloaded again after power-on.
- If downloaded to flash, the bitstream file will not be lost if the device is powered down.

3.2.2 USB Download Circuit

Figure 3-1 FPGA USB Download Diagram



3.2.3 Download Flow

Please plug USB download cable into the USB interface (J6) of the development board to download FPGA, and then open Programmer, click SRAM mode or Embedded flash mode to download bit stream file to SRAM or flash.

3.2.4 Pinout

Table 3-1 FPGA Download Pinout

Name	Pin No.	BANK	Description	I/O Level
TMS_FTDI	13	3	JTAG Signal	3.3V
TCK_ FTDI	14	3	JTAG Signal	3.3V
TDI_ FTDI	16	3	JTAG Signal	3.3V
TDO_ FTDI	18	3	JTAG Signal	3.3V
MODE0	144	3	Mode selection pin	3.3V
MODE1	143	3	Mode selection pin	3.3V
RECONFIG_N	20	3	RECONFIG_N	3.3V
DONE	21	3	DONE indicator	3.3V
READY	22	3	READY	3.3V

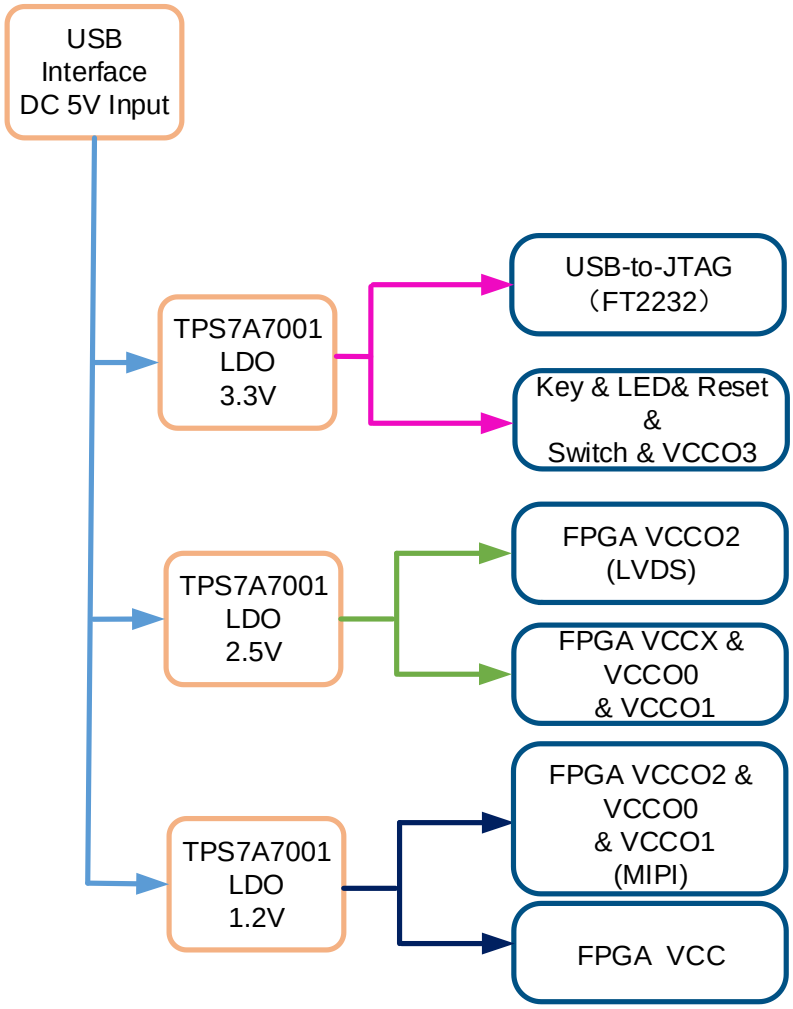
3.3 Power Supply

3.3.1 Overview

DC5V is input by USB interface. The TI LDO power supply chip is used to step down voltage from 5V to 3.3V, 1.8V, and 1.2V, which can meet the power demand of the development board.

3.3.2 Power System Distribution

Figure 3-2 Power System Distribution



3.3.3 Pinout

Table 3-2 FPGA Power Pinout

Name	Pin No.	BANK	Description	I/O Level
VCCO0	109, 127	0	I/O Bank Voltage	2.5V/1.2V
VCCO1	91, 103	1	I/O Bank Voltage	2.5V/1.2V
VCCO2	37, 55	2	I/O Bank Voltage	2.5V/1.2V
VCCO3	5, 19	3	I/O Bank Voltage	3.3V
VCCX	31、77	-	Auxiliary voltage	2.5V
VCC	1, 36, 73, 108	-	Core voltage	1.2V
VSS	2, 17, 33, 35, 53, 74, 89, 105, 107	-	GND	-

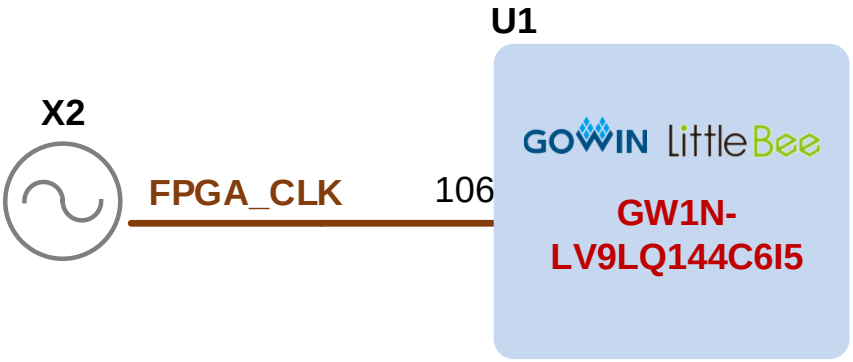
3.4 Clock

3.4.1 Overview

The development board provides a 50MHz crystal oscillator connected to the PLL input pin. This can be employed as the input clock for the PLL in FPGA. Frequency division and multiplication of PLL can provide clocks required by users.

3.4.2 Clock

Figure 3-3 Clock Circuit



3.4.3 Pinout

Table 3-3 FPGA Clock Pinout

Name	Pin No.	BANK	Description	I/O Level
FPGA_CLK	106	1	50MHz crystal oscillator input	2.5V/1.2V

3.5 LED

3.5.1 Overview

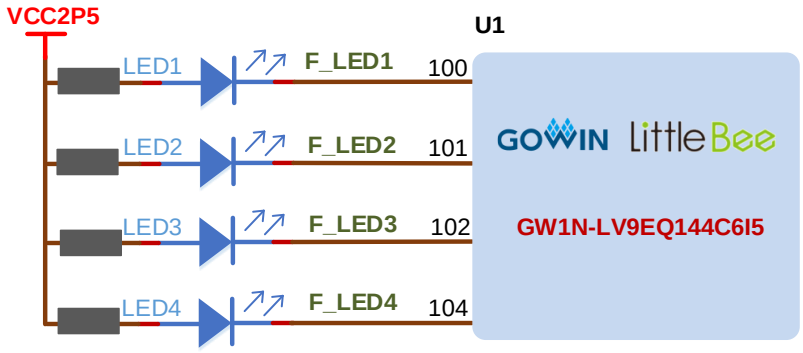
There are four green LEDs in the development board and users can display the required status through the LED. In addition, two LEDs are reserved to signify the power supply and FPGA loading status.

You can test the LEDs in the following ways:

- When the FPGA corresponding pin output signal is logic low, the LED is lit;
- If the signal is high, LED is off.

3.5.2 LED Circuit

Figure 3-4 LED Circuit



3.5.3 Pinout

Table 3-4 LED Pinout

Name	Pin No.	BANK	Description	I/O Level
F_LED1	100	1	LED1	2.5V/1.2V
F_LED2	101	1	LED2	2.5V/1.2V
F_LED3	102	1	LED3	2.5V/1.2V
F_LED4	104	1	LED 4	2.5V/1.2V

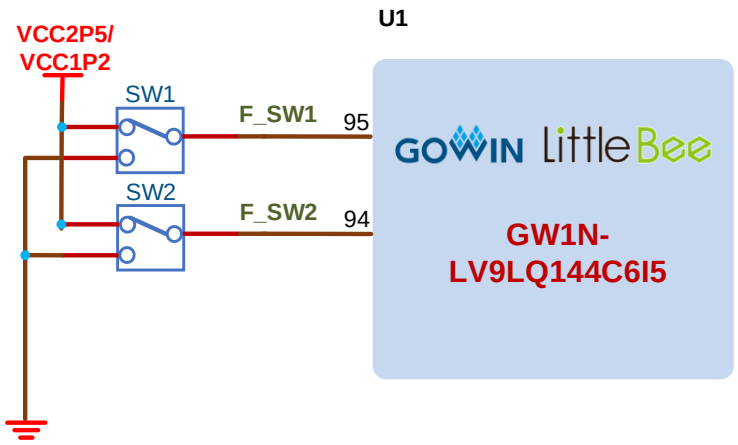
3.6 Switches

3.6.1 Overview

Two Slide switches are incorporated into the development board. These are used to control input during testing.

3.6.2 Switch Circuit

Figure 3-5 Switch Circuit



3.6.3 Pinout

Table 3-5 Switch Circuit Pinout

Name	Pin No.	BANK	Description	I/O Level
F_SW1	95	1	Slide Switch1	2.5V/1.2V
F_SW2	94	1	Slide Switch2	2.5V/1.2V

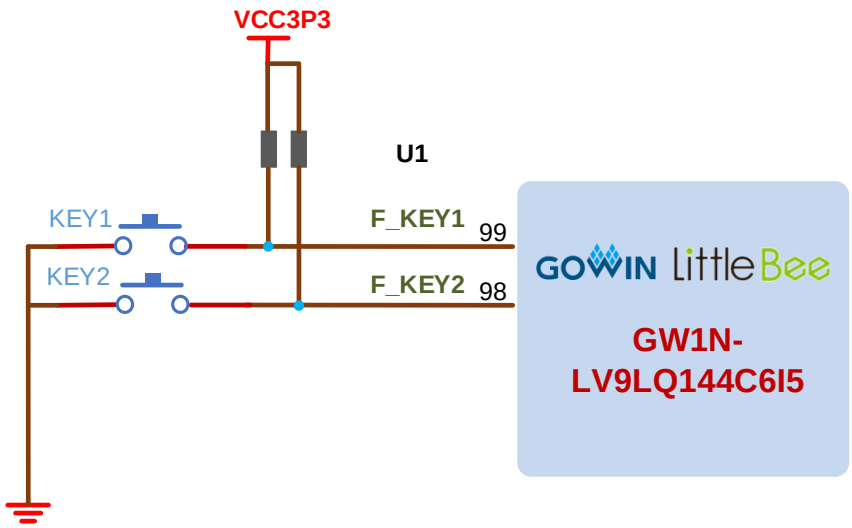
3.7 Key

3.7.1 Overview

Two key switches are embedded in the development board. Users can manually input a low level to the corresponding FPGA pins for testing purposes.

3.7.2 Key Circuit

Figure 3-6 Key Circuit Diagram



3.7.3 Pinout

Table 3-6 Key Circuit Pinout

Name	Pin No.	BANK	Description	I/O Level
F_KEY1	99	1	KEY1	2.5V/1.2V
F_KEY2	98	1	KEY2	2.5V/1.2V

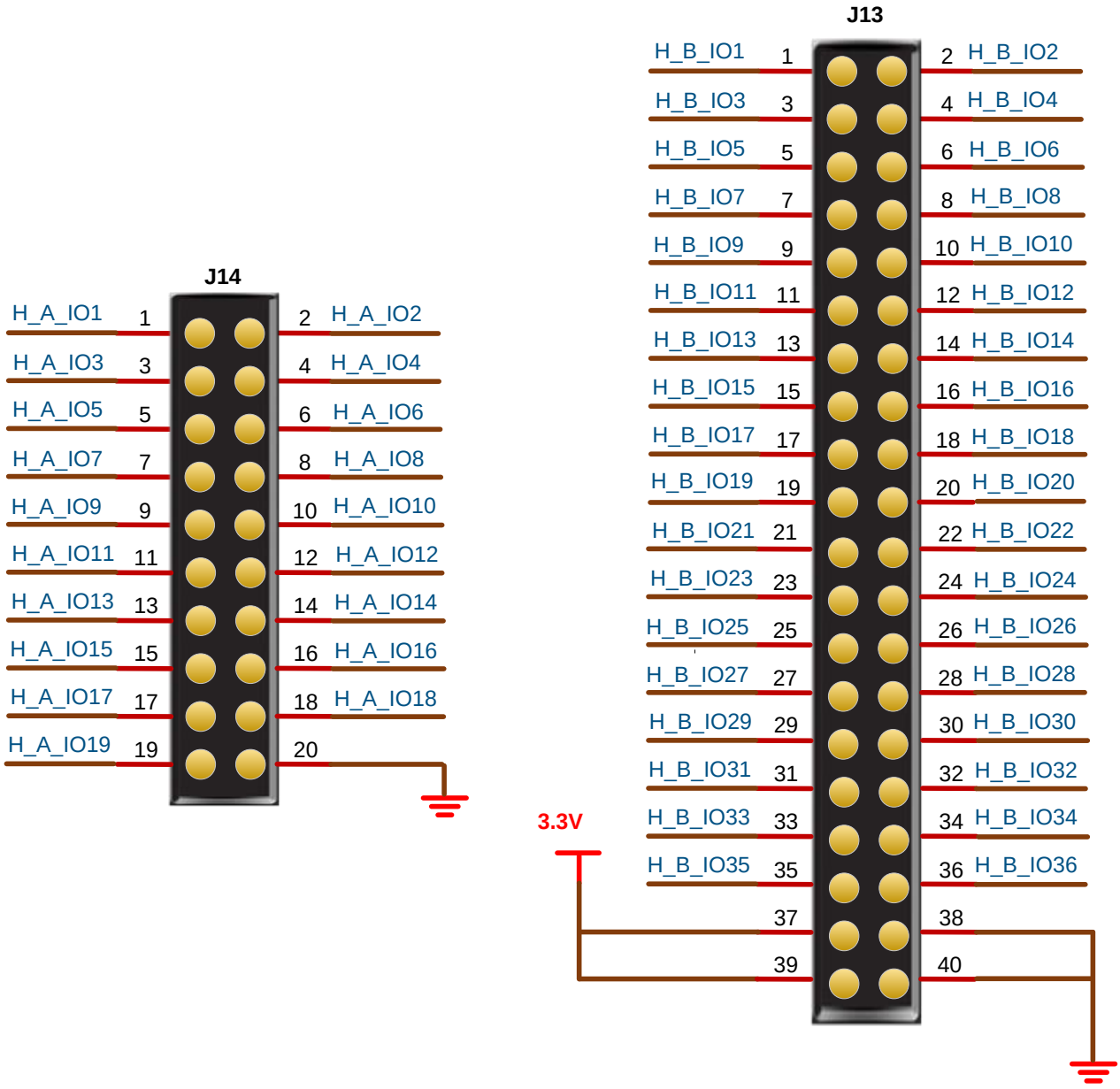
3.8 GPIO

3.8.1 Overview

One 2.54mm DC3-20P socket and one 2.54mm DC3-40P socket are reserved in the development board to facilitate the users to do the function expansion and testing.

3.8.2 GPIO Circuit

Figure 3-7 GPIO Circuit



3.8.3 Pinout

Table 3-7 J14 GPIO Pinout

Name	Pin No.	Socket Pin No.	BANK	Description	I/O Level
H_A_IO1	139	1	3	General I/O	3.3V
H_A_IO2	140	2	3	General I/O	3.3V
H_A_IO3	141	3	3	General I/O	3.3V
H_A_IO4	142	4	3	General I/O	3.3V
H_A_IO5	3	5	3	General I/O	3.3V
H_A_IO6	6	6	3	General I/O	3.3V
H_A_IO7	7	7	3	General I/O	3.3V
H_A_IO8	8	8	3	General I/O	3.3V
H_A_IO9	9	9	3	General I/O	3.3V
H_A_IO10	10	10	3	General I/O	3.3V
H_A_IO11	11	11	3	General I/O	3.3V
H_A_IO12	12	12	3	General I/O	3.3V
H_A_IO13	15	13	3	General I/O	3.3V
H_A_IO14	23	14	3	General I/O	3.3V
H_A_IO15	24	15	3	General I/O	3.3V
H_A_IO16	25	16	3	General I/O	3.3V
H_A_IO17	26	17	3	General I/O	3.3V
H_A_IO18	27	18	3	General I/O	3.3V
H_A_IO19	28	19	3	General I/O	3.3V
GND	-	20	-	GND	-

Table 3-8 J13 GPIO Pinout

Name	Pin No.	Socket Pin No.	BANK	Description	I/O Level
H_B_IO1	132	1	0	General I/O	2.5V/1.2V
H_B_IO2	131	2	0	General I/O	2.5V/1.2V
H_B_IO3	130	3	0	General I/O	2.5V/1.2V
H_B_IO4	129	4	0	General I/O	2.5V/1.2V
H_B_IO5	128	5	0	General I/O	2.5V/1.2V
H_B_IO6	126	6	0	General I/O	2.5V/1.2V
H_B_IO7	88	7	1	General I/O	2.5V/1.2V
H_B_IO8	87	8	1	General I/O	2.5V/1.2V
H_B_IO9	86	9	1	General I/O	2.5V/1.2V
H_B_IO10	85	10	1	General I/O	2.5V/1.2V

Name	Pin No.	Socket Pin No.	BANK	Description	I/O Level
H_B_IO11	84	11	1	General I/O	2.5V/1.2V
H_B_IO12	83	12	1	General I/O	2.5V/1.2V
H_B_IO13	82	13	1	General I/O	2.5V/1.2V
H_B_IO14	81	14	1	General I/O	2.5V/1.2V
H_B_IO15	80	15	1	General I/O	2.5V/1.2V
H_B_IO16	79	16	1	General I/O	2.5V/1.2V
H_B_IO17	68	17	2	General I/O	2.5V/1.2V
H_B_IO18	69	18	2	General I/O	2.5V/1.2V
H_B_IO19	72	19	2	General I/O	2.5V/1.2V
H_B_IO20	75	20	2	General I/O	2.5V/1.2V
H_B_IO21	44	21	2	General I/O	2.5V/1.2V
H_B_IO22	45	22	2	General I/O	2.5V/1.2V
H_B_IO23	48	23	2	General I/O	2.5V/1.2V
H_B_IO24	49	24	2	General I/O	2.5V/1.2V
H_B_IO25	65	25	2	General I/O	2.5V/1.2V
H_B_IO26	64	26	2	General I/O	2.5V/1.2V
H_B_IO27	61	27	2	General I/O	2.5V/1.2V
H_B_IO28	60	28	2	General I/O	2.5V/1.2V
H_B_IO29	57	29	2	General I/O	2.5V/1.2V
H_B_IO30	56	30	2	General I/O	2.5V/1.2V
H_B_IO31	54	31	2	General I/O	2.5V/1.2V
H_B_IO32	52	32	2	General I/O	2.5V/1.2V
H_B_IO33	32	33	2	General I/O	2.5V/1.2V
H_B_IO34	34	34	2	General I/O	2.5V/1.2V
H_B_IO35	40	35	2	General I/O	2.5V/1.2V
H_B_IO36	41	36	2	General I/O	2.5V/1.2V
VCC3P3	-	37	-	3.3V	-
GND	-	38	-	GND	-
VCC3P3	-	39	-	3.3V	-
GND	-	40	-	GND	-

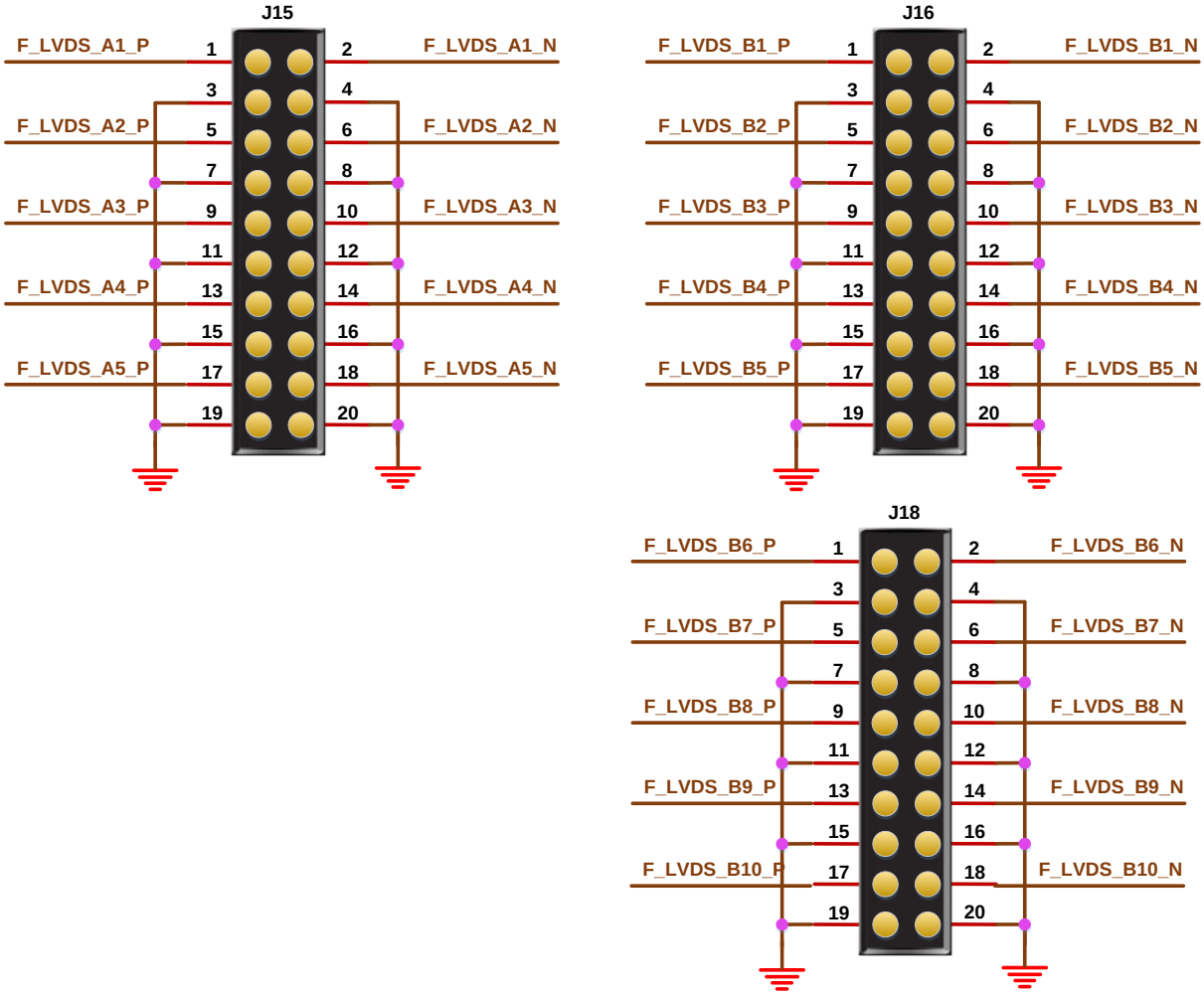
3.9 MIPI/LVDS

3.9.1 Overview

Two 2-mm DC3-20P sockets are reserved in the development board for MIPI/LVDS input/output performance testing and high-speed data transmission. Up to 10 pairs of differential input and 10 pairs of differential output can be satisfied.

3.9.2 MIPI/LVDS Circuit

Figure 3-8 MIPI/LVDS Circuit



3.9.3 Pinout

Table 3-9 J15 FPGA Pinout (IDES 16: 1 Supported)

Name	FPGA Pin No.	Socket Pin No.	BANK	Description	I/O Level
F_LVDS_A1_P	136	1	0	Differential input channel 1+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_A1_N	135	2	0	Differential input channel 1-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	3	-	-	-
GND	-	4	-	-	-
F_LVDS_A2_P	134	5	0	Differential input channel 2+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_A2_N	133	6	0	Differential input channel 2-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	7	-	-	-
GND	-	8	-	-	-
F_LVDS_A3_P	125	9	0	Differential input channel 3+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_A3_N	124	10	0	Differential input channel 3-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	11	-	-	-
GND	-	12	-	-	-
F_LVDS_A4_P	123	13	0	Differential input channel 4+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_A4_N	122	14	0	Differential input channel 4-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	15	-	-	-
GND	-	16	-	-	-
F_LVDS_A5_P	115	17	1	Differential input channel 5+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_A5_N	114	18	1	Differential input channel 5-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	19	-	-	-
GND	-	20	-	-	-

Table 3-10 J16 FPGA Pinout (IDES 16: 1 Supported)

Name	FPGA Pin No.	Socket Pin No.	BANK	Description	I/O Level
F_LVDS_B1_P	29	1	2	Differential output channel 1+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B1_N	30	2	2	Differential output channel 1-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	3	-	-	-
GND	-	4	-	-	-
F_LVDS_B2_P	38	5	2	Differential output channel 2+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B2_N	39	6	2	Differential output channel 2-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	7	-	-	
GND	-	8	-	-	
F_LVDS_B3_P	42	9	2	Differential output channel 3+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B3_N	43	10	2	Differential output channel 3-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	11	-	-	
GND	-	12	-	-	
F_LVDS_B4_P	46	13	2	Differential output channel 4+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B4_N	47	14	2	Differential output channel 4-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	15	-	-	
GND	-	16	-	-	
F_LVDS_B5_P	50	17	2	Differential output channel 5+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B5_N	51	18	2	Differential output channel 5-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	19	-	-	
GND	-	20	-	-	

Table 3-11 J18 FPGA Pinout (IDES 16: 1 Supported)

Name	FPGA Pin No.	Socket Pin No.	BANK	Description	I/O Level
F_LVDS_B6_P	58	1	2	Differential output channel 6+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B6_N	59	2	2	Differential output channel 6-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	3	-	-	-
GND	-	4	-	-	-
F_LVDS_B7_P	62	5	2	Differential output channel 7+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B7_N	63	6	2	Differential output channel 7-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	7	-	-	
GND	-	8	-	-	
F_LVDS_B8_P	66	9	2	Differential output channel 8+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B8_N	67	10	2	Differential output channel 8-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	11	-	-	
GND	-	12	-	-	
F_LVDS_B9_P	70	13	2	Differential output channel 9+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B9_N	71	14	2	Differential output channel 9-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	15	-	-	
GND	-	16	-	-	
F_LVDS_B9_P	78	17	2	Differential output channel 10+	2.5V(LVDS)/ 1.2V(MIPI)
F_LVDS_B9_N	76	18	2	Differential output channel 10-	2.5V(LVDS)/ 1.2V(MIPI)
GND	-	19	-	-	
GND	-	20	-	-	

4 Consideration

Considerations for the use of development board

1. Handle with care and pay attention to electrostatic protection;
2. VCCO2 Bank voltage needs to be set as 2.5V when the Bank2 output differential pairs serve as LVDS output; VCCO2 Bank voltage needs to be set as 1.2V when the Bank2 output differential pairs serve as MIPI output.
3. VCCO0 Bank voltage needs to be set as 2.5V when the Bank0 Input differential pairs serve as LVDS Input; VCCO0 Bank voltage needs to be set as 1.2V when the Bank0 Input differential pairs serve as MIPI Input.

5 Gowin Software

See SUG100, *Gowin Software User Guide* for details.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