WIDEBAND, LOW-NOISE, LOW-DISTORTION, FULLY-DIFFERENTIAL AMPLIFIER

Check for Samples: THS4513

FEATURES

- **Fully-Differential Architecture**
- **Centered Input Common-Mode Range**
- **Minimum Gain of 1 V/V (0 dB)**
- **Bandwidth: 1600 MHz**
- **Slew Rate: 5100 V/µs**
- **1% Settling Time: 2.9 ns**
- **HD_2: –75 dBc at 70 MHz**
- **HD_3: –86 dBc at 70 MHz**
- **OIP_2: 77 dBm at 70 MHz**
- **OIP_3: 42 dBm at 70 MHz**
- **Input Voltage Noise: 2.2 nV/√Hz (f > 10 MHz)**
- **Noise Figure: 19.8 dB**
- **Output Common-Mode Control**
- **Power Supply:**
  - **Voltage: 3 V (±1.5 V) to 5 V (±2.5 V)**
  - **Current: 37.7 mA**
- **Power-Down Capability: 0.65 mA**

APPLICATIONS

- **5-V Data Acquisition Systems, High Linearity ADC Amplifier**
- **Wireless Communication**
- **Medical Imaging**
- **Test and Measurement**

RELATED PRODUCTS

DEVICE	MIN. GAIN	COMMON-MODE RANGE OF INPUT(1)
THS4508	6 dB	–0.3 V to 2.3 V
THS4509	6 dB	1.1 V to 3.9 V
THS4511	0 dB	–0.3 V to 2.3 V
THS4513	0 dB	1.1 V to 3.9 V

1. Assumes a 5-V single-ended power supply.

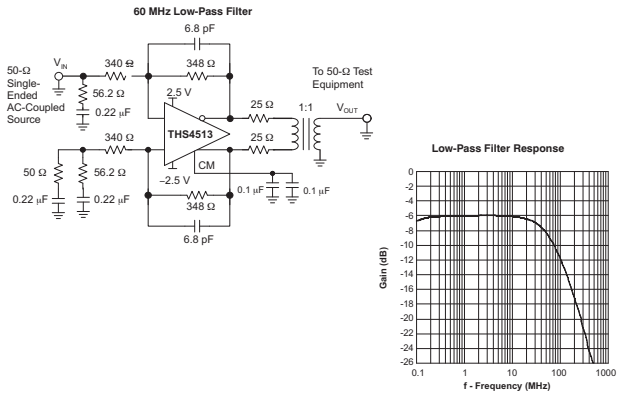
DESCRIPTION

The THS4513 is a wideband, fully-differential op amp designed for 3.3-V to 5-V data acquisition systems. It has very low noise at 2.2 nV/√Hz, and extremely low harmonic distortion of –75 dBc HD_2 and –86 dBc HD_3 at 70 MHz with 2-V_{PP} output, G = 0 dB, and 200-Ω load. Slew rate is very high at 5100 V/µs and with settling time of 2.9 ns to 1% (2-V step), it is ideal for pulsed applications. It is designed for a minimum gain of 0 dB.

To allow for dc-coupling to analog-to-digital converters (ADCs), its unique output common-mode control circuit maintains the output common-mode voltage within 5-mV offset (typ) from the set voltage, when set within 0.5 V of midsupply, with less than 4-mV differential offset voltage. The common-mode set point is set to midsupply by internal circuitry, which may be overdriven from an external source.

The input and output are optimized for best performance with their common-mode voltages set to midsupply. Along with high performance at low power-supply voltage, this design makes it ideal for extremely high-performance, single-supply 5-V data acquisition systems.

The THS4513 is offered in a quad, leadless QFN-16 package (RGT), and is characterized for operation over the full industrial temperature range from –40°C to +85°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION(1)

TEMPERATURE	PACKAGED DEVICES	
	QUAD QFN(2)(3) (RGT-16)	SYMBOL
–40°C to +85°C	THS4513RGTT	—
	THS4513RGTR	

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) This package is available taped and reeled. The ***R*** suffix standard quantity is 3000. The ***T*** suffix standard quantity is 250.
(3) The exposed thermal pad is electrically isolated from all other pins.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

			UNIT
V_{S-} to V_{S+}	Supply voltage		6 V
V_I	Input voltage		$\pm V_S$
V_{ID}	Differential input voltage		4 V
I_O	Output current(2)		200 mA
	Continuous power dissipation		See Dissipation Ratings Table
T_J	Maximum junction temperature		+150°C
T_A	Operating free-air temperature range		–40°C to +85°C
T_{STG}	Storage temperature range		–65°C to +150°C
	ESD ratings	HBM	2000 V
		CDM	1500 V
		MM	100 V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The THS4513 incorporates a (QFN) exposed thermal pad on the underside of the chip. This pad acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical briefs SLMA002 and SLMA004 for more information about utilizing the QFN thermally-enhanced package.

DISSIPATION RATINGS TABLE

PACKAGE	θ_{JC}	θ_{JA}	POWER RATING	
			$T_A \le +25°C$	$T_A = +85°C$
RGT (16)	2.4°C/W	39.5°C/W	2.3 W	225 mW

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ELECTRICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 5$ V

Test conditions at V_{S+} = 2.5 V, V_{S-} = –2.5 V, G = 0 dB, CM = open, V_O = 2 V_{PP}, R_F = 348 Ω, R_L = 200-Ω differential, T_A = +25°C, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE							
Small-signal bandwidth	G = 0 dB, V_O = 100 mV_{PP}			1.6		GHz	C
	G = 6 dB, V_O = 100 mV_{PP}			1.4		GHz	
Gain-bandwidth product	G = 6 dB			2.8		GHz	
Bandwidth for 0-dB flatness	G = 0 dB, V_O = 2 V_{PP}			150		MHz	
	G = 6 dB, V_O = 2 V_{PP}			700			
Large-signal bandwidth	G = 0 dB, V_O = 2 V_{PP}			1.4		GHz	
Slew rate (differential)	2-V step			5100		V/µs	
Rise time fall time				0.5		ns	
				0.5			
Settling time to 1%				2.9			
Settling time to 0.1%				16			
2nd-order harmonic distortion	f = 10 MHz			–110		dBc	
	f = 50 MHz			–80			
	f = 100 MHz			–66			
3rd-order harmonic distortion	f = 10 MHz			–108		dBc	
	f = 50 MHz			–94			
	f = 100 MHz			–81			
2nd-order intermodulation distortion	V_O = 2 V_{PP} envelope, 200-kHz tone spacing, R_L = 100 Ω	f_C = 70 MHz		–78		dBc	
		f_C = 140 MHz		–55			
3rd-order intermodulation distortion		f_C = 70 MHz		–88			
		f_C = 140 MHz		–72			
2nd-order output intercept point	200-kHz tone spacing R_L = 100 Ω	f_C = 70 MHz		77		dBm	
		f_C = 140 MHz		53			
3rd-order output intercept point		f_C = 70 MHz		42			
		f_C = 140 MHz		34			
1-dB compression point	f_C = 70 MHz			12.2		dBm	
	f_C = 140 MHz			10.8			
Noise figure	50-Ω system, 10 MHz, G = 6 dB			19.8		dB	
Input voltage noise	f > 10 MHz			2.2		nV/√Hz	
Input current noise	f > 10 MHz			1.7		pA/√Hz	
DC PERFORMANCE							
Open-loop voltage gain (A_{OL})				63		dB	C
Input offset voltage	T_A = +25°C			1	4	mV	A
	T_A = –40°C to +85°C			1	5	mV	
Average offset voltage drift	T_A = –40°C to +85°C			2.6		µV/°C	B
Input bias current	T_A = +25°C			8	15.5	µA	A
	T_A = –40°C to +85°C			8	18.5		
Average bias current drift	T_A = –40°C to +85°C			20		nA/°C	B
Input offset current	T_A = +25°C			1.6	3.6	µA	A
	T_A = –40°C to +85°C			1.6	7		
Average offset current drift	T_A = –40°C to +85°C			4		nA/°C	B

(1) Test levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

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ELECTRICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 5$ V (continued)

Test conditions at V_{S+} = 2.5 V, V_{S-} = –2.5 V, G = 0 dB, CM = open, V_O = 2 V_{PP}, R_F = 348 Ω, R_L = 200-Ω differential, T_A = +25°C, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
INPUT							
Common-mode input range high				1.4		V	B
Common-mode input range low				–1.4			
Common-mode rejection ratio				90		dB	
Differential input impedance				1.3 || 1.8		MΩ || pF	C
Common-mode input impedance				1.0 || 2.3			
OUTPUT							
Maximum output voltage high	Each output with 100 Ω to midsupply	T_A = +25°C	1.2	1.4		V	A
		T_A = –40°C to +85°C	1.1	1.4			
Minimum output voltage low		T_A = +25°C		–1.4	–1.2	V	
		T_A = –40°C to +85°C		–1.4	–1.1		
Differential output voltage swing	T_A = +25°C		4.8	5.6		V	
	T_A = –40°C to +85°C		4.4	5.6		V	
Differential output current drive	R_L = 10 Ω			96		mA	C
Output balance error	V_O = 100 mV, f = 1 MHz			–52		dB	
Closed-loop output impedance	f = 1 MHz			0.3		Ω	
OUTPUT COMMON-MODE VOLTAGE CONTROL							
Small-signal bandwidth				250		MHz	C
Slew rate				110		V/µs	
Gain				1		V/V	
Output common-mode offset from CM input	–1 V < CM < 1 V			5		mV	
CM input bias current	–1 V < CM < 1 V			±40		µA	
CM input voltage range				–1.5 to 1.5		V	
CM input impedance				23 || 1		kΩ || pF	
CM default voltage				0		V	
POWER SUPPLY							
Specified operating voltage			3	5	5.5	V	C
Maximum quiescent current	T_A = +25°C			37.7	40.9	mA	A
	T_A = –40°C to +85°C			37.7	41.9		
Minimum quiescent current	T_A = +25°C		34.5	37.7		mA	
	T_A = –40°C to +85°C		33.5	37.7			
Power-supply rejection (±PSRR)				90		dB	C
POWER-DOWN							
Enable voltage threshold	Referenced to V_{S-}, assured *on* above 2.1 V + V_{S-}			> 2.1 + V_{S-}		V	C
Disable voltage threshold	Assured *off* below 0.7 V + V_{S-}			< 0.7 + V_{S-}		V	
Power-down quiescent current	T_A = +25°C			0.65	0.9	mA	A
	T_A = –40°C to +85°C			0.65	1		
Input bias current	$\overline{PD}$ = V_{S-}			100		µA	C
Input impedance				50 || 2		kΩ || pF	
Turn-on time delay	Measured to output on			55		ns	
Turn-off time delay	Measured to output off			10		µs	

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ELECTRICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3$ V

Test conditions at V_{S+} = 1.5 V, V_{S-} = –1.5 V, G = 0 dB, CM = open, V_O = 1 V_{PP}, R_F = 348 Ω, R_L = 200-Ω differential, T_A = +25°C, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

PARAMETER	TEST CONDITIONS		TYP	UNIT	TEST LEVEL(1)
AC PERFORMANCE					
Small-signal bandwidth	G = 0 dB, V_O = 100 mV_{PP}		1.6	GHz	C
	G = 6 dB, V_O = 100 mV_{PP}		1.3	GHz	
Gain-bandwidth product	G = 6 dB		2.6	GHz	
Bandwidth for 0-dB Flatness	G = 0 dB, V_O = 1 V_{PP}		135	MHz	
	G = 6 dB, V_O = 1 V_{PP}		450		
Large-signal bandwidth	G = 10 dB, V_O = 1 V_{PP}		1.4	GHz	
Slew rate (differential)	1-V step		2700	V/µs	
Rise time			0.25	ns	
Fall time			0.25		
Settling time to 1%			2.9		
Settling time to 0.1%			16		
2nd-order harmonic distortion	f = 10 MHz		–116	dBc	
	f = 50 MHz		–86		
	f = 100 MHz		–60		
3rd-order harmonic distortion	f = 10 MHz		–83	dBc	
	f = 50 MHz		–61		
	f = 100 MHz		–49		
2nd-order intermodulation distortion	V_O = 1 V_{PP} 200-kHz tone spacing, R_L = 100 Ω	f_C = 70 MHz	–78	dBc	
		f_C = 140 MHz	–55		
3rd-order intermodulation distortion		f_C = 70 MHz	–82		
		f_C = 140 MHz	–65		
2nd-order output intercept point	200-kHz tone spacing R_L = 100 Ω	f_C = 70 MHz	70.2	dBm	
		f_C = 140 MHz	47		
3rd-order output intercept point		f_C = 70 MHz	32.7		
		f_C = 140 MHz	24.7		
1-dB compression point	f_C = 70 MHz		3	dBm	
	f_C = 140 MHz		2		
Noise figure	50-Ω system, 10 MHz, G = 6 dB		19.8	dB	
Input voltage noise	f > 10 MHz		3.3	nV/√Hz	
Input current noise	f > 10 MHz		1.7	pA/√Hz	
DC PERFORMANCE					
Open-loop voltage gain (A_{OL})			68	dB	
Input offset voltage	T_A = +25°C		1	mV	
Average offset voltage drift	T_A = –40°C to +85°C		2.6	µV/°C	
Input bias current	T_A = +25°C		6	µA	
Average bias current drift	T_A = –40°C to +85°C		20	nA/°C	
Input offset current	T_A = +25°C		1.6	µA	
Average offset current drift	T_A = –40°C to +85°C		4	nA/°C	
INPUT					
Common-mode input range high			0.4	V	
Common-mode input range low			–0.4		
Common-mode rejection ratio			90	dB	
Differential input impedance			1.3 || 1.8	MΩ || pF	
Common-mode input impedance			1.0 || 2.3		

(1) Test levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

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ELECTRICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3$ V (continued)

Test conditions at V_{S+} = 1.5 V, V_{S-} = –1.5 V, G = 0 dB, CM = open, V_O = 1 V_{PP}, R_F = 348 Ω, R_L = 200-Ω differential, T_A = +25°C, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted.

PARAMETER	TEST CONDITIONS	TYP	UNIT	TEST LEVEL(1)
OUTPUT				
Maximum output voltage high	Each output with 100 Ω to midsupply	0.45	V	
Minimum output voltage low		–0.45	V	
Differential output voltage swing		1.8	V	
Differential output current drive	R_L = 10 Ω	50	mA	
Output balance error	V_O = 100 mV, f = 1 MHz	–54	dB	
Closed-loop output Impedance	f = 1 MHz	0.3	Ω	
OUTPUT COMMON-MODE VOLTAGE CONTROL				
Small-signal bandwidth		150	MHz	
Slew rate		60	V/µs	
Gain		1	V/V	
Output common-mode offset from CM input	–0.5 V < CM < 0.5 V	4	mV	
CM input bias current	–0.5 V < CM < 0.5 V	±40	µA	
CM input voltage range		–1.5 to 1.5	V	C
CM input impedance		20 || 1	kΩ || pF	
CM default voltage		0	V	
POWER SUPPLY				
Quiescent current		34.8	mA	
Power-supply rejection (±PSRR)		80	dB	
POWER-DOWN				
Enable voltage threshold	Referenced to V_{S-}, assured *on* above 2.1 V + V_{S-}	> 2.1	V	
Disable voltage threshold	Assured *off* below 0.7 V + V_{S-}	< 0.7	V	
Power-down quiescent current		0.46	mA	
Input bias current	$\overline{PD}$ = V_{S-}	65	µA	
Input impedance		50 || 2	kΩ || pF	
Turn-on time delay	Measured to output on	100	ns	
Turn-off time delay	Measured to output off	10	µs	

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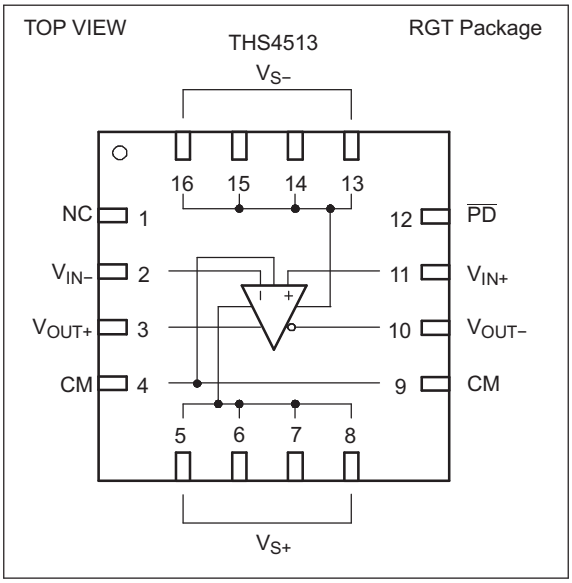
DEVICE INFORMATION



TERMINAL FUNCTIONS

TERMINAL (RGT PACKAGE)		DESCRIPTION
NO.	NAME	
1	NC	No internal connection
2	$V_{IN–}$	Inverting amplifier input
3	V_{OUT+}	Noninverting amplifier output
4, 9	CM	Common-mode voltage input
5-8	V_{S+}	Positive amplifier power-supply input
10	$V_{OUT–}$	Inverted amplifier output
11	V_{IN+}	Noninverting amplifier input
12	$\overline{PD}$	Power-down; $\overline{PD}$ = logic low puts part into low-power mode, $\overline{PD}$ = logic high or open for normal operation
13-16	$V_{S–}$	Negative amplifier power-supply input

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TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 5$ V

Small-Signal Frequency Response	G = 0 dB, V_{OD} = 100 mV_{PP}		Figure 1
	G = 6 dB, V_{OD} = 100 mV_{PP}		Figure 2
Large-Signal Frequency Response	G = 0 dB, V_{OD} = 2 V_{PP}		Figure 3
	G = 6 dB, V_{OD} = 2 V_{PP}		Figure 4
Harmonic Distortion	HD_2, G = 0 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 5
	HD_3, G = 0 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 6
	HD_2, G = 6 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 7
	HD_3, G = 6 dB, V_{OD} = 2 V_{PP}	vs Frequency	Figure 8
	HD_2, G = 0 dB	vs Output Voltage	Figure 9
	HD_3, G = 0 dB	vs Output Voltage	Figure 10
	HD_2, G = 0 dB	vs CM Output Voltage	Figure 11
	HD_3, G = 0 dB	vs CM Output Voltage	Figure 12
Intermodulation Distortion	IMD_2, G = 0 dB	vs Frequency	Figure 13
	IMD_3, G = 0 dB	vs Frequency	Figure 14
Output Intercept Point	OIP_2	vs Frequency	Figure 15
	OIP_3	vs Frequency	Figure 16
S-Parameters		vs Frequency	Figure 17
Transition Rate		vs Output Voltage	Figure 18
Transient Response			Figure 19
Settling Time			Figure 20
Rejection Ratio		vs Frequency	Figure 21
Output Impedance		vs Frequency	Figure 22
Overdrive Recovery			Figure 23
Output Voltage Swing		vs Load Resistance	Figure 24
Turn-Off Time			Figure 25
Turn-On Time			Figure 26
Input Offset Voltage		vs Input Common-Mode Voltage	Figure 27
Open-Loop Gain		vs Frequency	Figure 28
Input-Referred Noise		vs Frequency	Figure 29
Noise Figure		vs Frequency	Figure 30
Quiescent Current		vs Supply Voltage	Figure 31
Power-Supply Current		vs Supply Voltage in Power-Down Mode	Figure 32
Output Balance Error		vs Frequency	Figure 33
CM Input Impedance		vs Frequency	Figure 34
CM Small-Signal Frequency Response			Figure 35
CM Input Bias Current		vs CM Input Voltage	Figure 36
Differential Output Offset Voltage		vs CM Input Voltage	Figure 37
Output Common-Mode Offset		vs CM Input Voltage	Figure 38

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TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 5$ V

Test conditions at V_{S+} = +2.5 V, V_{S-} = –2.5V, CM = open, V_O = 2 V_{PP}, R_F = 348 Ω, R_L = 200-Ω differential, G = 0 dB, single-ended input, and input and output referenced to midsupply, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

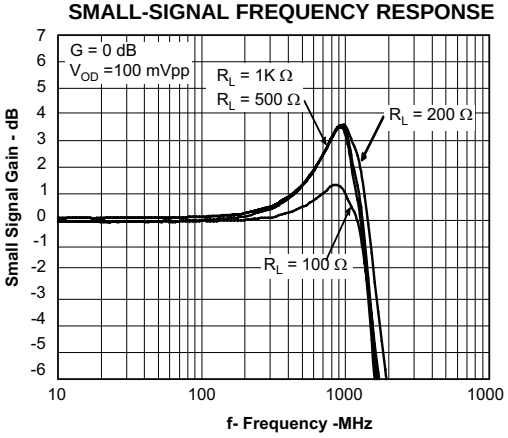

Figure 1.

SMALL-SIGNAL FREQUENCY RESPONSE

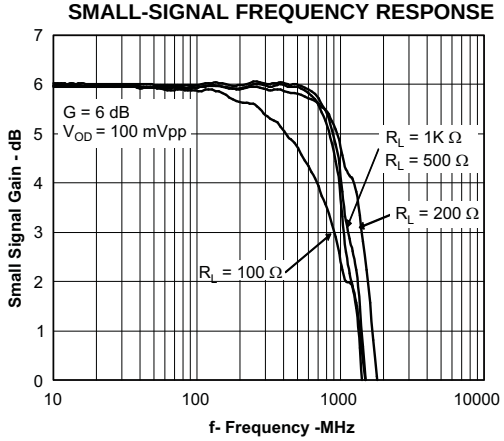

Figure 2.

LARGE-SIGNAL FREQUENCY RESPONSE

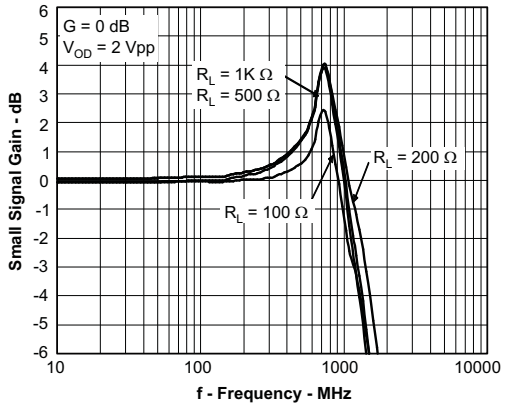

Figure 3.

LARGE-SIGNAL FREQUENCY RESPONSE

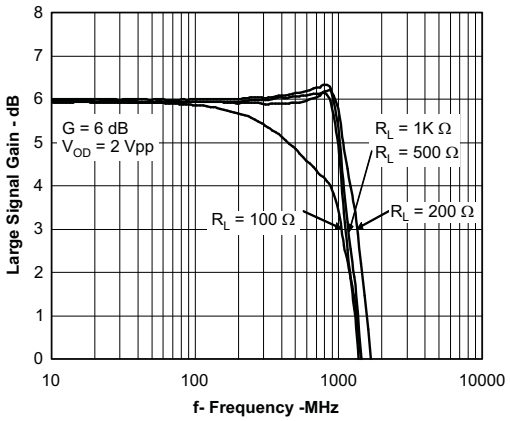

Figure 4.

HD_2 vs FREQUENCY

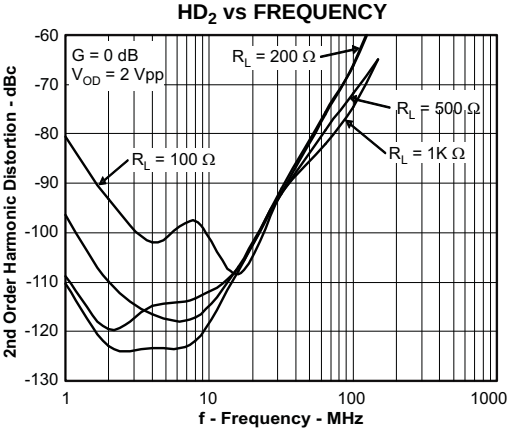

Figure 5.

HD_3 vs FREQUENCY

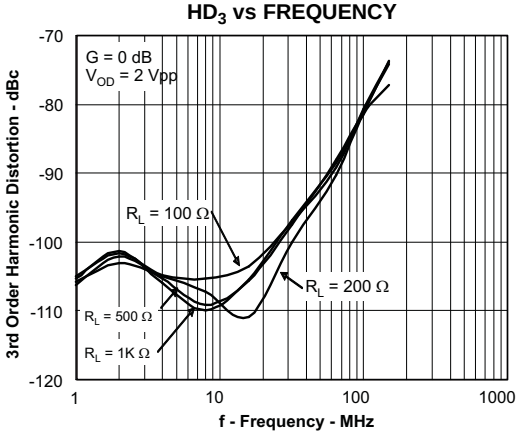

Figure 6.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 5$ V (continued)

Test conditions at V_{S+} = +2.5 V, V_{S-} = –2.5V, CM = open, V_O = 2 V_{PP}, R_F = 348 Ω, R_L = 200-Ω differential, G = 0 dB, single-ended input, and input and output referenced to midsupply, unless otherwise noted.

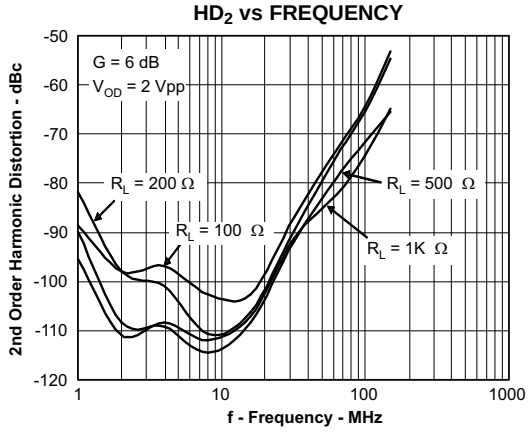

Figure 7.

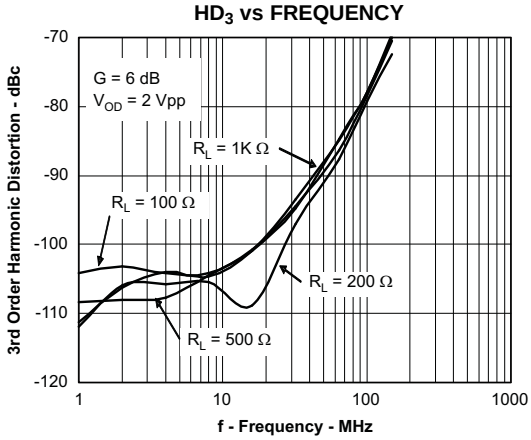

Figure 8.

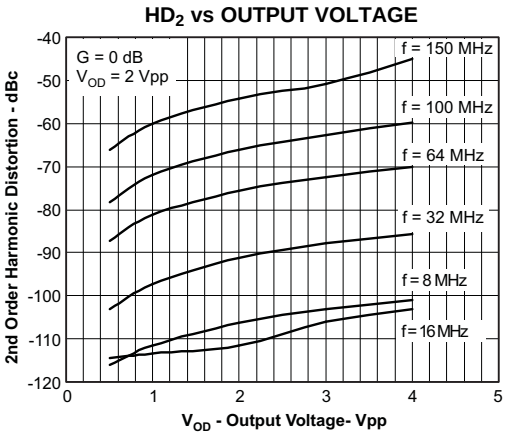

Figure 9.

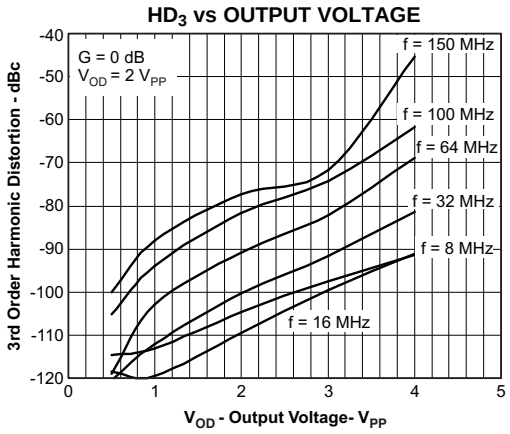

Figure 10.

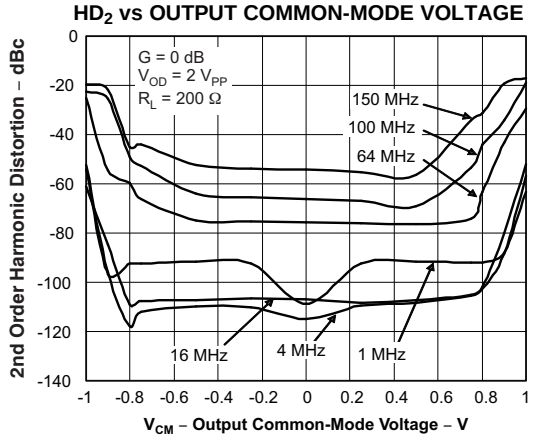

Figure 11.

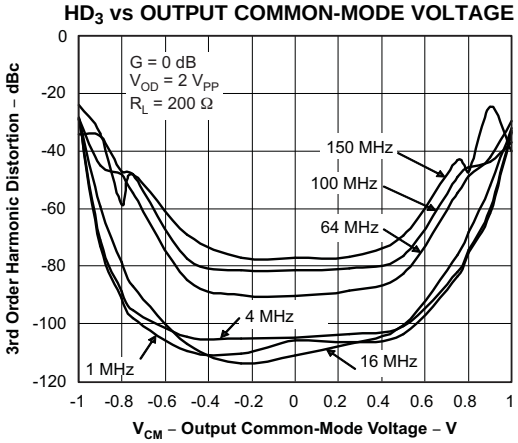

Figure 12.

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TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 5$ V (continued)

Test conditions at V_{S+} = +2.5 V, V_{S-} = –2.5V, CM = open, V_O = 2 V_{PP}, R_F = 348 Ω, R_L = 200-Ω differential, G = 0 dB, single-ended input, and input and output referenced to midsupply, unless otherwise noted.

IMD_2 vs FREQUENCY

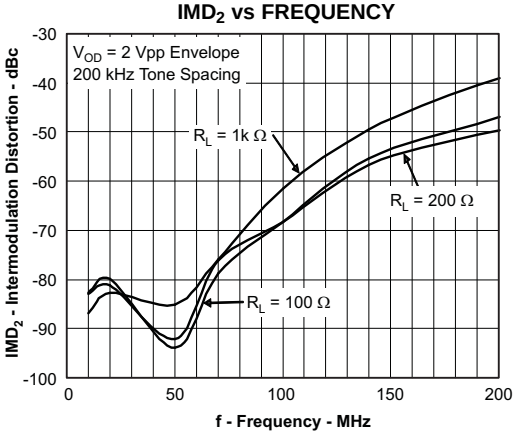

Figure 13.

IMD_3 vs FREQUENCY

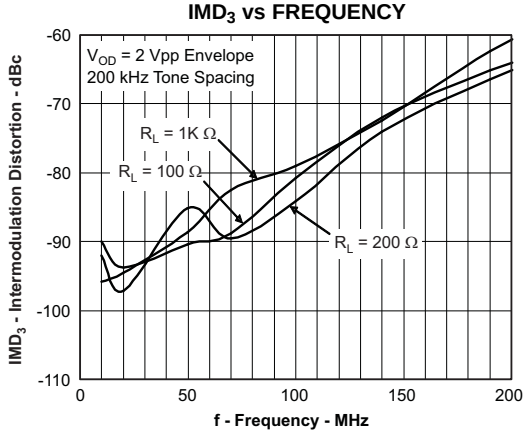

Figure 14.

OIP_2 vs FREQUENCY

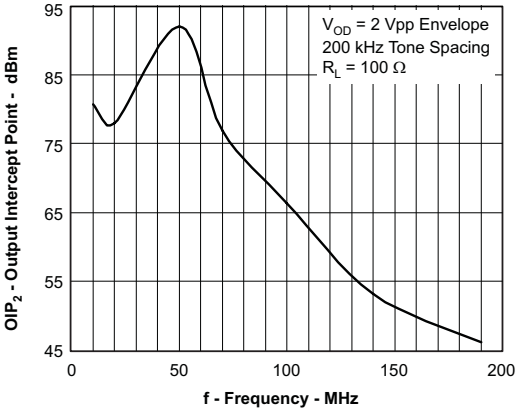

Figure 15.

OIP_3 vs FREQUENCY

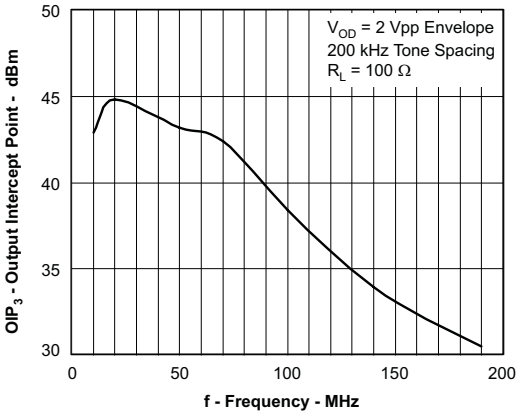

Figure 16.

S-PARAMETERS vs FREQUENCY

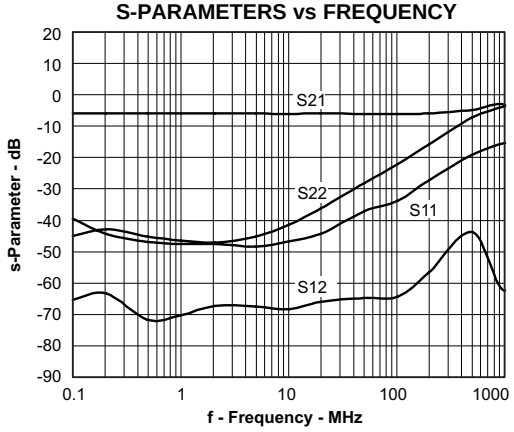

Figure 17.

TRANSITION RATE vs OUTPUT VOLTAGE

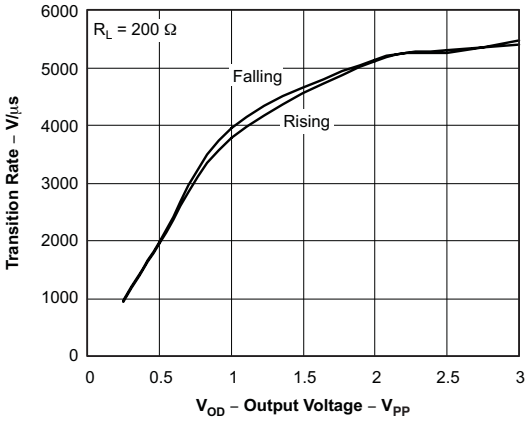

Figure 18.

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TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 5$ V (continued)

Test conditions at V_{S+} = +2.5 V, V_{S-} = –2.5V, CM = open, V_O = 2 V_{PP}, R_F = 348 Ω, R_L = 200-Ω differential, G = 0 dB, single-ended input, and input and output referenced to midsupply, unless otherwise noted.

TRANSIENT RESPONSE

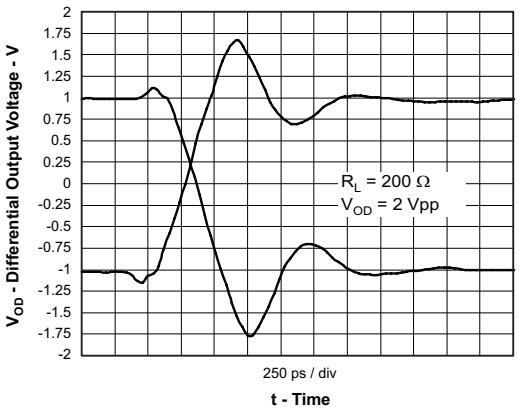

Figure 19.

SETTLING TIME

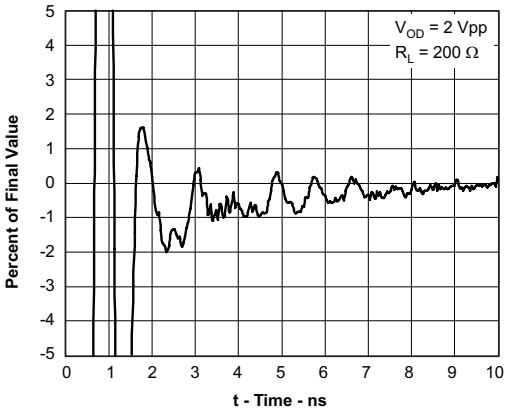

Figure 20.

REJECTION RATIO vs FREQUENCY

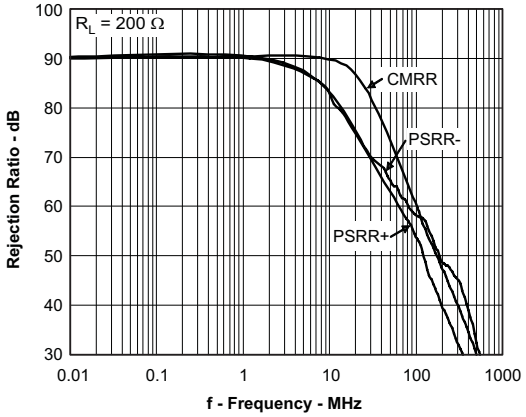

Figure 21.

OUTPUT IMPEDANCE vs FREQUENCY

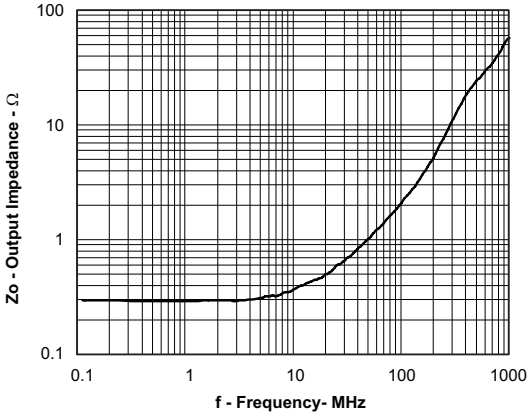

Figure 22.

OVERDRIVE RECOVERY

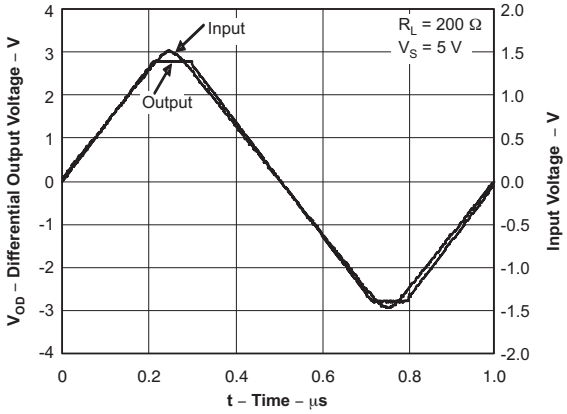

Figure 23.

OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

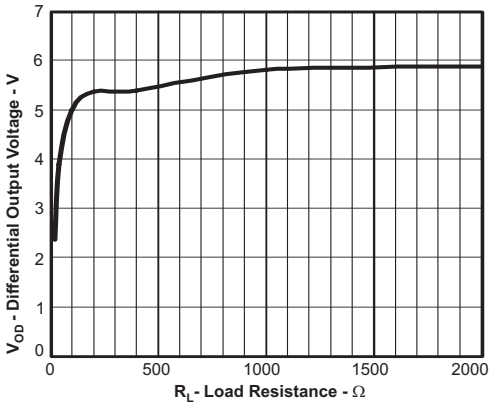

Figure 24.

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TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 5$ V (continued)

Test conditions at V_{S+} = +2.5 V, V_{S-} = –2.5V, CM = open, V_O = 2 V_{PP}, R_F = 348 Ω, R_L = 200-Ω differential, G = 0 dB, single-ended input, and input and output referenced to midsupply, unless otherwise noted.

TURN-OFF TIME

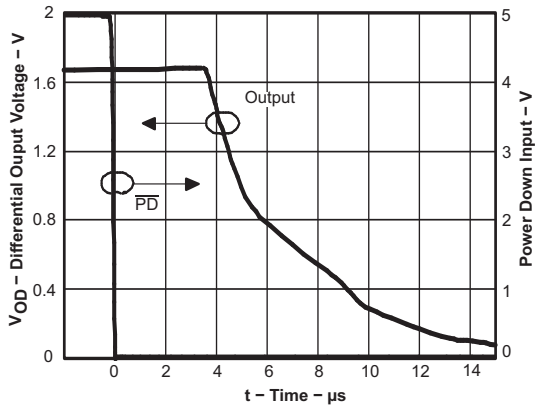

Figure 25.

TURN-ON TIME

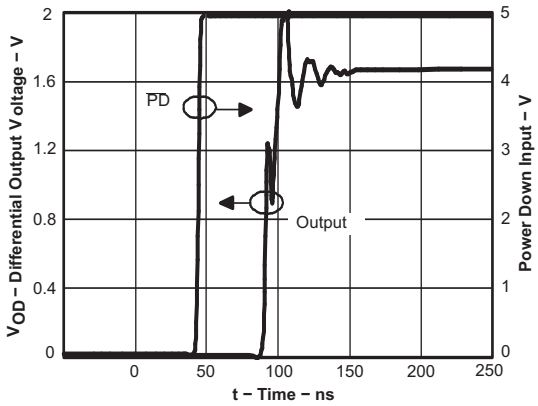

Figure 26.

INPUT OFFSET VOLTAGE vs INPUT COMMON-MODE VOLTAGE

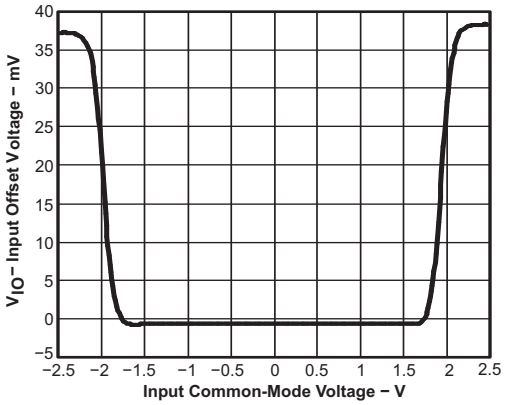

Figure 27.

OPEN-LOOP GAIN vs FREQUENCY

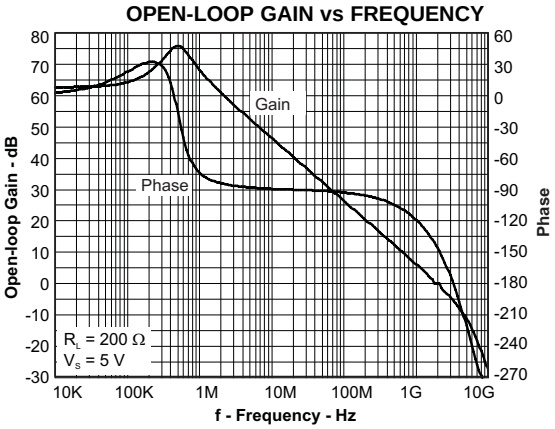

Figure 28.

INPUT-REFERRED NOISE vs FREQUENCY

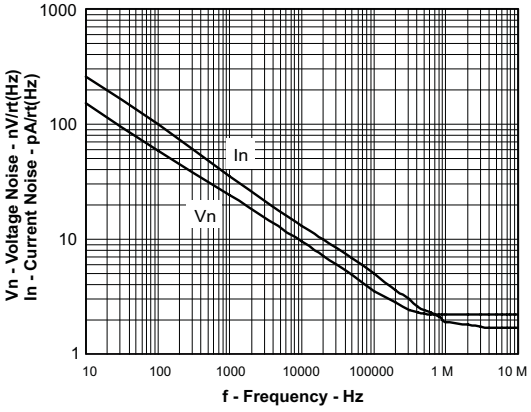

Figure 29.

NOISE FIGURE vs FREQUENCY

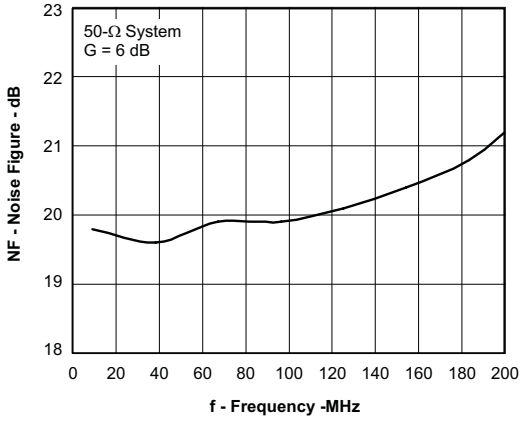

Figure 30.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 5$ V (continued)

Test conditions at V_{S+} = +2.5 V, V_{S-} = –2.5V, CM = open, V_O = 2 V_{PP}, R_F = 348 Ω, R_L = 200-Ω differential, G = 0 dB, single-ended input, and input and output referenced to midsupply, unless otherwise noted.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

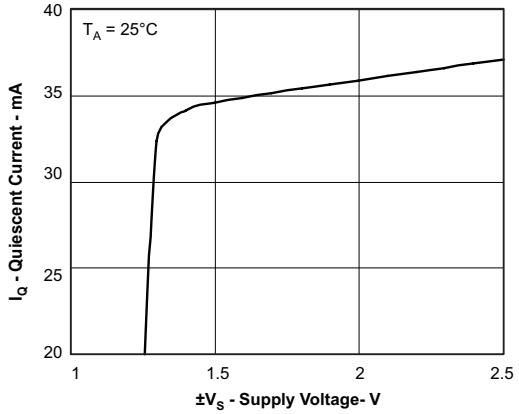

Figure 31.

POWER-DOWN QUIESCENT CURRENT vs SUPPLY VOLTAGE

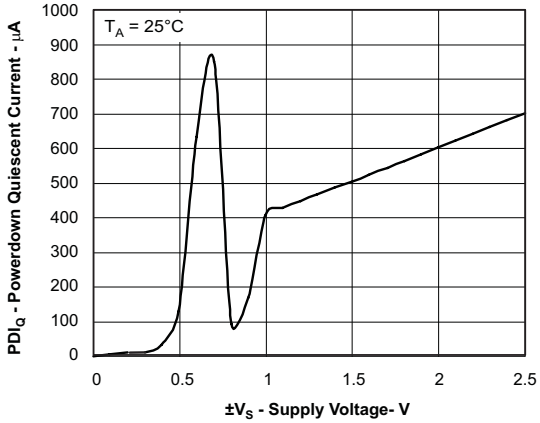

Figure 32.

OUTPUT BALANCE ERROR RESPONSE vs FREQUENCY

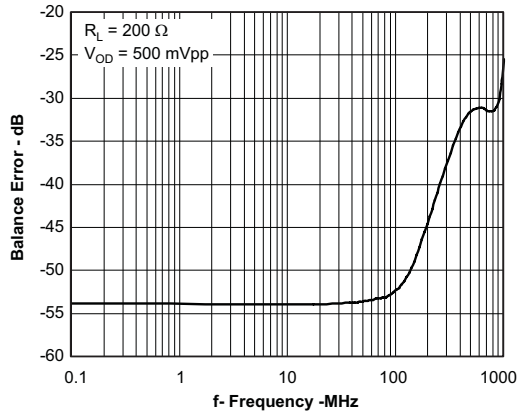

Figure 33.

CM INPUT IMPEDANCE vs FREQUENCY

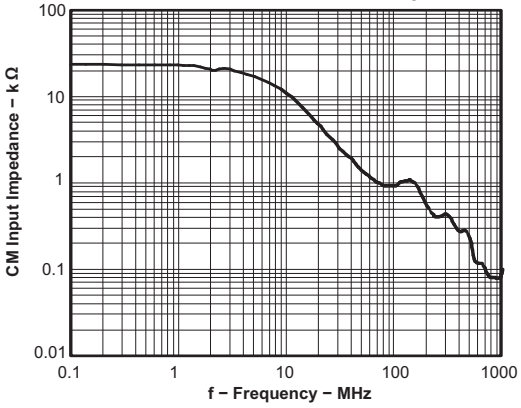

Figure 34.

CM SMALL-SIGNAL FREQUENCY RESPONSE

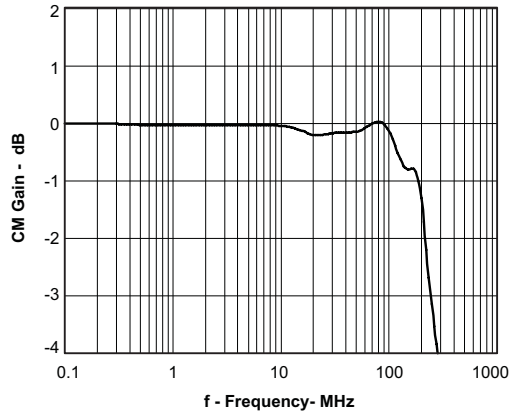

Figure 35.

CM INPUT BIAS CURRENT vs CM INPUT VOLTAGE

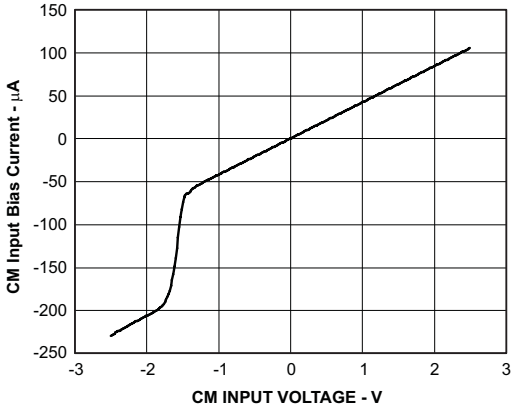

Figure 36.

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TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 5$ V (continued)

Test conditions at V_{S+} = +2.5 V, V_{S-} = –2.5V, CM = open, V_O = 2 V_{PP}, R_F = 348 Ω, R_L = 200-Ω differential, G = 0 dB, single-ended input, and input and output referenced to midsupply, unless otherwise noted.

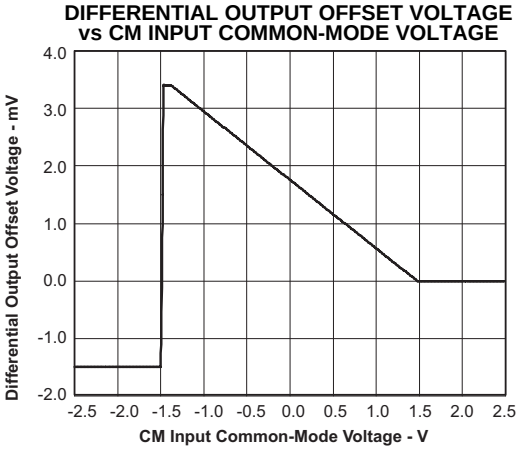

Figure 37.

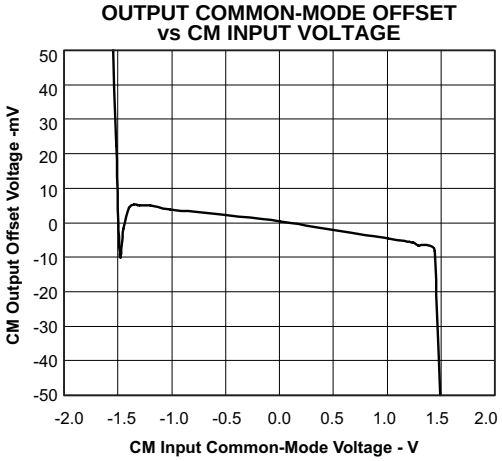

Figure 38.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3$ V

Small-Signal Frequency Response	G = 0 dB, V_{OD} = 100 mV_{PP}		Figure 39
	G = 6 dB, V_{OD} = 100 mV_{PP}		Figure 40
Large-Signal Frequency Response	G = 0 dB, V_{OD} = 1 V_{PP}		Figure 41
	G = 6 dB, V_{OD} = 1 V_{PP}		Figure 42
Harmonic Distortion	HD_2, G = 0 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 43
	HD_3, G = 0 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 44
	HD_2, G = 6 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 45
	HD_3, G = 6 dB, V_{OD} = 1 V_{PP}	vs Frequency	Figure 46
	HD_2, G = 0 dB	vs Output Voltage	Figure 47
	HD_3, G = 0 dB	vs Output Voltage	Figure 48
	HD_2, G = 0 dB	vs CM Output Voltage	Figure 49
	HD_3, G = 0 dB	vs CM Output Voltage	Figure 50
Intermodulation Distortion	IMD_2, G = 0 dB	vs Frequency	Figure 51
	IMD_3, G = 0 dB	vs Frequency	Figure 52
Output Intercept Point	OIP_2	vs Frequency	Figure 53
	OIP_3	vs Frequency	Figure 54
S-Parameters		vs Frequency	Figure 55
Transition Rate		vs Output Voltage	Figure 56
Transient Response			Figure 57
Settling Time			Figure 58
Output Voltage Swing		vs Load Resistance	Figure 59
Rejection Ratio		vs Frequency	Figure 60
Overdrive Recovery			Figure 61
Output Impedance		vs Frequency	Figure 62
Turn-Off Time			Figure 63
Turn-On Time			Figure 64
Output Balance Error		vs Frequency	Figure 65
Noise Figure		vs Frequency	Figure 66
CM Small-Signal Frequency Response			Figure 67
CM Input Impedance		vs Frequency	Figure 68
Differential Output Offset Voltage		vs CM Input Voltage	Figure 69
Output Common-Mode Offset		vs CM Input Voltage	Figure 70

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TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3$ V

Test conditions at V_{S+} = +1.5 V, V_{S-} = –1.5V, CM = open, V_{OD} = 1 V_{PP}, R_F = 348 Ω, R_L = 200-Ω differential, G = 0 dB, single-ended input, and input and output referenced to midsupply, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

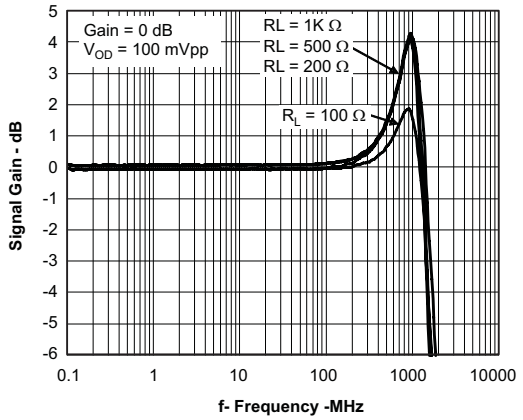

Figure 39.

SMALL-SIGNAL FREQUENCY RESPONSE

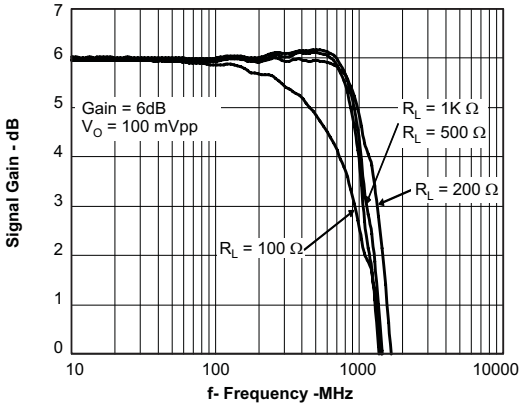

Figure 40.

LARGE-SIGNAL FREQUENCY RESPONSE

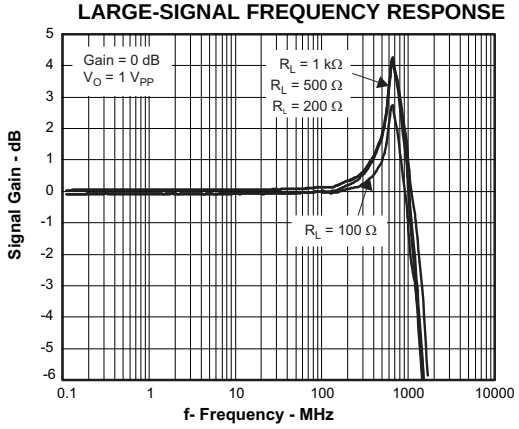

Figure 41.

LARGE-SIGNAL FREQUENCY RESPONSE

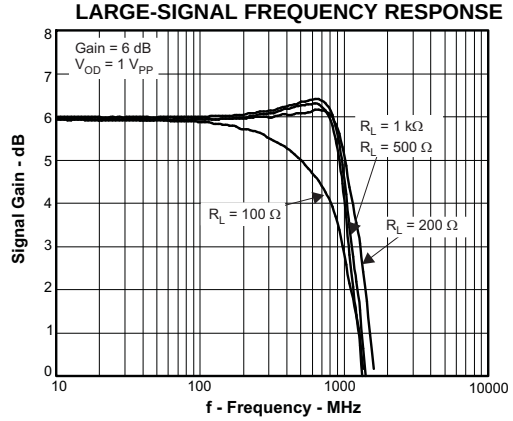

Figure 42.

HD_2 vs FREQUENCY

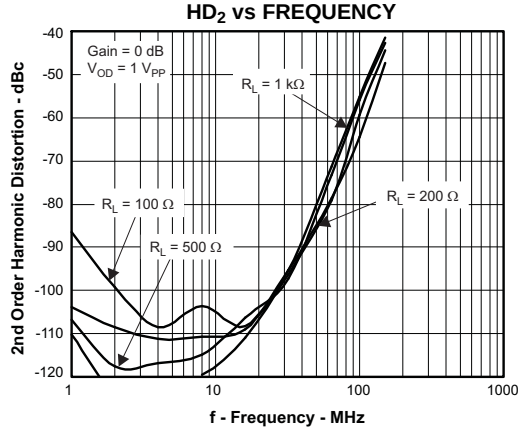

Figure 43.

HD_3 vs FREQUENCY

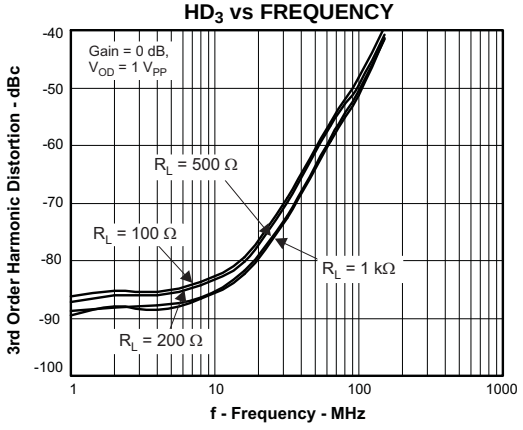

Figure 44.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3$ V (continued)

Test conditions at V_{S+} = +1.5 V, V_{S-} = –1.5V, CM = open, V_{OD} = 1 V_{PP}, R_F = 348 Ω, R_L = 200-Ω differential, G = 0 dB, single-ended input, and input and output referenced to midsupply, unless otherwise noted.

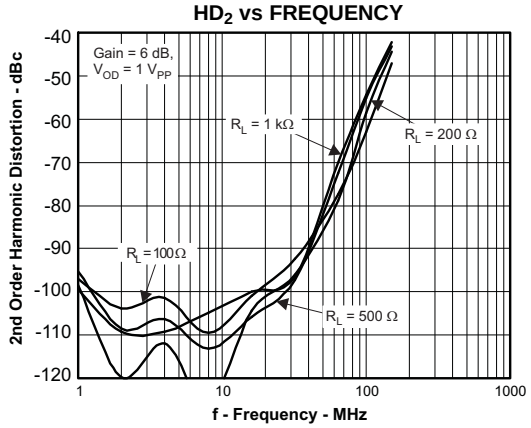

Figure 45.

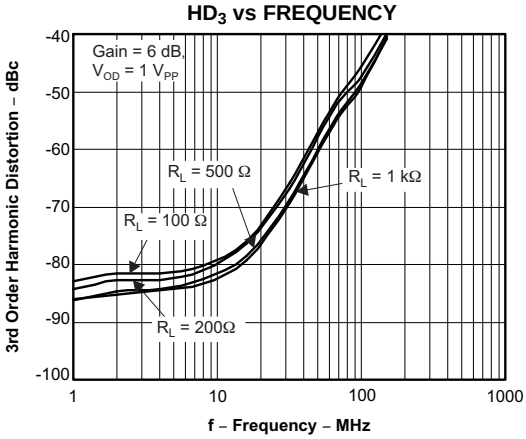

Figure 46.

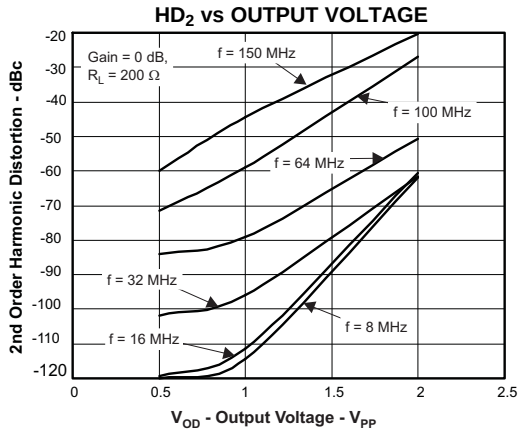

Figure 47.

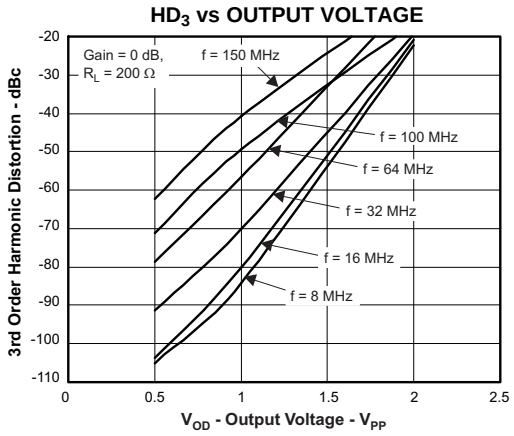

Figure 48.

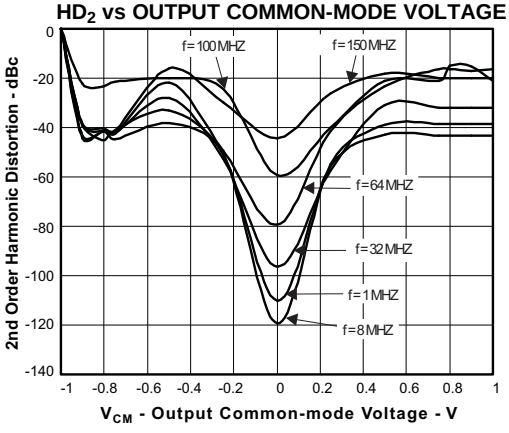

Figure 49.

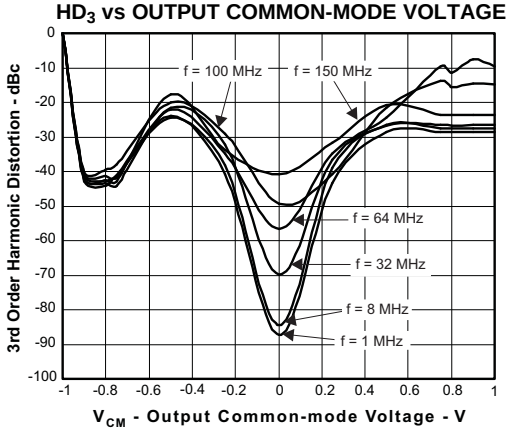

Figure 50.

Copyright © 2005–2013, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3$ V (continued)

Test conditions at V_{S+} = +1.5 V, V_{S-} = –1.5V, CM = open, V_{OD} = 1 V_{PP}, R_F = 348 Ω, R_L = 200-Ω differential, G = 0 dB, single-ended input, and input and output referenced to midsupply, unless otherwise noted.

IMD_2 vs FREQUENCY

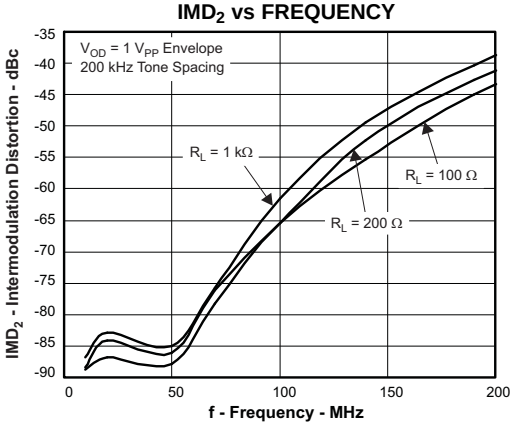

Figure 51.

IMD_3 vs FREQUENCY

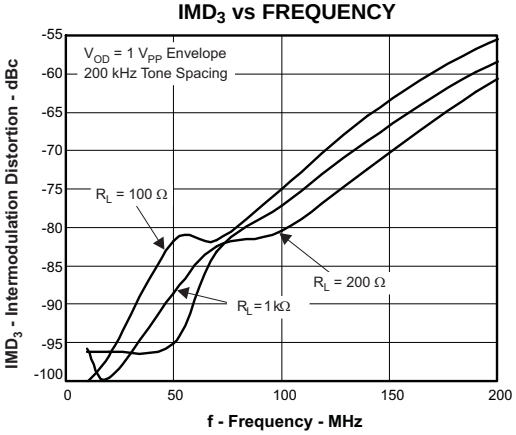

Figure 52.

OIP_2 vs FREQUENCY

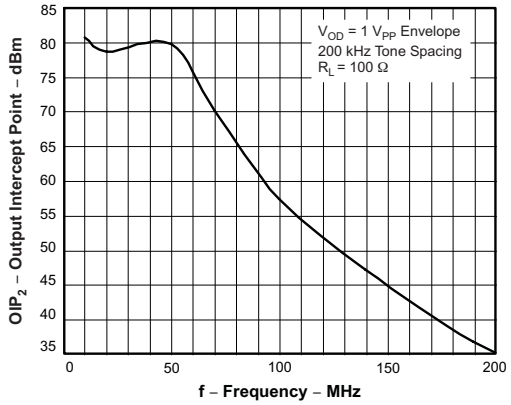

Figure 53.

OIP_3 vs FREQUENCY

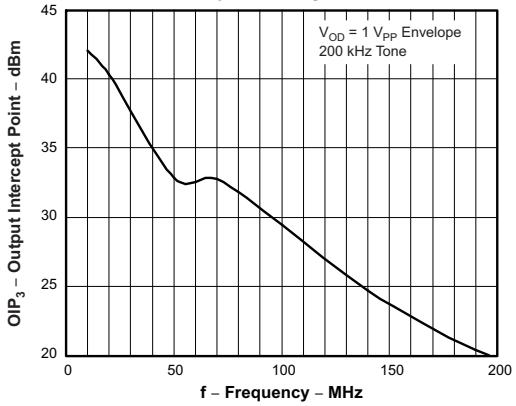

Figure 54.

S-PARAMETERS vs FREQUENCY

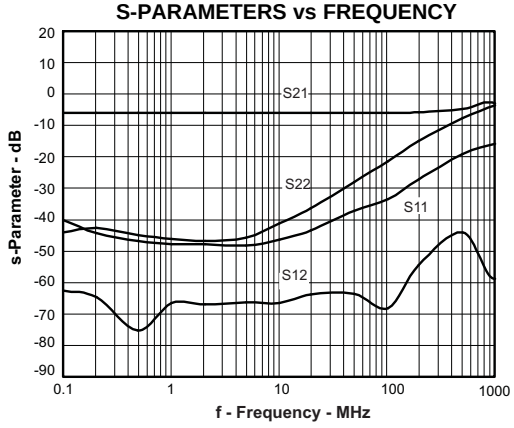

Figure 55.

TRANSITION RATE vs OUTPUT VOLTAGE

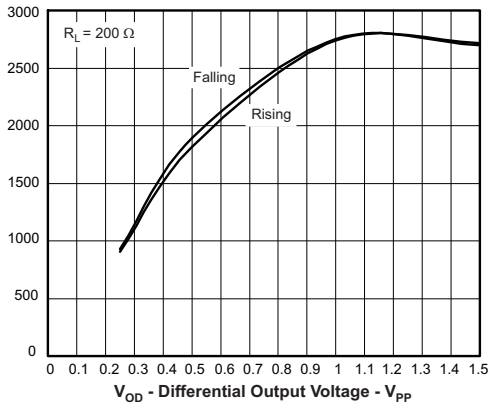

Figure 56.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3$ V (continued)

Test conditions at V_{S+} = +1.5 V, V_{S-} = –1.5V, CM = open, V_{OD} = 1 V_{PP}, R_F = 348 Ω, R_L = 200-Ω differential, G = 0 dB, single-ended input, and input and output referenced to midsupply, unless otherwise noted.

TRANSIENT RESPONSE

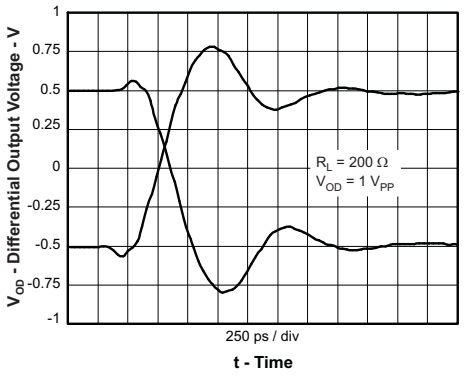

Figure 57.

SETTLING TIME

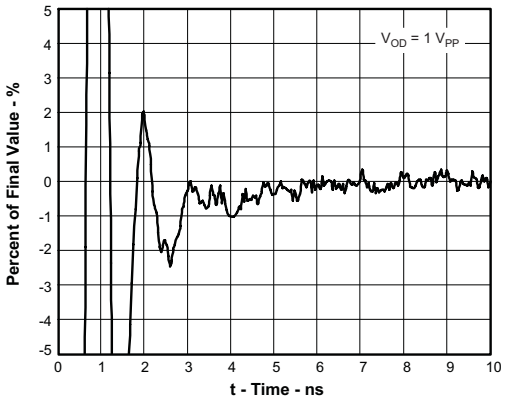

Figure 58.

OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

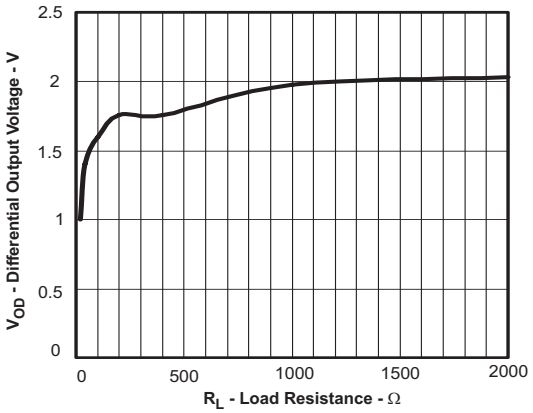

Figure 59.

REJECTION RATIO vs FREQUENCY

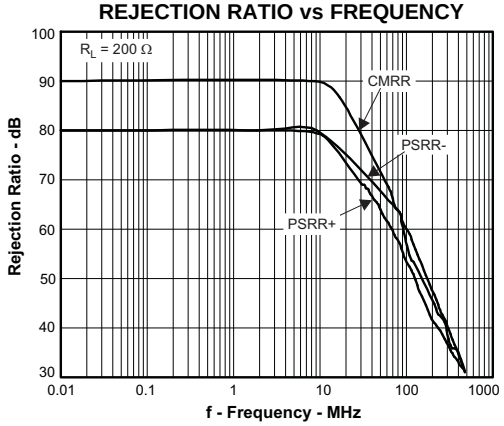

Figure 60.

OVERDRIVE RECOVERY

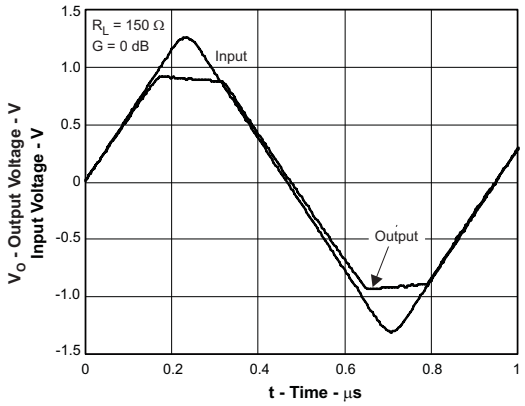

Figure 61.

OUTPUT IMPEDANCE VS FREQUENCY

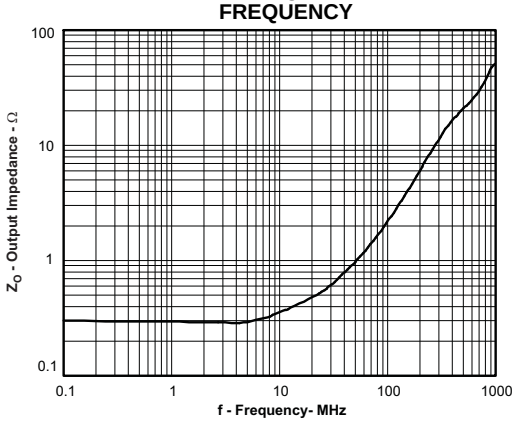

Figure 62.

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TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3$ V (continued)

Test conditions at V_{S+} = +1.5 V, V_{S-} = –1.5V, CM = open, V_{OD} = 1 V_{PP}, R_F = 348 Ω, R_L = 200-Ω differential, G = 0 dB, single-ended input, and input and output referenced to midsupply, unless otherwise noted.

TURN-OFF TIME

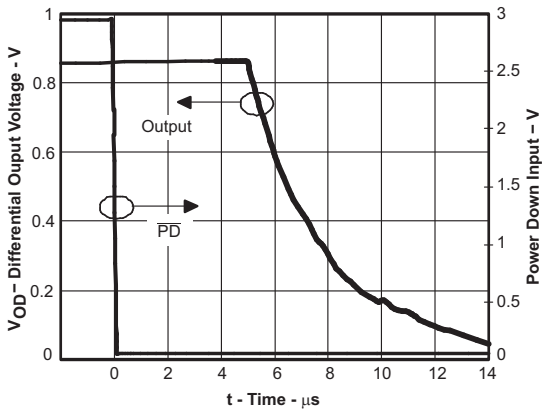

Figure 63.

TURN-ON TIME

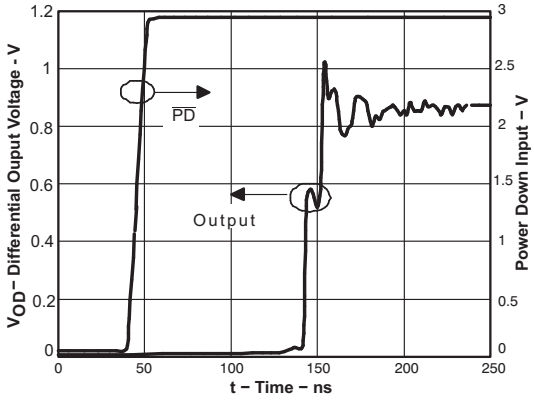

Figure 64.

OUTPUT BALANCE ERROR vs FREQUENCY

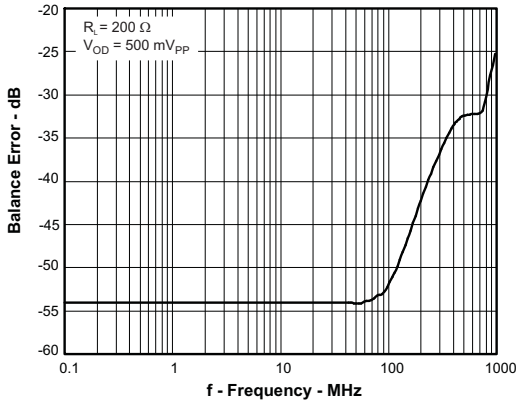

Figure 65.

NOISE FIGURE vs FREQUENCY

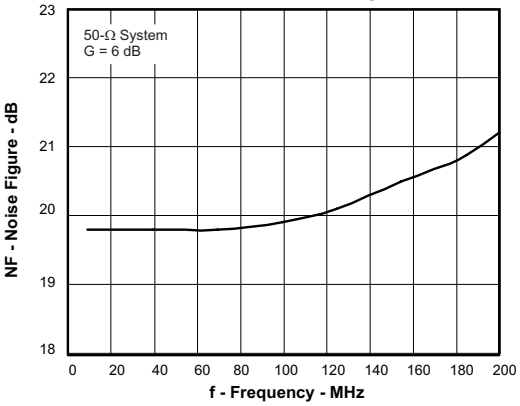

Figure 66.

CM SMALL-SIGNAL FREQUENCY RESPONSE

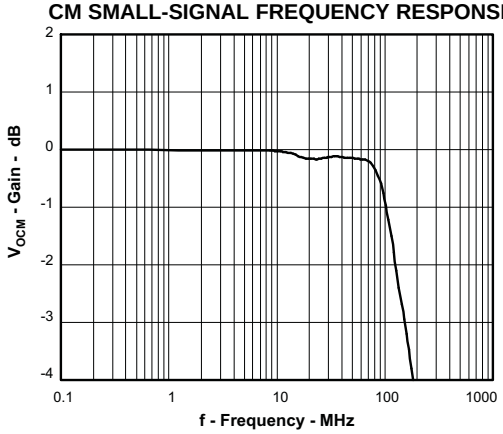

Figure 67.

CM INPUT IMPEDANCE vs FREQUENCY

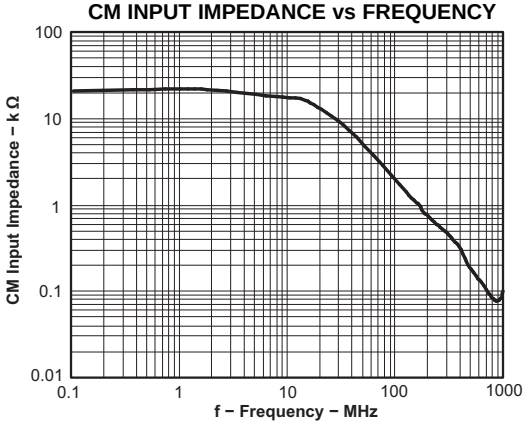

Figure 68.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3$ V (continued)

Test conditions at V_{S+} = +1.5 V, V_{S-} = –1.5V, CM = open, V_{OD} = 1 V_{PP}, R_F = 348 Ω, R_L = 200-Ω differential, G = 0 dB, single-ended input, and input and output referenced to midsupply, unless otherwise noted.

DIFFERENTIAL OUTPUT OFFSET VOLTAGE vs CM INPUT VOLTAGE

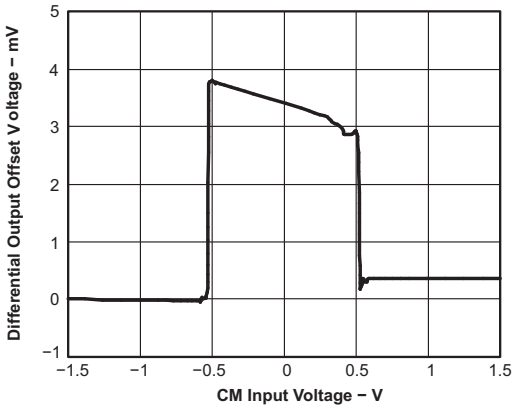

Figure 69.

OUTPUT COMMON-MODE OFFSET vs CM INPUT VOLTAGE

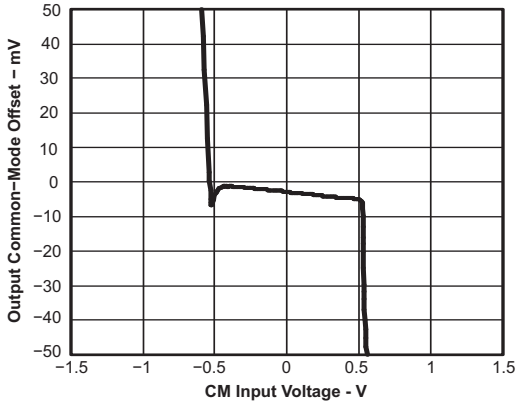

Figure 70.

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TEST CIRCUITS

The THS4513 is tested with the following test circuits built on the evaluation module (EVM). For simplicity, power-supply decoupling is not shown—see *Layout Recommendations* in the *Applications* section for recommendations. Depending on the test conditions, component values are changed per the following tables, or as otherwise noted. The signal generators used are ac-coupled, 50-Ω sources and a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input to balance the circuit. A split power supply is used to ease the interface to common test equipment, but the amplifier can be operated single-supply as described in the applications section with no impact on performance.

Table 1. Gain Component Values

GAIN	R_F	R_G	R_{IT}
0 dB	348 Ω	340 Ω	56.2 Ω
6 dB	348 Ω	165 Ω	61.9 Ω

Note the gain setting includes 50-Ω source impedance. Components are chosen to achieve gain and 50-Ω input termination.

Table 2. Load Component Values

R_L	R_O	R_{OT}	Atten.
100 Ω	25 Ω	Open	6 dB
200 Ω	86.6 Ω	69.8 Ω	16.8 dB
499 Ω	237 Ω	56.2 Ω	25.5 dB
1k Ω	487 Ω	52.3 Ω	31.8 dB

Note the total load includes 50-Ω termination by the test equipment. Components are chosen to achieve load and 50-Ω line termination through a 1:1 transformer.

Due to the voltage divider on the output formed by the load component values, the amplifier output is attenuated. The column *Atten* in Table 2 shows the attenuation expected from the resistor divider. When using a transformer at the output as shown in Figure 72, the signal will see slightly more loss, and these numbers will be approximate.

Frequency Response

The circuit shown in Figure 71 is used to measure the frequency response of the circuit.

A network analyzer is used as the signal source and as the measurement device. The output impedance of the network analyzer is 50 Ω. R_{IT} and R_G are chosen to impedance match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input.

The output is probed using a high-impedance differential probe across the 100-Ω resistor. The gain is referred to the amplifier output by adding back the 6-dB loss due to the voltage divider on the output.

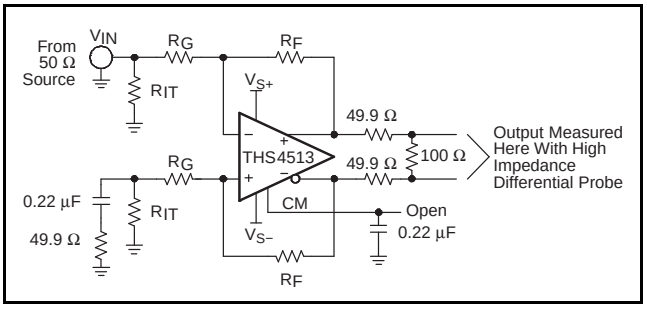

Figure 71. Frequency Response Test Circuit

Distortion and 1-dB Compression

The circuit shown in Figure 72 is used to measure harmonic distortion, intermodulation distortion, and 1-db compression point of the amplifier.

A signal generator is used as the signal source and the output is measured with a spectrum analyzer. The output impedance of the signal generator is 50 Ω. R_{IT} and R_G are chosen to impedance-match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input.

A low-pass filter is inserted in series with the input to reduce harmonics generated at the signal source. The level of the fundamental is measured, then a high-pass filter is inserted at the output to reduce the fundamental so that it does not generate distortion in the input of the spectrum analyzer.

The transformer used in the output to convert the signal from differential to single-ended is an ADT1-1WT. It limits the frequency response of the circuit so that measurements cannot be made below approximately 1 MHz.

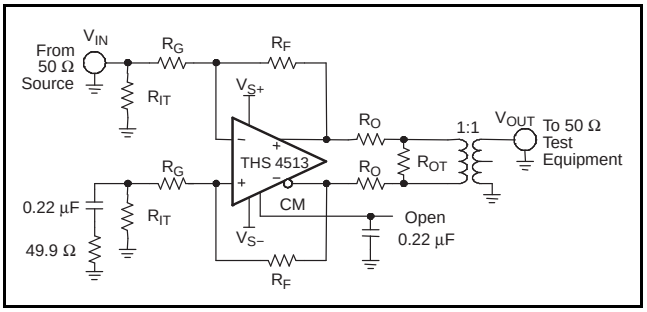

Figure 72. Distortion Test Circuit

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The 1-dB compression point is measured with a spectrum analyzer with 50-Ω double termination or 100-Ω termination; see Table 2. The input power is increased until the output is 1 dB lower than expected. The number reported in the table data is the power delivered to the spectrum analyzer input. Add 3 dB to refer to the amplifier output.

S-Parameter, Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive, Output Voltage, and Turn-On/Off Time

The circuit shown in Figure 73 is used to measure s-parameters, slew rate, transient response, settling time, output impedance, overdrive recovery, output voltage swing, and turn-on/turn-off times of the amplifier. For output impedance, the signal is injected at V_{OUT} with V_{IN} left open and the drop across the 49.9-Ω resistor is used to calculate the impedance seen looking into the amplifier output.

Because S_{21} is measured single-ended at the load with 50-Ω double termination, add 12 dB to refer to the amplifier's output as a differential signal.

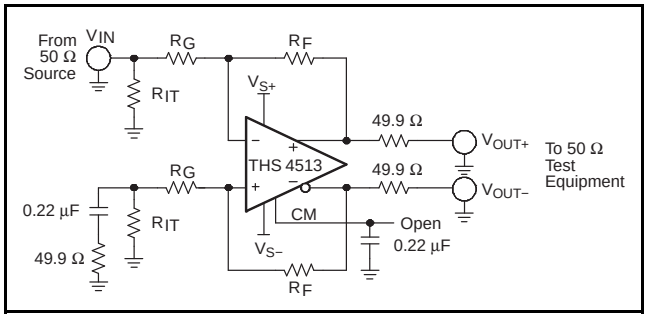

Figure 73. S-Parameter, SR, Transient Response, Settling Time, Z_O, Overdrive Recovery, V_{OUT} Swing, and Turn-On/Off Test Circuit

CM Input

The circuit shown in Figure 74 is used to measure the frequency response and input impedance of the CM input. Frequency response is measured single-ended at V_{OUT+} or $V_{OUT–}$ with the input injected at V_{IN}, R_{CM} = 0 Ω and R_{CMT} = 49.9 Ω. The input impedance is measured with R_{CM} = 49.9 Ω with R_{CMT} = open, and calculated by measuring the voltage drop across R_{CM} to determine the input current.

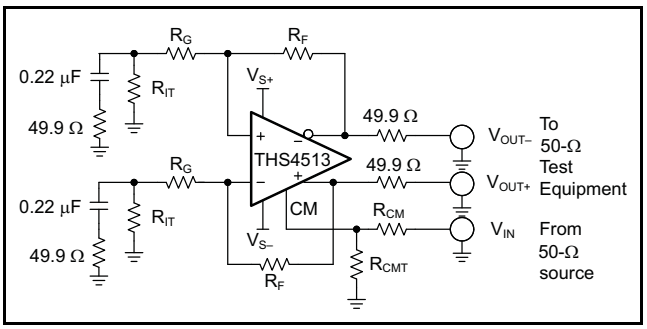

Figure 74. CM Input Test Circuit

CMRR and PSRR

The circuit shown in Figure 75 is used to measure the CMRR and PSRR of V_{S+} and $V_{S–}$. The input is switched appropriately to match the test being performed.

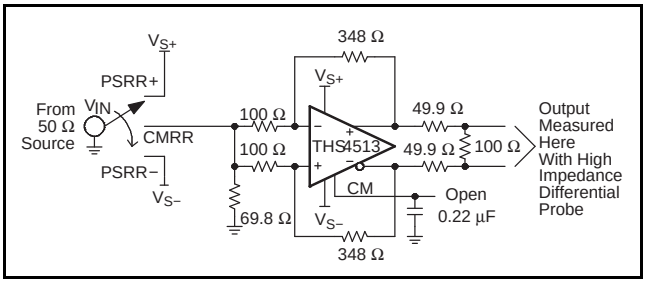

Figure 75. CMRR and PSRR Test Circuit

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APPLICATION INFORMATION

APPLICATIONS

The following circuits show application information for the THS4513. For simplicity, power-supply decoupling capacitors are not shown in these diagrams. Please see the *THS4513 EVM* section for recommendations. For more detail on the use and operation of fully-differential op amps refer to the application report, *Fully-Differential Amplifiers* (SLOA054).

Differential Input to Differential Output Amplifier

The THS4513 is a fully-differential op amp, and can be used to amplify differential input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 76 (CM input not shown). The gain of the circuit is set by R_F divided by R_G.

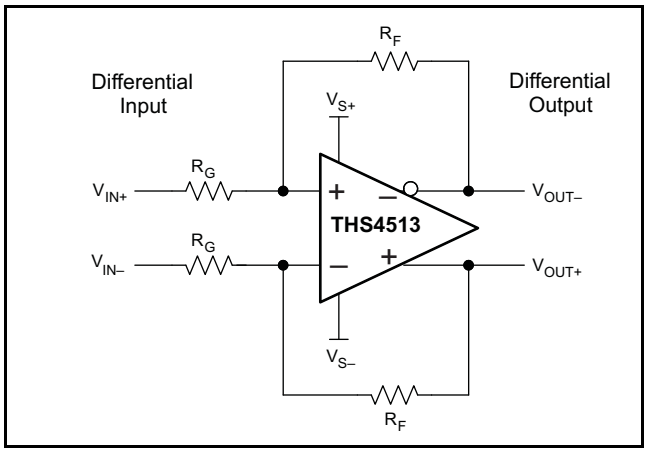

Figure 76. Differential Input to Differential Output Amplifier

Depending on the source and load, input and output termination can be accomplished by adding R_{IT} and R_O.

Single-Ended Input to Differential Output

Amplifier

The THS4513 can be used to amplify and convert single-ended input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 77 (CM input not shown). The gain of the circuit is again set by R_F divided by R_G.

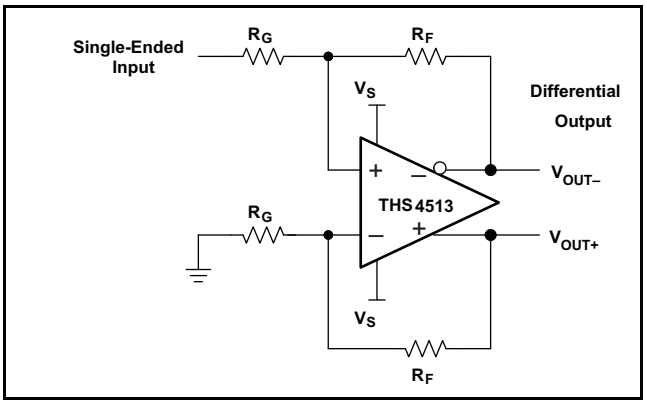

Figure 77. Single-Ended Input to Differential Output Amplifier

Input Common-Mode Voltage Range

The input common-model voltage of a fully differential op amp is the voltage at the '+' and '–' input pins of the op amp.

It is important to not violate the input common-mode voltage range (V_{ICR}) of the op amp. Assuming the op amp is in linear operation the voltage across the input pins is only a few millivolts at most. So finding the voltage at one input pin will determine the input common-mode voltage of the op amp.

Treating the negative input as a summing node, the voltage is given by Equation 1:

$$V_{IC} = \left(V_{OUT+} \times \frac{R_G}{R_G + R_F} \right) + \left(V_{IN-} \times \frac{R_F}{R_G + R_F} \right) \quad (1)$$

To determine the V_{ICR} of the op amp, the voltage at the negative input is evaluated at the extremes of V_{OUT+}.

As the gain of the op amp increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

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Setting the Output Common-Mode Voltage

The output common-mode voltage is set by the voltage at the CM pin(s). The internal common-mode control circuit maintains the output common-mode voltage within 3-mV offset (typ) from the set voltage, when set within 0.5 V of midsupply, with less than 4-mV differential offset voltage. If left unconnected, the common-mode set point is set to midsupply by internal circuitry, which may be over-driven from an external source. Figure 78 is representative of the CM input. The internal CM circuit has about 700 MHz of –3-dB bandwidth, which is required for best performance, but it is intended to be a dc bias input pin. Bypass capacitors are recommended on this pin to reduce noise at the output. The external current required to overdrive the internal resistor divider is given by Equation 2:

$$I_{EXT} = \frac{2V_{CM} - (V_{S+} - V_{S-})}{50\ k\Omega} \quad (2)$$

where V_{CM} is the voltage applied to the CM pin.

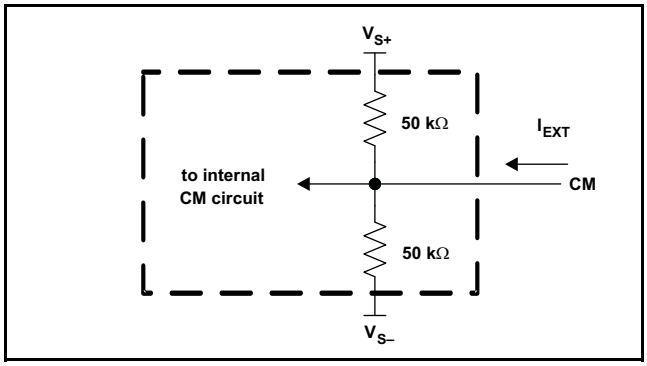

Figure 78. CM Input Circuit

Single-Supply Operation (3 V to 5 V)

To facilitate testing with common lab equipment, the THS4513 EVM allows split-supply operation, and the characterization data presented in this data sheet were taken with split-supply power inputs. The device can easily be used with a single-supply power input without degrading the performance. Figure 79, Figure 80, and Figure 81 show dc and ac-coupled single-supply circuits with single-ended inputs. These configurations all allow the input and output common-mode voltage to be set to midsupply allowing for optimum performance. The information presented here can also be applied to differential input sources.

In Figure 79, the signal source is referenced to a voltage derived from the CM pin via a unity-gain wideband buffer such as the BUF602. V_{CM} is set to midsupply by THS4513 internal circuitry. R_T along with the input impedance of the amplifier provides input termination, which is also referenced to V_{CM}.

Note that R_S and R_T are added to the alternate input from the signal input to balance the amplifier. Alternately, one resistor can be used equal to the combined value R_G+ R_S || R_T on this input. This technique is also true of the circuits shown in Figure 80 and Figure 81.

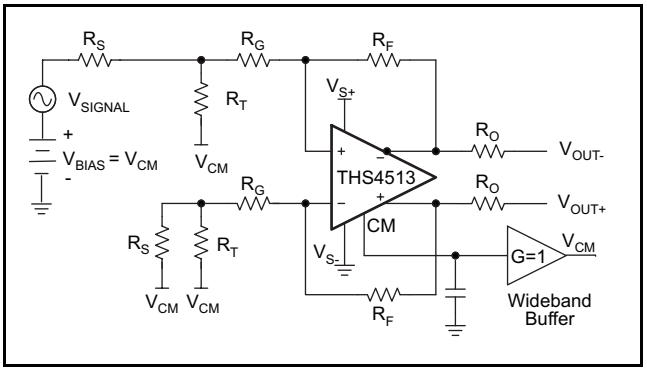

Figure 79. THS4513 DC-Coupled Single-Supply with Input Biased to V_{CM}

In Figure 80, the source is referenced to ground and so is the input termination resistor. R_{PU} is added to the circuit to avoid violating the V_{ICR} of the op amp. The proper value of resistor to add can be calculated from Equation 3:

$$R_{PU} = \frac{(V_{IC} - V_{S+})}{V_{CM}\left(\frac{1}{R_F}\right) - V_{IC}\left(\frac{1}{R_{IN}} + \frac{1}{R_F}\right)} \quad (3)$$

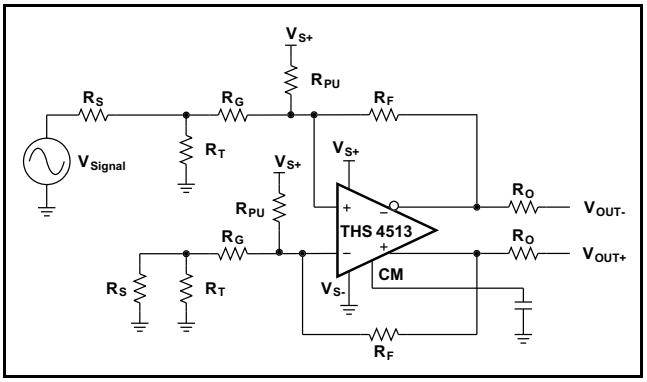

Figure 80. THS4513 DC-Coupled Single-Supply with R_{PU} Used to Set V_{IC}

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V_{IC} is the desired input common-mode voltage, V_{CM} = CM, and R_{IN} = R_G+ R_S || R_T. To set to midsupply, make the value of R_{PU} = R_G+ R_S || R_T.

Table 3 is a modification of Table 1 to add the proper values with R_{PU} assuming a 50-Ω source impedance and setting the input and output common-mode voltage to midsupply.

There are two drawbacks to this configuration. One is that it requires additional current from the power supply. Using the values shown for a gain of 0 dB requires 14 mA more current with 5-V supply, and 8.2 mA more current with 3-V supply.

The other drawback is that this configuration also increases the noise gain of the circuit. In the 10-dB gain case, noise gain increases by a factor of 1.5.

Table 3. R_{PU} Values for Various Gains

Gain	R_F	R_G	R_{IT}	R_{PU}
0 dB	348 Ω	340 Ω	56.2 Ω	365 Ω
6 dB	348 Ω	168 Ω	64.9 Ω	200 Ω

Figure 81 shows ac-coupling to the source. Using capacitors in series with the termination resistors allows the amplifier to self-bias both input and output to midsupply.

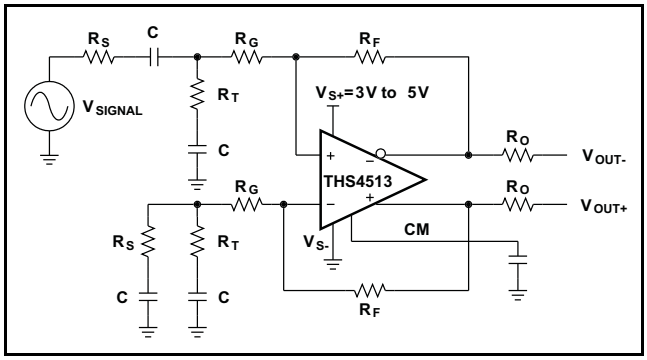

Figure 81. THS4513 AC-Coupled Single-Supply

Low-Pass Filter

One application for the THS4513 is as a unity-gain buffer with low-pass filtering. Figure 82 shows a circuit that is driven by an ac-coupled 50-Ω source. A 1:1 transformer converts the differential output of the THS4513 into a single-ended output capable of driving 50-Ω test equipment. The circuit as shown has an overall gain of –6 dB due to the voltage divider on the device output, and has a roll-off frequency of approximately 60 MHz. The measured gain versus frequency response of the overall circuit is shown in Figure 83. The low-frequency roll-off is due to losses in the output transformer at those frequencies.

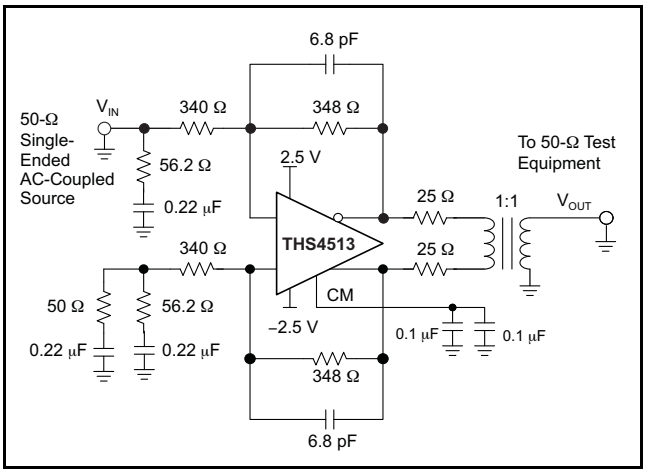

Figure 82. 60-MHz Low-Pass Filter

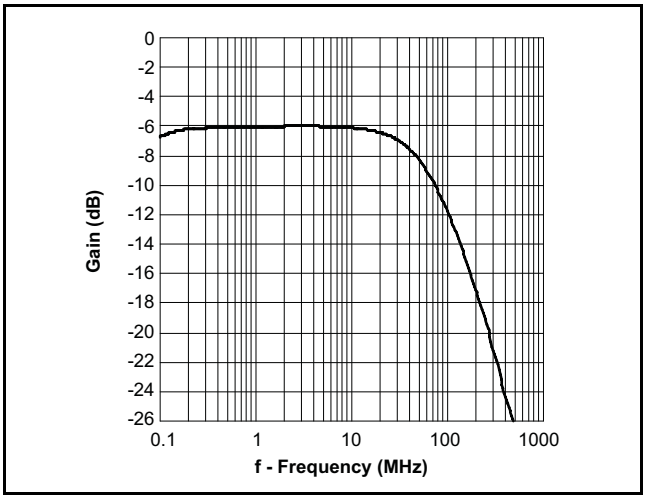

Figure 83. Low-Pass Filter Measured Frequency Response

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THS4513 and ADS5500 Combined Performance

The THS4513 is designed to be a high-performance drive amplifier for high-performance data converters like the ADS5500 14-bit 125-MSPS ADC. Figure 84 shows a circuit combining the two devices. The THS4513 amplifier circuit provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5500. The 100-Ω resistors and 2.7-pF capacitor between the THS4513 outputs and ADS5500 inputs along with the input capacitance of the ADS5500 limit the bandwidth of the signal to 115 MHz (–3 dB). For testing, a signal generator is used for the signal source. The generator is an ac-coupled 50-Ω source. A band-pass filter is inserted in series with the input to reduce harmonics and noise from the signal source. Input termination is accomplished via the 69.8-Ω resistor and 0.22-µF capacitor to ground in conjunction with the input impedance of the amplifier circuit. A 0.22-µF capacitor and 49.9-Ω resistor is inserted to ground across the 69.8-Ω resistor and 0.22-µF capacitor on the alternate input to balance the circuit. Gain is a function of the source impedance, termination, and 348-Ω feedback resistor. Refer to Table 3 for component values to set proper 50-Ω termination for other common gains. A split power supply of +4 V and –1 V is used to set the input and output common-mode voltages to approximately midsupply while setting the input common-mode of the ADS5500 to the recommended +1.55 V. This configuration maintains maximum headroom on the internal transistors of the THS4513 to ensure optimum performance.

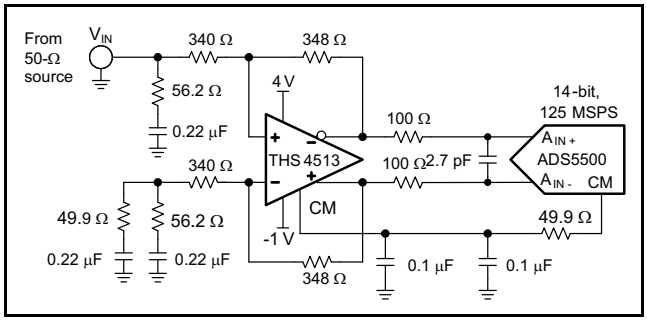

Figure 84. THS4513 and ADS5500 Circuit

Figure 85 shows the two-tone FFT of the THS4513 and ADS5500 circuit with 65 MHz and 70 MHz input frequencies. The SFDR is 90 dBc.

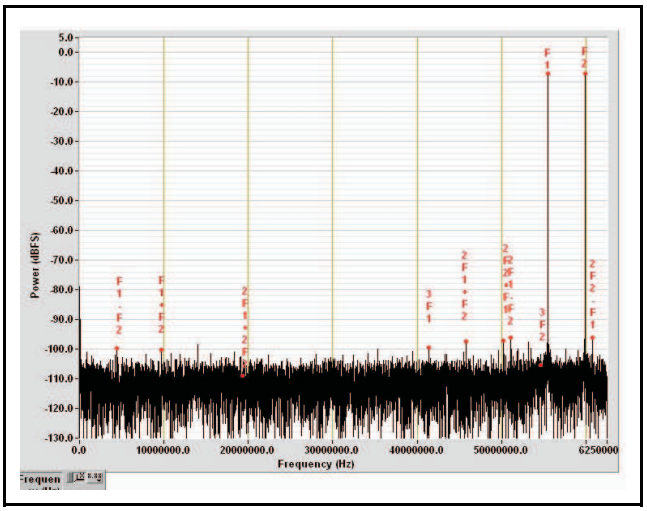

Figure 85. THS4513 and ADS5500 2-Tone FFT with 65-MHz and 70-MHz Inputs

THS4513 and ADS5424 Combined Performance

Figure 86 shows the THS4513 driving the ADS5424 ADC.

As before, the THS4513 amplifier provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5424. Input termination and circuit testing is the same as described above for the THS4513 and ADS5500 circuit.

The 225-Ω resistors and 2.7-pF capacitor between the THS4513 outputs and ADS5424 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 100 MHz (–3 dB).

Since the ADS5424 recommended input common-mode voltage is 2.4 V, the THS4513 is operated from a single power-supply input with V_{S+} = 5 V and V_{S-} = 0 V (ground).

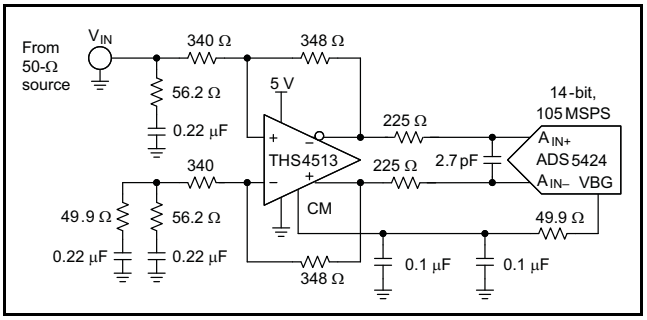

Figure 86. THS4513 and ADS5424 Circuit

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Layout Recommendations

It is recommended to follow the layout of the external components near the amplifier, ground plane construction, and power routing of the EVM as closely as possible. General guidelines are:

1. Signal routing should be direct and as short as possible into and out of the op amp circuit.
2. The feedback path should be short and direct; avoid vias.
3. Ground or power planes should be removed from directly under the amplifier input and output pins.
4. An output resistor is recommended on each output, as near to the output pin as possible.
5. Two 10-µF and two 0.1-µF power-supply decoupling capacitors should be placed as near to the power-supply pins as possible.
6. Two 0.1-µF capacitors should be placed between the CM input pins and ground. This configuration limits noise coupled into the pins. One each should be placed to ground near pin 4 and pin 9.
7. It is recommended to split the ground panel on layer 2 (L2) as shown below and to use a solid ground on layer 3 (L3). A single-point connection should be used between each split section on L2 and L3.
8. A single-point connection to ground on L2 is recommended for the input termination resistors R1 and R2. This configuration should be applied to the input gain resistors if termination is not used.
9. The recommended printed circuit board (PCB) footprint for the THS4513 is shown in the Land Pattern of Figure 88.

PowerPAD™ DESIGN CONSIDERATIONS

The THS4513 is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe on which the die is mounted (see Figure 87a and Figure 87b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package (see Figure 87c). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

Note that the THS4513 has no electrical connection between the PowerPAD and circuitry on the die. Connecting the PowerPAD to any potential voltage between V_{S+} and V_{S-} is acceptable. It is most important that it be connected for maximum heat dissipation.

The PowerPAD package allows both assembly and thermal management in one manufacturing operation.

During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface-mount with the previously awkward mechanical methods of heatsinking.

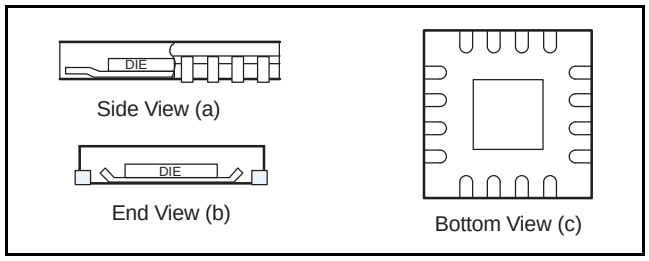

Figure 87. Views of Thermally-Enhanced Package

PowerPAD PCB LAYOUT CONSIDERATIONS

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

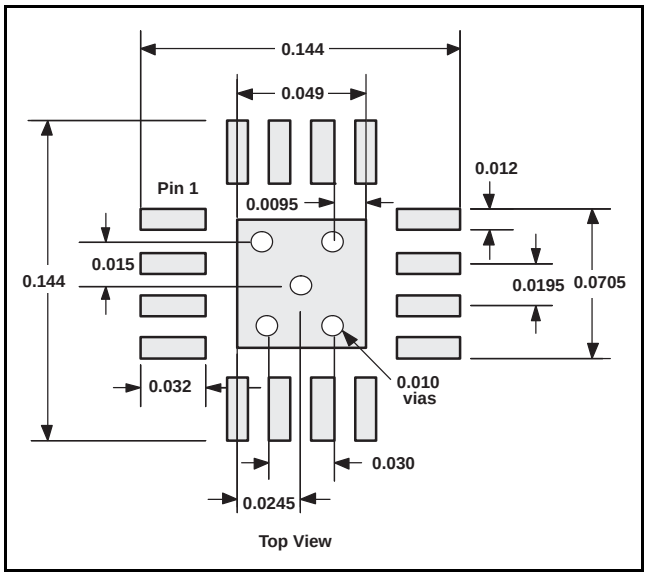

Figure 88. PowerPAD PCB Etch and Via Pattern

1. Prepare the PCB with a top side etch pattern as shown in Figure 88. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. The holes should be 13 mils (0.013 in, 0.33 mm) in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. They help dissipate the heat generated by the IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered, so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This resistance makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the IC PowerPAD package should make the connection to the internal ground plane, with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This configuration prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This process results in a part that is properly installed.

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multi-amplifier devices. Because these devices have linear output stages (Class AB), most of the heat dissipation is at low output voltages with high output currents.

The other key factor when dealing with power dissipation is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. For a single package, the sum of the RMS output currents and voltages should be used to choose the proper package.

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THS4513 EVM

Figure 89 is the THS4513 EVAL1 EVM schematic; layers 1 through 4 of the PCB are shown Figure 91, and Table 4 is the bill of materials for the EVM as supplied from TI.

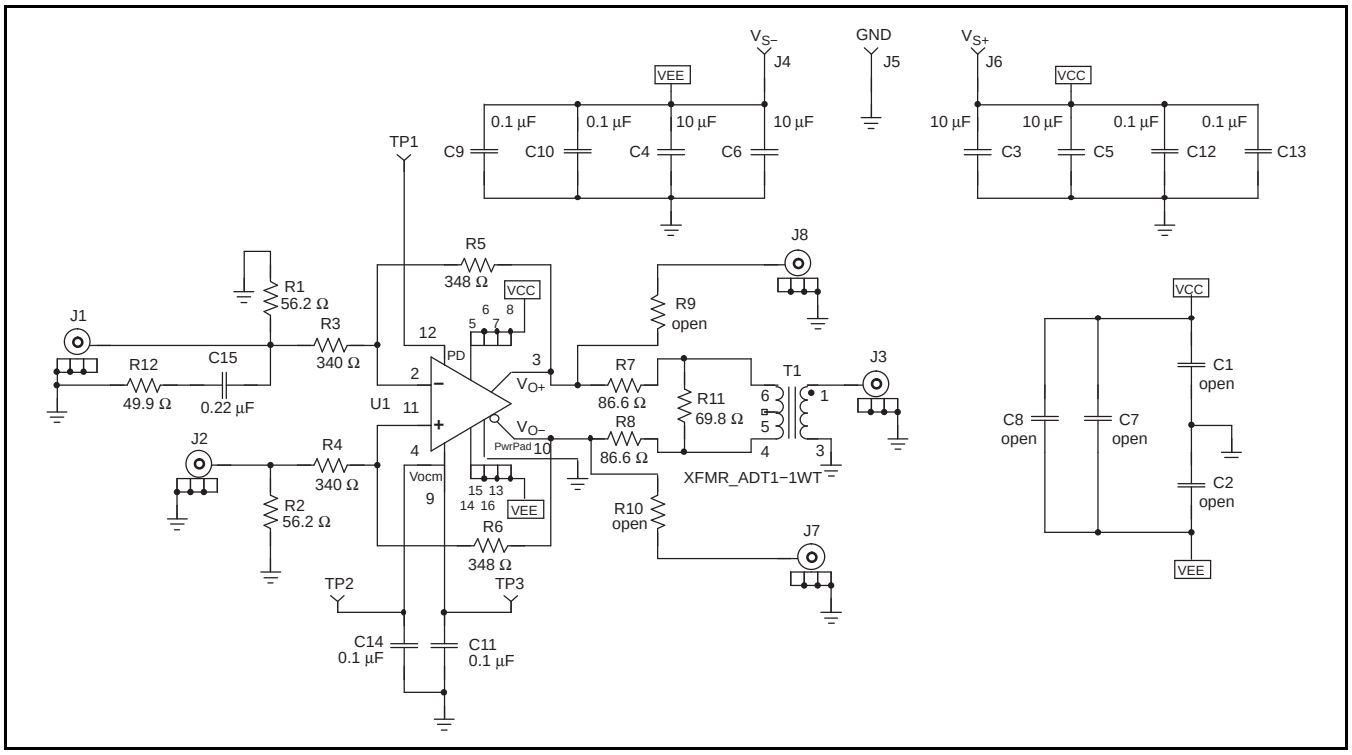

Figure 89. THS4513 EVAL1 EVM Schematic

Figure 90.

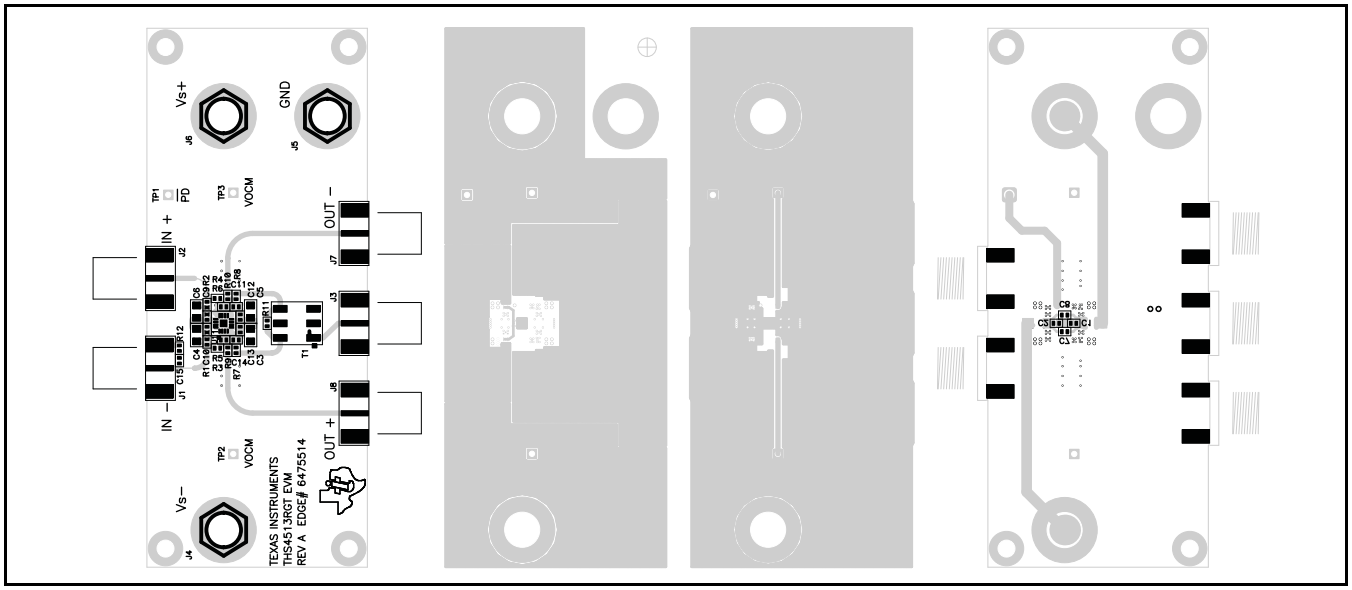

Figure 91. THS4513 EVAL1 EVM Layer 1 through Layer 4

Table 4. THS4513 EVAL1 EVM Bill of Materials

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	PCB QTY	MANUFACTURER PART NUMBER
1	CAP, 10.0 µF, Ceramic, X5R, 6.3 V	0805	C3, C4, C5, C6	4	(AVX) 08056D106KAT2A
2	CAP, 0.1 µF, Ceramic, X5R, 10 V	0402	C9, C10, C11, C12, C13, C14	6	(AVX) 0402ZD104KAT2A
3	CAP, 0.22 µF, Ceramic, X5R, 6.3 V	0402	C15	1	(AVX) 04026D224KAT2A
4	OPEN	0402	C1, C2, C7, C8	4	
5	OPEN	0402	R9, R10	2	
6	Resistor, 49.9 Ω, 1/16 W, 1%	0402	R12	1	(KOA) RK73H1ETTP49R9F
7	Resistor, 56.2 Ω, 1/16 W, 1%	0402	R1, R2	2	(KOA) RK73H1ETTP56R2F
8	Resistor, 69.8 Ω, 1/16 W, 1%	0402	R11	1	(KOA) RK73H1ETTP69R8F
9	Resistor, 86.6 Ω, 1/16 W, 1%	0402	R7, R8	2	(KOA) RK73H1ETTP86R6F
10	Resistor, 340 Ω, 1/16 W, 1%	0402	R3, R4	2	(KOA) RK73H1ETTP3400F
11	Resistor, 348 Ω, 1/16 W, 1%	0402	R5, R6	2	(KOA) RK73H1ETTP3480F
12	Transformer, RF		T1	1	(MINI-CIRCUITS) ADT1-1WT
13	Jack, banana receptance, 0.25" diameter hole		J4, J5, J6	3	(HH SMITH) 101
14	OPEN		J1, J7, J8	3	
15	Connector, edge, SMA PCB Jack		J2, J3	2	(JOHNSON) 142-0701-801
16	Test point, Red		TP1, TP2, TP3	3	(KEYSTONE) 5000
17	IC, THS4513		U1	1	(TI) THS4513RGT
18	Standoff, 4-40 HEX, 0.625" length			4	(KEYSTONE) 1808
19	SCREW, PHILLIPS, 4-40, 0.250"			4	SHR-0440-016-SN
20	Printed circuit board			1	(TI) EDGE# 6475514

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (September 2009) to Revision E **Page**

- Changed R_G and R_{IT} values in Table 1 23

Changes from Revision C (May 2008) to Revision D **Page**

- Changed title of *Typical Characteristics:* $V_{S+} - V_{S-} = 5$ *V* 8
- Deleted conditions from *Typical Characteristics:* $V_{S+} - V_{S-} = 5$ *V* table of graphs 8
- Changed title of *Typical Characteristics:* $V_{S+} - V_{S-} = 3$ *V* 16
- Deleted conditions from *Typical Characteristics:* $V_{S+} - V_{S-} = 3$ *V* table of graphs 16
- Changed item 9 of the *Layout Recommendations* 29
- Added the *PowerPAD Design Considerations* section 29
- Added the *PowerPAD PCB Layout Considerations* section 30
- Moved Figure 88 and associated sentence to beginning of *PowerPAD PCB Layout Considerations* section 30

Changes from Revision B (November 2006) to Revision C **Page**

- Updated document format 1
- Added Related Products table 1
- Added footnote 1 to Absolute Maximum Ratings table 2
- Added V (volts) to unit column of ESD ratings rows in Absolute Maximum Ratings table 2
- Changed $V_{S+} - V_{S-} = 5$ V *Input* specifications from 1.75 V typ (common-mode input range high) to 1.4 V typ; –1.75 V (common-mode input range low) to –1.4 V; 1.67 MΩ || 1.32 pF (differential input impedance) to 1.3 MΩ || 1.8 pF; 1.2 MΩ || 1.45 pF (common-mode input impedance) to 1.0 MΩ || 2.3 pF 3
- Added V (volts) to unit column of second *differential output voltage swing* row in *Output* section of $V_{S+} - V_{S-} = 5$ V specifications 3
- Changed $V_{S+} - V_{S-} = 3$ V *Input* specifications from 0.75 V typ (common-mode input range high) to 0.4 V typ; –0.75 V (common-mode input range low) to –0.4 V 5
- Added 1.3 MΩ || 1.8 pF (differential input impedance); 1.0 MΩ || 2.3 pF (common-mode input impedance) to $V_{S+} - V_{S-} = 3$ V *Input* specifications 5
- Changed y-axis of Figure 11 to match rest of curves 10
- Changed y-axis of Figure 12 to match rest of curves 10
- Added 1.0 at end of x-axis in Figure 23 12
- Changed last number in x-axis of Figure 46 from 100 to 1000 17
- Changed last number in y-axis of Figure 53 from 90 to 35 19

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4513RGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4513	Samples
THS4513RGTRG4	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4513	Samples
THS4513RGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4513	Samples
THS4513RGTTG4	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4513	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF THS4513 :

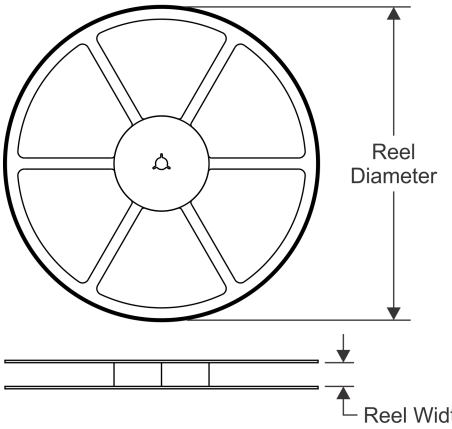
- Space: THS4513-SP

NOTE: Qualified Version Definitions:

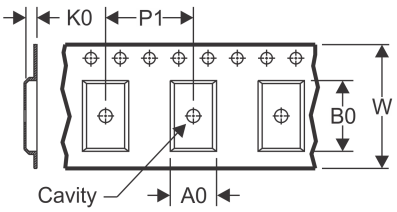
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

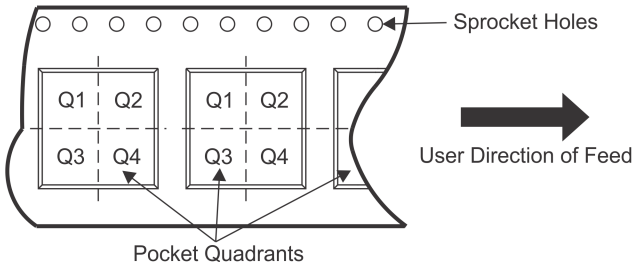


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

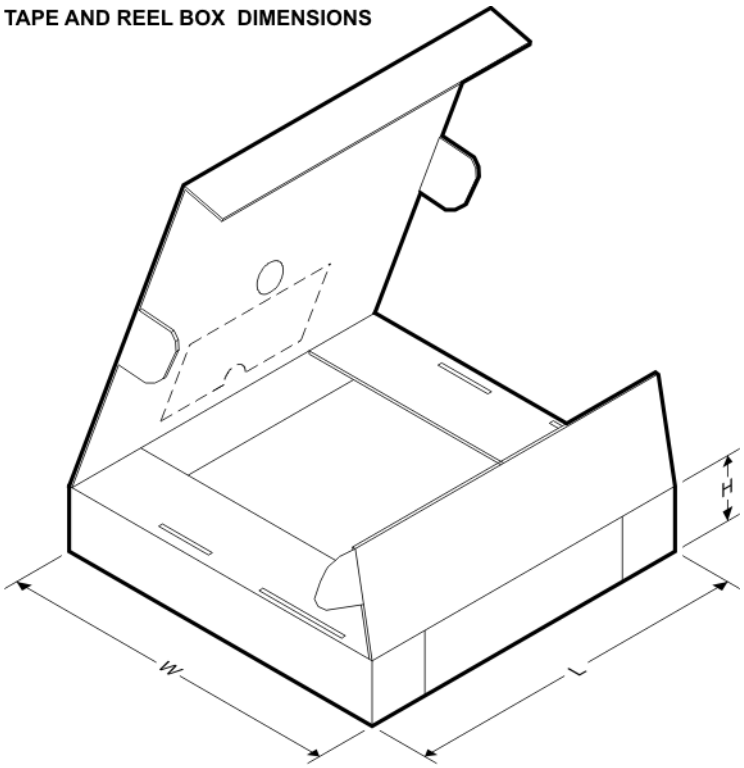
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4513RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THS4513RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

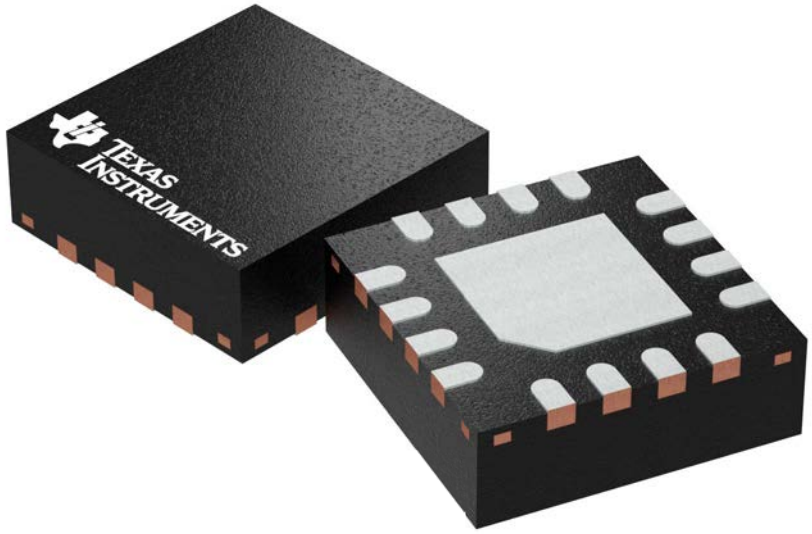
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4513RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
THS4513RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGT 16

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

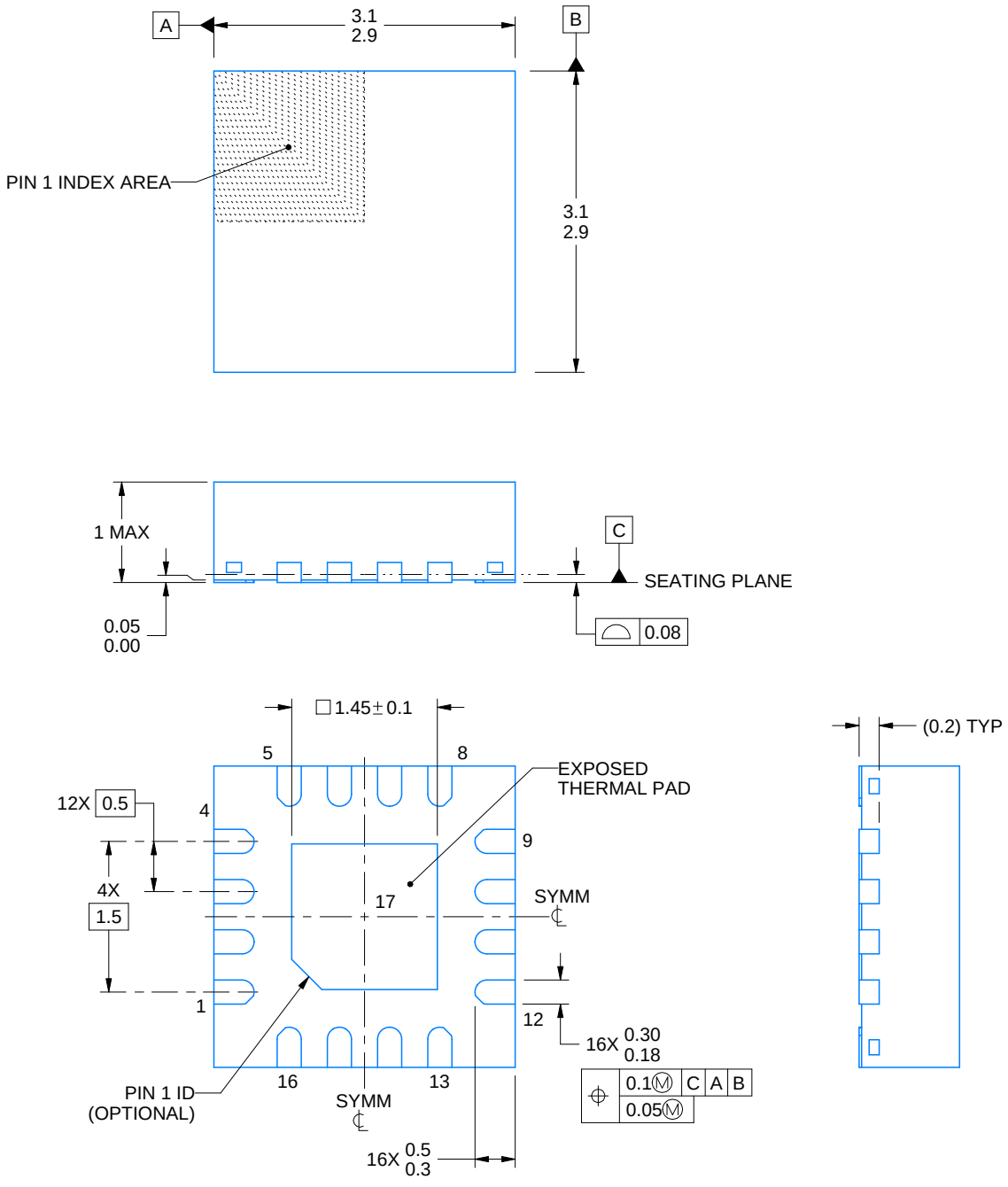
4203495/I

RGT0016A

PACKAGE OUTLINE

VQFN - 1 mm max height

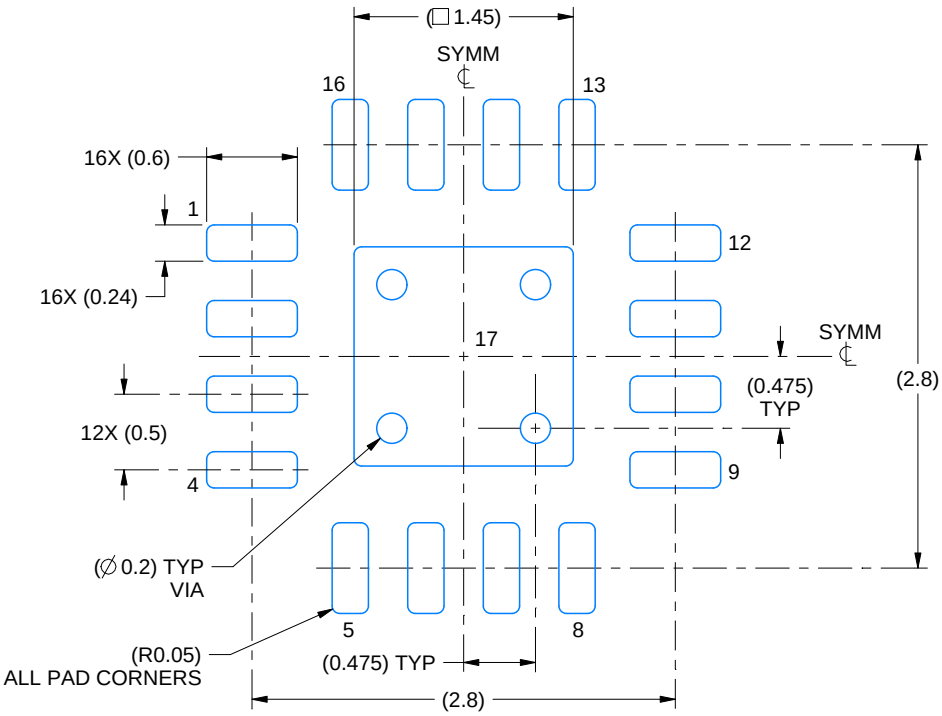
PLASTIC QUAD FLATPACK - NO LEAD



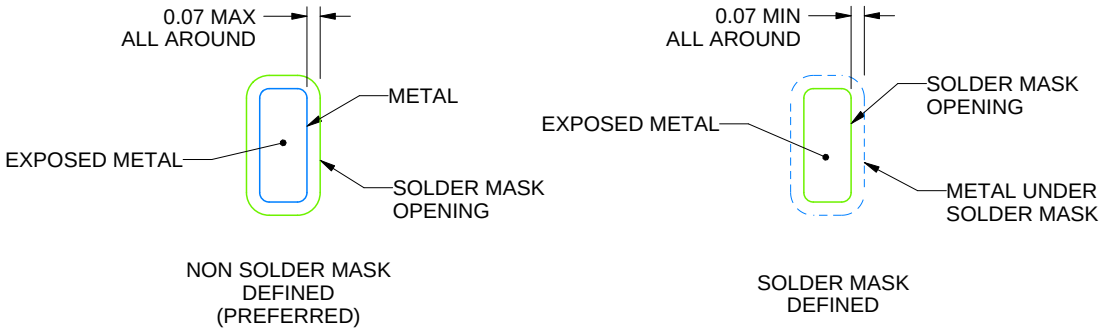
4219032/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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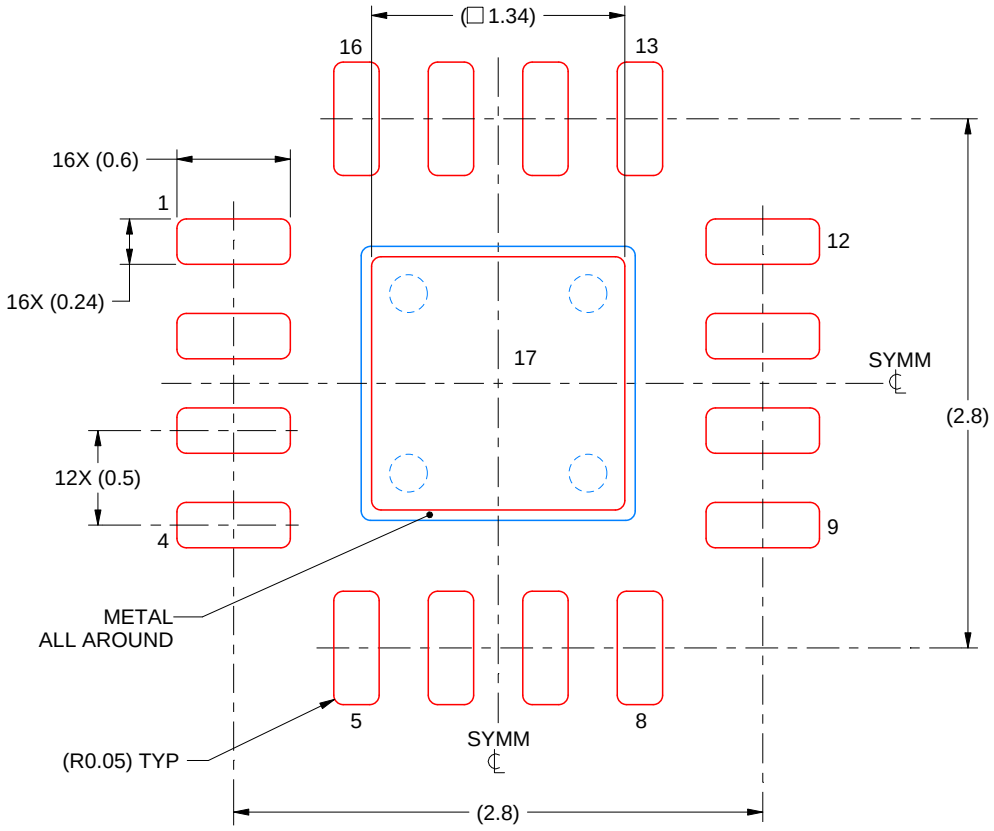
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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