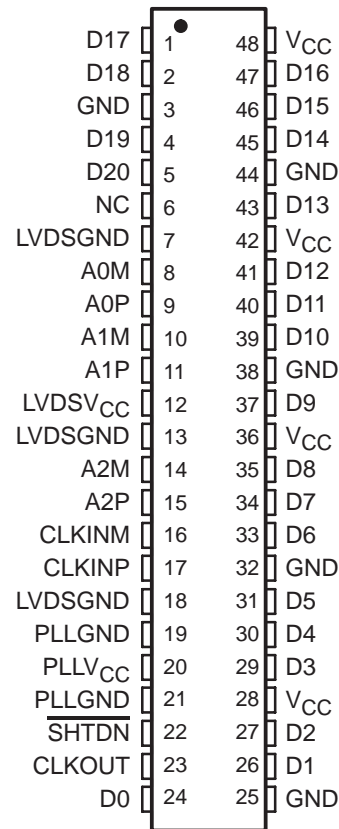


- **3:21 Data Channel Expansion at up to 178.5 Mbytes/s Throughput**
- **Suited for SVGA, XGA, or SXGA Display Data Transmission From Controller to Display With Very Low EMI**
- **Three Data Channels and Clock Low-Voltage Differential Channels In and 21 Data and Clock Low-Voltage TTL Channels Out**
- **Operates From a Single 3.3-V Supply**
- **Tolerates 4-kV HBM ESD**
- **Packaged in Thin Shrink Small-Outline Package (TSSOP) With 20-Mil Terminal Pitch**
- **Consumes Less Than 1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range of 31 MHz to 68 MHz**
- **No External Components Required for PLL**
- **Inputs Meet or Exceed the Standard Requirements of ANSI EIA/TIA-644 Standard**
- **Improved Replacement for the DS90C364 and SN75LVDS86**
- **Improved Jitter Tolerance**
- **See SN65LVDS86A-Q1 Data Sheet for Information About the Automotive Qualified Version**

DGG PACKAGE
(TOP VIEW)



NC – Not connected

description

The SN65LVDS86A/SN75LVDS86A FlatLink™ receiver contains three serial-in 7-bit parallel-out shift registers and four low-voltage differential signaling (LVDS) line receivers in a single integrated circuit. These functions allow receipt of synchronous data from a compatible transmitter, such as the SN75LVDS81, '83, '84, or '85, over four balanced-pair conductors and expansion to 21 bits of single-ended low-voltage LVTTTL synchronous data at a lower transfer rate.

When receiving, the high-speed LVDS data is received and loaded into registers at seven times the LVDS input clock (CLKIN) rate. The data is then unloaded to a 21-bit-wide LVTTTL parallel bus at the CLKIN rate. The 'LVDS86A presents valid data on the falling edge of the output clock (CLKOUT).

The 'LVDS86A requires only four line-termination resistors for the differential inputs and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only user intervention is the possible use of the shutdown/clear (SHTDN) active-low input to inhibit the clock and shut off the LVDS receivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

The SN75LVDS86A is characterized for operation over ambient free-air temperatures of 0°C to 70°C. The SN65LVDS86A is characterized for operation over the full Automotive temperature range of –40°C to 125°C.



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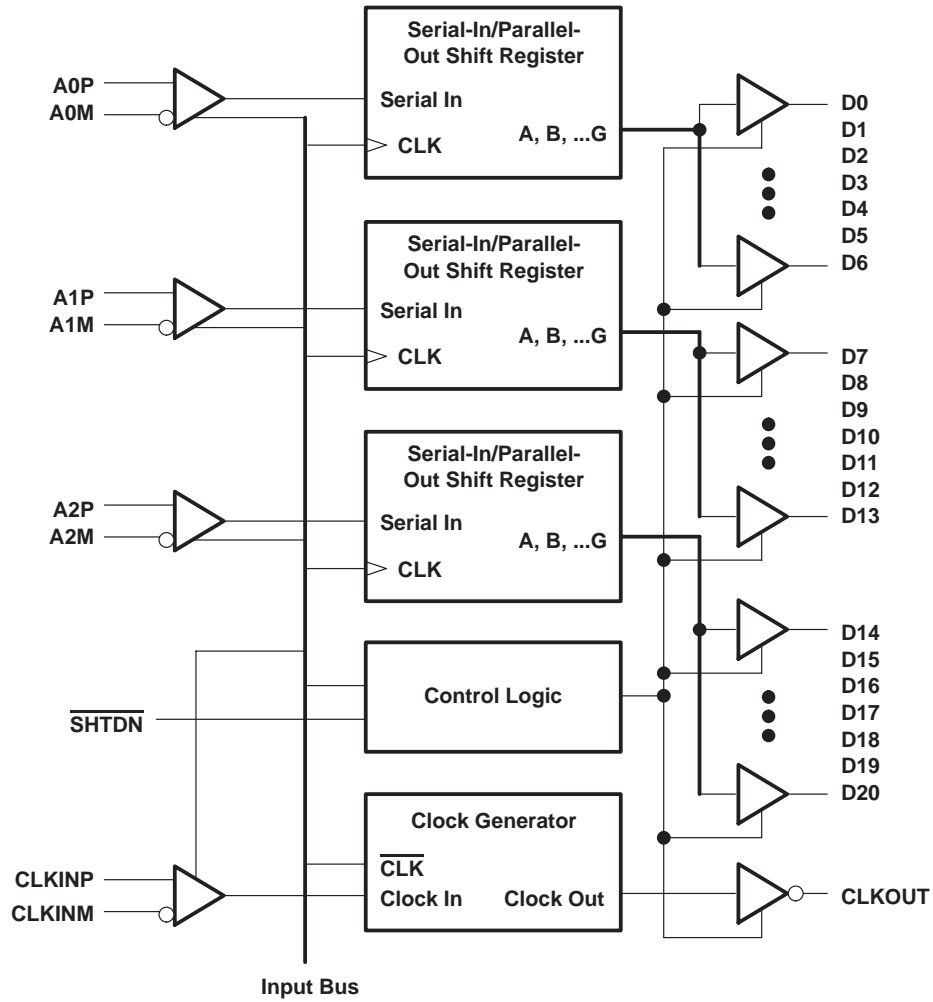
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SN65LVDS86A, SN75LVDS86A FlatLink™ RECEIVER

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functional block diagram



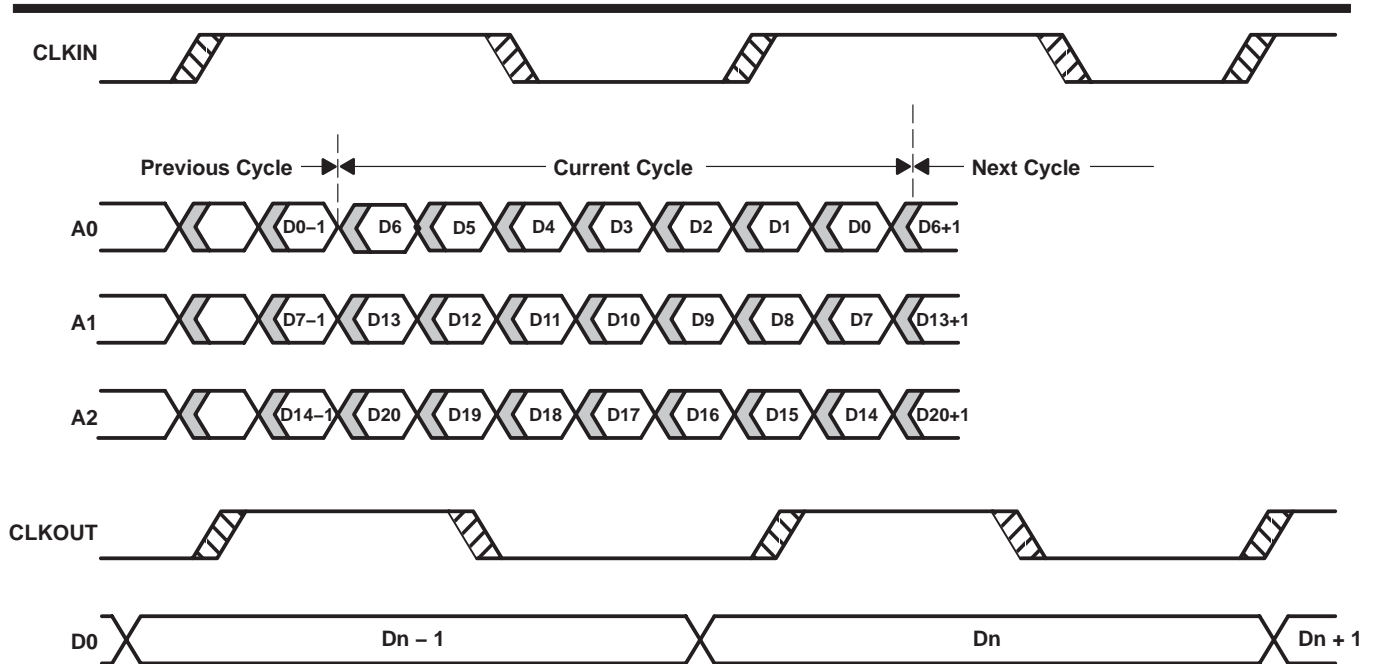
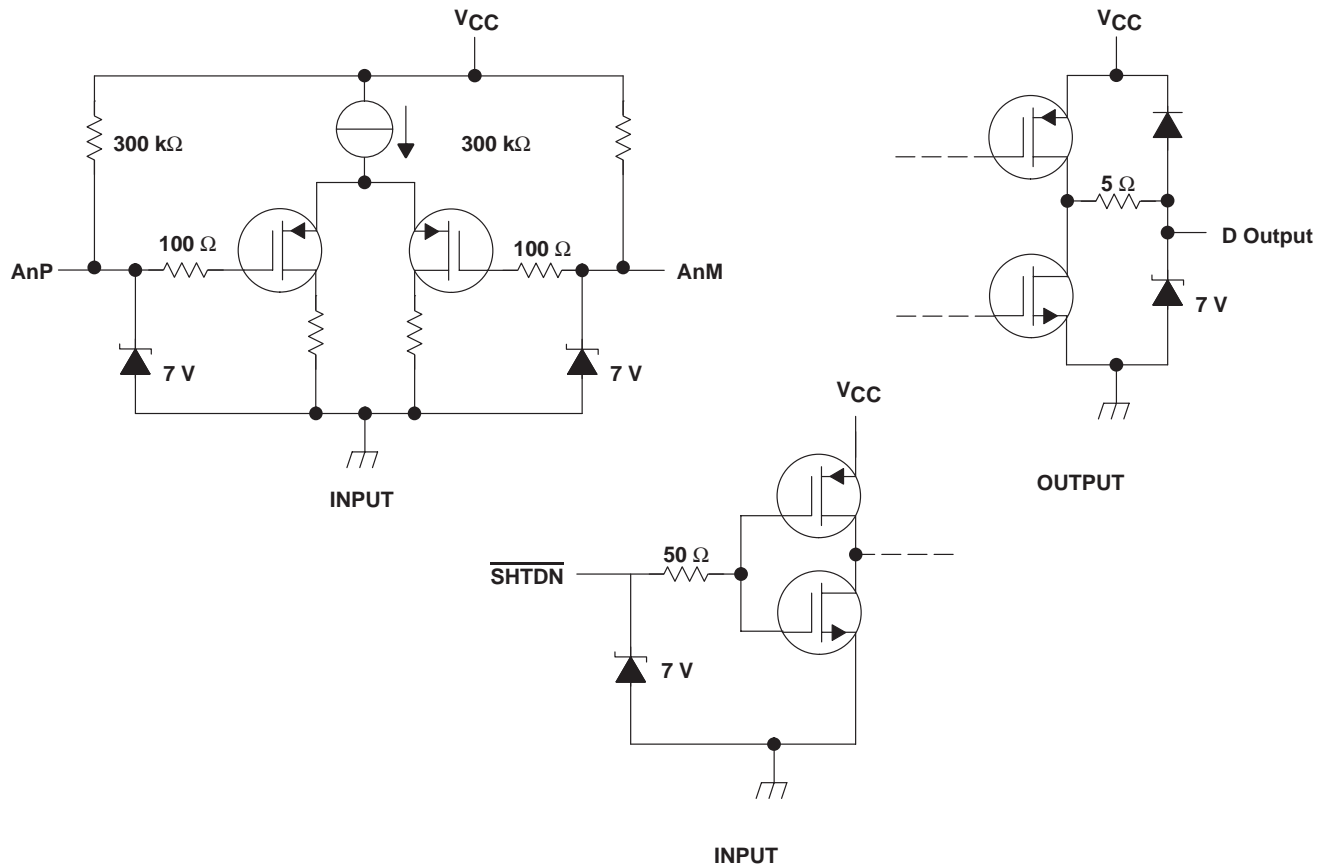


Figure 1. SN65LVDS86A/SN75LVDS86A Load and Shift Timing Sequences

equivalent input and output schematic diagrams



electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IT+}	Positive-going differential input threshold voltage				100	mV
V _{IT-}	Negative-going differential input threshold voltage‡		-100			mV
V _{OH}	High-level output voltage	I _{OH} = -4 mA	2.4			V
V _{OL}	Low-level output voltage	I _{OL} = 4 mA			0.4	V
I _{CC}	Quiescent current (average)	Disabled, All inputs to GND			280	μA
		Enabled, AnP = 1 V, AnM = 1.4 V, t _c = 15.38 ns		33	40	mA
		Enabled, C _L = 8 pF, Grayscale pattern (see Figure 3), t _c = 15.38 ns		43		
		Enabled, C _L = 8 pF, Worst-case pattern (see Figure 4) t _c = 15.38 ns		68		
I _{IH}	High-level input current ($\overline{\text{SHTDN}}$)	V _{IH} = V _{CC}			±20	μA
I _{IL}	Low-level input current ($\overline{\text{SHTDN}}$)	V _{IL} = 0	SN75LVDS86A		±20	μA
			SN65LVDS86A		±25	
I _I	Input current A inputs	0 ≤ V _I ≤ 2.4 V			±20	μA
I _{OZ}	High-impedance output current	V _O = 0 or V _{CC}			±10	μA

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going input voltage threshold only.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t _{su}	Setup time, D0–D20 to CLKOUT↓	C _L = 8 pF, See Figure 5	5			ns
t _h	Data hold time, CLKOUT↓ to D0–D20		5			ns
t _(RSKM)	Receiver input skew margin§ (see Figure 7)	t _c = 15.38 ns (±0.2%), Input clock jitter < 50 ps¶	550	700		ps
t _d	Delay time, CLKIN↑ to CLKOUT↓ (see Figure 7)	V _{CC} = 3.3 V, t _c = 15.38 ns (±0.2%), T _A = 25°C	3	5	7	ns
t _{en}	Enable time, $\overline{\text{SHTDN}}$ to phase lock	See Figure 7		1		ms
t _{dis}	Disable time, $\overline{\text{SHTDN}}$ to off state	See Figure 8		400		ns
t _t	Transition time, output (10% to 90% t _r or t _f) (data only)	C _L = 8 pF		3		ns
t _t	Transition time, output (10% to 90% t _r or t _f) (clock only)	C _L = 8 pF		1.5		ns
t _w	Pulse duration, output clock			0.50 t _c		ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

§ The parameter t_(RSKM) is the timing margin available to allocate to the transmitter and interconnection skews and clock jitter. The value of this parameter at clock periods other than 15.38 ns can be calculated from t_(RSKM) = t_c/14 – 550 ps.

¶ |Input clock jitter| is the magnitude of the change in input clock period.

PARAMETER MEASUREMENT INFORMATION

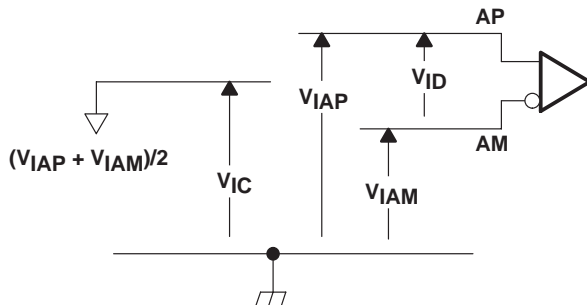
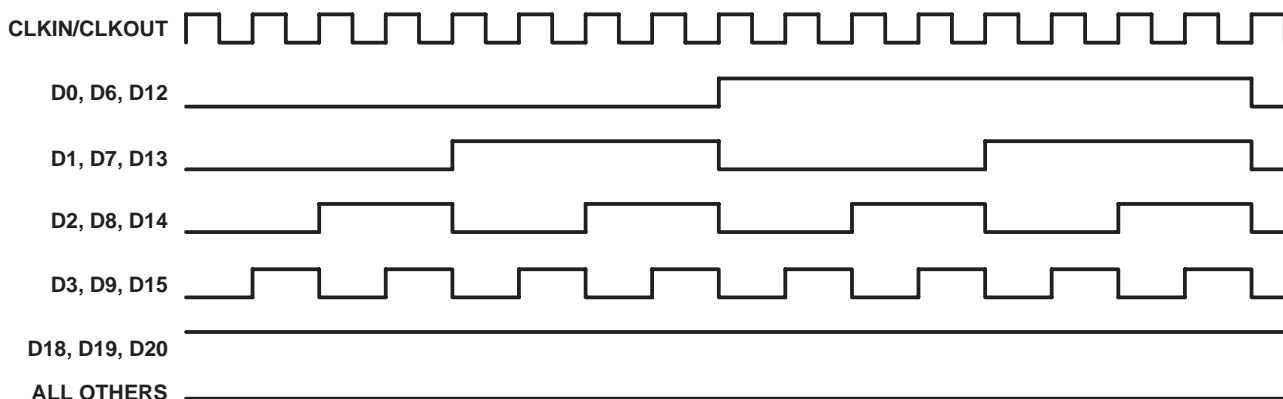
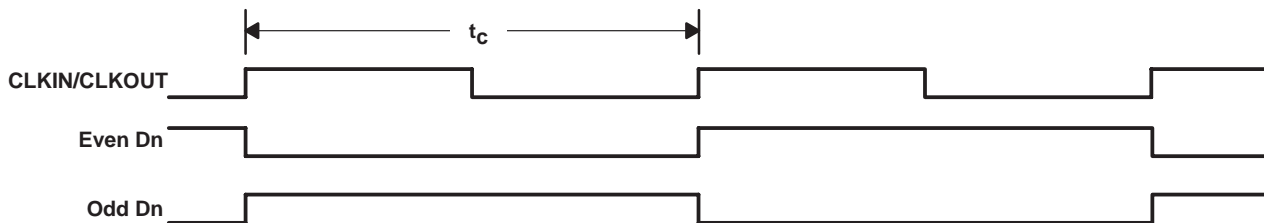


Figure 2. Voltage Definitions



NOTE A: The 16-grayscale test-pattern test device power consumption for a typical display pattern.

Figure 3. 16-Grayscale Test-Pattern Waveforms



NOTE A: The worst-case test pattern produces nearly the maximum switching frequency for all of the LVTTTL outputs.

Figure 4. Worst-Case Test-Pattern Waveforms

PARAMETER MEASUREMENT INFORMATION

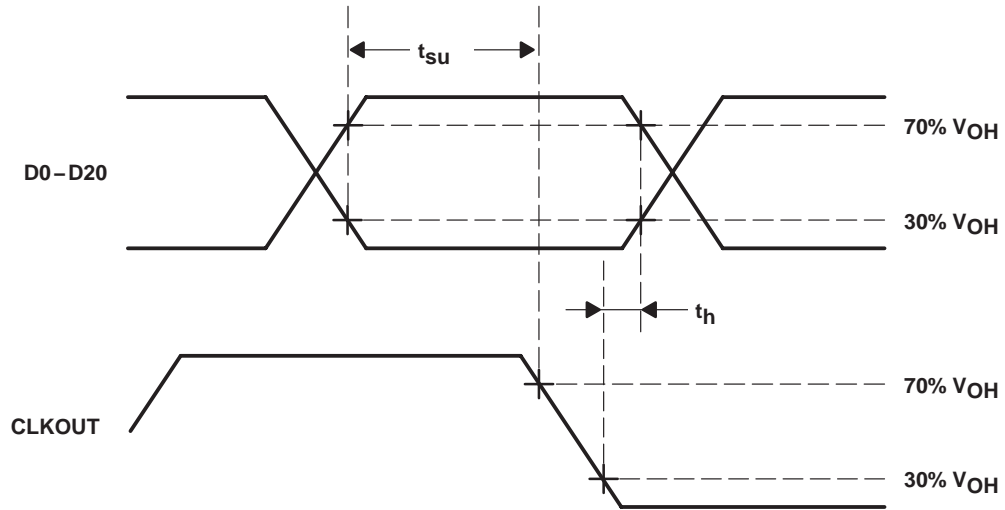
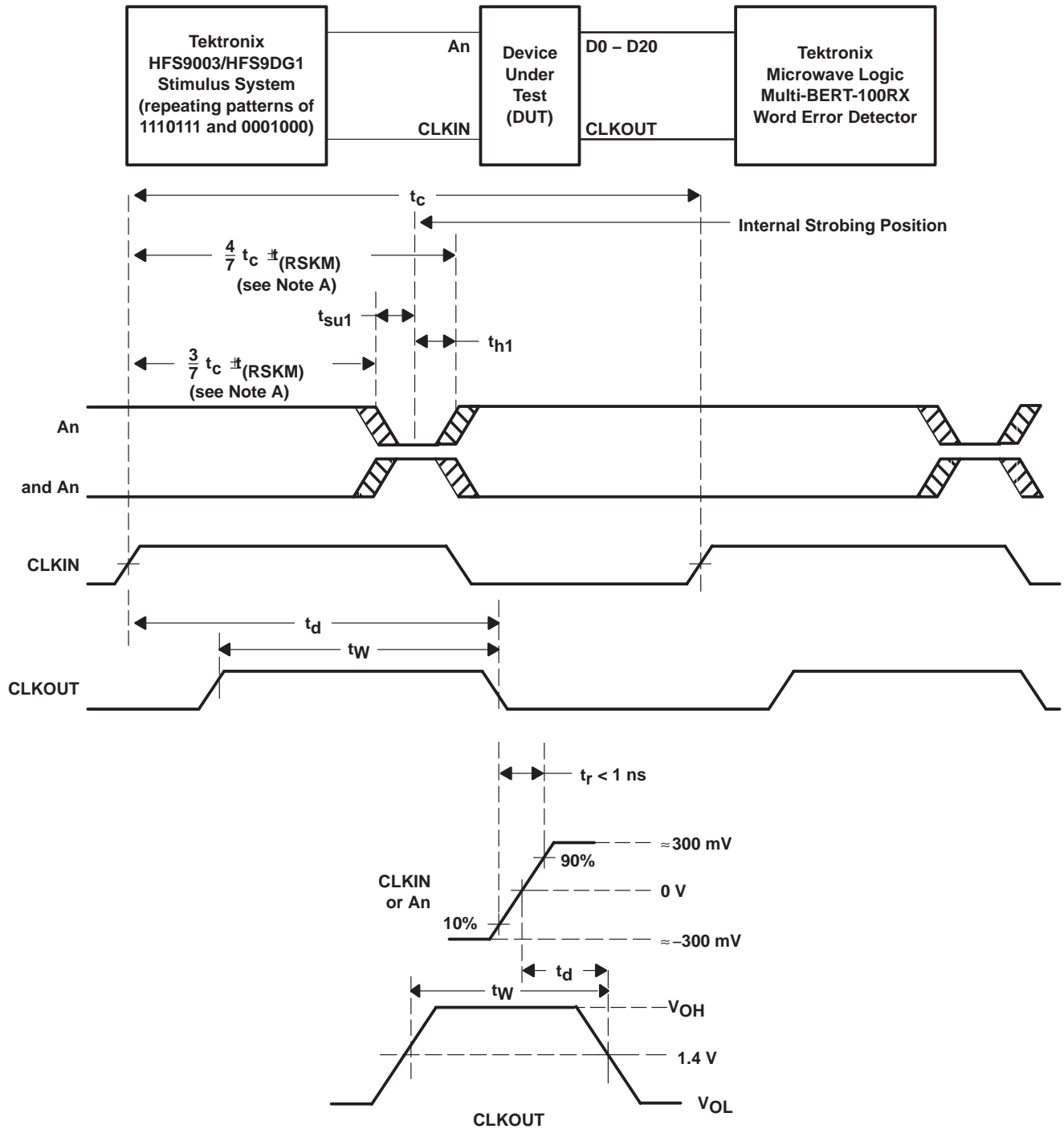


Figure 5. Setup and Hold Time Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: CLKIN is advanced or delayed with respect to data until errors are observed at the receiver outputs. The advance or delay is then reduced until there are no data errors observed. The magnitude of the advance or delay is t_{RSKM} .

Figure 6. Receiver Input Skew Margin, Setup/Hold Time, and Delay Time Definitions

PARAMETER MEASUREMENT INFORMATION

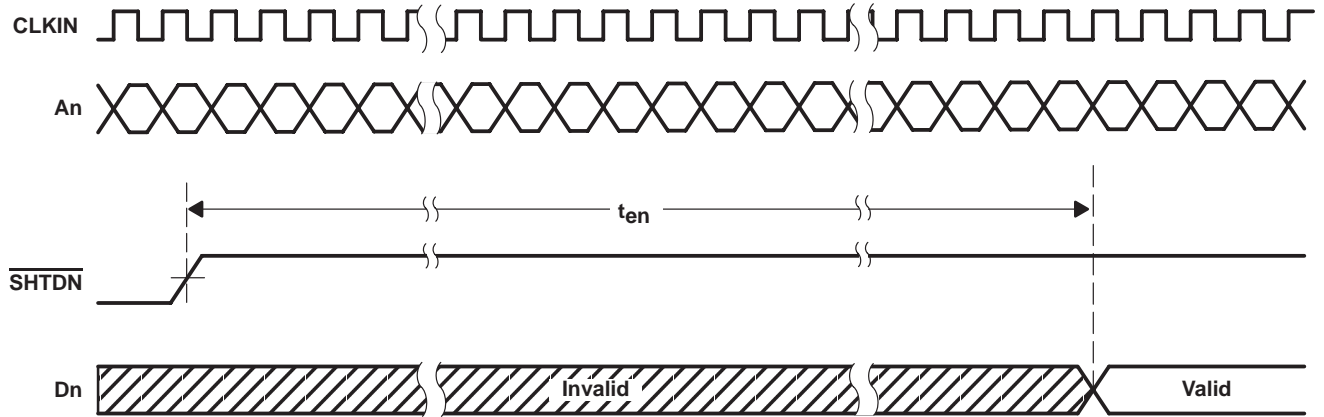


Figure 7. Enable Time Waveforms

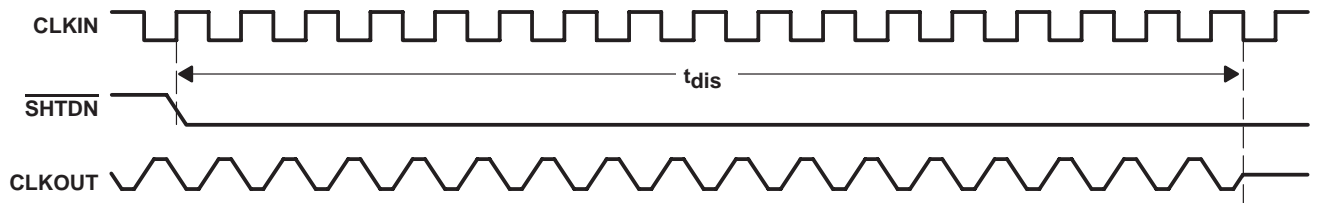


Figure 8. Disable Time Waveforms

TYPICAL CHARACTERISTICS

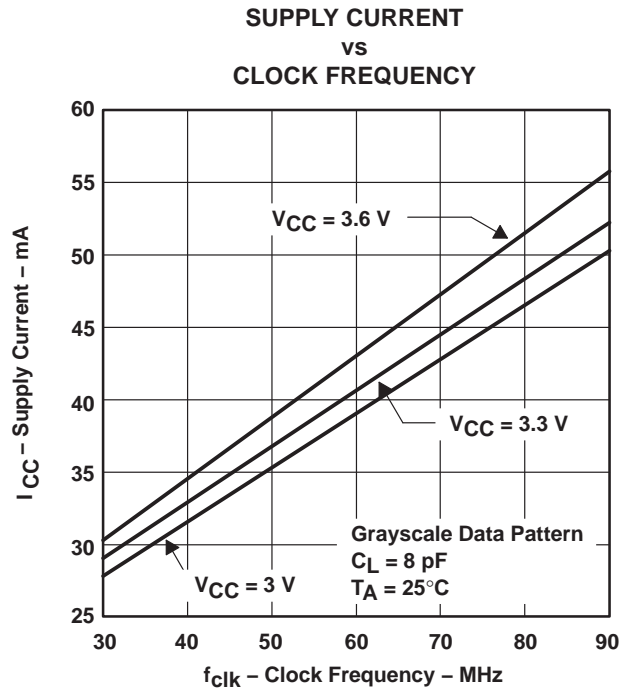
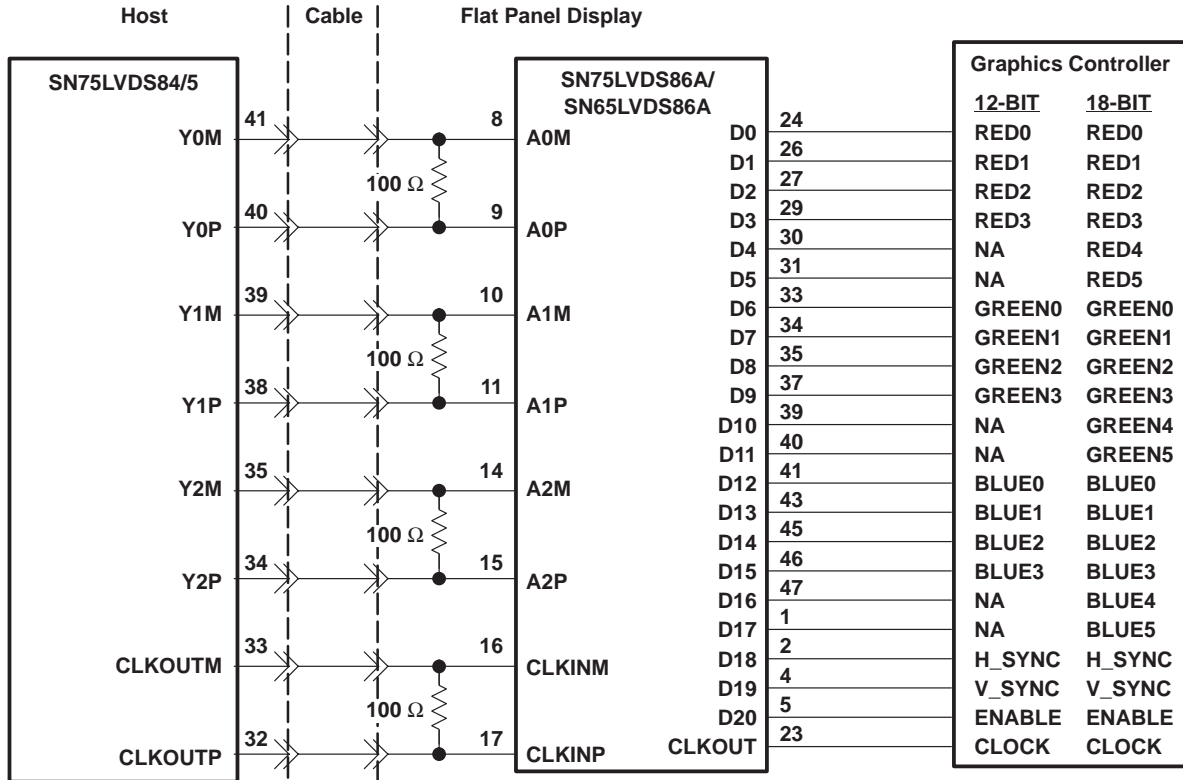


Figure 9. RMS Grayscale I_{CC} vs Clock Frequency

APPLICATION INFORMATION



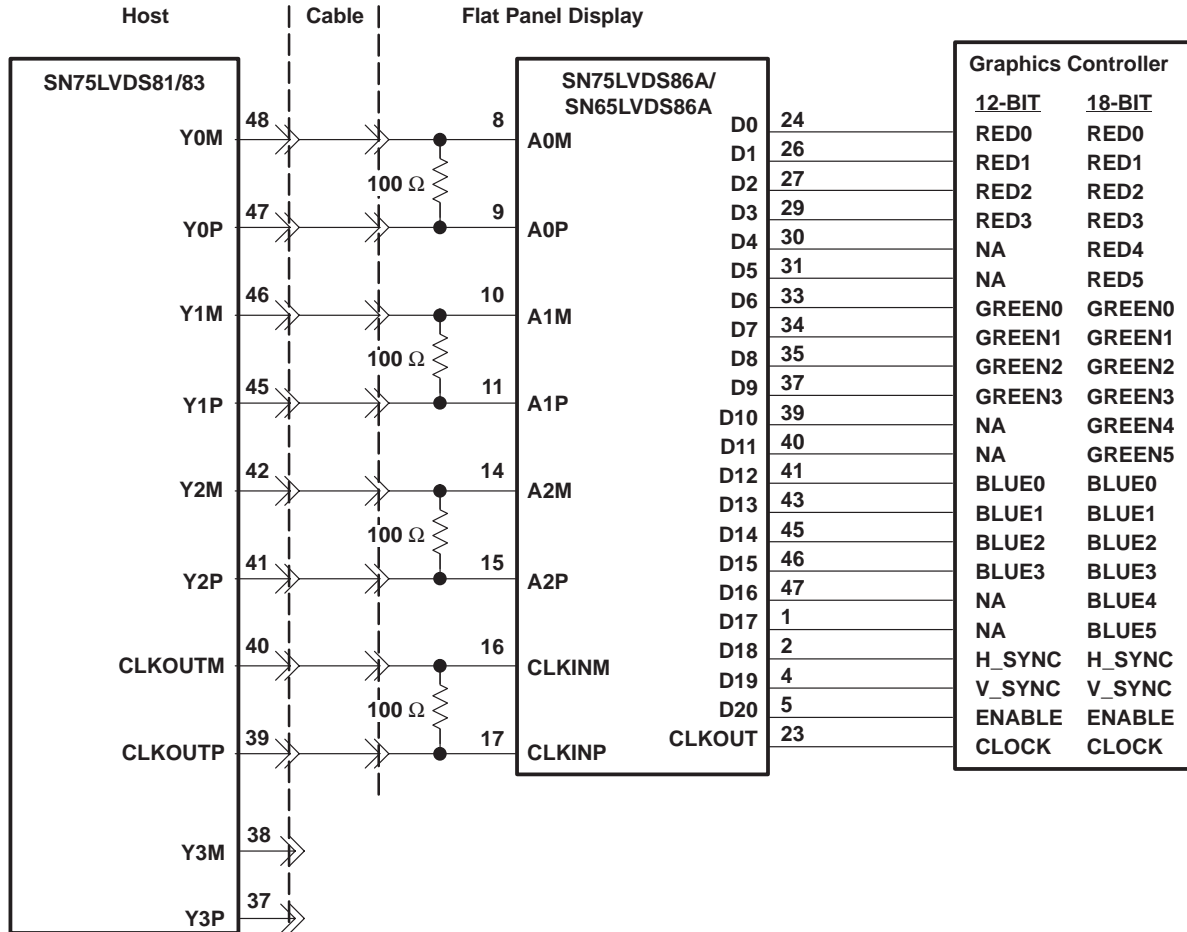
- NOTES: A. The four 100-Ω terminating resistors are recommended to be 0603 types.
 B. NA - not applicable, these unused inputs should be left open.

Figure 10. 18-Bit Color Host to Flat Panel Display Application

SN65LVDS86A, SN75LVDS86A FlatLink™ RECEIVER

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APPLICATION INFORMATION



- NOTES: A. The four 100-Ω terminating resistors are recommended to be 0603 types.
B. NA - not applicable, these unused inputs should be left open.

Figure 11. 24-Bit Color Host to 18-Bit Color LCD Panel Display Application

See the *FlatLink™ Designer's Guide* (SLLA012) for more application information.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS86AQDGG	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65LVDS86AQ	Samples
SN65LVDS86AQDGGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65LVDS86AQ	Samples
SN75LVDS86ADGG	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS86A	Samples
SN75LVDS86ADGGG4	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS86A	Samples
SN75LVDS86ADGGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		SN75LVDS86A	Samples
SN75LVDS86ADGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		SN75LVDS86A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN65LVDS86A :

- Automotive: [SN65LVDS86A-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS86AQDGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN75LVDS86ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS86AQDGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN75LVDS86ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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