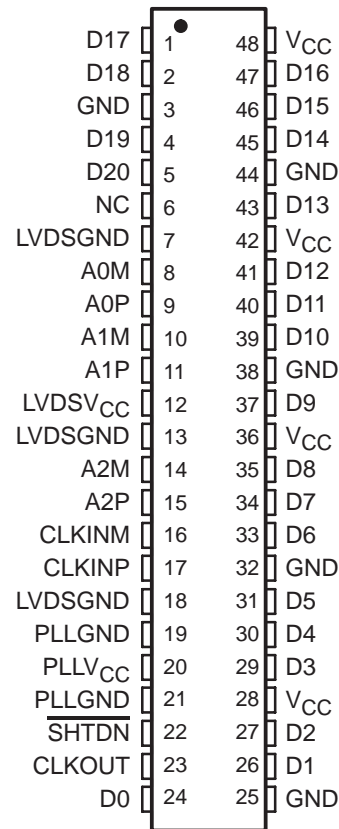- **3:21 Data Channel Expansion at up to 178.5 Mbytes/s Throughput**
- **Suited for SVGA, XGA, or SXGA Display Data Transmission From Controller to Display With Very Low EMI**
- **Three Data Channels and Clock Low-Voltage Differential Channels In and 21 Data and Clock Low-Voltage TTL Channels Out**
- **Operates From a Single 3.3-V Supply**
- **Tolerates 4-kV HBM ESD**
- **Packaged in Thin Shrink Small-Outline Package (TSSOP) With 20-Mil Terminal Pitch**
- **Consumes Less Than 1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range of 31 MHz to 68 MHz**
- **No External Components Required for PLL**
- **Inputs Meet or Exceed the Standard Requirements of ANSI EIA/TIA-644 Standard**
- **Improved Replacement for the DS90C364 and SN75LVDS86**
- **Improved Jitter Tolerance**
- **See SN65LVDS86A-Q1 Data Sheet for Information About the Automotive Qualified Version**

DGG PACKAGE
(TOP VIEW)

D17	1	48	V_{CC}
D18	2	47	D16
GND	3	46	D15
D19	4	45	D14
D20	5	44	GND
NC	6	43	D13
LVDSGND	7	42	V_{CC}
A0M	8	41	D12
A0P	9	40	D11
A1M	10	39	D10
A1P	11	38	GND
LVDSV$_{CC}$	12	37	D9
LVDSGND	13	36	V_{CC}
A2M	14	35	D8
A2P	15	34	D7
CLKINM	16	33	D6
CLKINP	17	32	GND
LVDSGND	18	31	D5
PLLGND	19	30	D4
PLLV$_{CC}$	20	29	D3
PLLGND	21	28	V_{CC}
$\overline{SHTDN}$	22	27	D2
CLKOUT	23	26	D1
D0	24	25	GND

NC – Not connected

description

The SN65LVDS86A/SN75LVDS86A FlatLink™ receiver contains three serial-in 7-bit parallel-out shift registers and four low-voltage differential signaling (LVDS) line receivers in a single integrated circuit. These functions allow receipt of synchronous data from a compatible transmitter, such as the SN75LVDS81, '83, '84, or '85, over four balanced-pair conductors and expansion to 21 bits of single-ended low-voltage LVTTL synchronous data at a lower transfer rate.

When receiving, the high-speed LVDS data is received and loaded into registers at seven times the LVDS input clock (CLKIN) rate. The data is then unloaded to a 21-bit-wide LVTTL parallel bus at the CLKIN rate. The 'LVDS86A presents valid data on the falling edge of the output clock (CLKOUT).

The 'LVDS86A requires only four line-termination resistors for the differential inputs and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only user intervention is the possible use of the shutdown/clear ($\overline{SHTDN}$) active-low input to inhibit the clock and shut off the LVDS receivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

The SN75LVDS86A is characterized for operation over ambient free-air temperatures of 0°C to 70°C. The SN65LVDS86A is characterized for operation over the full Automotive temperature range of −40°C to 125°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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functional block diagram
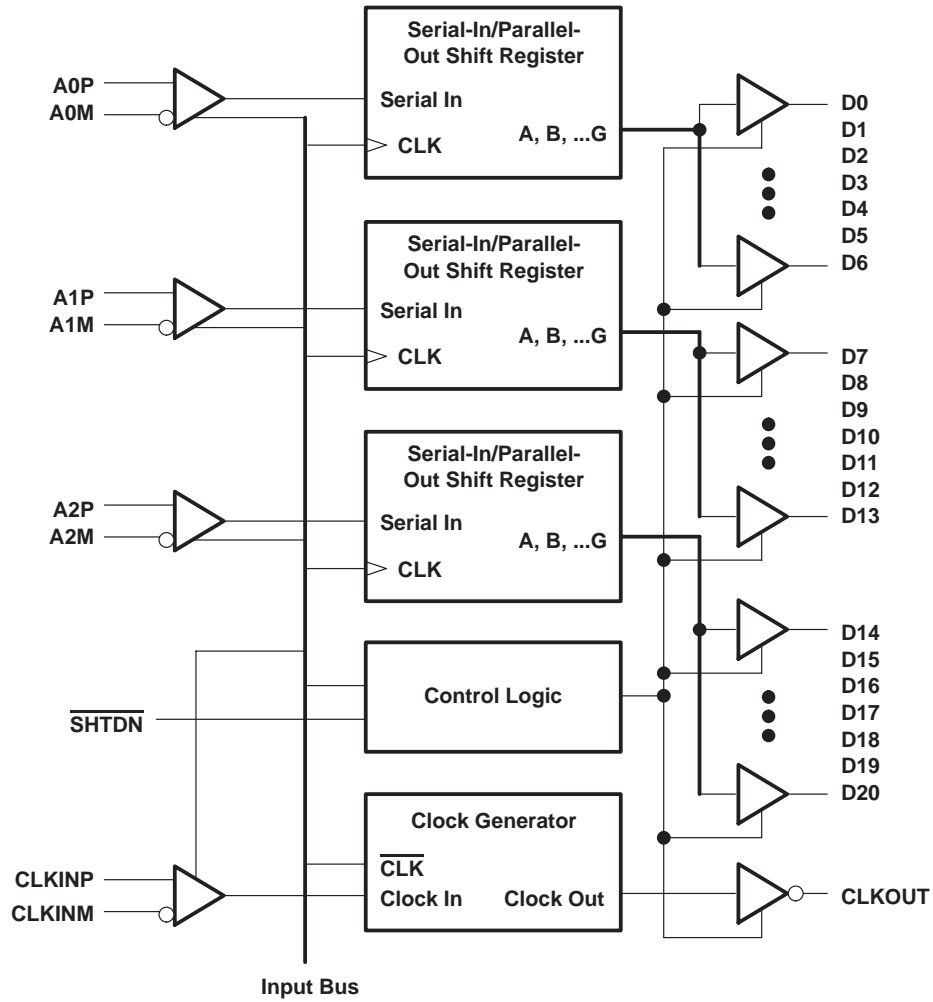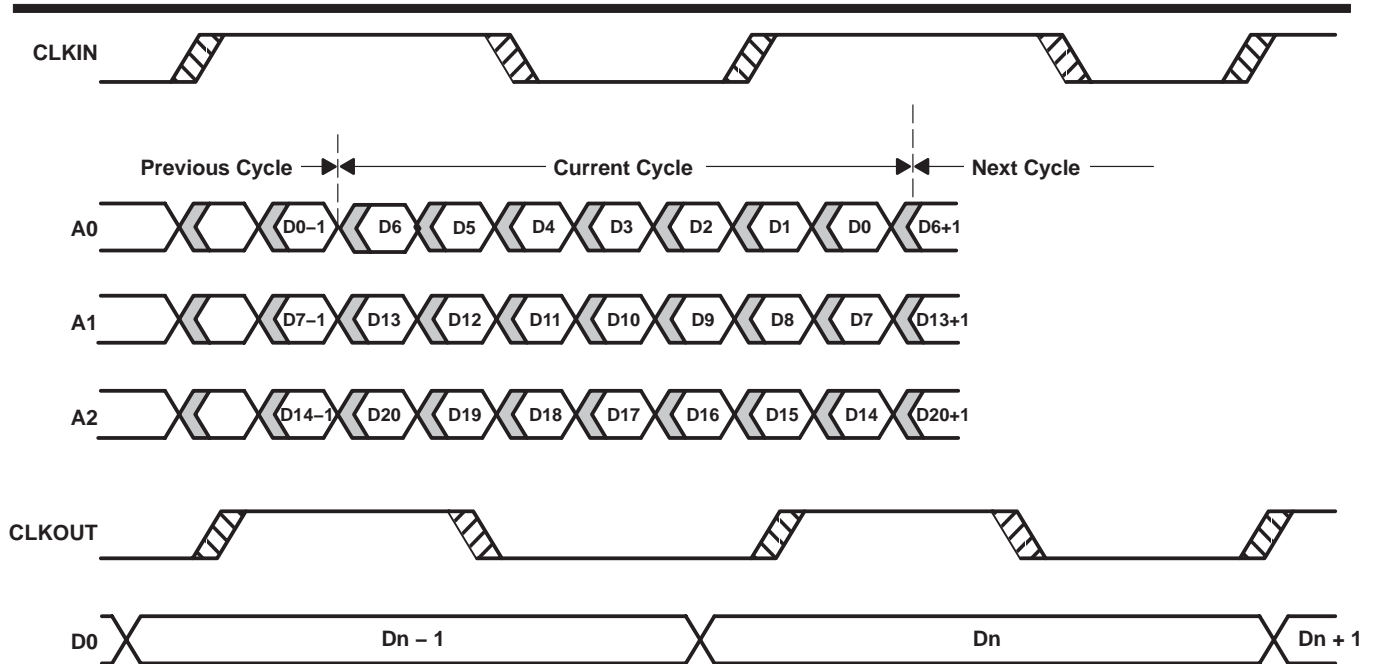
Figure 1. SN65LVDS86A/SN75LVDS86A Load and Shift Timing Sequences

equivalent input and output schematic diagrams

SN65LVDS86A, SN75LVDS86A
FlatLink™ RECEIVER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . −0.5 V to 4 V
Voltage range at any terminal . . . . −0.5 V to V_{CC} + 0.5 V
Electrostatic discharge (see Note 2): All pins (Class 3A) . . . . 4 KV
                                                              All pins (Class 2B) . . . . 200 V
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating virtual junction temperature range, T_J . . . . −40°C to 150°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. All voltage values are with respect to the GND terminals unless otherwise noted.
        2. This rating is measured using MIL-STD-883C Method, 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 125°C POWER RATING
DGG	1637 mW	13.1 mW/°C	1048 mW	327 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

recommended operating conditions (see Figure 2)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH} ($\overline{\text{SHTDN}}$)		2			V
Low-level input voltage, V_{IL} ($\overline{\text{SHTDN}}$)				0.8	V
Magnitude differential input voltage, $|V_{ID}|$		0.1		0.6	V
Common-mode input voltage, V_{IC}		$\dfrac{|V_{ID}|}{2}$		$2.4 - \dfrac{|V_{ID}|}{2}$	V
Operating free-air temperature, T_A	SN75LVDS86A	0		70	°C
	SN65LVDS86A	−40		125	

timing requirements

	MIN	NOM	MAX	UNIT
Cycle time, input clock, t_c§	14.7	t_c	32.4	ns

§ Parameter t_c is defined as the mean duration of a minimum of 32 000 clock cycles.

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electrical characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage					100	mV
V_{IT-}	Negative-going differential input threshold voltage‡			−100			mV
V_{OH}	High-level output voltage	$I_{OH} = -4$ mA		2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA				0.4	V
I_{CC}	Quiescent current (average)	Disabled, All inputs to GND				280	µA
		Enabled, AnP = 1 V, AnM = 1.4 V, $t_c = 15.38$ ns			33	40	mA
		Enabled, $C_L = 8$ pF, Grayscale pattern (see Figure 3), $t_c = 15.38$ ns			43		
		Enabled, $C_L = 8$ pF, Worst-case pattern (see Figure 4) $t_c = 15.38$ ns			68		
I_{IH}	High-level input current ($\overline{SHTDN}$)	$V_{IH} = V_{CC}$				±20	µA
I_{IL}	Low-level input current ($\overline{SHTDN}$)	$V_{IL} = 0$	SN75LVDS86A			±20	µA
			SN65LVDS86A			±25	
I_I	Input current A inputs	$0 \leq V_I \leq 2.4$ V				±20	µA
I_{OZ}	High-impedance output current	$V_O = 0$ or V_{CC}				±10	µA

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25°C$.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going input voltage threshold only.

switching characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{su}	Setup time, D0–D20 to CLKOUT↓	$C_L = 8$ pF, See Figure 5	5			ns
t_h	Data hold time, CLKOUT↓ to D0–D20		5			ns
$t_{(RSKM)}$	Receiver input skew margin§ (see Figure 7)	$t_c = 15.38$ ns (±0.2%), |Input clock jitter| < 50 ps¶,	550	700		ps
t_d	Delay time, CLKIN↑ to CLKOUT↓ (see Figure 7)	$V_{CC} = 3.3$ V, $t_c = 15.38$ ns (±0.2%), $T_A = 25°C$	3	5	7	ns
t_{en}	Enable time, $\overline{SHTDN}$ to phase lock	See Figure 7		1		ms
t_{dis}	Disable time, $\overline{SHTDN}$ to off state	See Figure 8		400		ns
t_t	Transition time, output (10% to 90% t_r or t_f) (data only)	$C_L = 8$ pF		3		ns
t_t	Transition time, output (10% to 90% t_r or t_f) (clock only)	$C_L = 8$ pF		1.5		ns
t_w	Pulse duration, output clock			0.50 t_c		ns

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25°C$.
§ The parameter $t_{(RSKM)}$ is the timing margin available to allocate to the transmitter and interconnection skews and clock jitter. The value of this parameter at clock periods other than 15.38 ns can be calculated from $t_{RSKM} = t_c/14 - 550$ ps.
¶ \|Input clock jitter\| is the magnitude of the change in input clock period.

PARAMETER MEASUREMENT INFORMATION
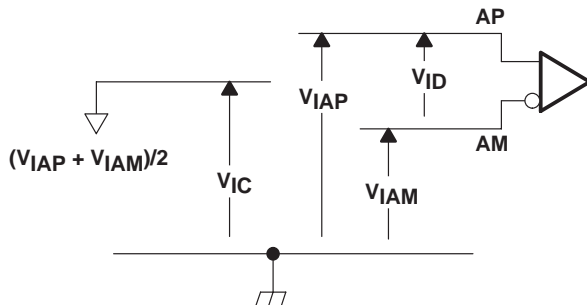
Figure 2. Voltage Definitions
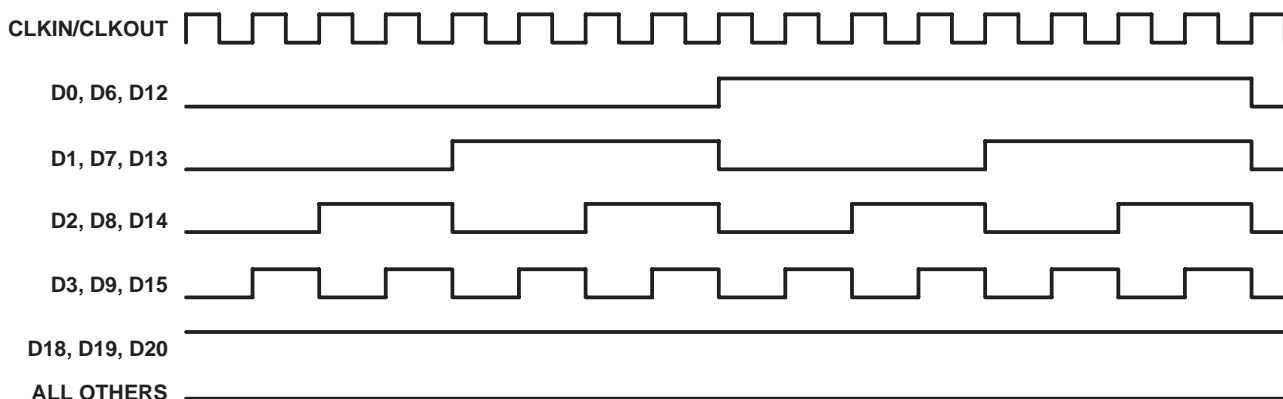
NOTE A: The 16-grayscale test-pattern test device power consumption for a typical display pattern.

Figure 3. 16-Grayscale Test-Pattern Waveforms
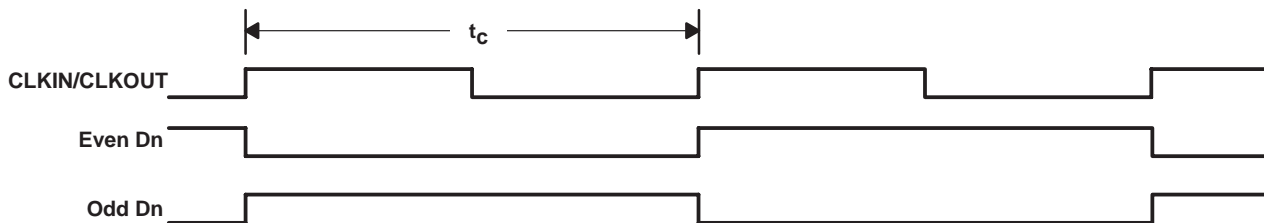
NOTE A: The worst-case test pattern produces nearly the maximum switching frequency for all of the LVTTL outputs.

Figure 4. Worst-Case Test-Pattern Waveforms

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PARAMETER MEASUREMENT INFORMATION

Figure 5. Setup and Hold Time Waveforms

PARAMETER MEASUREMENT INFORMATION
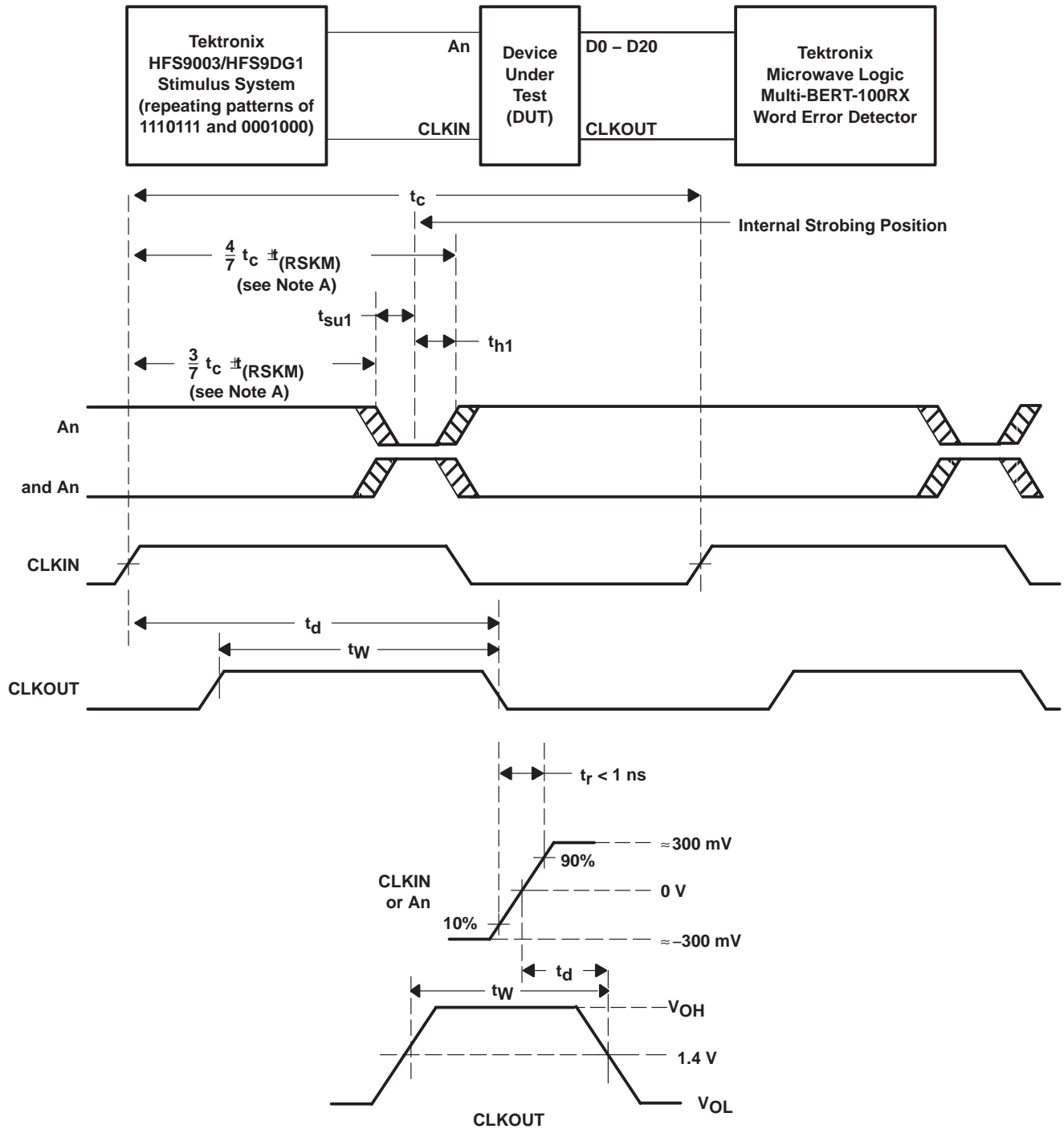
NOTE A: CLKIN is advanced or delayed with respect to data until errors are observed at the receiver outputs. The advance or delay is then reduced until there are no data errors observed. The magnitude of the advance or delay is $t_{(RSKM)}$.

Figure 6. Receiver Input Skew Margin, Setup/Hold Time, and Delay Time Definitions

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PARAMETER MEASUREMENT INFORMATION
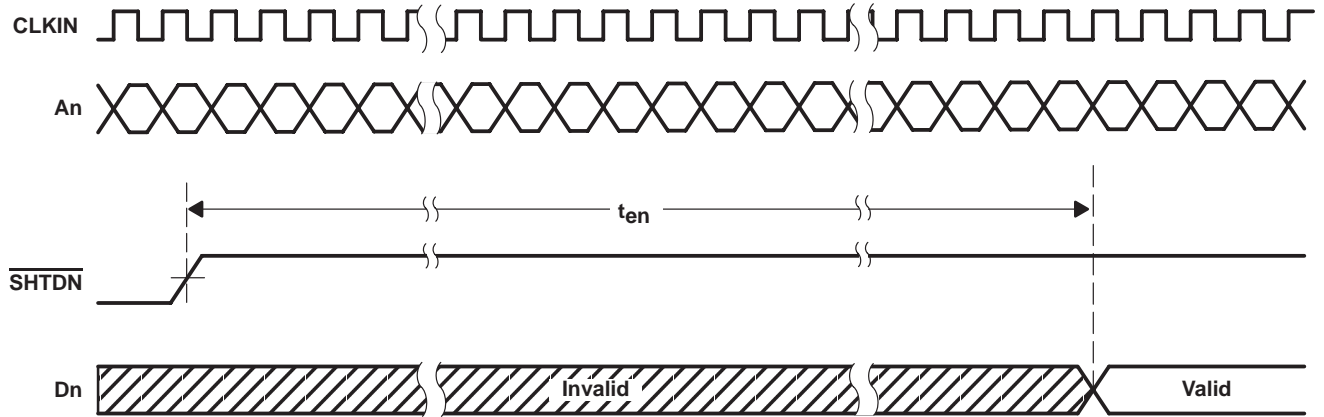
Figure 7. Enable Time Waveforms
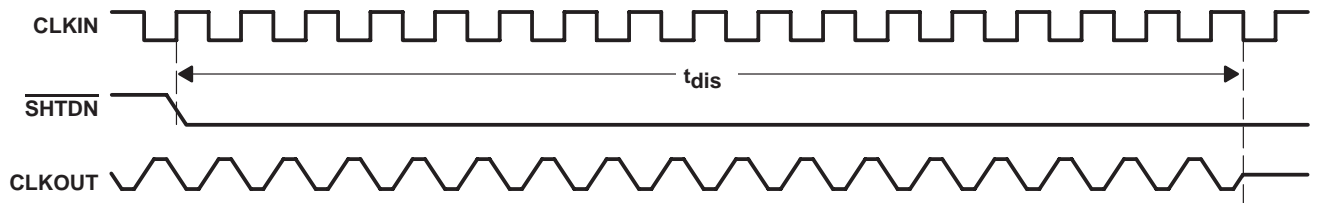
Figure 8. Disable Time Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
CLOCK FREQUENCY
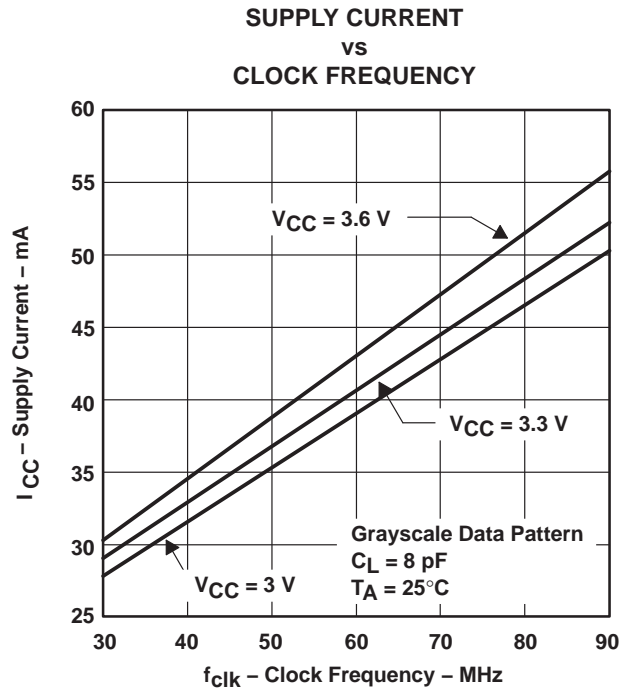
Figure 9. RMS Grayscale I$_{CC}$ vs Clock Frequency

APPLICATION INFORMATION
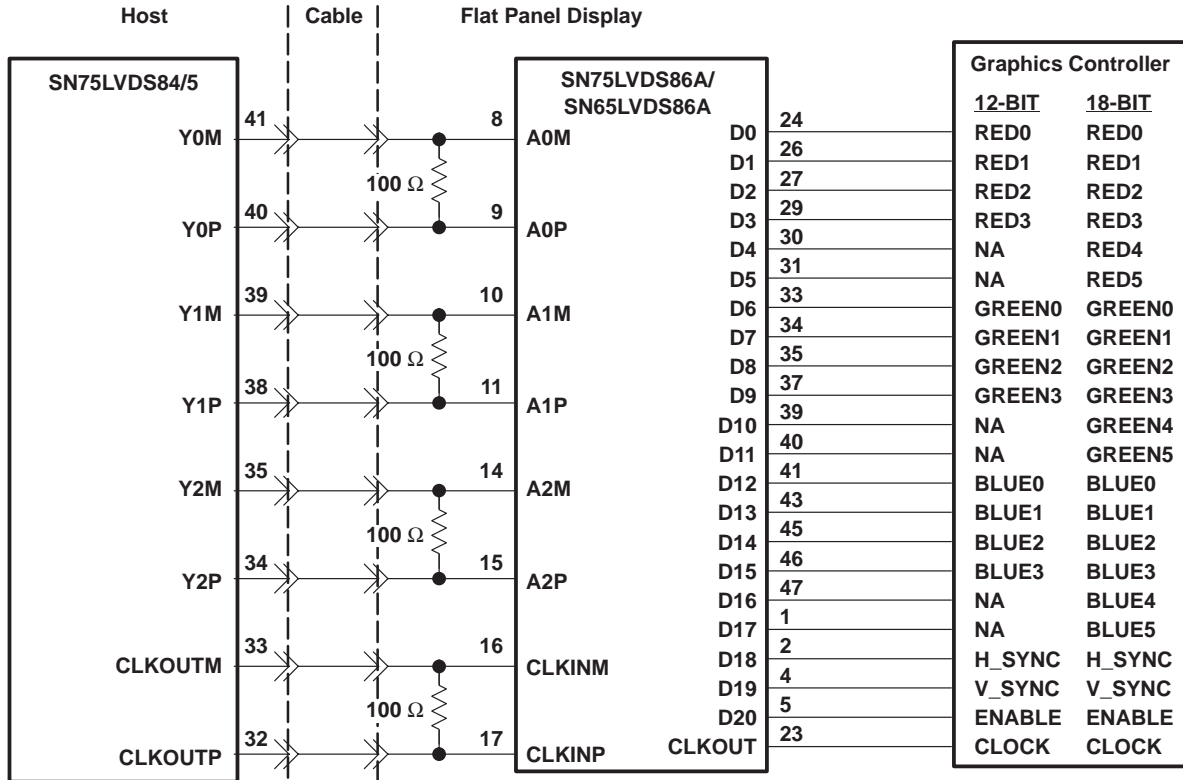
	12-BIT	18-BIT
D0 (24)	RED0	RED0
D1 (26)	RED1	RED1
D2 (27)	RED2	RED2
D3 (29)	RED3	RED3
D4 (30)	NA	RED4
D5 (31)	NA	RED5
D6 (33)	GREEN0	GREEN0
D7 (34)	GREEN1	GREEN1
D8 (35)	GREEN2	GREEN2
D9 (37)	GREEN3	GREEN3
D10 (39)	NA	GREEN4
D11 (40)	NA	GREEN5
D12 (41)	BLUE0	BLUE0
D13 (43)	BLUE1	BLUE1
D14 (45)	BLUE2	BLUE2
D15 (46)	BLUE3	BLUE3
D16 (47)	NA	BLUE4
D17 (1)	NA	BLUE5
D18 (2)	H_SYNC	H_SYNC
D19 (4)	V_SYNC	V_SYNC
D20 (5)	ENABLE	ENABLE
CLKOUT (23)	CLOCK	CLOCK

NOTES: A. The four 100-Ω terminating resistors are recommended to be 0603 types.
B. NA - not applicable, these unused inputs should be left open.

Figure 10. 18-Bit Color Host to Flat Panel Display Application

APPLICATION INFORMATION

NOTES: A. The four 100-Ω terminating resistors are recommended to be 0603 types.
        B. NA - not applicable, these unused inputs should be left open.

Figure 11. 24-Bit Color Host to 18-Bit Color LCD Panel Display Application

See the *FlatLink™ Designer's Guide* (SLLA012) for more application information.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS86AQDGG	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65LVDS86AQ	Samples
SN65LVDS86AQDGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65LVDS86AQ	Samples
SN75LVDS86ADGG	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS86A	Samples
SN75LVDS86ADGGG4	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS86A	Samples
SN75LVDS86ADGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		SN75LVDS86A	Samples
SN75LVDS86ADGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		SN75LVDS86A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN65LVDS86A :

● Automotive: SN65LVDS86A-Q1

NOTE: Qualified Version Definitions:

● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS86AQDGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN75LVDS86ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS86AQDGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN75LVDS86ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0

DGG (R-PDSO-G**)　　　　　　　　　　　　　　　　　　**PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

0,50

$\frac{0,27}{0,17}$　⊕　0,08 Ⓜ

48　　　　　　　　　　　25

$\frac{6,20}{6,00}$　$\frac{8,30}{7,90}$

0,15 NOM

Gage Plane

0,25

0°−8°

0,75 / 0,50

1　　　　　　　　　24

A

1,20 MAX

$\frac{0,15}{0,05}$

Seating Plane

△　0,10

DIM ＼ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES:　A.　All linear dimensions are in millimeters.
　　　　B.　This drawing is subject to change without notice.
　　　　C.　Body dimensions do not include mold protrusion not to exceed 0,15.
　　　　D.　Falls within JEDEC MO-153

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