



SCCS054C - August 1994 - Revised October 2003

# CY74FCT16373T CY74FCT162373T

## 16-Bit Latches

### Features

- $I_{off}$  supports partial-power-down mode operation
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- $V_{CC} = 5\text{V} \pm 10\%$

#### CY74FCT16373T Features:

- 64 mA sink current, 32 mA source current
- Typical  $V_{OLP}$  (ground bounce) < 1.0V at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$

#### CY74FCT162373T Features:

- Balanced 24 mA output drivers
- Reduced system switching noise
- Typical  $V_{OLP}$  (ground bounce) < 0.6V at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$

### Functional Description

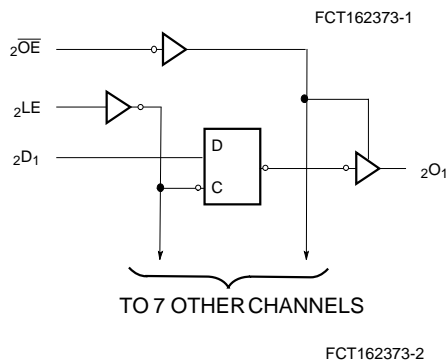
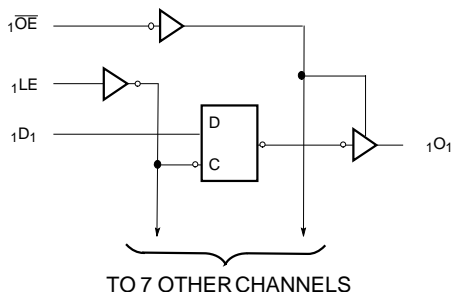
CY74FCT16373T and CY74FCT162373T are 16-bit D-type latches designed for use in bus applications requiring high speed and low power. These devices can be used as two independent 8-bit latches or as a single 16-bit latch by connecting the Output Enable ( $\overline{OE}$ ) and Latch (LE) inputs. Flow-through pinout and small shrink packaging aid in simplifying board layout.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CY74FCT16373T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162373T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162373T is ideal for driving transmission lines.

### Logic Block Diagrams



### Pin Configuration

#### SSOP/TSSOP/TVSOP

##### Top View

$\overline{1OE}$	1	48	$\overline{1LE}$
$\overline{1O1}$	2	47	$\overline{1D1}$
$\overline{1O2}$	3	46	$\overline{1D2}$
GND	4	45	GND
$\overline{1O3}$	5	44	$\overline{1D3}$
$\overline{1O4}$	6	43	$\overline{1D4}$
$V_{CC}$	7	42	$V_{CC}$
$\overline{1O5}$	8	41	$\overline{1D5}$
$\overline{1O6}$	9	40	$\overline{1D6}$
GND	10	39	GND
$\overline{1O7}$	11	38	$\overline{1D7}$
$\overline{1O8}$	12	37	$\overline{1D8}$
$\overline{2O1}$	13	36	$\overline{2D1}$
$\overline{2O2}$	14	35	$\overline{2D2}$
GND	15	34	GND
$\overline{2O3}$	16	33	$\overline{2D3}$
$\overline{2O4}$	17	32	$\overline{2D4}$
$V_{CC}$	18	31	$V_{CC}$
$\overline{2O5}$	19	30	$\overline{2D5}$
$\overline{2O6}$	20	29	$\overline{2D6}$
GND	21	28	GND
$\overline{2O7}$	22	27	$\overline{2D7}$
$\overline{2O8}$	23	26	$\overline{2D8}$
$\overline{2OE}$	24	25	$\overline{2LE}$

FCT162373-3

## Pin Description

Name	Description
D	Data Inputs
LE	Latch Enable Inputs (Active HIGH)
$\overline{OE}$	Output Enable Inputs (Active LOW)
O	Three-State Outputs

## Function Table<sup>[1]</sup>

Inputs			Outputs
D	LE	$\overline{OE}$	O
H	H	L	H
L	H	L	L
X	L	L	Q <sub>0</sub>
X	X	H	Z

## Maximum Ratings<sup>[2, 3]</sup>

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l -55°C to +125°C

Ambient Temperature with  
Power Applied ..... Com'l -55°C to +125°C

DC Input Voltage ..... -0.5V to +7.0V

DC Output Voltage ..... -0.5V to +7.0V

DC Output Current  
(Maximum Sink Current/Pin) ..... -60 to +120 mA

Power Dissipation ..... 1.0W

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	5V ± 10%

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage		2.0			V
V <sub>IL</sub>	Input LOW Voltage				0.8	V
V <sub>H</sub>	Input Hysteresis <sup>[5]</sup>			100		mV
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA		-0.7	-1.2	V
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>I</sub> =V <sub>CC</sub>			±1	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> =Max., V <sub>I</sub> =GND			±1	μA
I <sub>OZH</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.7V			±1	μA
I <sub>OZL</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.5V			±1	μA
I <sub>OS</sub>	Short Circuit Current <sup>[6]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =GND	-80	-140	-200	mA
I <sub>O</sub>	Output Drive Current <sup>[6]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.5V	-50		-180	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> ≤4.5V <sup>[7]</sup>			±1	μA

## Output Drive Characteristics for CY74FCT16373T

Parameter	Description	Test Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-3 mA	2.5	3.5		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA	2.4	3.5		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-32 mA	2.0	3.0		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA		0.2	0.55	V

### Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance. Q<sub>0</sub>=Previous state of flip-flop.
2. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
4. Typical values are at V<sub>CC</sub>=5.0V, T<sub>A</sub>= +25°C ambient.
5. This parameter is specified but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
7. Tested at +25°C.

**Output Drive Characteristics for CY74FCT162373T**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
$I_{ODL}$	Output LOW Current <sup>[6]</sup>	$V_{CC}=5V$ , $V_{IN}=V_{IH}$ or $V_{IL}$ , $V_{OUT}=1.5V$	60	115	150	mA
$I_{ODH}$	Output HIGH Current <sup>[6]</sup>	$V_{CC}=5V$ , $V_{IN}=V_{IH}$ or $V_{IL}$ , $V_{OUT}=1.5V$	-60	-115	-150	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC}=\text{Min.}$ , $I_{OH}=-24\text{ mA}$	2.4	3.3		V
$V_{OL}$	Output LOW Voltage	$V_{CC}=\text{Min.}$ , $I_{OL}=24\text{ mA}$		0.3	0.55	V

**Capacitance<sup>[5]</sup>** ( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )

Parameter	Description	Test Conditions	Typ. <sup>[4]</sup>	Max.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	4.5	6.0	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	5.5	8.0	pF

**Power Supply Characteristics**

Parameter	Description	Test Conditions	Typ. <sup>[4]</sup>	Max.	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC}=\text{Max.}$ $V_{IN}\leq 0.2V$ , $V_{IN}\geq V_{CC}-0.2V$	5	500	$\mu\text{A}$
$\Delta I_{CC}$	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC}=\text{Max.}$ $V_{IN}=3.4V^{[8]}$	0.5	1.5	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>[9]</sup>	$V_{CC}=\text{Max.}$ , One Input Toggling, 50% Duty Cycle, Outputs Open, $OE=\text{GND}$ $V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$	60	100	$\mu\text{A}/\text{MHz}$
$I_C$	Total Power Supply Current <sup>[10]</sup>	$V_{CC}=\text{Max.}$ , $f_1=10\text{ MHz}$ , 50% Duty Cycle, Outputs Open, One Bit Toggling, $OE=\text{GND}$ , $LE=V_{CC}$ $V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$	0.6	1.5	mA
		$V_{IN}=3.4V$ or $V_{IN}=\text{GND}$	0.9	2.3	mA
		$V_{CC}=\text{Max.}$ , $f_1=2.5\text{ MHz}$ , 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $OE=\text{GND}$ , $LE=V_{CC}$ $V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$	2.4	4.5 <sup>[11]</sup>	mA
		$V_{IN}=3.4V$ or $V_{IN}=\text{GND}$	6.4	16.5 <sup>[11]</sup>	mA

**Notes:**

8. Per TTL driven input ( $V_{IN}=3.4V$ ); all other inputs at  $V_{CC}$  or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10.  $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input ( $V_{IN}=3.4V$ )  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$   
 All currents are in milliamperes and all frequencies are in megahertz.
11. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are specified but not tested.

**Switching Characteristics** Over the Operating Range<sup>[12]</sup>

Parameter	Description	CY74FCT16373AT CY74FCT162373AT		Unit	Fig. No. <sup>[13]</sup>
		Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D to O	1.5	5.2	ns	1, 3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LE to O	2.0	6.7	ns	1, 5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time	1.5	6.1	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time	1.5	5.5	ns	1, 7, 8
t <sub>SU</sub>	Set-Up Time HIGH or LOW, D to LE	2.0		ns	9
t <sub>H</sub>	Hold Time HIGH or LOW, D to LE	1.5		ns	9
t <sub>W</sub>	LE Pulse Width HIGH	3.3		ns	5
t <sub>SK(O)</sub>	Output Skew <sup>[14]</sup>		0.5	ns	—

Parameter	Description	CY74FCT16373CT CY74FCT162373CT		Unit	Fig. No. <sup>[13]</sup>
		Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D to O	1.5	4.2	ns	1, 3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LE to O	2.0	5.5	ns	1, 5
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time	1.5	5.5	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time	1.5	5.0	ns	1, 7, 8
t <sub>SU</sub>	Set-Up Time HIGH or LOW, D to LE	2.0		ns	9
t <sub>H</sub>	Hold Time HIGH or LOW, D to LE	1.5		ns	9
t <sub>W</sub>	LE Pulse Width HIGH	3.3		ns	5
t <sub>SK(O)</sub>	Output Skew <sup>[14]</sup>		0.5	ns	—

**Notes:**

12. Minimum limits are specified but not tested on Propagation Delays.

13. See "Parameter Measurement Information" in the General Information section.

14. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

**Ordering Information CY74FCT16373**

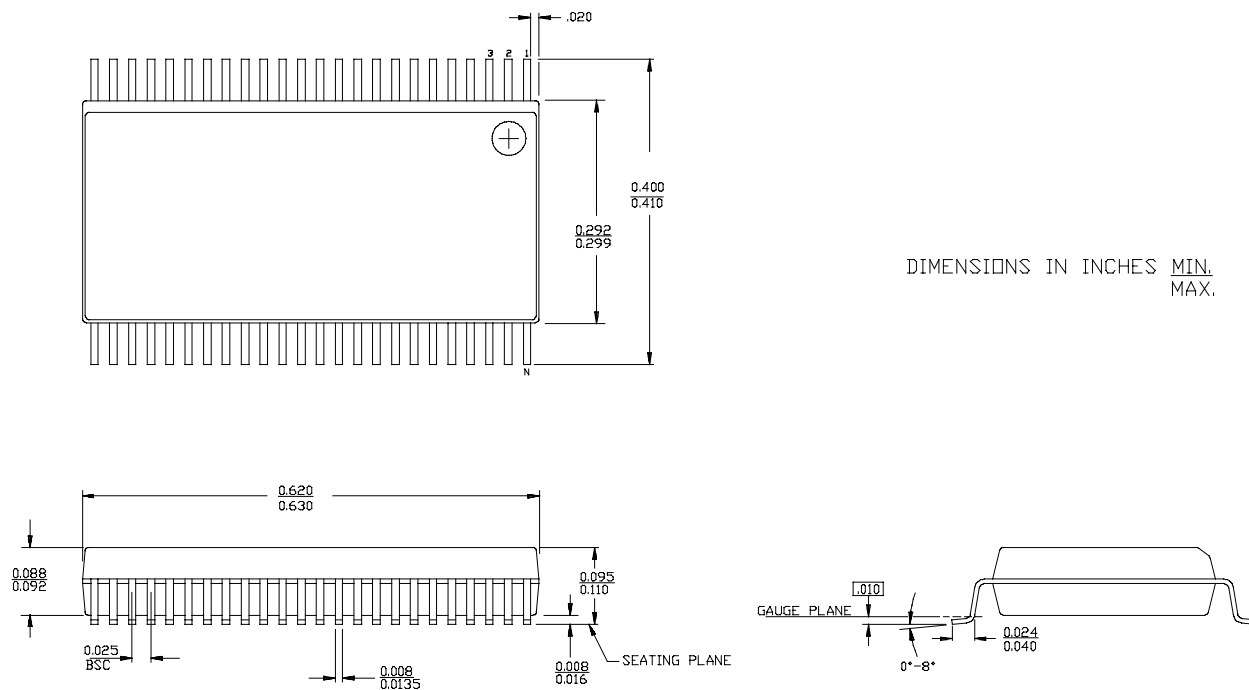
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT16373CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16373CTPVC/PVCT	O48	48-Lead (300-Mil) SSOP	
	CY74FCT16373CTVR	-	48-Lead (173-Mil) TVSOP	
5.2	CY74FCT16373ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16373ATPVC/PVCT	O48	48-Lead (300-Mil) SSOP	
	CY74FCT16373ATVR	-	48-Lead (173-Mil) TVSOP	

**Ordering Information CY74FCT162373**

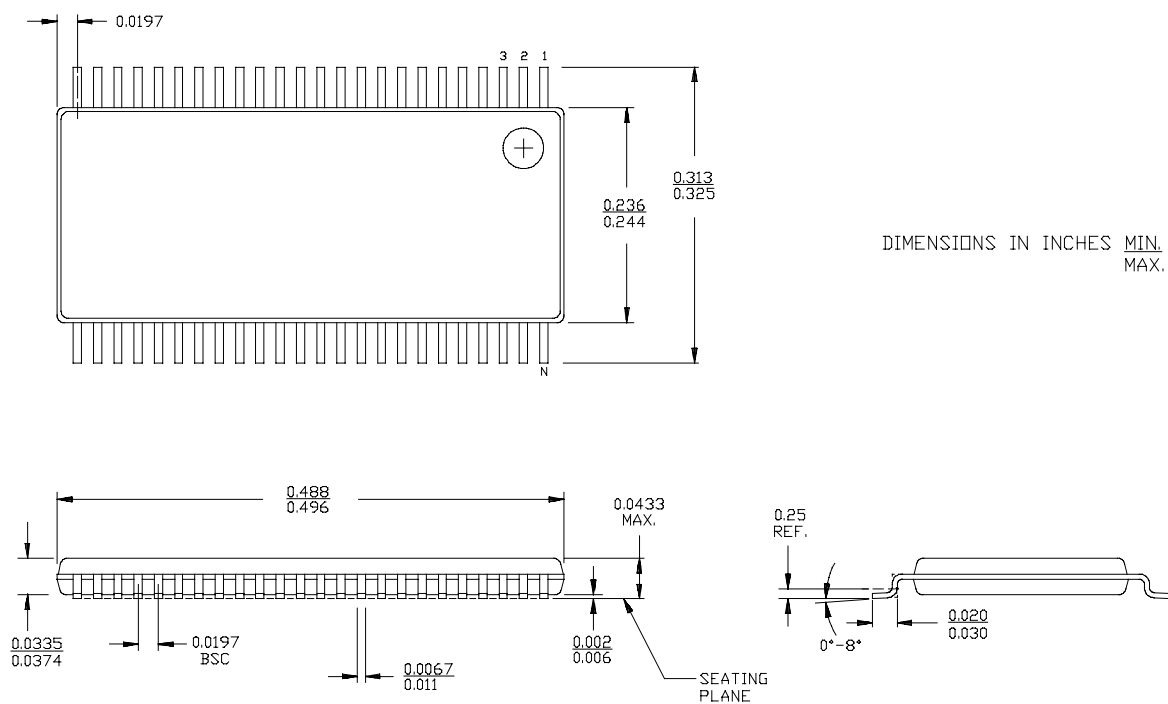
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	74FCT162373CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162373CTPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162373CTPVCT	O48	48-Lead (300-Mil) SSOP	
5.2	74FCT162373ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162373ATPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162373ATPVCT	O48	48-Lead (300-Mil) SSOP	

**Package Diagrams**

**48-Lead Shrunk Small Outline Package O48**



**48-Lead Thin Shrunk Small Outline Package Z48**



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74FCT162373ATPACT	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162373A	<a href="#">Samples</a>
74FCT162373ATPVC4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162373A	<a href="#">Samples</a>
74FCT162373ATPVCT	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162373A	<a href="#">Samples</a>
74FCT162373CTPVC4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162373C	<a href="#">Samples</a>
74FCT16373ATPACTG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373A	<a href="#">Samples</a>
74FCT16373ATPVC4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373A	<a href="#">Samples</a>
CY74FCT162373ATPVC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162373A	<a href="#">Samples</a>
CY74FCT162373CTPVC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162373C	<a href="#">Samples</a>
CY74FCT16373ATPACT	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373A	<a href="#">Samples</a>
CY74FCT16373ATPVC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373A	<a href="#">Samples</a>
CY74FCT16373ATPVCT	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373A	<a href="#">Samples</a>
CY74FCT16373CTPACT	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373C	<a href="#">Samples</a>
CY74FCT16373CTPVC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16373C	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

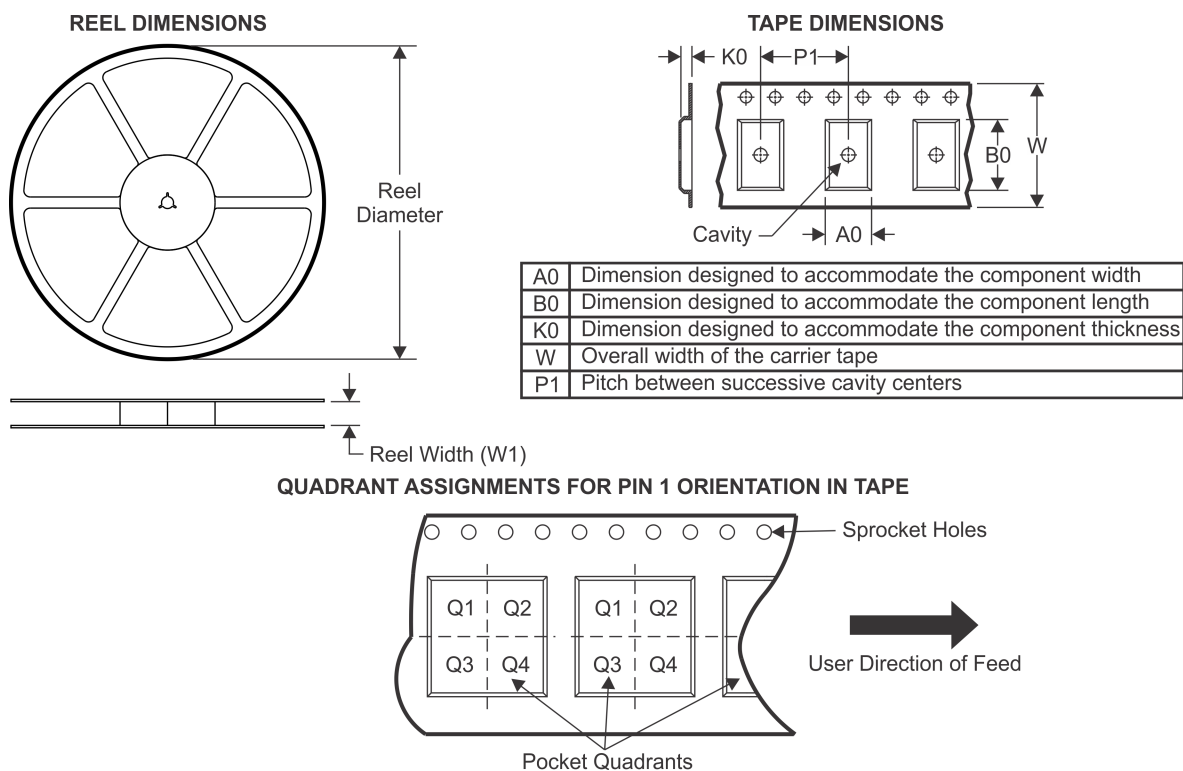
<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74FCT162373ATPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
74FCT162373ATPVCT	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
CY74FCT16373ATPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
CY74FCT16373ATPVCT	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
CY74FCT16373CTPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

## TAPE AND REEL BOX DIMENSIONS



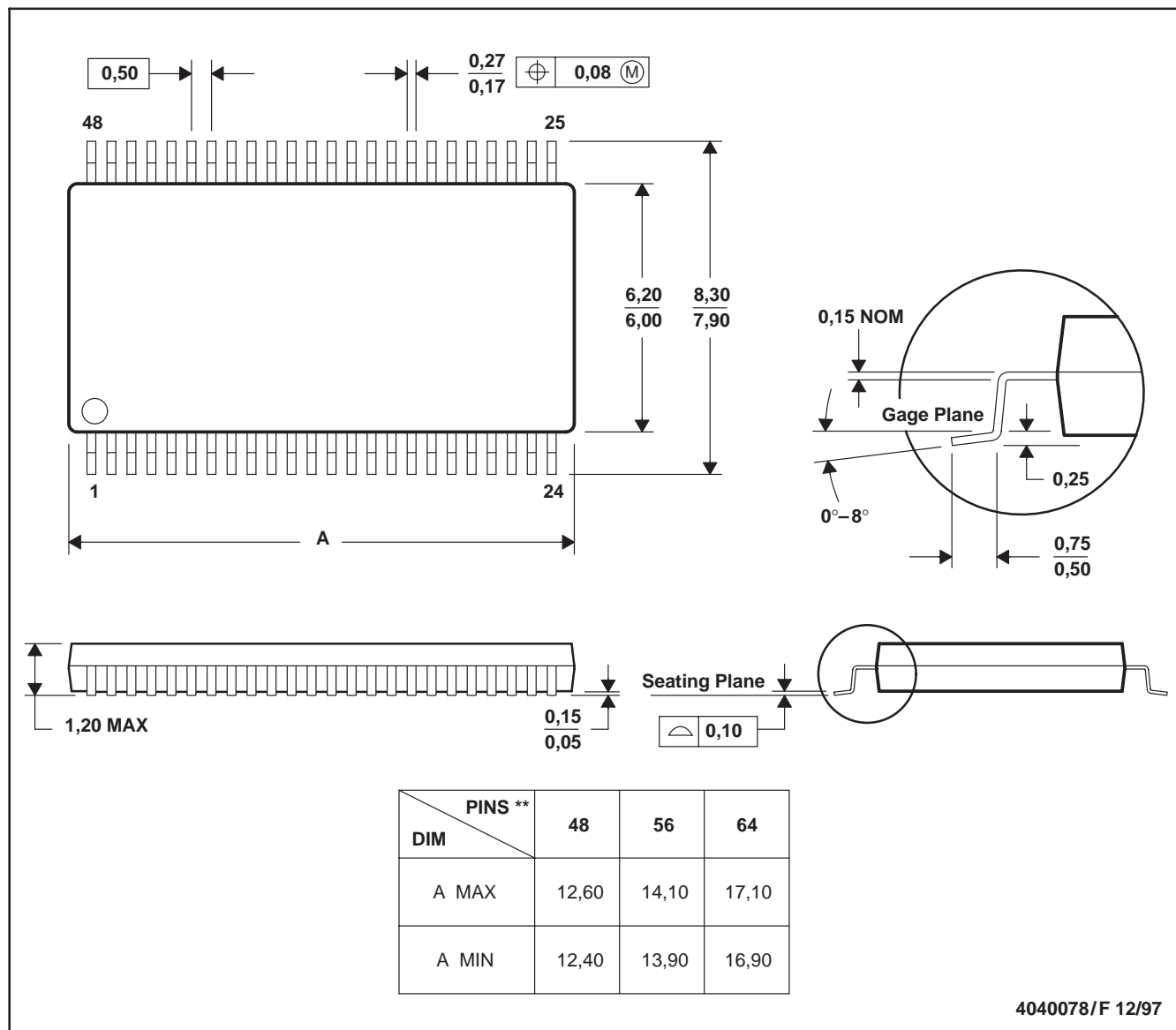
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74FCT162373ATPACT	TSSOP	DGG	48	2000	367.0	367.0	45.0
74FCT162373ATPVCT	SSOP	DL	48	1000	367.0	367.0	55.0
CY74FCT16373ATPACT	TSSOP	DGG	48	2000	367.0	367.0	45.0
CY74FCT16373ATPVCT	SSOP	DL	48	1000	367.0	367.0	55.0
CY74FCT16373CTPACT	TSSOP	DGG	48	2000	367.0	367.0	45.0

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

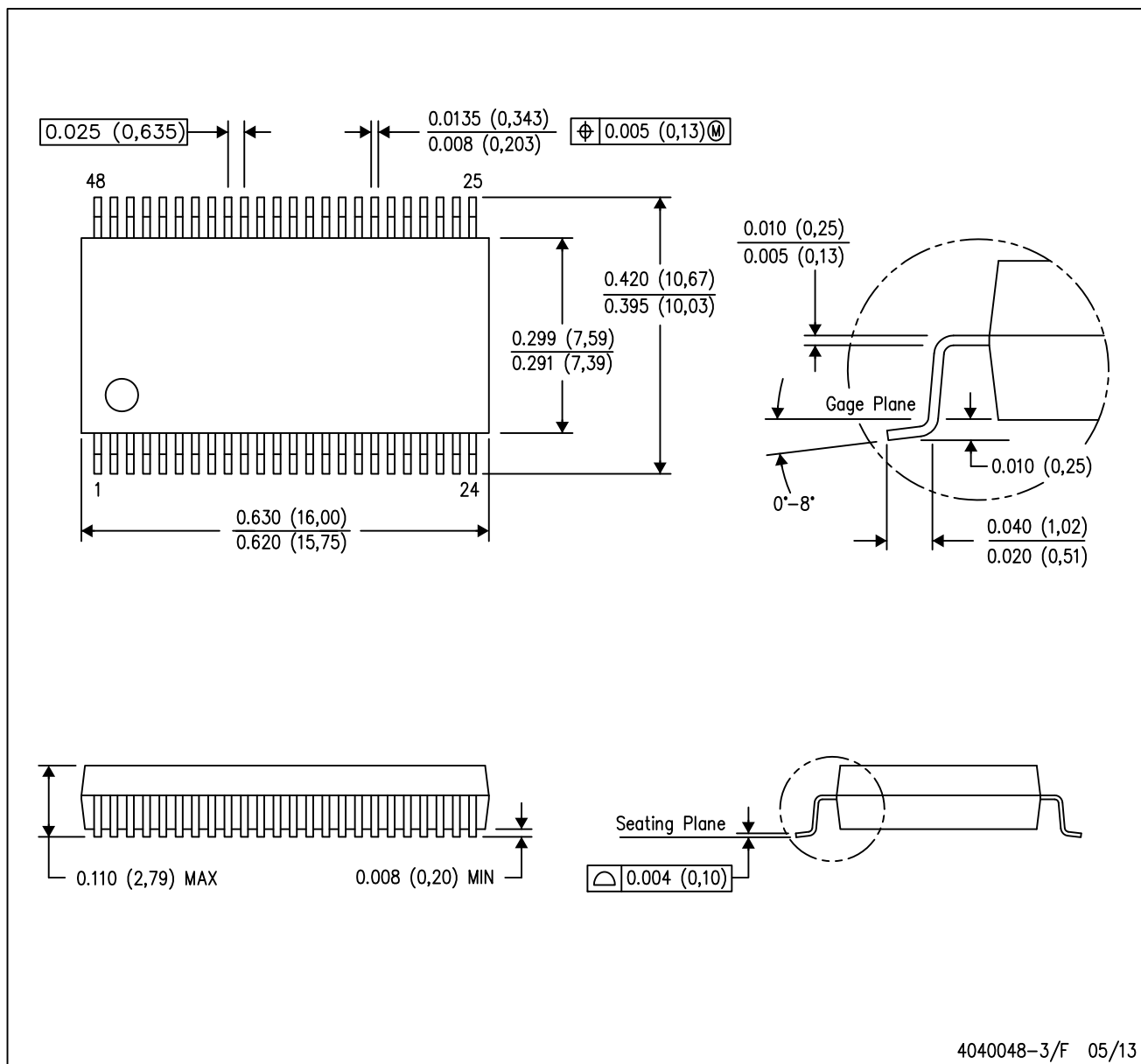
48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MO-118

## IMPORTANT NOTICE

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