IEEE 802.3af PoE HIGH POWER PD CONTROLLER

FEATURES

- **Adjustable Turn-on Thresholds**
- **Permits high-power 26 W designs**
- **Integrated 0.58-Ω, 100-V, Low-Side Switch**
- **15-kV System Level ESD Capable**
- **Industrial Temperature Range: -40°C to 85°C**
- **8-Pin PowerPad™ SOIC Package**

APPLICATIONS

- **VoIP Video and Speaker Phones**
- **WiMAX Access Points**
- **Security Cameras**
- **RFID Readers**

PRODUCT SELECTOR

Device	UVLO	Protection	Package(1)	Rated Current
TPS2376-H	Adjustable	Auto-Retry	DDA	600 mA
TPS2375-1	802.3af	Auto-Retry	PW	400 mA
TPS2377-1	Legacy	Auto-Retry	D	400 mA
TPS2375	802.3af	Latch	PW, D	400 mA
TPS2376	Adjustable	Latch	PW, D	400 mA
TPS2377	Legacy	Latch	PW, D	400 mA

(1) Packages codes as follows: D = S0, DDA = SO PowerPad, PW = TSSOP

DESCRIPTION

The 8-pin integrated circuit contains all of the features needed to develop a high power IEEE 802.3af style powered device (PD). The TPS2376-H offers a higher current limit and increased thermal dissipation capability over the TPS237X family of devices. The TPS2376-H implements a fully compliant PoE interface while permitting non-standard implementations that draw more power. A 26 W PD may be constructed when working from a 52 V minimum PSE over 100 m of CAT-5 cable. The TPS2376-H features a 100 V rating, 600 mA capability, adjustable inrush limiting, fault protection with auto-retry, and true open-drain power-good functionality.

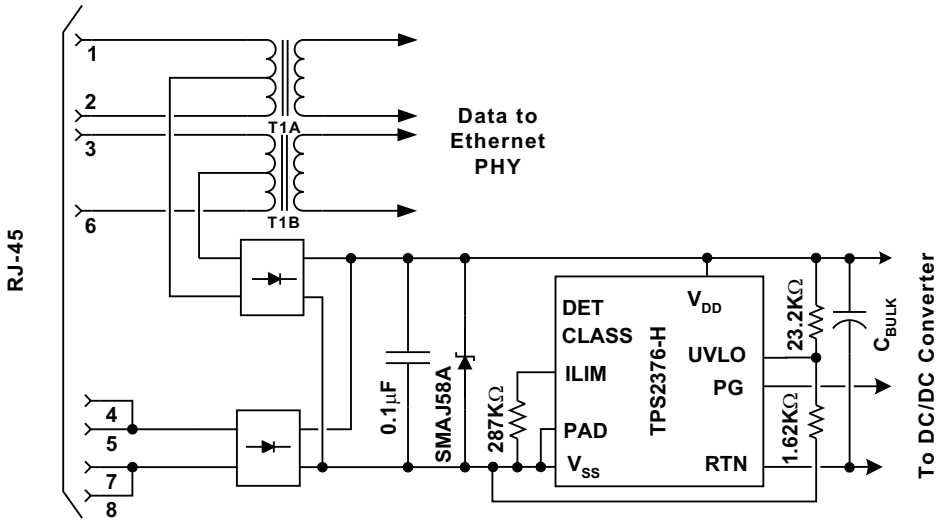


Figure 1. Typical Application Circuit

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS

T_A	UVLO THRESHOLDS (NOMINAL)			PACKAGE(1)	MARKING
	TYPE	LOW	HIGH	SO-8 PowerPad	
-40°C to 85°C	Adjustable	1.93 V	2.49 V	TPS2376DDA-H	2376-H

(1) Add an R suffix to the device type for tape and reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1), voltages are referenced to $V_{(VSS)}$

			TPS2376-H
	Voltage	VDD, RTN(2), DET, PG	-0.3 V to 100 V
		ILIM, UVLO	-0.3 V to 10 V
		CLASS	-0.3 V to 12 V
	Current, sinking	RTN(3)	Internally Limited
		PG	0 to 5 mA
		DET	0 to 1 mA
	Current, sourcing	CLASS	0 to 50 mA
		ILIM	0 to 1 mA
	ESD	Human body model	2 kV
		System level (contact/air) at RJ-45(4)	8/15 kV
T_J	Maximum junction temperature range		Internally limited
T_{stg}	Storage temperature range		-65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) $I_{(RTN)} = 0$
(3) SOA limited to $V_{(RTN)} = 80$ V and $I_{(RTN)} = 900$ mA.
(4) Surges applied to RJ-45 of Figure 1 between pins of RJ-45, and between pins and output voltage rails per EN61000-4-2, 1999.

DISSIPATION RATING TABLE(1)

PACKAGE(2)	θ_{JA} (Modified HIGH-K) °C/W	θ_{JA} (Modified LOW-K) °C/W	θ_{JA} (Best) ° C/W
DDA	58.6	50	45

(1) Tested per JEDEC JESD51, natural convection. The definitions of high-k and low-k are per JESD 51-7 and JESD 51-3. Modified low-k (2 signal - no plane, 3 in. by 3 in. board, 0.062 in. thick, 1 oz. copper) test board with the pad soldered, and an additional 0.12 $in.^2$ of top-side copper added to the pad. Modified high-k is a (2 signal – 2 plane) test board with the pad soldered. The best case thermal resistance is obtained using the recommendations per SLMA002 (2 signal - 2 plane with the pad connected to the plane).
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
	Input voltage range	VDD, PG, RTN	0	57	V
	Operating current range (sinking)	RTN	0	600	mA
	Classification resistor(1)	CLASS	255	4420	Ω
$R_{(ILIM)}$	Inrush limit program resistor (1)		125	1000	kΩ
	Sinking current	PG	0	2	mA
T_J	Operating junction temperature	$I_{RTN} \le 400$ mA	-40	125	°C
		400 mA < $I_{RTN} \le 600$ mA(2)	-40	105	
T_A	Operating free–air temperature		-40	85	°C

(1) Voltage should not be externally applied to CLASS and ILIM.
(2) Temperature limitation is for 10 year life-expectancy at this temperature. Short-term operation to 125 °C is permissable.

ELECTRICAL CHARACTERISTICS

$V_{(VDD)}$ = 48 V, $R_{(DET)}$ = 24.9 kΩ, $R_{(CLASS)}$ = 255 Ω, $R_{(ILIM)}$ = 287 kΩ, and –40°C ≤ T_J ≤ 125°C, unless otherwise noted. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to VSS unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DETECTION							
	Offset current	DET open, $V_{(VDD)} = V_{(RTN)}$ = 1.9 V, measure $I_{(VDD)} + I_{(RTN)}$			0.3	3	µA
	Sleep current	DET open, $V_{(VDD)} = V_{(RTN)}$ = 10.1 V, measure $I_{(VDD)} + I_{(RTN)}$			4	12	µA
	DET leakage current	$V_{(DET)} = V_{(VDD)}$ = 57 V, measure $I_{(DET)}$			0.1	5	µA
	Detection current	$V_{(RTN)} = V_{(VDD)}$, $R_{(DET)}$ = 24.9 kΩ, measure $I_{(VDD)} + I_{(RTN)} + I_{(DET)}$	$V_{(VDD)}$ = 1.4 V	53.7	56	58.3	µA
			$V_{(VDD)}$ = 10.1 V	395	410	417	µA
CLASSIFICATION							
$I_{(CLASS)}$	Classification current(1)	Measure $I_{(VDD)} + I_{(RTN)}$, 13 V ≤ $V_{(VDD)}$ ≤ 21 V, $V_{(VDD)} = V_{(RTN)}$					mA
		$R_{(CLASS)}$ = 4420 Ω		2.2	2.4	2.8	
		$R_{(CLASS)}$ = 953 Ω		10.3	10.6	11.3	
		$R_{(CLASS)}$ = 549 Ω		17.7	18.3	19.5	
		$R_{(CLASS)}$ = 357 Ω		27.1	28	29.5	
		$R_{(CLASS)}$ = 255 Ω		38	39.4	41.2	
$V_{(CL\_ON)}$	Classification lower threshold	Regulator turns on, $V_{(VDD)}$ rising		10.2	11.3	13	V
		Hysteresis		1.6	1.8	1.95	
$V_{(CU\_OFF)}$	Classification upper threshold	Regulator turns off, $V_{(VDD)}$ rising		21	21.9	23	V
$V_{(CU\_H)}$		Hysteresis		0.5	0.78	1	V
I_{lkg}	Leakage current	$V_{(CLASS)}$ = 0 V, $V_{(VDD)}$ = 57 V				1	µA
PASS DEVICE							
$r_{DS(on)}$	On resistance				0.58	1	Ω
	Leakage current	$V_{(VDD)} = V_{(RTN)}$ = 30 V				15	µA
	Current limit	$V_{(RTN)}$ = 1 V		625	765	900	mA
$I_{(LIM)}$	Inrush limit	$V_{(RTN)}$ = 2 V, $R_{(ILIM)}$ = 178 kΩ		160	224	296	mA
	Inrush current termination (2)	$V_{(RTN)}$ falling, $R_{(ILIM)}$ = 287 kΩ, inrush state→normal operation		85%	91%	100%	
	Leakage current, ILIM	$V_{(VDD)}$ = 15 V, $V_{(UVLO)}$ = 0 V				1	µA

(1) Classification is tested with exact resistor values. A 1% tolerance classification resistor ensures compliance with IEEE 802.3af limits.
(2) This parameter specifies the RTN current value, as a percentage of the steady state inrush current, below which it must fall to make PG assert (open-drain).

ELECTRICAL CHARACTERISTICS (continued)

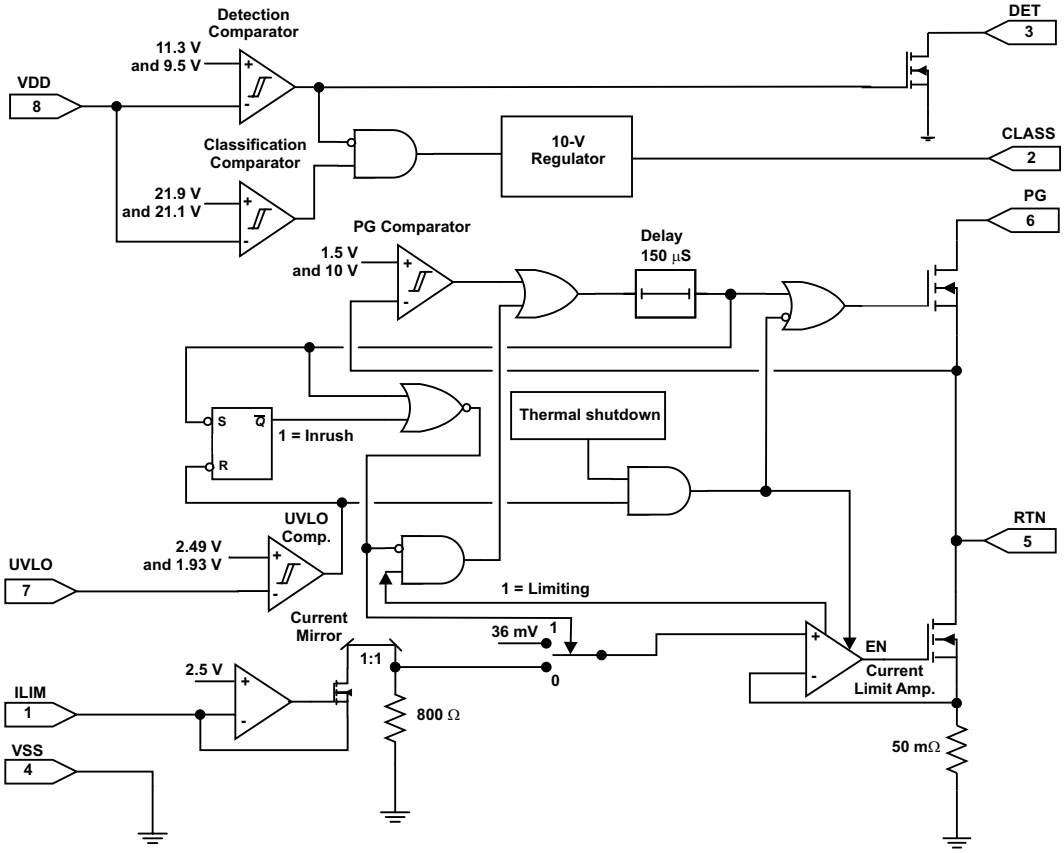
$V_{(VDD)}$ = 48 V, $R_{(DET)}$ = 24.9 kΩ, $R_{(CLASS)}$ = 255 Ω, $R_{(ILIM)}$ = 287 kΩ, and –40°C ≤ T_J ≤ 125°C, unless otherwise noted. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to VSS unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PG						
	Voltage threshold rising (3)	$V_{(RTN)}$ rising	9.5	10	10.5	V
	PG deglitch	Delay rising and falling PG	75	150	225	µs
	Output low voltage	$I_{(PG)}$ = 2 mA, $V_{(RTN)}$ = 34 V, $V_{(VDD)}$ = 38 V, $V_{(RTN)}$ falling		0.12	0.4	V
		$I_{(PG)}$ = 2 mA, $V_{(RTN)}$ = 0 V, $V_{(VDD)}$ = 25 V		0.12	0.4	V
	Leakage current	$V_{(PG)}$ = 57 V, $V_{(RTN)}$ = 0 V		0.1	1	µA
UVLO						
$V_{(UVLO\_R)}$	Voltage at UVLO - TPS2376-H	$V_{(UVLO)}$ rising	2.43	2.49	2.57	V
$V_{(UVLO\_F)}$		$V_{(UVLO)}$ falling	1.87	1.93	1.98	
		Hysteresis	0.53	0.56	0.58	
THERMAL SHUTDOWN						
	Shutdown temperature	Temperature rising	135			°C
	Hysteresis			20		°C
BIAS CURRENT						
	Operating current	$I_{(VDD)}$		240	450	µA

(3) Start with $V_{(RTN)}$ = 0 V, then increase $V_{(RTN)}$ until PG switches. Measure before thermal shutdown occurs.

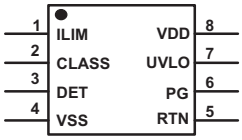
DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM



DEVICE INFORMATION (continued)

TPS2376-H
(TOP VIEW)



TERMINAL FUNCTIONS

PIN NAME	PIN NUMBER '76-H	I/O	DESCRIPTION
ILIM	1	O	Connect a resistor from ILIM to VSS to set the start-up inrush current limit. The equation for calculating the resistor is shown in the detailed pin description section for ILIM.
CLASS	2	O	Connect a resistor from CLASS to VSS to set the classification of the powered device (PD). The IEEE classification levels and corresponding resistor values are shown in Table 1.
DET	3	O	Connect a 24.9-kΩ detection resistor from DET to VDD.
VSS	4	I	Return line on the source side of the TPS2376-H from the PSE.
RTN	5	O	Switched output side return line used as the low-side reference for the TPS2376-H load.
PG	6	O	Open-drain, power-good output, active high, referenced to RTN.
UVLO	7	I	UVLO comparator input that controls pass-device turn-on and off. Connect UVLO to a resistor divider from VDD to VSS.
VDD	8	I	Positive line from the rectified PSE provided input.
PowerPad™	-	I	The PowerPad must be connected to VSS. The VSS copper on the circuit board must be a large fill area to assist in heat dissipation.

Detailed Pin Description

The following descriptions refer to the schematic of Figure 1 and the functional block diagram.

ILIM: A resistor from this pin to VSS sets the inrush current limit per Equation 1:

$$I_{(LIM)} = \frac{40000}{R_{(ILIM)}} \quad (1)$$

where ILIM is the desired inrush current value, in Amperes, and $R_{(ILIM)}$ is the value of the programming resistor from ILIM to VSS, in ohms. The practical limits on $R_{(ILIM)}$ are 125 kΩ to 1 MΩ. A value of 287 kΩ is recommended for compatibility with legacy power sourcing equipment (PSE).

Inrush current limiting prevents current drawn by the bulk capacitor from causing the line voltage to sag below the lower UVLO threshold. Adjustable inrush current limiting allows the use of arbitrarily large capacitors and also accommodates legacy systems that require low inrush currents.

The ILIM pin must not be left open or shorted to VSS.

CLASS: Classification is implemented by means of an external resistor, $R_{(CLASS)}$, connected between CLASS and VSS. The controller draws current from the input line through $R_{(CLASS)}$ when the input voltage lies between 13 V and 21 V. The classification currents specified in the electrical characteristics table include the bias current flowing into VDD and any RTN leakage current.

A high power system will not meet the standard power CLASS ranges defined in IEEE 802.3af, which are shown for reference in Table 1. An end-to-end high power system may either redefine the CLASS power, or dispense with CLASS entirely.

The CLASS pin must not be shorted to ground.

Table 1. CLASSIFICATION - IEEE 802.3af values

CLASS	PD POWER (W)	$R_{(CLASS)}$ (Ω)	802.3af LIMITS (mA)	NOTE
0	0.44 – 12.95	4420 ±1%	0 - 4	Default class
1	0.44 – 3.84	953 ±1%	9 - 12	
2	3.84 – 6.49	549 ±1%	17 - 20	
3	6.49 – 12.95	357 ±1%	26 - 30	
4	-	255 ±1%	36 - 44	Reserved for future use

DET: $R_{(DET)}$ should be connected between VDD and the DET pin when it is used. $R_{(DET)}$ is connected across the input line when $V_{(VDD)}$ lies between 1.4 V and 11.3 V, and is disconnected when the line voltage exceeds this range to conserve power.

The parallel combination of $R_{(DET)}$ and the UVLO program resistors must equal 24.9 kΩ, ±1%. Minimizing $R_{(DET)}$, and maximizing the UVLO program resistors, improves efficiency during normal operation. Conversely, $R_{(DET)}$ may be eliminated with the UVLO divider providing the 24.9 kΩ signature to reduce component count.

VSS: This is the input supply negative rail that serves as a local ground. The PowerPad must be connected to this pin.

RTN: This pin provides the switched negative power rail used by the downstream circuits. The operational and inrush current limit control current into the pin. The PG circuit monitors the RTN voltage and also uses it as the return for the PG pin pulldown transistor. The internal MOSFET body diode clamps VSS to RTN when voltage is present between VDD and RTN and the Power-over-Ethernet (PoE) input is not present.

PG: This pin goes to a high resistance state when the internal MOSFET that feeds the RTN pin is enabled, and the device is not in inrush current limiting. In all other states except detection, the PG output is pulled to RTN by the internal open-drain transistor. Performance is ensured with at least 4 V between VDD and RTN.

PG is an open-drain output, which may require a pullup resistor or other interface to the dc/dc converter. PG may be left open if not used.

UVLO: The UVLO pin is used with an external resistor divider between VDD and VSS to set the upper and lower UVLO thresholds. The TPS2376-H enables the output when $V_{(UVLO)}$ exceeds the upper UVLO threshold, and turns it off when the input falls below the lower threshold.

The UVLO divider resistance may be used alone to provide the 24.9 kΩ detection signature, or be used in conjunction with $R_{(DET)}$. Eliminating $R_{(DET)}$ reduces the component count at the cost of lower operating efficiency. Figure 1 demonstrates the elimination of $R_{(DET)}$.

VDD: This is the positive input supply that is also common to downstream load circuits. This pin provides operating power and allows the controller to monitor the line voltage to determine the mode of operation.

TYPICAL CHARACTERISTICS

Graphs over temperature are interpolations between the marked data points.

$I_{(VDD)}$ + $I_{(RTN)}$ IN DETECTION

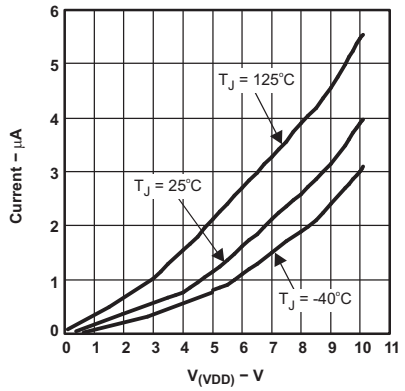


Figure 2.

PD DETECTION RESISTANCE vs $V_{(PI)}$

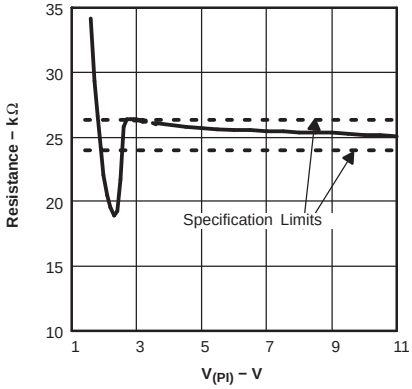


Figure 3.

CLASSIFICATION TURN ON VOLTAGE vs TEMPERATURE

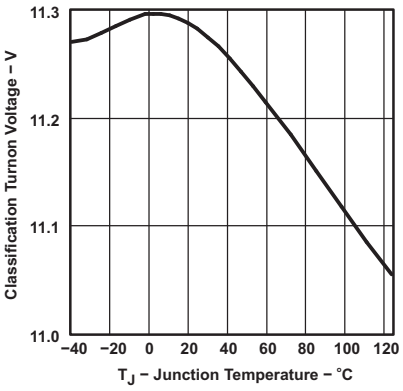


Figure 4.

CLASSIFICATION TURN OFF VOLTAGE vs TEMPERATURE

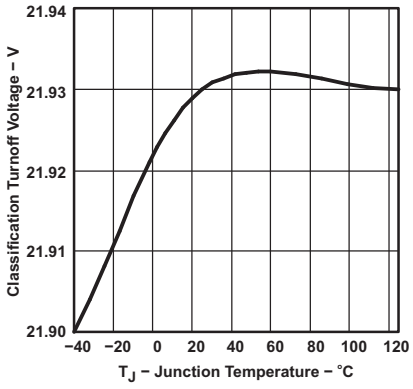


Figure 5.

$I_{(VDD)}$ vs VDD

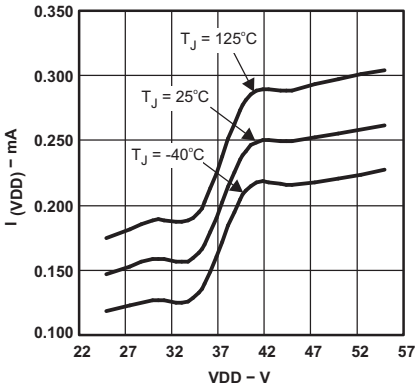


Figure 6.

PASS DEVICE RESISTANCE vs TEMPERATURE

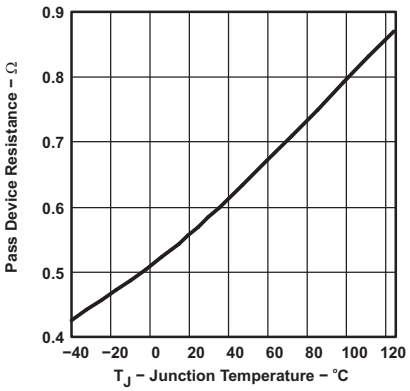


Figure 7.

UVLO RISING vs TEMPERATURE

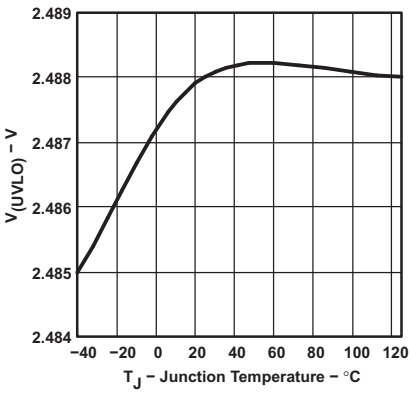


Figure 8.

UVLO FALLING vs TEMPERATURE

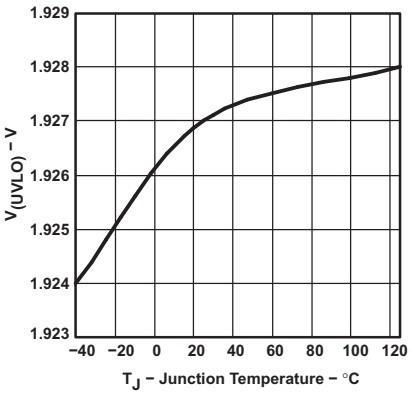


Figure 9.

INRUSH CURRENT vs TEMPERATURE

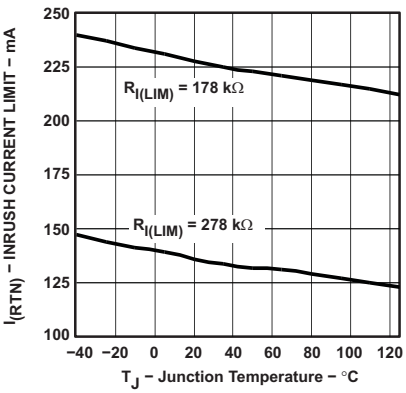


Figure 10.

TYPICAL CHARACTERISTICS (continued)

Graphs over temperature are interpolations between the marked data points.

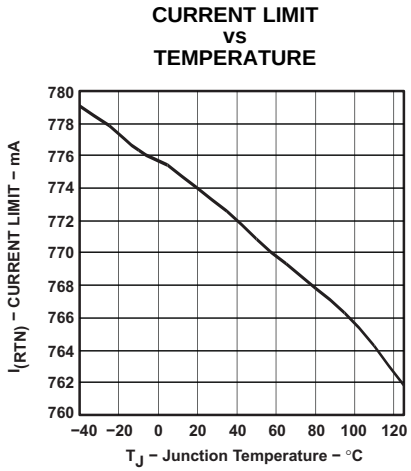


Figure 11.

APPLICATION INFORMATION

OVERVIEW

The IEEE 802.3af specification defines a process for safely providing power over an ethernet cable when a capable device is connected, and then removing power if it is disconnected. The process proceeds through three operational states: detection, classification, and operation. An unterminated cable is not powered. The PSE periodically probes the cable with low voltage, looking for a 25 kΩ signature; this is referred to as detection. The low power levels used during detection are unlikely to cause damage to devices not designed for PoE. If a valid powered device (PD) signature is present during detection, then the PSE may optionally inquire about the amount of power the PD requires; this is referred to as classification. The PD may return a default full-power signature, or one of four other defined choices. In a high-power system, class may not be required, or the levels may be redefined to suit that particular system. The PSE may use the class power to determine if it has adequate power to operate this device, and later to determine if a device is using more power than it requested. At this point in the process, the PSE may choose to power the PD. The PSE output is protected against shorts and overloads when the PD is powered. The maintain power signature (MPS) is presented by the powered PD to assure the PSE that it is present. The MPS is either a minimum dc current, a maximum ac impedance, or both. When the MPS disappears, the PSE removes power and returns to its initial state. Figure 12 shows the operational states as a function of PD input voltage range as defined in IEEE 802.3af.

The PD input is typically an RJ-45 (8-pin) connector, referred to as the power interface (PI). PD input requirements differ from PSE output requirements to account for voltage drops in the cable. The IEEE 802.3af specification uses a cable resistance of 20 Ω to derive the voltage limits at the PD from the PSE output requirements. While the 20 Ω specification covers telecom type wiring, CAT-5 infrastructure will meet a 12.5 Ω limit. Specifying the high-power system to operate over CAT-5 cable allows significantly more power to be delivered.

A high-power nonstandard system need not support all combinations of voltage delivery polarities and pair sets. The IEEE 802.3af PSE allows voltage of either polarity between the RX and TX pairs, or between the two spare pairs. An input diode or bridge is recommended to provide reverse input polarity protection. The bridge maintains compatibility with auto-MDIX systems that have reverse RX-TX pair assignments. The voltage drops associated with the input diode(s) cause a difference between the limits at the PI and the TPS2376-H specifications.

Two-pair power delivery is the simplest to implement, and is preferred if adequate power can be achieved. Application report SLVA225 presents a number of considerations for a high power PoE end-to-end system. Power delivery on all four pairs is significantly more complex, and is only recommended when two pair systems do not suffice. Considerations for high power systems are presented in Application Report SLVA225.

The following discussion is intended as an aid in understanding the operation of the TPS2376-H, but not as a substitute for the IEEE 802.3af standard. Standards change and should always be referenced when making design decisions.

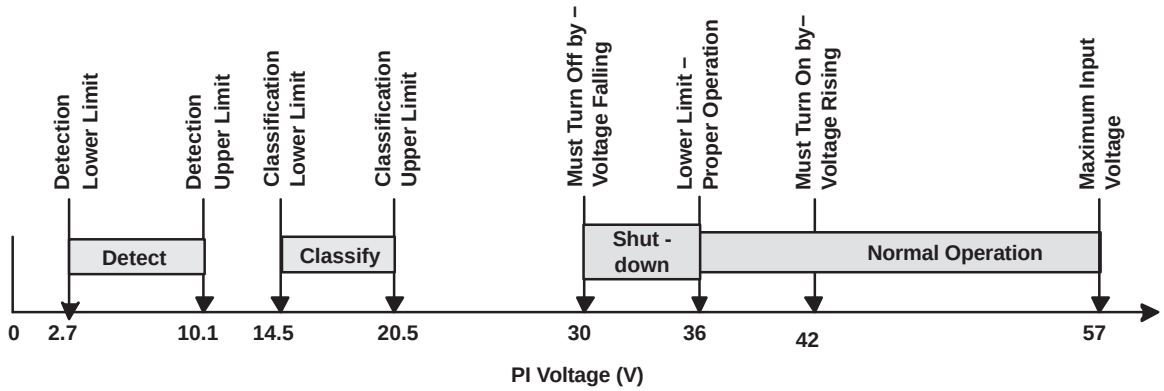


Figure 12. IEEE 802.3 PD Voltage Limits

APPLICATION INFORMATION (continued)

INTERNAL THRESHOLDS

In order to implement the defined PoE functions shown in Figure 12, the TPS2376-H has a number of internal comparators with hysteresis for stable switching between the various states. Figure 13 relates the parameters in the Electrical Characteristics section to the PoE states. The mode labeled *idle* between classification and PD powered implies that the DET, CLASS, PG, and RTN pins are all high impedance.

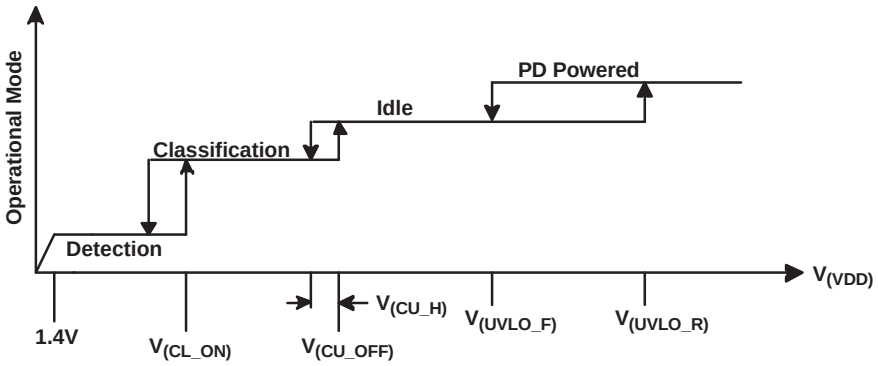


Figure 13. Threshold Voltages

DETECTION

The 25 kΩ PD signature is measured by applying two voltages between 2.7 V to 10.1 V, that are at least 1 V apart, to the PD's PI and measuring the current. The resistance is calculated as a $\Delta V/\Delta I$, with an acceptable range of 23.75 kΩ to 26.25 kΩ.

The TPS2376-H is in detection mode whenever the supply voltage is below the lower classification threshold. The TPS2376-H draws a minimum of bias power in this condition, while PG and RTN are high impedance and the circuits associated with ILIM and CLASS are disabled. The DET pin is pulled to VSS during detection. Current flowing through $R_{(DET)}$ to VSS (Figure 1) produces the detection signature.

CLASSIFICATION

The classification process applies a voltage between 14.5 V and 20.5 V, for a maximum of 75 ms, to the input of the PD, which in turn draws a fixed current set by $R_{(CLASS)}$. An 802.3af PSE measures the PD current to determine which of the five available classes (Table 1) that the PD is signaling. The total current drawn from the PSE during classification is the sum of bias currents and current through $R_{(CLASS)}$. The TPS2376-H disconnects $R_{(CLASS)}$ at voltages above the classification range to avoid excessive power dissipation (Figure 12 and Figure 13).

A high power end-to-end system may choose to not implement classification, or redefine the power associated with each class. Low-voltage systems, for example 24 V, may not be able to use CLASS because the operational voltage may lie within the classification voltage range. This would cause the TPS2376-H classification circuits to dissipate power continuously.

The power rating of the class resistor should be chosen so that it is not overstressed for the required 75-ms classification period, during which 10 V is applied. A higher wattage resistor might be required to withstand testing over longer time periods.

UNDERVOLTAGE LOCKOUT (UVLO)

The TPS2376-H incorporates an undervoltage lockout (UVLO) circuit that monitors line voltage to determine when to apply power to the downstream load and allow the PD to power up. The IEEE 802.3af specification dictates a maximum PD turn on voltage of 42 V and a minimum turn-off voltage of 30 V (Figure 13). The UVLO pin provides the flexibility to adjust the turn on and turn off to the IEEE 802.3af limits, or a custom set. Design the turn-on for 39.5 V if a design which uses the IEEE 802.3af limits is desired.

APPLICATION INFORMATION (continued)

PROGRAMMABLE INRUSH CURRENT LIMIT AND FIXED OPERATIONAL CURRENT LIMIT

Inrush limiting has several benefits. First, it maintains the cable voltage above the UVLO turn-off threshold as the bulk capacitor charges. Second, it keeps the PSE from going into current limit. This reduces stress on the PSE and allows an arbitrarily large bulk capacitor to be charged. Third, the inrush limit is used as the foldback current during a hard overload.

The TPS2376-H operational current limit protects the internal power switch from sudden output faults and current surges. The minimum operational current limit level of 625 mA lies above the minimum TPS23841 output current limit of 600 mA. This current limit enables the PD to draw the maximum available power.

The TPS2376-H incorporates a state machine that controls the inrush and operational current limit states. When $V_{(VDD)}$ is below the lower UVLO threshold, the current limit state machine is reset. In this condition, the RTN pin is high impedance, and floats to $V_{(VDD)}$ once the output capacitor is discharged. When $V_{(VDD)}$ rises above the UVLO turn on threshold, the TPS2376-H enables the internal power MOSFET with the current limit set to the inrush value programmed by $R_{(ILIM)}$. The load capacitor charges and the RTN pin voltage falls from $V_{(VDD)}$ to nearly $V_{(VSS)}$. Once the inrush current falls about 10% below the programmed limit for 150-µs, the current limit switches to the 765-mA operational level and PG goes open-drain. The internal power MOSFET is disabled if the input voltage drops below the lower UVLO threshold and the state machine is reset.

An output overload, or increasing input voltage step, may cause the operational current limit to become active. The MOSFET voltage will then start to rise, causing high power dissipation. Current-limit foldback controls this MOSFET power dissipation to a manageable level. Foldback is achieved by switching the current limit state machine from the operational level to inrush when the MOSFET voltage exceeds 10 V for 150-µs. An additional layer of protection is provided by thermal shutdown if the overload persists long enough.

Practical values of $R_{(ILIM)}$ lie between 125 kΩ and 1 MΩ; however, selecting lower inrush current values reduces peak stresses under output-short circuit conditions. An inrush level of 140 mA, set by an $R_{(ILIM)}$ of 287 kΩ, is recommended for most applications.

THERMAL PROTECTION

The TPS2376-H may overheat if the ambient temperature becomes excessive, or if it operates for an extended period of time in classification or current limit. The TPS2376-H protects itself by disabling the RTN and CLASS pins and pulling PG low when the internal die temperature reaches about 140°C. It automatically restarts when the die temperature has fallen approximately 20°C. If $V_{(RTN-VSS)}$ is less than 10 V when the TPS2376-H restarts, the current limit remains at 765 mA and PG goes open-drain. If the overload has caused $V_{(RTN-VSS)}$ to exceed 10 V while disabled, the current limit is set to the inrush level and PG remains low. This process is referred to as thermal cycling. Thermal protection is active whenever the TPS2376-H is not in detection.

Short periods of thermal cycling do not significantly impact the reliability or life expectancy, but prolonged periods may. Other components in the power path can be overstressed if this condition exists for a prolonged time as well.

MAINTAIN POWER SIGNATURE

Once a valid PD has been detected and powered, the PSE uses the maintain power signature (MPS) to determine when to remove power from the PI. The PSE removes power from that output port if it detects loss of MPS for 300 ms or more. A valid MPS requires that the PD to draw at least 10 mA and have an ac impedance less than 26.25 kΩ in parallel with 0.05 µF.

POWER GOOD

The TPS2376-H includes a power-good (PG) output for use as a dc/dc converter enable once the load capacitor is fully charged. The PG pin is the safest way to ensure that there are no undesired interactions between the inrush limit, the converter startup characteristic, and the size of the bulk capacitor.

The PG output is pulled to RTN whenever the MOSFET is disabled, is in inrush current limiting, or the $V_{(RTN)}$ rises above 10 V. The PG pin goes to an open-drain state approximately 150 µs after the inrush current falls 10% below the regulated value. PG pull down current is only specified for $V_{(VDD-RTN)}$ greater than 4 V, below which the dc/dc converter should not be able to operate. The PG interface to the downstream dc/dc converter is simplified by referencing it to RTN.

APPLICATION INFORMATION (continued)

The PG pin can be left open if it is not used.

DC/DC CONVERTER STARTUP

The PSE and TPS2376-H are power and current limited sources, which imposes certain constraints on the PD power supply design. Improper design of the system can prevent PD startup with some combinations of Ethernet lines and PSE sources. The root of most startup problems revolves around the dc/dc converter.

Dc/dc converters have a constant input power characteristic that causes them to draw high currents at low voltage. Also, a converter may draw in excess of 125% of its rated power during startup when the output voltage approaches its regulated value, and the output capacitors are charging while the load draws its full power. These characteristics lead to two undesired events. First, if the converter starts up during inrush, it can draw more current than available from the TPS2376-H and cause the startup cycle to fail. Second, if the converter startup current exceeds the TPS2376-H current limit, it may discharge the bulk capacitor until $V_{(RTN-VSS)}$ exceeds 10 V and forces the TPS2376-H into inrush.

The following guidelines should be used:

1. Set the TPS2376-H inrush to a moderate value such as 140 mA.
2. Hold the dc/dc converter off during inrush using PG.
3. Implement a softstart that keeps the peak start-up current below 600 mA, and preferably only a modest amount over the operating current, at the minimum PSE voltage and maximum feed resistance.
4. If step 3 cannot be met, the bulk input capacitor should not discharge more than 8 V during start-up at the minimum PSE voltage and maximum feed resistance. Start-up must be completed in less than 50 ms.

Step 4 requires a balance between the converter output capacitance, load, and input bulk capacitance. While there are some cases which may not require all these measures, it is always a good practice to follow them.

Downstream converters that use PG control are turned off during a hard fault or thermal cycle, and will go through an orderly restart once the bulk capacitor is recharged. Converters that do not use PG need to permit a restart by either drawing less current than the inrush current limit provides, or by disabling long enough to allow the bulk capacitor to recharge. A converter that has bootstrap startup can be designed to accomplish this goal.

AUXILIARY POWER SOURCE ORING

Many PoE-capable devices are designed to operate from either a wall adapter or PoE power. A local power solution adds cost and complexity, but allows a product to be used regardless of PoE availability. Attempting to create solutions where the two power sources coexist in a specific controlled manner results in additional complexity, and is not generally recommended. Figure 14 demonstrates three methods of diode ORing external power into a PD. Option 1 inserts power on the output side of the PoE power conversion. Option 2 inserts power on the TPS2376-H output. Option 3 applies power to the TPS2376-H input. Each of these options has advantages and disadvantages. The wall adapter must meet a minimum 1500-Vac dielectric withstand test voltage to the ac input power and to ground for options 2 and 3.

APPLICATION INFORMATION (continued)

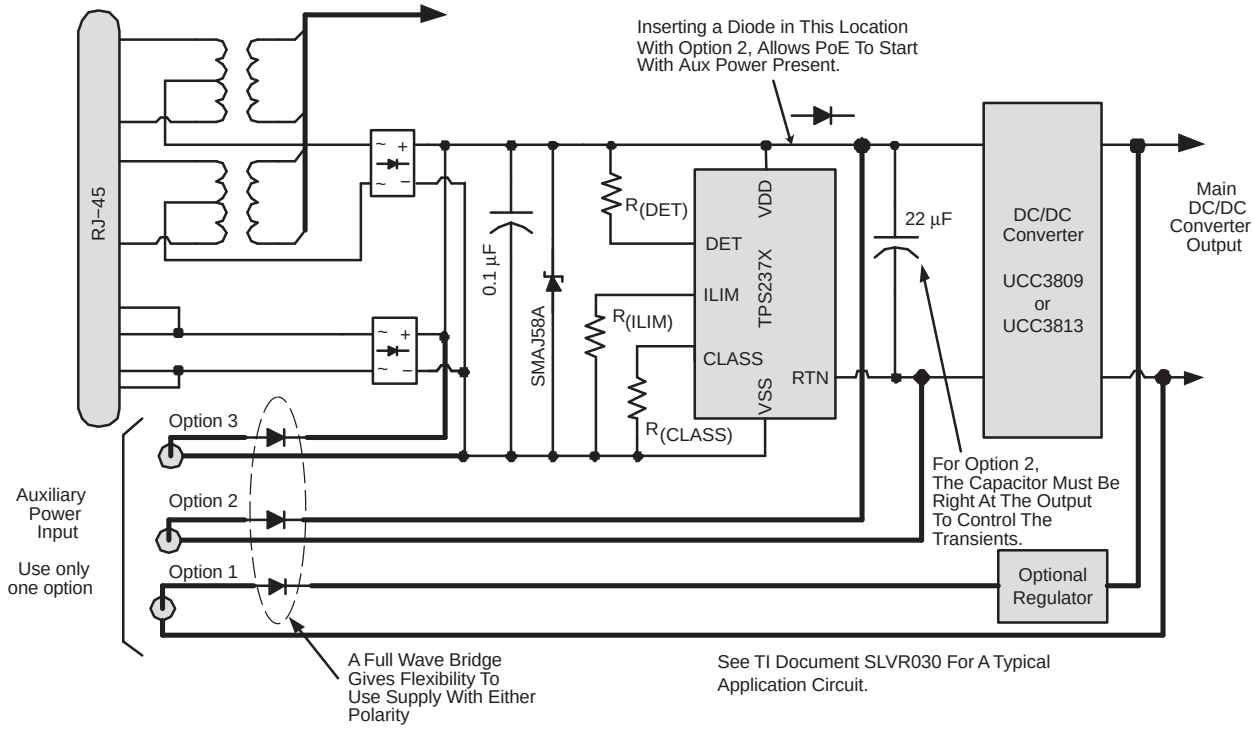


Figure 14. Auxiliary Power ORing

Option 1 consists of ORing power to the output of the PoE dc/dc converter. This option is preferred in cases where PoE is added to an existing design that uses a low-voltage wall adapter. The relatively large PD capacitance reduces the potential for harmful transients when the adapter is plugged in. The wall adapter output may be grounded if the PD incorporates an isolated converter. This solution requires two separate regulators, but low-voltage adapters are readily available. The PoE power can be given priority by setting its output voltage above the adapter's.

Option 2 has the benefits that the adapter voltage may be lower than the TPS2376-H UVLO, and that the bulk capacitor shown controls voltage transients caused by plugging an adapter in. The capacitor size and location are chosen to control the amount of ringing that can occur on this node, which can be affected by additional filtering components specific to a dc/dc converter design. The optional diode blocks the adapter voltage from reverse biasing the input, and allows a PoE source to supply power provided that the PSE output voltage is greater than the adapter voltage. The penalty of the diode is an additional power loss when running from PSE power. The PSE may not be able to detect and start powering without the diode. This means that the adapter may continue to power the PD until removed. Auxiliary voltage sources can be selected to be above or below the PoE operational voltage range. If automatic PoE precedence is desired when using the low-voltage auxiliary source option, make sure that the TPS2376-H inrush program limit is set higher than the maximum converter input current at its lowest operating voltage. It is difficult to use PG with the low-voltage auxiliary source because the converter must operate during a condition when the TPS2376-H would normally disable it. Circuits may be designed to force operation from one source or the other depending on the desired operation and the auxiliary source voltage chosen. However, they are not recommended because they increase complexity and thus cost.

Option 3 inserts the power before the TPS2376-H. The adapter output voltage must meet the TPS2376-H UVLO turn-on requirement and limit the maximum voltage to 57 V. This option provides a valid power-good signal and simplifies power priority issues. Option 3 is the most likely to create transient voltage problems when a powered adapter is plugged in. This causes the cabling inductance and PD input capacitance to ring to a high voltage that must be clamped by the TVS. If the adapter applies voltage to the PD before the PSE, it prevents the PSE from detecting the PD. If the PSE is already powering the PD when the adapter is plugged in, priority is given to the higher supply voltage.

APPLICATION INFORMATION (continued)

ESD

The TPS2376-H has been tested using the surge of EN61000-4-2 in evaluation circuit similar to Figure 1. The levels used were 8-kV contact discharge and 15-kV air discharge. Surges were applied between the RJ-45 and the outputs, and between an auxiliary power input jack and the dc outputs. No failures were observed.

ESD requirements for a unit that incorporates the TPS2376-H have much broader scope and operational implications than those used in TI's testing. Unit level requirements should not be confused with EVM testing that only validated the TPS2376-H.

EXTERNAL COMPONENTS

Detection Resistor and UVLO Divider

The UVLO divider shown in Figure 1 is suitable where elimination of the detection resistor is desirable and the IEEE 802.3af compatible turn on is desired. The upper resistor dissipates about 116 mW at 55.5 V (57 V minus 1.5 V for an input diode bridge) at the maximum input, and supports 52 V. An 0805 size resistor is recommended for this resistor while an 0603 size resistor is suitable for the lower resistor.

Improved efficiency is obtained by using a detection resistor along with high-value UVLO resistors. The maximum UVLO divider resistance may be determined by considering the effect of the UVLO pin leakage current. The error is equal to the leakage current times the parallel resistance of the divider resistors. This may be simplified for the 39.5 V turn-on case to the leakage current times the lower divider resistance. The maximum resistance is the error voltage divided by the leakage current. For a 0.5% error, the maximum resistance is (0.005 * 2.49 V) / 1 μA, or approximately 12.4 kΩ. A possible divider for a turn-on voltage of 39.5 V is 178 kΩ / 12.1 kΩ resulting in a turn-on voltage of 39.1 V. A suitable value for R_{DET} is 28.7 kΩ, yielding a detection resistance of 24.93 kΩ. The operating power loss at 55.5 V is 16 mW.

The input diode bridge's incremental resistance can be hundreds of ohms at the low currents seen at 2.7 V on the PI. The bridge resistance is in series with $R_{(DET)}$ and increases the total resistance seen by the PSE. This varies with the type of diode selected by the designer, and it is not usually specified on the diode data sheet. The value of $R_{(DET)}$ may be adjusted downwards to accommodate a particular diode type. The non-linear resistance of Figure 3 at low currents is the result of the diodes.

Magnetics

A high-power PoE system places additional burden on power extraction from data pairs. Data transmission properties must be maintained while carrying higher current and withstanding higher difference current between the conductors in a pair. This difference current is the result of unbalanced resistances between the conductors of a pair (see IEEE 802.3af annex 33E).

Either a higher current center-tapped transformer as shown in Figure 1, or the addition of a center-tapped inductor, can be implemented. Proper termination is required around the transformer to provide correct impedance matching and to avoid radiated and conducted emissions.

Input Diodes or Diode Bridges

The IEEE 802.3af requires the PD to accept power on either set of input pairs in either polarity. This requirement is satisfied by using two full-wave input bridge rectifiers as shown in Figure 1. The full configuration may not be required when a custom high-power system is implemented. Silicon p-n diodes with a 1-A or 1.5-A rating and a minimum breakdown of 100 V are recommended, however Schottky diodes will yield a somewhat lower power loss. Diodes exhibit large dynamic resistance under low-current operating conditions such as in detection. The diodes should be tested for their behavior under this condition. The total forward drops must be less than 1.5 V at 500 μA and at the lowest operating temperature.

Input Capacitor

The IEEE 802.3af requires a PD input capacitance between 0.05 μF and 0.12 μF during detection. This capacitor should be located directly adjacent to the TPS2376-H as shown in Figure 1. A 100-V, 10%, X7R ceramic capacitor meets the specification over a wide temperature range.

APPLICATION INFORMATION (continued)

Load Capacitor

The IEEE 802.3af specification requires that the PD maintain a minimum load capacitance of 5 μF.

A PD can fail the dc MPS requirement if the load current to capacitance ratio is too small. This is caused by having a long input current dropout after a drop in input voltage. The PD should begin to draw input current within 300 ms of an abrupt 13 V input droop.

A particular design may have a tendency to cause ringing at the RTN pin during startup, inadvertent hot-plugs of the PoE input, or plugging in a wall adapter. It is recommended that a minimum value of 1 μF be used at the output of the TPS2376-H if downstream filtering prevents placing the larger bulk capacitor right on the output. When using ORing option 2, it is recommended that a large capacitor such as a 22 μF be placed across the TPS2376-H output.

Transient Suppressor

Voltage transients on the TPS2376-H can be caused by connecting or disconnecting the PD, or by other environmental conditions like ESD. A transient voltage suppressor, such as the SMAJ58A, should be installed after the bridge and across the TPS2376-H input as shown in Figure 1.

Some form of protection may be required from $V_{(VDD-RTN)}$ if adequate capacitance is not present. RTN is a high impedance node when the MOSFET is off. Some topologies may cause large transients to occur on this pin when the PD is plugged into an active supply.

Layout

The layout of the PoE front end must use good practices for power and EMI/ESD. A basic set of recommendations include:

1. The parts placement must be driven by the power flow in a point-to-point manner such as RJ-45 → Ethernet interface → diode bridges → TVS and 0.1-μF capacitor → TPS2376-H → output capacitor.
2. There should not be any crossovers of signals from one part of the flow to another.
3. All leads should be as short as possible with wide power traces and paired signal and return.
4. Spacing consistent with safety standards like IEC60950 must be observed between the 48-V input voltage rails and between the input and an isolated converter output.
5. The TPS2376-H should be over a local ground plane or fill area referenced to VSS.
6. Large SMT component pads should be used on power dissipating devices such as the diodes and the TPS2376-H.

Use of generous copper area on VSS and to help the PCB spread and dissipate the heat is recommended. Assuming a worst-case power dissipation of 0.4 W, the required thermal resistance may be calculated as: $\theta_{JA} = (t_{J\_MAX} - t_{A\_MAX}) / P$. A thermal resistance of 50°C/W is required for a junction temperature of 105°C at an ambient of 85°C. The effect of additional local heating on the circuit board from other devices must be considered. The thermal resistance cases provided in the dissipation rating table should be used as a guide in determining the required area.

Figure 15 provides an example of a single sided layout with liberal copper plane areas to help spread the heat. The active circuit area could be reduced by locating the small resistors on the backside of the board. The TPS2376-H PowerPad is covered by copper fill, which has multiple vias to a backside mirror-image fill. There are 5 small vias under the PowerPad per the guidelines of SLMA0002 which are masked by the graphics of the tool. The fills for RTN and VDD also help spread the heat. A copper fill clearance of 0.030 inches was used for VDD to RTN or VSS. A spacing of 0.025 inches for the full PoE voltage was met elsewhere.

APPLICATION INFORMATION (continued)

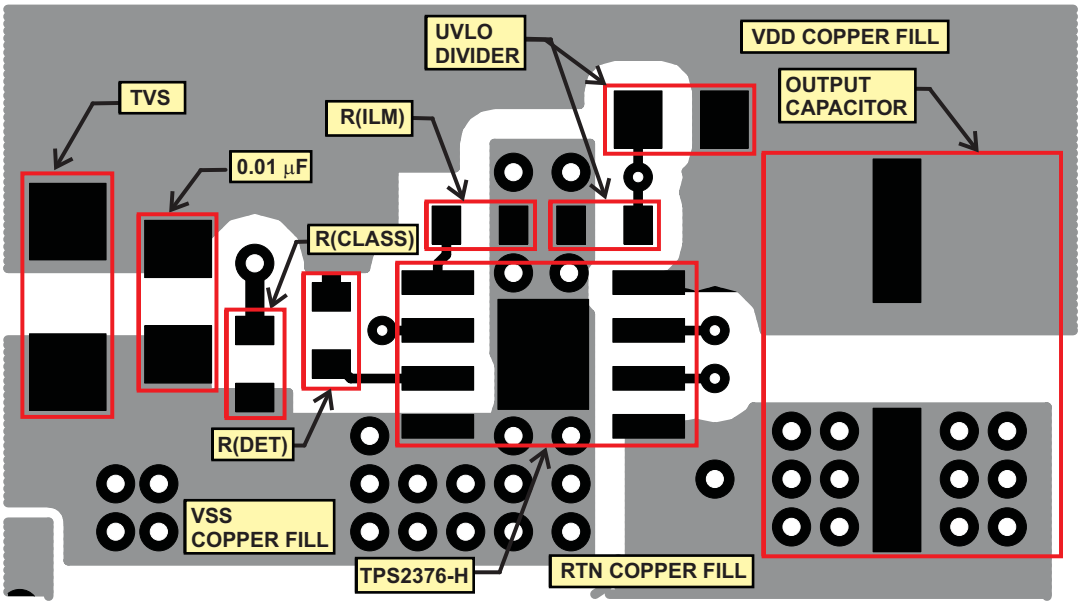


Figure 15. Layout Example

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS2376DDA-H	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2376H	Samples
TPS2376DDA-HG4	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2376H	Samples
TPS2376DDAR-H	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2376H	Samples
TPS2376DDAR-HG4	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2376H	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

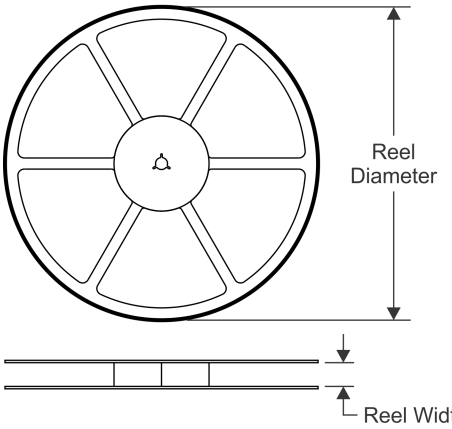
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

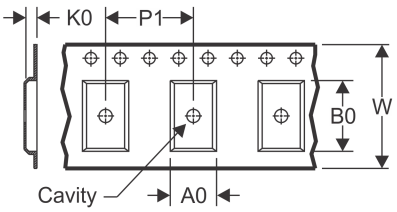
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

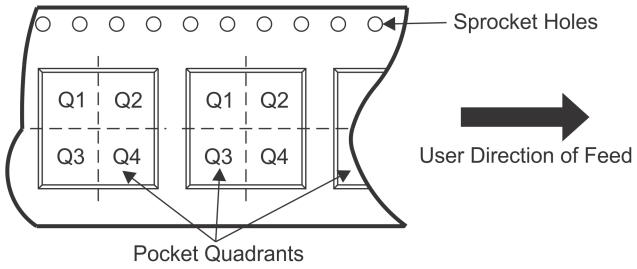


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

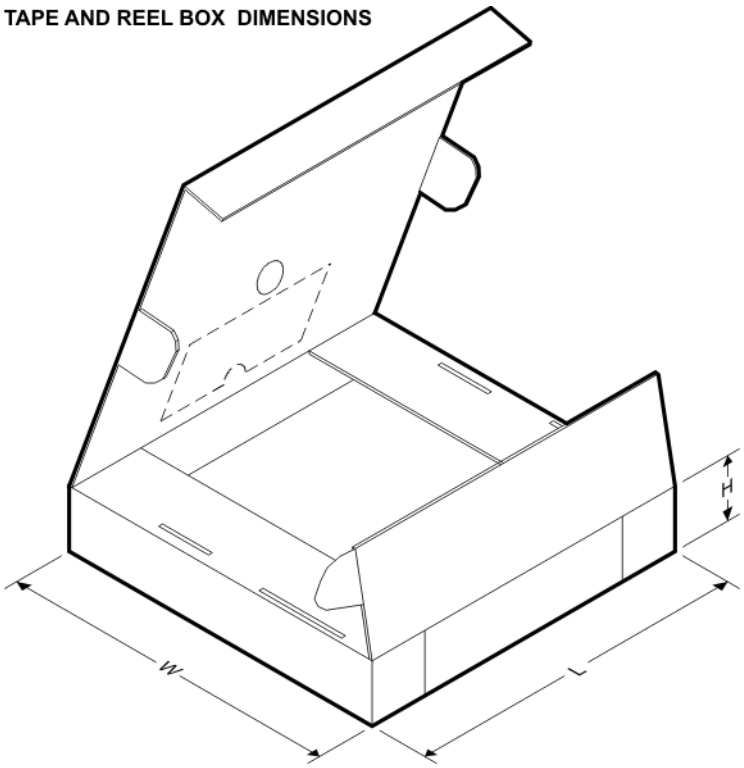
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2376DDAR-H	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

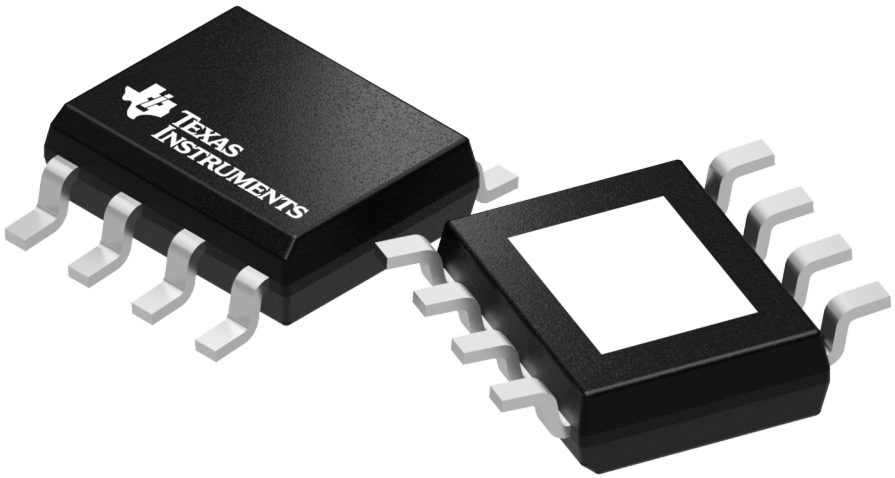


*All dimensions are nominal

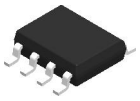
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2376DDAR-H	SO PowerPAD	DDA	8	2500	358.0	335.0	35.0

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

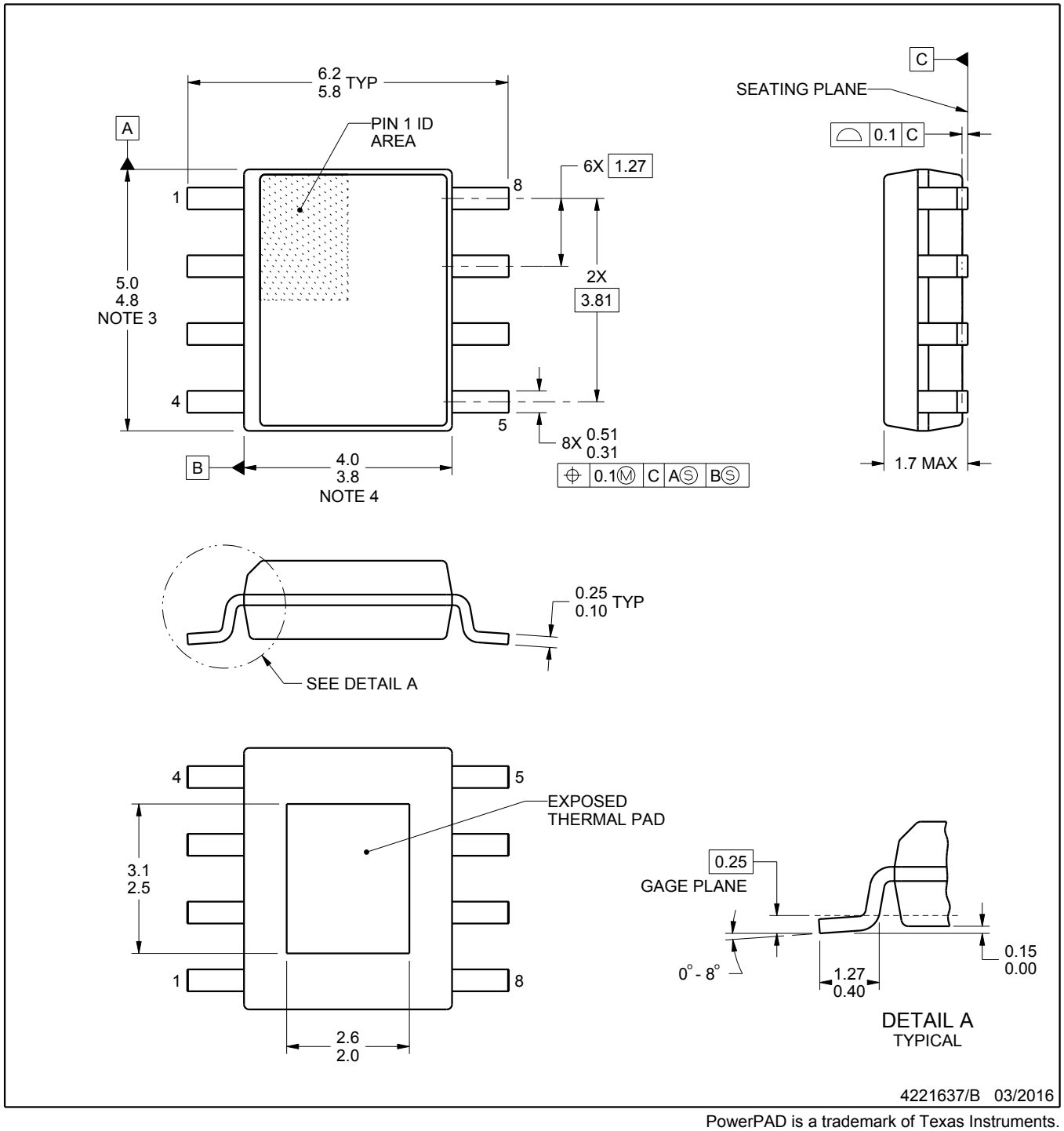


PACKAGE OUTLINE

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

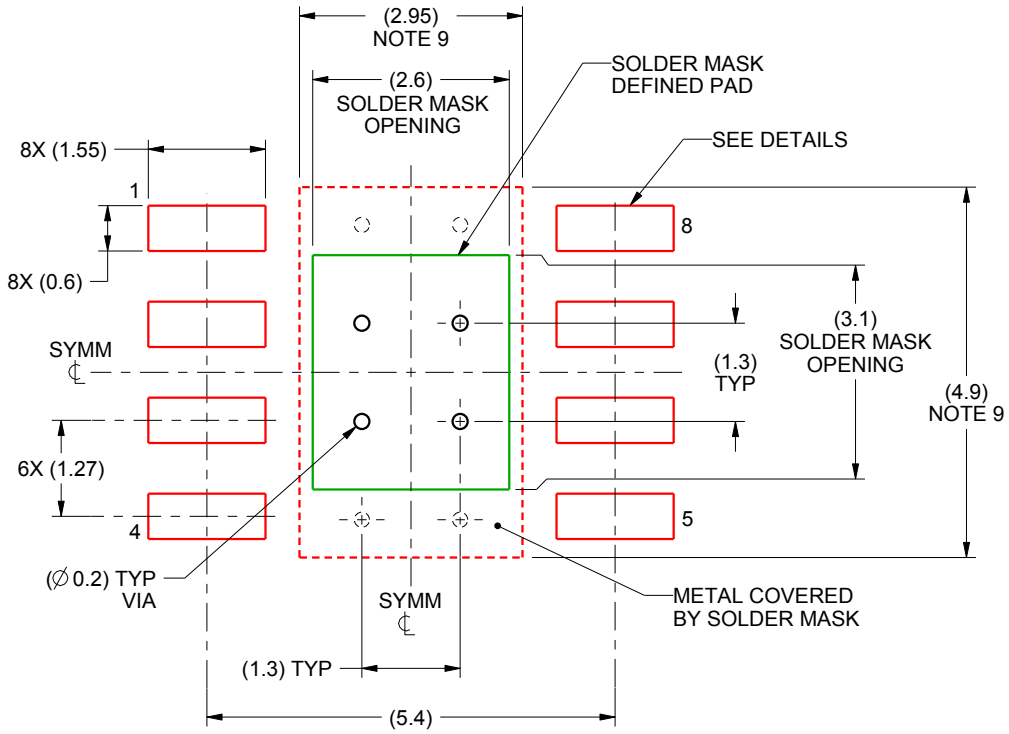
PLASTIC SMALL OUTLINE



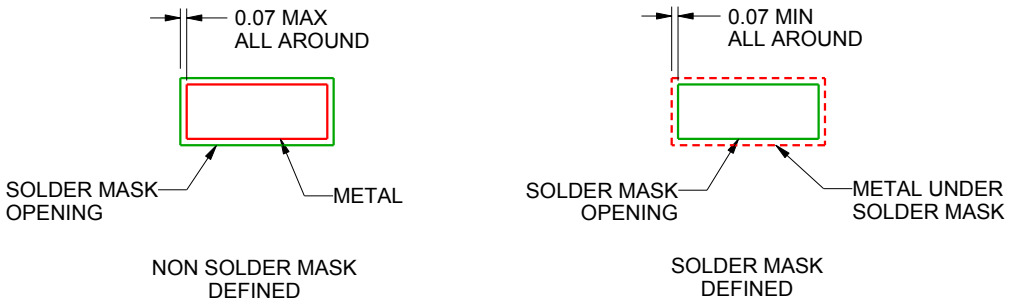
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

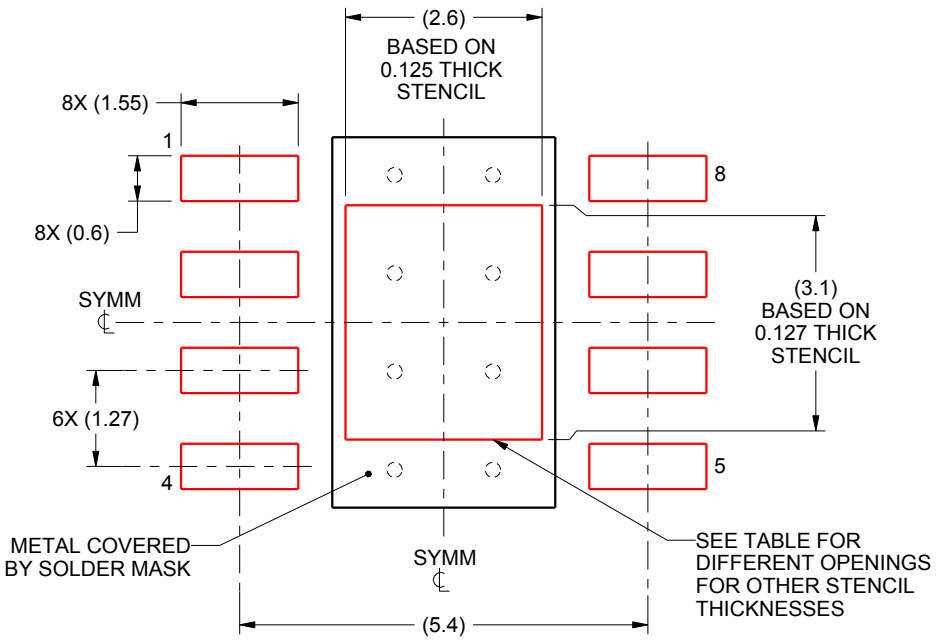


SOLDER MASK DETAILS

4221637/B 03/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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