SONY

CXD2529Q

CD Digital Signal Processor

Description

The CXD2529Q is a digital signal processor LSI for CD players and is equipped with built-in digital filters, zero detection circuit, 1-bit DAC, and analog low-pass filter on a single chip.

Features

Digital Signal Processor (DSP) Block

- Playback mode supporting CAV (Constant Angular Velocity)
  - Frame jitter-free
  - Allows 0.5 to double-speed continuous playback
  - Allows relative rotational velocity readout
  - Supports external spindle control
- Wide capture range mode
  - Spindle rotational velocity following method
  - Supports normal-speed and double-speed playback
- 16K RAM
- EFM data demodulation
- Enhanced EFM frame sync signal protection
- SEC strategy-based error correction
- Subcode demodulation and Sub Q data error detection
- Digital spindle servo
- 16-bit traverse counter
- Asymmetry compensation circuit
- Serial bus-based CPU interface
- Error correction monitor signals, etc. are output from a new CPU interface.
- Servo auto sequencer
- Digital audio interface output
- Digital peak meter

Digital Filter, DAC, Analog Low-Pass Filter Block

- DBB (Digital Bass Boost)
- Supports double-speed playback
- Digital de-emphasis
- Digital attenuation function
- Zero detection function
- 8fs oversampling digital filter
- S/N ratio: 100dB or more (master clock: 384fs typ.)
  Logical value: 109dB
- THD + N: 0.007% or less (master clock: 384fs typ.)
- Rejection band attenuation: –60dB or more

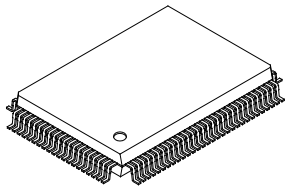
Applications

CD players

Structure

Silicon gate CMOS IC

100 pin QFP (Plastic)



Absolute Maximum Ratings

• Supply voltage	V_{DD}	–0.3 to +7.0	V
• Input voltage	V_I	–0.3 to +7.0	V
		(Vss – 0.3V to V_{DD} + 0.3V)	
• Output voltage	V_O	–0.3 to +7.0	V
• Storage temperature	Tstg	–40 to +125	°C
• Supply voltage difference			
	V_{SS} – AV_{SS}	–0.3 to +0.3	V
	V_{DD} – AV_{DD}	–0.3 to +0.3	V

Note) AV_{DD} includes XV_{DD}, and AV_{SS} includes XV_{SS}.

Recommended Operating Conditions

• Supply voltage	V_{DD}	3.4 to 5.25	V
• Operating temperature	Topr	–20 to +75	°C

Note) The V_{DD} (min.) for the CXD2519Q varies according to the playback speed selection.

Playback speed	V_{DD} (min.) [V]	
	CD-DSP block	DAC block
× 2	3.4V	4.5V
× 1	3.4V	3.4V
× 1*1	3.4V	

*1 When the internal operation of the CD-DSP side is set to double-speed mode and the crystal oscillation frequency is halved, normal-speed playback results.

Input/Output Capacitances

• Input pin	C_I	12 (max.)	pF
• Output pin	C_O	12 (max.)	pF

Note) Measurement conditions V_{DD} = V_I = 0V
f_M = 1MHz

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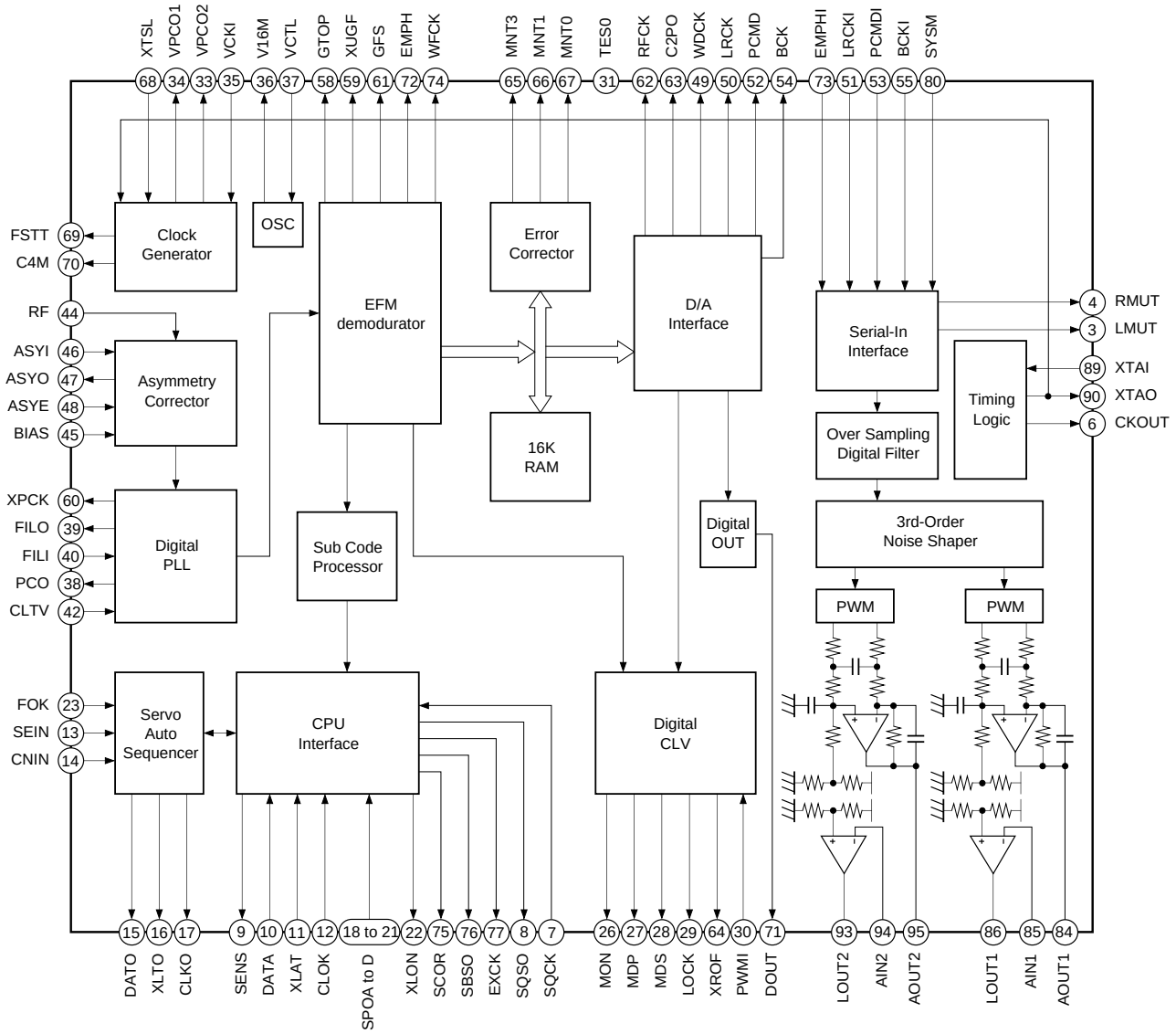
Block Diagram



Pin Configuration

Pin Description

Pin No.	Symbol	I/O		Description
1	V_{DD}	—	—	Power supply (+5V).
2	V_{SS}	—	—	GND.
3	LMUT	O	1, 0	Left-channel zero detection flag.
4	RMUT	O	1, 0	Right-channel zero detection flag.
5	TES2	O	1, 0	TEST output pin; normally open.
6	CKOUT	O	1, 0	Master clock frequency-divider output. Selects and outputs XTAI × 1, × 1/2, × 1/4 or low only.
7	SQCK	I		SQSO readout clock input.
8	SQSO	O	1, 0	Sub Q 80-bit serial output.
9	SENS	O	1, 0	SENS output to CPU.
10	DATA	I		Serial data input from CPU.
11	XLAT	I		Latch input from CPU. Serial data is latched at the falling edge.
12	CLOK	I		Serial data transfer clock input from CPU.
13	SEIN	I		SENS input from SSP.
14	CNIN	I		Track jump count signal input.
15	DATO	O	1, 0	Serial data output to SSP.
16	XLTO	O	1, 0	Serial data latch output to SSP. Latched at the falling edge.
17	CLKO	O	1, 0	Serial data transfer clock output to SSP.
18	SPOA	I		Microcomputer extended interface (input A).
19	SPOB	I		Microcomputer extended interface (input B).
20	SPOC	I		Microcomputer extended interface (input C).
21	SPOD	I		Microcomputer extended interface (input D).
22	XLON	O	1, 0	Microcomputer extended interface (output).
23	FOK	I		Focus OK input. Used for SENS output and the servo auto sequencer.
24	V_{DD}	—	—	Power supply (+5V).
25	V_{SS}	—	—	GND.
26	MON	O	1, 0	Spindle motor on/off control output.
27	MDP	O	1, Z, 0	Spindle motor servo control.
28	MDS	O	1, Z, 0	Spindle motor servo control.
29	LOCK	O	1, 0	GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low.
30	PWMI	I		Spindle motor external control input.
31	TES0	I		TEST pin; normally GND.
32	TES1	I		TEST pin; normally GND.
33	VPCO2	O	1, Z, 0	Wide-band EFM PLL charge pump output. Turned on/off by FCSW of address E.

Pin No.	Symbol	I/O		Description
34	VPCO1	O	1, Z, 0	Charge pump output for wide-band EFM PLL.
35	VCKI	I		VCO2 oscillation input for the wide-band EFM PLL.
36	V16M	O	1, 0	VCO2 oscillation output for the wide-band EFM PLL.
37	VCTL	I		VCO2 control voltage input for the wide-band EFM PLL.
38	PCO	O	1, Z, 0	Master PLL charge pump output.
39	FILO	O	Analog	Master PLL (slave = digital PLL) filter output.
40	FILI	I		Master PLL filter input.
41	AV_{SS}	—	—	Analog GND.
42	CLTV	I		Master VCO control voltage input.
43	AV_{DD}	—	—	Analog power supply (+5V).
44	RF	I		EFM signal input.
45	BIAS	I		Constant current input of the asymmetry circuit.
46	ASYI	I		Asymmetry comparator voltage input.
47	ASYO	O	1, 0	EFM full-swing output (low = V_{SS}, high = V_{DD}).
48	ASYE	I		Low: asymmetry circuit off; high: asymmetry circuit on
49	WDCK	O	1, 0	D/A interface. Word clock f = 2fs
50	LRCK	O	1, 0	D/A interface. LR clock output f = fs
51	LRCKI	I		LR clock input.
52	PCMD	O	1, 0	D/A interface. Serial data output (two's complement, MSB first).
53	PCMDI	I		D/A interface. Serial data input (two's complement, MSB first).
54	BCK	O	1, 0	D/A interface. Bit clock output.
55	BCKI	I		D/A interface. Bit clock input.
56	V_{SS}	—	—	GND.
57	V_{DD}	—	—	Power supply (+5V).
58	GTOP	O	1, 0	GTOP output.
59	XUGF	O	1, 0	XUGF output.
60	XPCK	O	1, 0	XPLCK output.
61	GFS	O	1, 0	GFS output.
62	RFCK	O	1, 0	RFCK output.
63	C2PO	O	1, 0	C2PO output.
64	XROF	O	1, 0	XRAOF output.
65	MNT3	O	1, 0	MNT3 output.
66	MNT1	O	1, 0	MNT1 output.
67	MNT0	O	1, 0	MNT0 output.
68	XTSL	I		Crystal selector input. Low: 16.9344MHz; high: 33.8688MHz.
69	FSTT	O	1, 0	2/3 frequency-divider output for Pins 89 and 90.

Pin No.	Symbol	I/O		Description
70	C4M	O	1, 0	4.2336MHz output. 1/4 frequency-divided VCKI output in CAV-W mode.
71	DOUT	O	1, 0	Digital Out output.
72	EMPH	O	1, 0	Outputs a high signal when the playback disc has emphasis, and a low signal when there is no emphasis.
73	EMPHI	I		Inputs a high signal when de-emphasis is on, and a low signal when de-emphasis is off.
74	WFCK	O	1, 0	WFCK output.
75	SCOR	O	1, 0	Outputs a high signal when either subcode sync S0 or S1 is detected.
76	SBSO	O	1, 0	Sub P to W serial output.
77	EXCK	I		SBSO readout clock input.
78	V_{SS}	—	—	GND.
79	V_{DD}	—	—	Power supply (+5V).
80	SYSM	I		Mute input. Active when high.
81	NC			
82	AV_{SS}	—	—	Analog GND.
83	AV_{DD}	—	—	Analog power supply (+5V).
84	AOUT1	O		Left-channel analog output.
85	AIN1	I		Left-channel operational amplifier input.
86	LOUT1	O		Left-channel LINE output.
87	AV_{SS}	—	—	Analog GND.
88	XV_{DD}			Power supply for master clock.
89	XTAI	I		Crystal oscillation circuit input. Input the external master clock via this pin.
90	XTAO	O		Crystal oscillation circuit output.
91	XV_{SS}			GND for master clock.
92	AV_{SS}	—	—	Analog GND.
93	LOUT2	O		Right-channel LINE output.
94	AIN2	I		Right-channel operational amplifier input.
95	AOUT2	O		Right-channel analog output.
96	AV_{DD}	—	—	Analog power supply (+5V).
97	AV_{SS}	—	—	Analog GND.
98	NC			
99	NC			
100	XRST	I		System reset. Reset when low.

Notes)
- PCMD is an MSB first, two's complement output.
- GTOP is used to monitor the frame sync protection status. (High: sync protection window released.)
- XUGF is the negative pulse for the frame sync derived from the EFM signal. It is the signal before sync protection.
- XPLCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge of XPLCK and the EFM signal transition point coincide.
- GFS goes high when the frame sync and the insertion protection timing match.
- RFCK is derived with the crystal accuracy. This signal has a cycle of 136µs (during normal-speed).
- C2PO represents the data error status.
- XRAOF is generated when the 16K RAM exceeds the ±4F jitter margin.

Electrical Characteristics

DC Characteristics (V_{DD} = AV_{DD} = 5.0V ± 5%, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)*

Item			Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level input voltage	V_{IH} (1)		0.7V_{DD}			V	*1
	Low level input voltage	V_{IL} (1)				0.3V_{DD}	V	
Input voltage (2)	High level input voltage	V_{IH} (2)	Schmitt input	0.8V_{DD}			V	*2
	Low level input voltage	V_{IL} (2)				0.2V_{DD}	V	
Input voltage (3)	Input voltage	V_{IN} (3)	Analog input	Vss		V_{DD}	V	*3
Output voltage (1)	High level output voltage	V_{OH} (1)	I_{OH} = –1mA	V_{DD} – 0.5		V_{DD}	V	*4
	Low level output voltage	V_{OL} (1)	I_{OL} = 1mA	0		0.4	V	
Output voltage (2)	High level output voltage	V_{OH} (2)	I_{OH} = –1mA	V_{DD} – 0.5		V_{DD}	V	*5
	Low level output voltage	V_{OL} (2)	I_{OL} = 2mA	0		0.4	V	
Output voltage (4)	High level output voltage	V_{OH} (4)	I_{OH} = –0.28mA	V_{DD} – 0.5		V_{DD}	V	*6
	Low level output voltage	V_{OL} (4)	I_{OL} = 0.36mA	0		0.4	V	
Input leak current		I_{LI}	V_I = 0 to 5.50V	–5		5	µA	*1, *2, *3
Tri-state pin output leak current		I_{LO}	V_O = 0 to 5.50V	–5		5	µA	*7

Applicable pins

*1 XTSL, DATA, XLAT, PWMI, SYSM, EMPHI, PCMDI

*2 CLOK, XRST, EXCK, SQCK, FOK, SEIN, CNIN, VCKI, ASYE, LRCKI, BCKI, SPOA to D

*3 CLTV, FILI, RF, VCTL, AIN1, AIN2

*4 MDP, PCO, VPCO1, VPCO2

*5 ASYO, DOUT, FSTT, C4M, SBSO, SQSO, SCOR, EMPH, MON, LOCK, WDCK, DATO, CLKO, XLTO, SENS, MDS, MNT0 to 3, WFCK, V16M, CKOUT, LMUT, RMUT, XLON, LRCK, PCMD, BCK, GTOP, XUGF, XPCK, GFS, RFCK, C2PO, XRAOF

*6 FILO

*7 MDS, MDP, $PC\overline{O}$, VPCO1, VPCO2

*note) : XV_{DD} and XV_{SS} are included for AV_{DD} and AV_{SS}, respectively.
Those are the same for the explanation from the next page.

AC Characteristics

1. XTAI pin

(1) When using self-excited oscillation

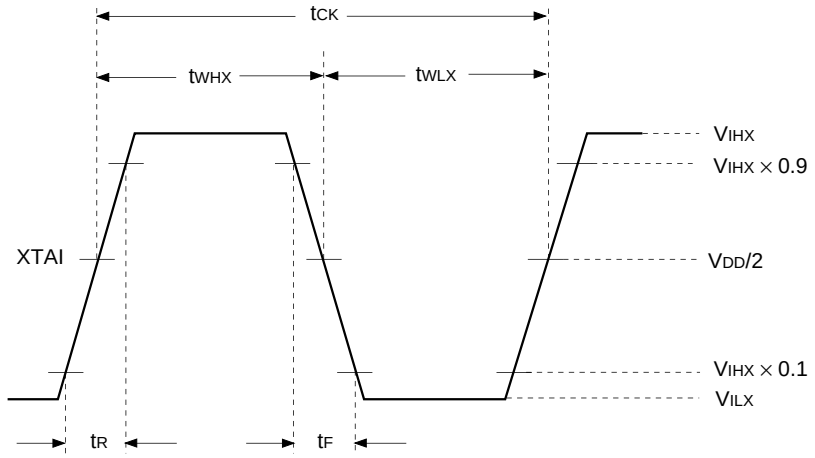
(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ± 5%)

Item	Symbol	Min.	Typ.	Max	Unit
Oscillation frequency	f_{MAX}	15		34	MHz

(2) When inputting pulses to XTAI

(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ± 5%)

Item	Symbol	Min.	Typ.	Max	Unit
High level pulse width	t_{WHX}	13		500	ns
Low level pulse width	t_{WLX}	13		500	ns
Pulse cycle	t_{CK}	26		1,000	ns
Input high level	V_{IHX}	V_{DD} – 1.0			V
Input low level	V_{ILX}			0.8	V
Rise time, fall time	t_R, t_F			10	ns



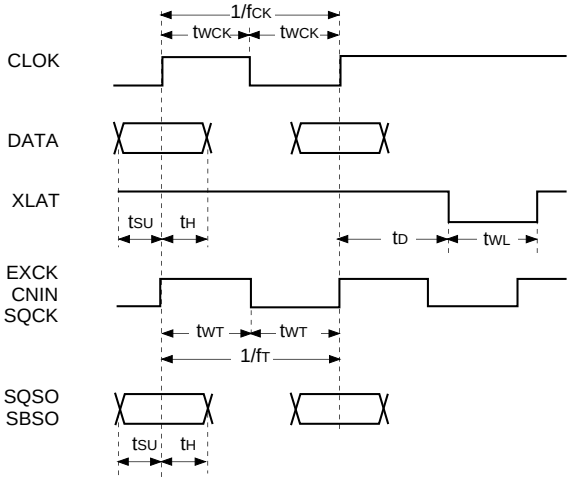
(3) When inputting sine waves to XTAI via a capacitor

(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ± 5%)

Item	Symbol	Min.	Typ.	Max	Unit
Input amplitude	V_1	2.0		V_{DD} + 0.3	Vp-p

2. CLOK, DATA, XLAT, CNIN, SQCK and EXCK pins (V_{DD} = AV_{DD} = 5.0V ± 5%, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)

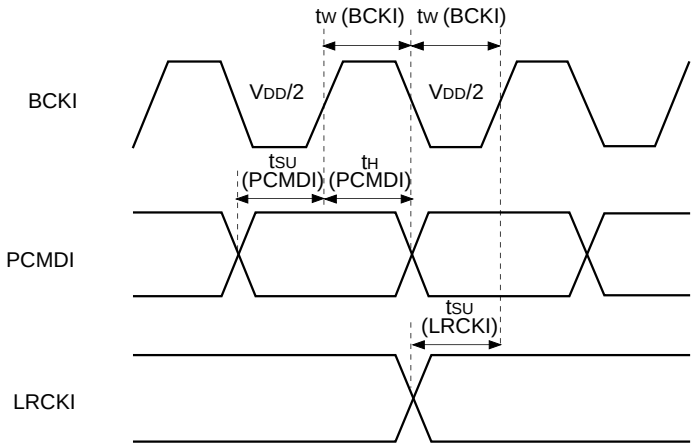
Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CK}			0.65	MHz
Clock pulse width	t_{WCK}	750			ns
Setup time	t_{SU}	300			ns
Hold time	t_H	300			ns
Delay time	t_D	300			ns
Latch pulse width	t_{WL}	750			ns
EXCK SQCK frequency	f_T			0.65*	MHz
EXCK SQCK pulse width	f_{WT}	750*			ns



* In pseudo double-speed playback mode, except when SQSO is Sub Q Read, the maximum operating frequency for SQCK is 300kHz and the minimum pulse width is 1.5µs.

3. BCKI, LRCKI, PCMDI pins (V_{DD} = AV_{DD} = 5.0V ± 5%, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
BCK pulse width	t_W		94			ns
DATAL, R setup time	t_{SU}		18			ns
DATAL, R hold time	t_H		18			ns
LRCK setup time	t_{SU}		18			ns



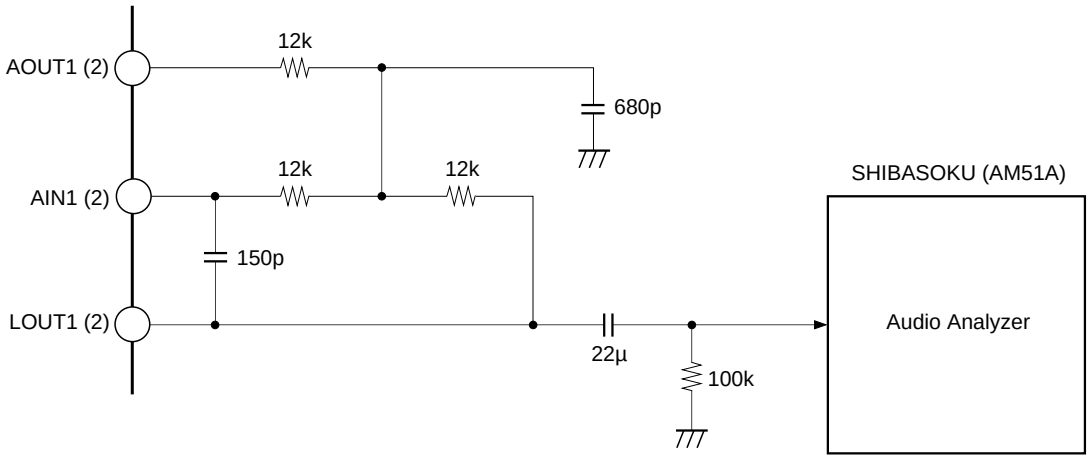
1-bit DAC, LPF Block Analog Characteristics

Analog Characteristics (V_{DD} = AV_{DD} = 5.0V, V_{SS} = AV_{SS} = 0V, Ta = 25°C)

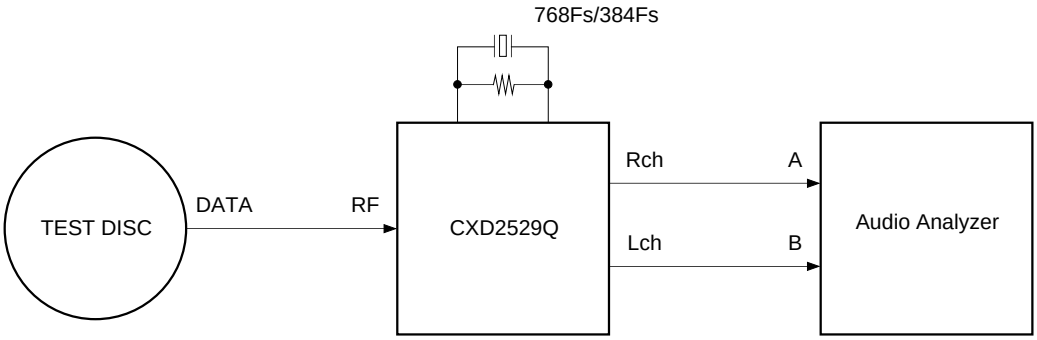
Item	Symbol	Conditions	Crystal	Min.	Typ.	Max.	Unit
Total harmonic distortion	THD	1kHz, 0dB data	384Fs		0.0050	0.0070	%
			768Fs		0.0045	0.0065	
S/N ratio	S/N	1kHz, 0dB data (using A-weighting filter)	384Fs	96	100		dB
			768Fs	96	100		

For both items, Fs = 44.1kHz.

The circuits for measuring the total harmonic distortion and S/N ratio are shown below.



LPF External Circuit Diagram



Block Diagram for Measuring Analog Characteristics

(V_{DD} = AV_{DD} = 5.0V, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Applicable pins
Output voltage	V_{OUT}		1.23*		Vrms	*1
Load resistance	R_L	8			kΩ	*1

* When the sine wave of 1kHz and 0dB is output and it is measured using the circuit shown on the previous page.

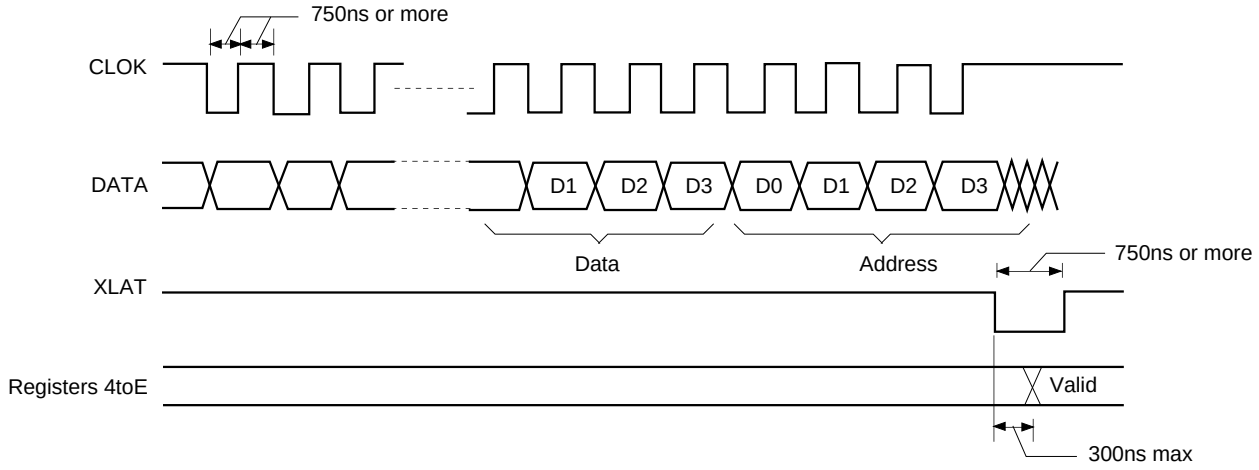
Applicable pins

*1 LOUT1, LOUT2

Description of Functions

1. CPU Interface and Instructions

- CPU Interface
  This interface uses DATA, CLOK and XLAT to set the modes.
  The interface timing chart is shown below.



- Information on each address and the data is provided in Table 1-1.
- The internal registers are initialized by a reset when XRST is low; the initialization data is shown in Table 1-2.
  Note) When XLAT is low, SQCK must be set high.

Command Table

Register name	Command	Address				Data 1				Data 2				Data 3				Data 4				Data 5				Data 6			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	AS3	AS2	AS1	AS0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5	Blind (A, E), Overflow (C)	0	1	0	1	0.18ms	0.09ms	0.05ms	0.02ms	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Brake (B)					0.36ms	0.18ms	0.09ms	0.05ms																				
6	Kick (D)	0	1	1	0	11.6ms	5.8ms	2.9ms	1.45ms	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
7	Auto sequence (N) track jump count	0	1	1	1	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	—	—	—	—	—	—	—	—
8	MODE specification	1	0	0	0	CDROM	DOUT Mute	DOUT ON/OFF	WSEL	VCO SEL1	0	SOCT	VCO SEL2	KSL3	KSL2	KSL1	KSL0	0	0	1	0	—	—	—	—	—	—	—	—
9	Function specification	1	0	0	1	0	DSPB ON/OFF	0	0	0	0	0	SYCOF	OPSL1 0	MCSL	CKOSL1	CKOSL0	ZDPL	ZMUT	—	—	—	—	—	—	—	—	—	—
		1	0	0	1	0	DSPB ON/OFF	0	0	0	0	0	SYCOF	OPSL1 1	MCSL	CKOSL1	CKOSL0	ZDPL	ZMUT	0	0	0	DCOF	0	0	—	—	—	—
A	Audio CTRL	1	0	1	0	0	0	Mute	ATT	0	0	OPSL2 0	EMPH	SMUT	0	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	—	—	—	—
		1	0	1	0	0	0	Mute	ATT	0	0	OPSL2 1	EMPH	SMUT	0	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FMUT	LRWO	BSBST	BBSL
B	Serial bus CTRL	1	0	1	1	SL1	SL0	CPUSR	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
C	Servo coefficient setting	1	1	0	0	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
D	CLV CTRL	1	1	0	1	DCLV PWM MD	TB	TP	Gain CLVS	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	—	—	—	—	—	—	—	—	—	—	—	—
E	CLV mode	1	1	1	0	CM3	CM2	CM1	CM0	EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON	Gain CAV1	Gain CAV0	FCSW	0	—	—	—	—	—	—	—	—

Table 1-1.

Reset Initialization

Register name	Command	Address				Data 1				Data 2				Data 3				Data 4				Data 5				Data 6			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5	Blind (A, E), Overflow (C) / Brake (B)	0	1	0	1	0	1	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
6	Kick (D)	0	1	1	0	0	1	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
7	Auto sequence (N) track jump count	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
8	MODE specification	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	—	—	—	—	—	—	—	—
9	Function specification	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—
A	Audio CTRL	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B	Serial bus CTRL	1	0	1	1	0	0	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
C	Servo coefficient setting	1	1	0	0	0	1	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
D	CLV CTRL	1	1	0	1	0	0	0	0	1	1	1	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
E	CLV mode	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—

Table 1-2.

1-1. The meaning of the data for each address is explained below.

$4X commands

Command	AS3	AS2	AS1	AS0
CANCEL	0	0	0	0
FOCUS-ON	0	1	1	1
1 TRACK JUMP	1	0	0	RXF
10 TRACK JUMP	1	0	1	RXF
2N TRACK JUMP	1	1	0	RXF
N TRACK MOVE	1	1	1	RXF

RXF = 0 FORWARD
RXF = 1 REVERSE

- When the Focus-on command ($47) is canceled ($40), $02 is sent and the auto sequence is interrupted.
- When the Track jump/move commands ($48 to $4F) are canceled ($40), $25 is sent and the auto sequence is interrupted.

$5X commands

Auto sequence timer setting
Setting timers: A, E, C, B

Command	D3	D2	D1	D0
Blind (A, E), Over flow (C)	0.18ms	0.09ms	0.05ms	0.02ms
Brake (B)	0.36ms	0.18ms	0.09ms	0.05ms

Ex.) D2 = D0 = 1, D3 = D1 = 0 (Initial Reset)
A = E = C = 0.11ms
B = 0.23ms

$6X commands

Auto sequence timer setting
Setting timer: D

Command	D3	D2	D1	D0
KICK (D)	11.6ms	5.8ms	2.9ms	1.45ms

Ex.) D3 = 0, D2 = D1 = D0 = 1(Initial Reset)
D = 10.15ms

$7X commands

Auto sequence track jump/move count setting (N)

Command	Data 1				Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Auto sequence track jump count setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

This command is used to set N when a 2N track jump and an N track move are executed for auto sequence.

- The maximum track count is 65,535, but note that with 2N track jumps the maximum track jump count is determined by the mechanical limitations of the optical system.
- The number of track jump is counted according to the signals input from the CNIN pin.

$8X commands

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
MODE specification	CDROM	DOUT Mute	DOUT ON/OFF	WSEL	VCO SEL1	0	SOCT	VCO SEL2	KSL3	KSL2	KSL1	KSL0

See the $BX commands.

Data 4			
D3	D2	D1	D0
0	0	1	0

Command bit	C2PO timing	Processing
CDROM = 1	See the Timing Chart 1-1.	CDROM mode; average value interpolation and pre-value hold are not performed.
CDROM = 0	See the Timing Chart 1-1.	Audio mode; average value interpolation and pre-value hold are performed.

Command bit	Processing
DOUT Mute = 1	Digital Out output is muted. (DA output is not muted.)
DOUT Mute = 0	When no other mute conditions are set, Digital Out output is not muted.

Command bit	Processing
DOUT ON/OFF = 1	Digital Out is output from the DOUT pin.
DOUT ON/OFF = 0	Digital Out is not output from the DOUT pin.

Command bit	Sync protection window width	Application
WSEL = 1	±26 channel clock*1	Anti-rolling is enhanced.
WSEL = 0	±6 channel clock	Sync window protection is enhanced.

*1 In normal-speed playback, channel clock = 4.3218MHz.

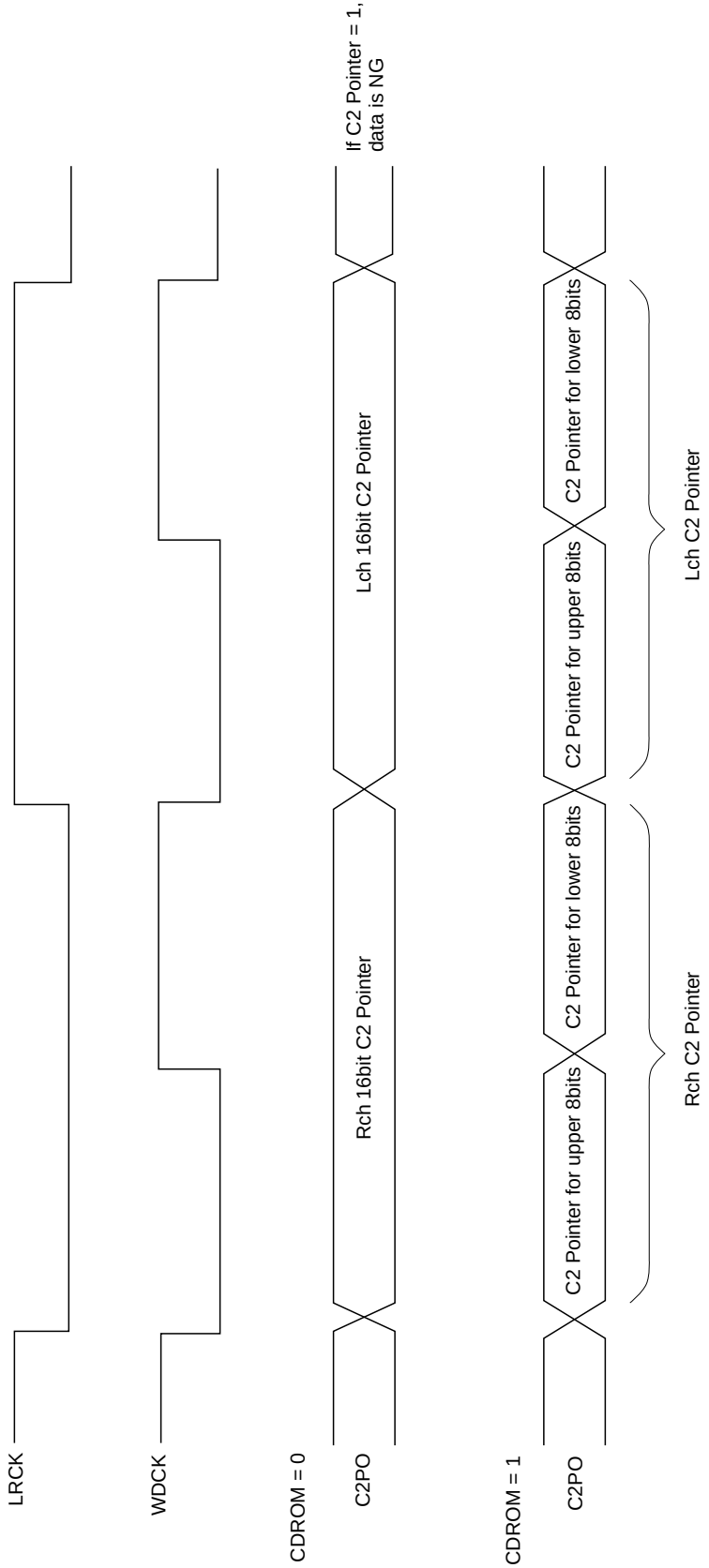
Command bit			Processing
VCOSEL1	KSL3	KSL2	
0	0	0	Multiplier PLL VCO1 is set to normal speed, and the output is 1/1 frequency-divided.
0	0	1	Multiplier PLL VCO1 is set to normal speed, and the output is 1/2 frequency-divided.
0	1	0	Multiplier PLL VCO1 is set to normal speed, and the output is 1/4 frequency-divided.
0	1	1	Multiplier PLL VCO1 is set to normal speed, and the output is 1/8 frequency-divided.
1	0	0	Multiplier PLL VCO1 is set to high speed*1, and the output is 1/1 frequency-divided.
1	0	1	Multiplier PLL VCO1 is set to high speed*1, and the output is 1/2 frequency-divided.
1	1	0	Multiplier PLL VCO1 is set to high speed*1, and the output is 1/4 frequency-divided.
1	1	1	Multiplier PLL VCO1 is set to high speed*1, and the output is 1/8 frequency-divided.

*1 Approximately twice the normal speed.

Command bit			Processing
VCOSEL2	KSL1	KSL0	
0	0	0	Wide-band PLL VCO2 is set to normal speed, and the output is 1/1 frequency-divided.
0	0	1	Wide-band PLL VCO2 is set to normal speed, and the output is 1/2 frequency-divided.
0	1	0	Wide-band PLL VCO2 is set to normal speed, and the output is 1/4 frequency-divided.
0	1	1	Wide-band PLL VCO2 is set to normal speed, and the output is 1/8 frequency-divided.
1	0	0	Wide-band PLL VCO2 is set to high speed*2, and the output is 1/1 frequency-divided.
1	0	1	Wide-band PLL VCO2 is set to high speed*2, and the output is 1/2 frequency-divided.
1	1	0	Wide-band PLL VCO2 is set to high speed*2, and the output is 1/4 frequency-divided.
1	1	1	Wide-band PLL VCO2 is set to high speed*2, and the output is 1/8 frequency-divided.

*2 Approximately twice the normal speed.

Timing Chart 1-1



$9X commands (OPSL1 = 0)

* Data 2 D0 and subsequent data are DF/DAC function settings.

Command	Data 1				Data 2		Data 3				Data 4			
	D3	D2	D1	D0	D3 to D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Function specifications	0	DSPB ON/OFF	0	0	000	SYCOF	0	MCSL	CKOSL1	CKOSL0	ZDPL	ZMUT	—	—

OPSL1

Data 5			
D3	D2	D1	D0
—	—	—	—

$9X commands (OPSL1 = 1)

* Data 2 D0 and subsequent data are DF/DAC function settings.

Command	Data 1				Data 2		Data 3				Data 4			
	D3	D2	D1	D0	D3 to D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Function specifications	0	DSPB ON/OFF	0	0	000	SYCOF	1	MCSL	CKOSL1	CKOSL0	ZDPL	ZMUT	0	0

OPSL1

Data 5			
D3	D2	D1	D0
0	DCOF	0	0

Command bit	Processing
DSPB = 1	Double-speed playback (CD-DSP block)
DSPB = 0	Normal-speed playback (CD-DSP block)

Command bit	Processing
SYCOF = 1	LRCK asynchronous mode
SYCOF = 0	Normal operation

* Set SYCOF = 0 in advance when setting the $AX command LRWO to 1.

Command bit	Processing
OPSL1 = 1	DCOF can be set.
OPSL1 = 0	DCOF cannot be set.

Command bit	Processing
MCSL = 1	DF/DAC block master clock selection. Crystal = 768Fs (33.8688MHz)
MCSL = 0	DF/DAC block master clock selection. Crystal = 384Fs (16.9344MHz)

Command bit		Processing
CKOSL1	CKOSL0	
0	0	The CKOUT pin output is 1/1-frequency divided of the crystal input.
0	1	The CKOUT pin output is 1/2-frequency divided of the crystal input.
1	0	The CKOUT pin output is 1/4-frequency divided of the crystal input.
1	1	The CKOUT pin output is fixed to low.

Command bit	Processing
ZDPL = 1	LMUT and RMUT pins are set to high for mute.
ZDPL = 0	LMUT and RMUT pins are set to low for mute.

* See the description of “Mute Flag Output” for the conditions of the mute flag output.

Command bit	Processing
ZMUT = 1	Zero detection mute is on.
ZMUT = 0	Zero detection mute is off.

Command bit	Processing
DCOF = 1	DC offset is off.
DCOF = 0	DC offset is on.

* DCOF can be set when OPSL is 1.
* Set the DC offset to off when the zero detection mute is on.

$AX commands (OPSL2=0)

* Data 2 and subsequent data are DF/DAC function settings.

Command	Data 1				Data 2				Data 3	
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2
Audio CTRL	0	0	Mute	ATT	0	0	0	EMPH	SMUT	0

OPSL2

Data 3		Data 4				Data 5				Data 6			
D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	—	—	—	—

$AX commands (OPSL2 = 1)

* Data 2 and subsequent data are DF/DAC function settings.

Command	Data 1				Data 2				Data 3	
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2
Audio CTRL	0	0	Mute	ATT	0	0	1	EMPH	SMUT	0

OPSL2

Data 3		Data 4				Data 5				Data 6			
D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FMUT	LRWO	BSBST	BBSL

Command bit	Processing
Mute = 1	CD-DSP block mute is on. The zero data is output from the CD-DSP block.
Mute = 0	CD-DSP block mute is off.

Command bit	Processing
ATT = 1	Attenuation (–12dB) is applied to the CD-DSP block output.
ATT = 0	Attenuation of the CD-DSP block output is off.

Command bit	Meaning
OPSL2 = 1	FMUT, LRWO, BSBST and BBSL can be set.
OPSL2 = 0	FMUT, LRWO, BSBST and BBSL cannot be set.

Command bit	Processing
EMPH = 1	De-emphasis is on.
EMPH = 0	De-emphasis is off.

* If either the EMPHI pin or EMPH is high, de-emphasis is on.

Command bit	Processing
SMUT = 1	Soft mute is on.
SMUT = 0	Soft mute is off.

* If either the SYSM pin or SMUT is high, soft mute is on.

Command bit	Meaning
AD9 to 0	Attenuation data

The attenuation data consists of 10 bits, and is set as follows.

Attenuation data	Audio output
3FFh	0dB
3FEh 3FDh : 001h	–0.0085dB –0.017dB –60.198dB
000h	–∞

1023 settings are available because the attenuation data (AD9 to AD0) consists of 10 bits.
The audio output for 001h to 3FFh can be obtained by the following equation.

$$\text{Audio output} = 20 \log \frac{\text{attenuation data}}{1024} \quad [\text{dB}]$$

Command bit	Meaning
FMUT = 1	Forced mute is on.
FMUT = 0	Forced mute is off.

* FMUT can be set when OPSL2 is 1.

Command bit	Meaning
LRWO = 1	Forced sync mode Note)
LRWO = 0	Normal operation

* LRWO can be set when OPSL2 is 1.
* Set the $9X command SYCOF = 0 in advance when setting LRWO to 1.

Note) Synchronization is performed at the first LRCK falling edge during reset, so that normally this mode is unnecessary. However, synchronization can be forcibly applied by setting LRWO to 1.

Command bit	Processing
BSBST = 1	Bass boost is on.
BSBST = 0	Bass boost is off.

* BSBSTcan be set when OPSL2 is 1.

Command bit	Processing
BBSL = 1	Bass boost is Max.
BBSL = 0	Bass boost is Mid.

* BBSL can be set when OPSL2 is 1.

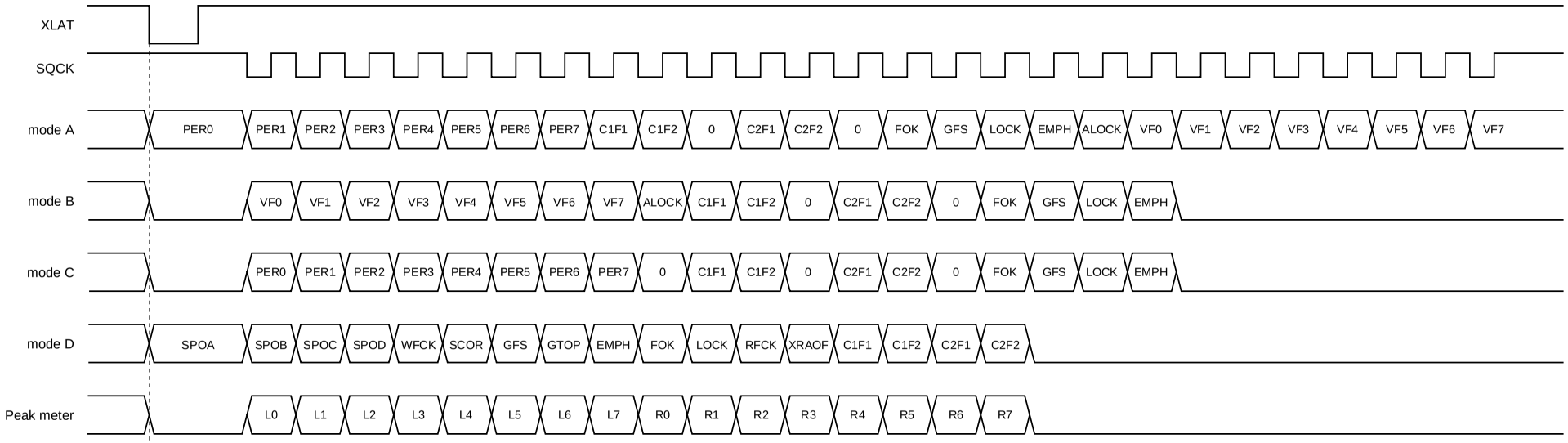
$BX commands

Command	Data 1			
	D3	D2	D1	D0
Serial bus CTRL	SL1	SL0	CPUSR	0

SOCT	SL1	SL0	mode
0	0	0	SubQ
0	0	1	Peak meter
0	1	0	SENS
0	1	1	D
1	0	0	SubQ
1	0	1	A
1	1	0	B
1	1	1	C

The SQSO pin output can be switched to the various signals by setting the $8X command SOCT and $BX commands SL1 and SL0. Set SQCK to high at the falling edge of XLAT.

Except for Sub Q and peak meter, the signals are loaded to the register when they are set at the falling edge of XLAT. Sub Q is loaded to the register with each SCOR, and peak meter is loaded when a peak is detected.



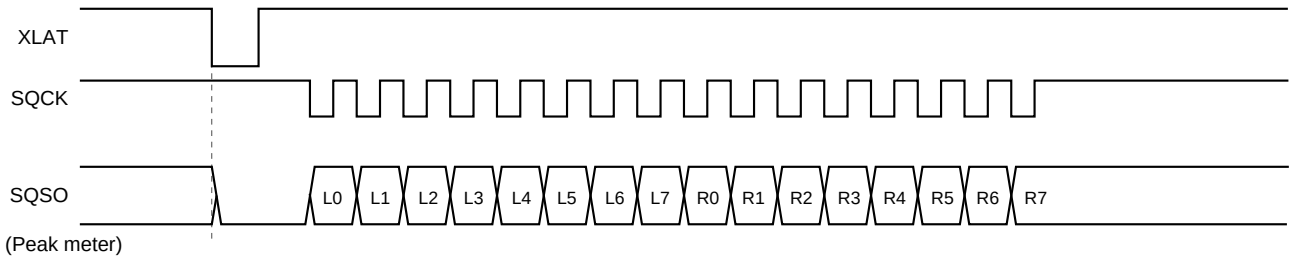
Signal	Description
PER0 to 7	RF jitter amount (used to adjust the focus bias). 8-bit binary data in PER0 = LSB, PER7 = MSB.
FOK	Focus OK
GFS	High when the frame sync and the insertion protection timing match.
LOCK	GFS is sampled at 460Hz; when GFS is high, a high signal is output. If GFS is low eight consecutive samples, a low signal is output.
EMPH	High when the playback disc has emphasis.
ALOCK	GFS is sampled at 460Hz; when GFS is high eight consecutive samples, a high signal is output. If GFS is low eight consecutive samples, a low signal is output.
VF0 to 7	Used during CAV-W mode. Results of measuring the disc rotational velocity. (See the Timing Chart 2-3.) VF0 = LSB, VF7 = MSB.
SPOA to D	SPOA to D pin inputs.
WFCK	Write frame clock output.
SCOR	High when either subcode sync S0 or S1 is detected.
GTOP	High when the sync protection window is released.
RFCK	Read frame clock output.
XRAOF	Low when the built-in 16K RAM exceeds the ±4 frame jitter margin.
L0 to L7, R0 to R7	Peak meter register output. L0 to 7 are the left-channel and R0 to 7 are the right-channel peak data. L0 and R0 are LSB.

C1F1	C1F2	C1 correction status
0	0	No Error
1	0	Single Error Correction
1	1	Irretrievable Error

C2F1	C2F2	C2 correction status
0	0	No Error
1	0	Single Error Correction
1	1	Irretrievable Error

Command bit	Processing
CPUSR = 1	XLON pin is high.
CPUSR = 0	XLON pin is low.

Peak meter



The LSI is set to peak detection mode by setting SOCT = 0, SL1 = 0 and SL0 = 1 with the $8X and $BX commands. In peak detection mode, the SQSO output is connected to the peak detection register. The maximum PCM data values (absolute value, upper 8 bits) for the left and right channels can be read out from SQSO by inputting 16 clocks to SQCK. Peak detection is not performed while inputting to SQCK, and the peak detection register does not change during readout. This SQCK input is judged using a retriggerable monostable multivibrator with a time constant of 270 to 400µs. Set the time for which SQCK input is high to 270µs or less. Peak detection restarts from 270 to 400µs after SQCK input.

The peak detection register is reset to zero for each readout (16 clocks input to SQCK). The maximum value during peak detection mode is detected and held in this condition until the next readout. When setting the LSI to peak detection mode, perform readout one time initially to reset the peak detection register.

Pre-value hold and average value interpolation data are also detected by peak detection.

$CX commands

Command	D3	D2	D1	D0
Servo coefficient setting	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0
CLV CTRL ($DX)				Gain CLVS

• CLV mode gain setting: GCLVS

Gain MDS1	Gain MDS0	Gain CLVS	GCLVS
0	0	0	–12dB
0	0	1	–6dB
0	1	0	–6dB
0	1	1	0dB
1	0	0	0dB
1	0	1	+6dB

• CLVP mode gain setting: GMDP, GMDS

Gain MDP1	Gain MDP0	GMDP
0	0	–6dB
0	1	0dB
1	0	+6dB

Gain MDS1	Gain MDS0	GMDS
0	0	–6dB
0	1	0dB
1	0	+6dB

$DX commands

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
CLV CTRL	DCLV PWM MD	TB	TP	Gain CLVS	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0

See the $CX commands.

Command bit	Description
DCLV PWM MD = 1	Digital CLV PWM mode specified. Both MDS and MDP are used. CLV-W and CAV-W modes can not be used.
DCLV PWM MD = 0	Digital CLV PWM mode specified. Ternary MDP values are output. CLV-W and CAV-W modes can be used.

Command bit	Description
TB = 0	Bottom hold at a cycle of RFCK/32 in CLVS mode.
TB = 1	Bottom hold at a cycle of RFCK/16 in CLVS mode.
TP = 0	Peak hold at a cycle of RFCK/4 in CLVS mode.
TP = 1	Peak hold at a cycle of RFCK/2 in CLVS mode.

Command bit	Description
VP0 to 7 = F0 (H)	Playback at half (normal) speed
⋮	to
VP0 to 7 = E0 (H)	Playback at normal (double) speed

The rotational velocity R of the spindle can be expressed with the following equation.

$$R = \frac{256 - n}{32}$$

R: Relative velocity at normal speed = 1

n: VP0 to 7 setting value

Note)

- Values in parentheses are for when DSPB is 1.
- Values when crystal is 16.9344 MHz and XTSL is low or when crystal is 33.8688 MHz and XTSL is high.
- VP0 to 7 setting values are valid in CAV-W mode.

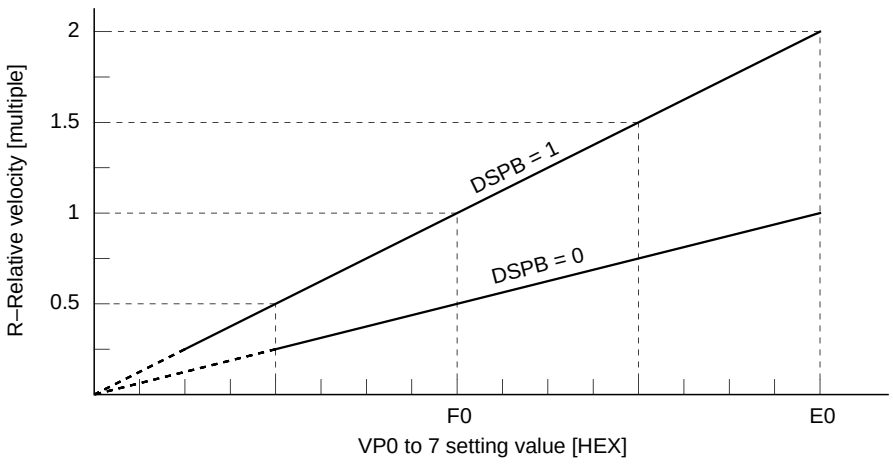


Fig. 1-1

$EX commands

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
CLV mode	CM3	CM2	CM1	CM0	EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON

Command bit				Mode	Description
CM3	CM2	CM1	CM0		
0	0	0	0	STOP	Spindle stop mode.*1
1	0	0	0	KICK	Spindle forward rotation mode.*1
1	0	1	0	BRAKE	Spindle reverse rotation mode. Valid only when LPWR = 0, in any modes.*1
1	1	1	0	CLVS	Rough servo mode. When the RF-PLL circuit isn't locked, this mode is used to adjust the disc rotations within the RF-PLL capture range.
1	1	1	1	CLVP	PLL servo mode.
0	1	1	0	CLVA	Automatic CLVS/CLVP switching mode. Used for normal playback.

*1 See the Timing Charts 1-2 to 1-7.

Command bit								Mode	Description
EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON		
0	0	0	0	0	0	0	0	CLV-N	Crystal reference CLV servo.
0	0	0	0	1	1	0	0	CLV-W	Used for playback in CLV-W mode.*2
0	1	1	0	0	1	0	1	CAV-W	Spindle control with VP0 to 7.
1	0	1	0	0	1	0	1	CAV-W	Spindle control with the external PWM.

*2 Figs. 3-1 and 3-2 show the control flow with the microcomputer software in CLV-W mode.

Command	Data 4			
	D3	D2	D1	D0
SPD mode	Gain CAV1	Gain CAV0	FCSW	0

Gain CAV1	Gain CAV0	Gain
0	0	0dB
0	1	–6dB
1	0	–12dB
1	1	–18dB

- This sets the gain when controlling the spindle with the phase comparator in CAV-W mode.

Command bit	Processing
FCSW = 0	The VPCO2 pin is not used and is high impedance.
FCSW = 1	The VPCO2 pin is used and the pin signal is the same as VPCO1.

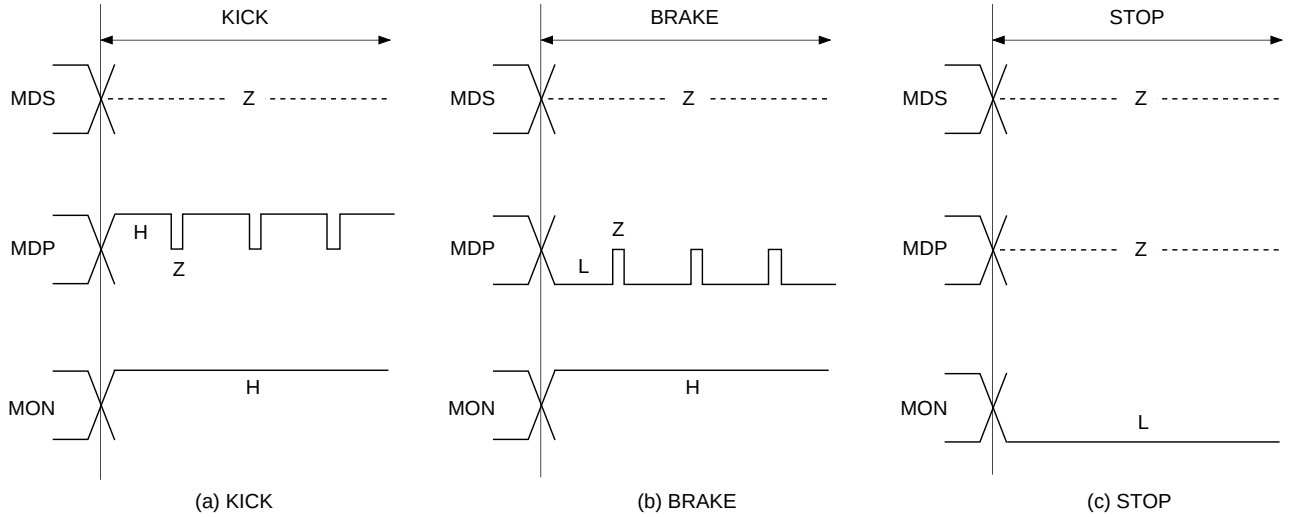
Mode	DCLV PWM MD	LPWR	Command	Timing chart
CLV-N	0	0	KICK	1-2 (a)
			BRAKE	1-2 (b)
			STOP	1-2 (c)
	1	0	KICK	1-3 (a)
			BRAKE	1-3 (b)
			STOP	1-3 (c)
CLV-W	0	0	KICK	1-4 (a)
			BRAKE	1-4 (b)
			STOP	1-4 (c)
		1	KICK	1-5 (a)
			BRAKE	1-5 (b)
			STOP	1-5 (c)
CAV-W	0	0	KICK	1-6 (a)
			BRAKE	1-6 (b)
			STOP	1-6 (c)
		1	KICK	1-7 (a)
			BRAKE	1-7 (b)
			STOP	1-7 (c)

Mode	DCLV PWM MD	LPWR	Timing chart
CLV-N	0	0	1-8
	1	0	1-9
CLV-W	0	0	1-10
		1	1-11
CAV-W	0	0	1-12 (EPWM = 0)
		1	1-13 (EPWM = 0)
		0	1-14 (EPWM = 1)
		1	1-15 (EPWM = 1)

Note) The CLV-W and CAV-W modes support control only by the ternary output of the MDP pin. Therefore, when using the CLV-W and CAV-W modes, set DCLV PWM MD to 0.

Timing Chart 1-2

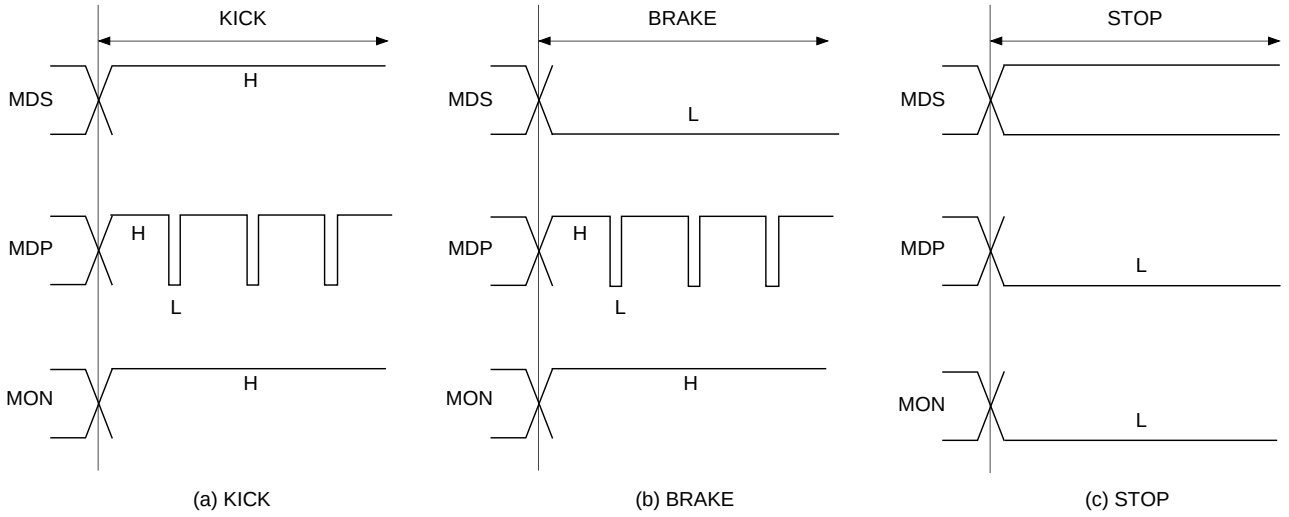
CLV-N mode DCLV PWM MD = LPWR = 0



(a) KICK (b) BRAKE (c) STOP

Timing Chart 1-3

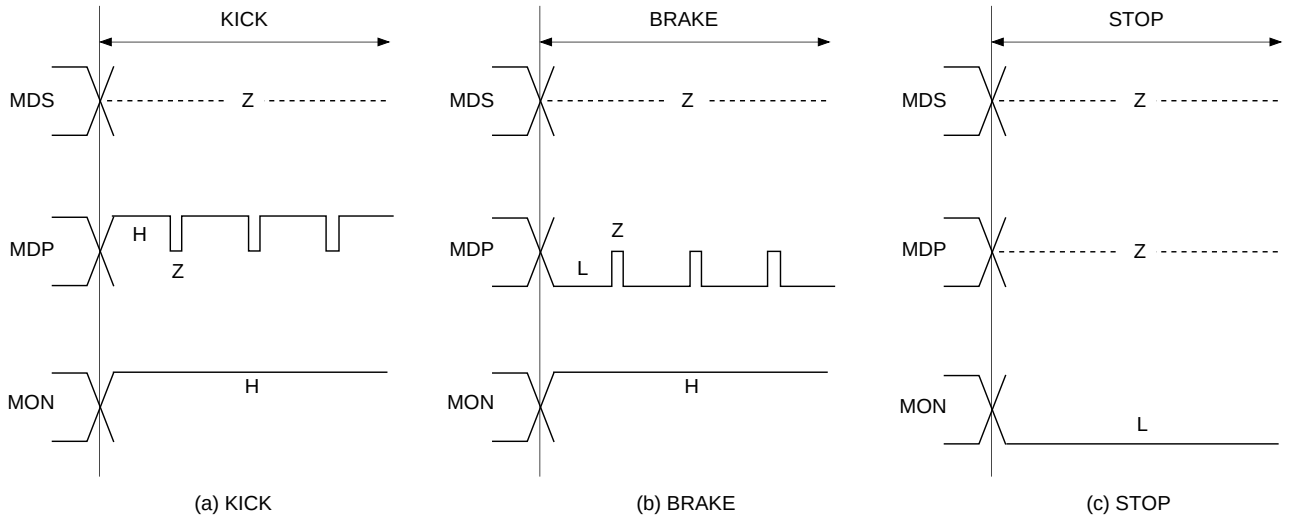
CLV-N mode DCLV PWM MD = 1, LPWR = 0



(a) KICK (b) BRAKE (c) STOP

Timing Chart 1-4

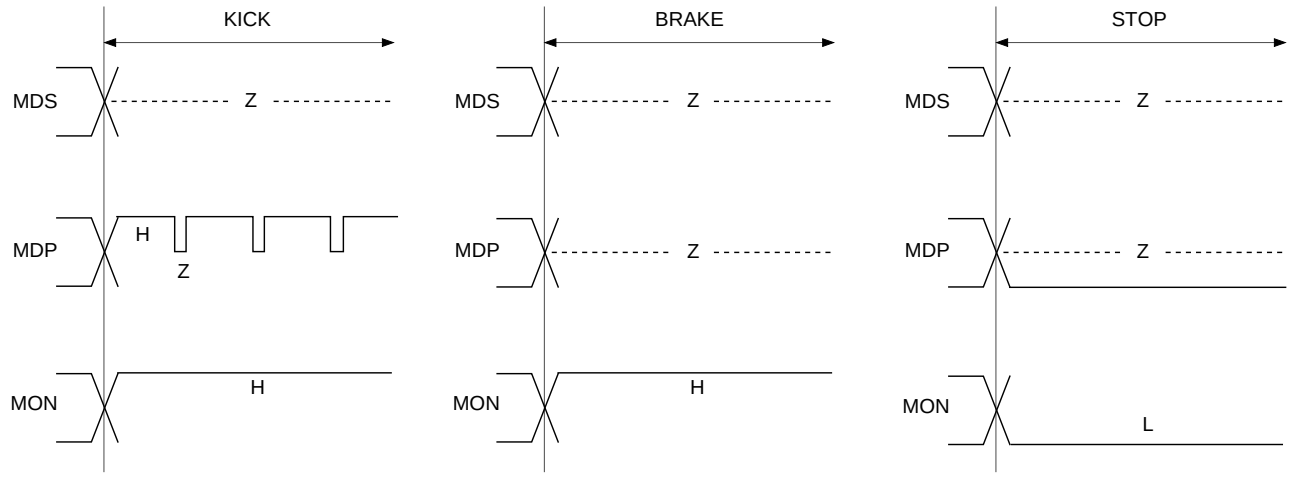
CLV-W mode (when following the spindle rotational velocity) DCLV PWM MD = LPWR = 0



(a) KICK (b) BRAKE (c) STOP

Timing Chart 1-5

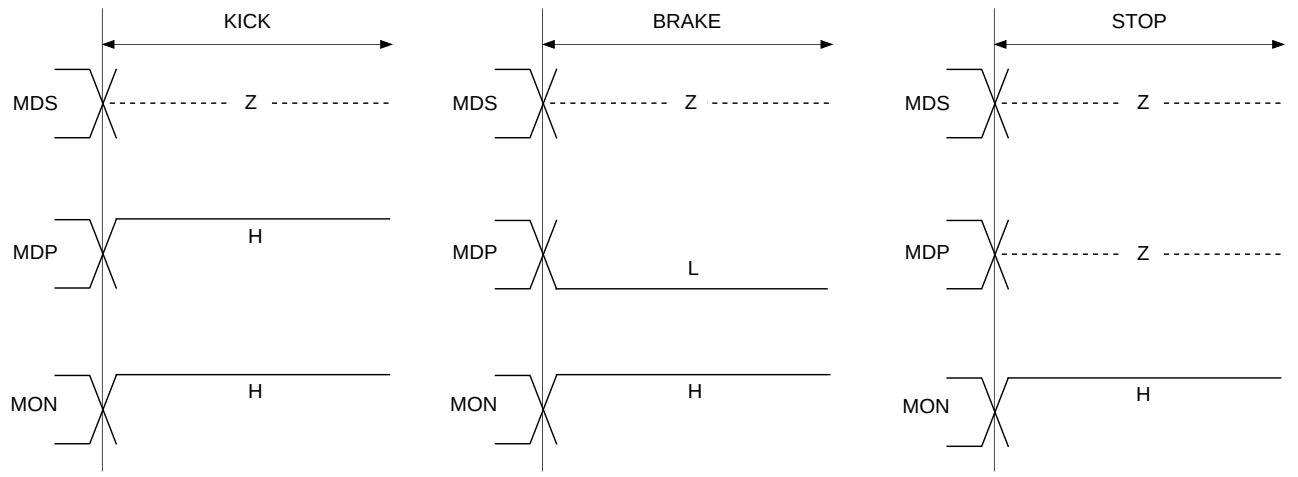
CLV-W mode (when following the spindle rotational velocity) DCLV PWM MD = 0, LPWR = 1



(a) KICK (b) BRAKE (c) STOP

Timing Chart 1-6

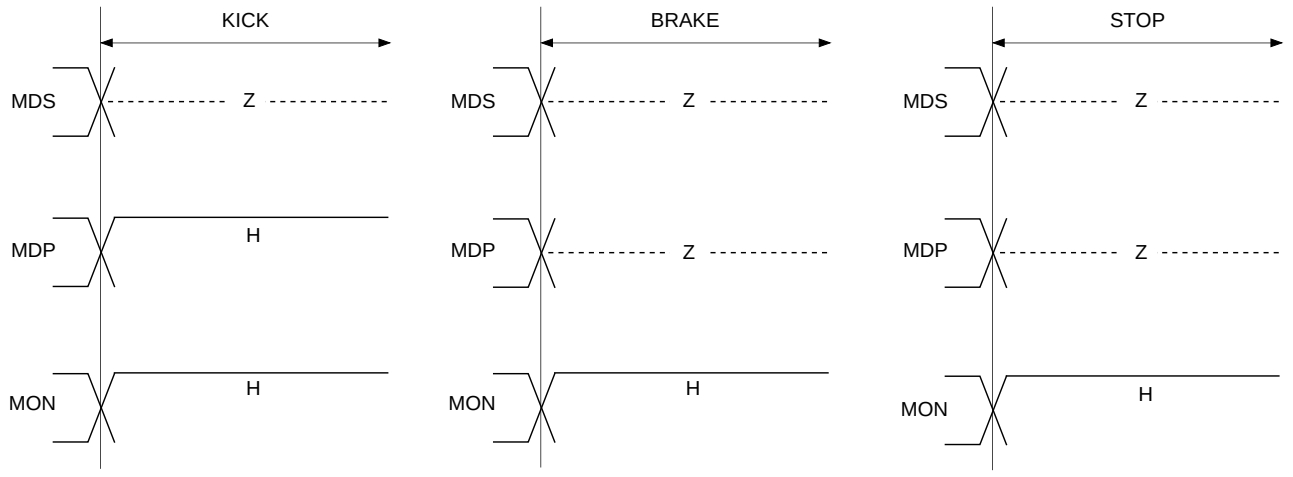
CAV-W mode DCLV PWM MD = LPWR = 0



(a) KICK (b) BRAKE (c) STOP

Timing Chart 1-7

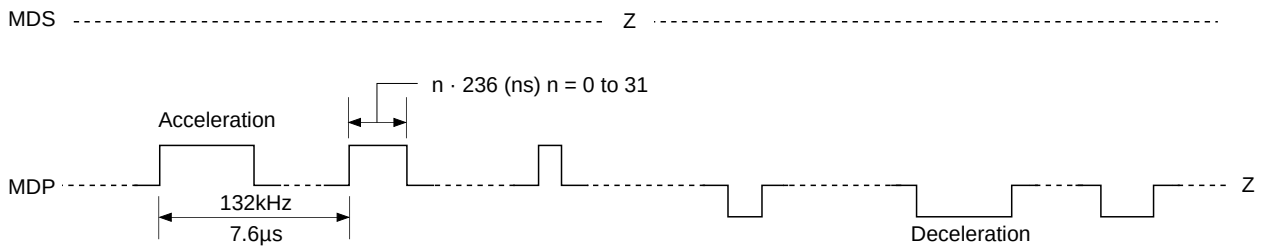
CAV-W mode DCLV PWM MD = 0, LPWR = 1



(a) KICK (b) BRAKE (c) STOP

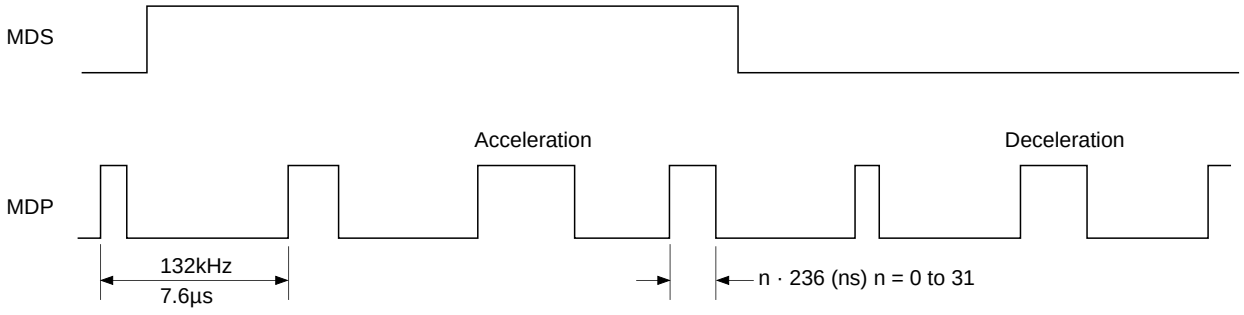
Timing Chart 1-8

CLV-N mode DCLV PWM MD = LPWR = 0



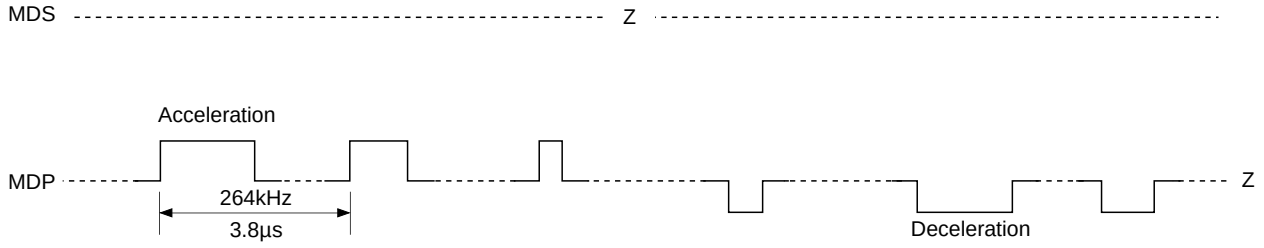
Timing Chart 1-9

CLV-N mode DCLV PWM MD = 1, LPWR = 0



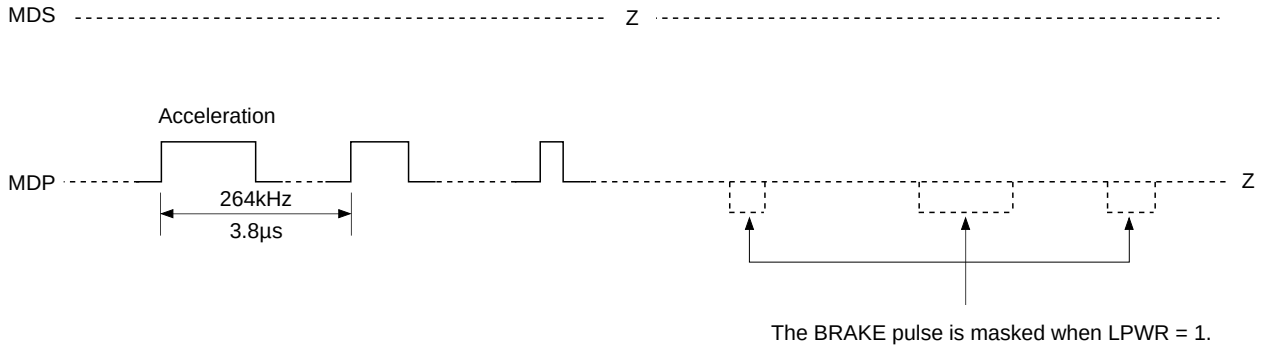
Timing Chart 1-10

CLV-W mode DCLV PWM MD = LPWR = 0



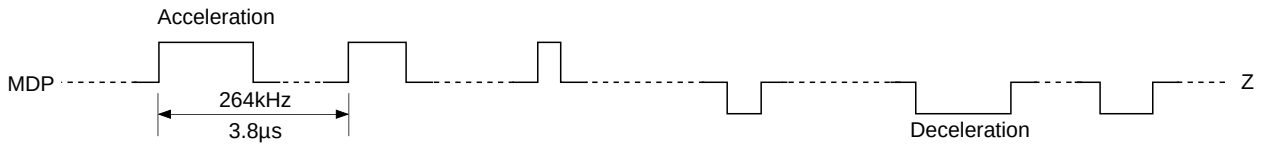
Timing Chart 1-11

CLV-W mode DCLV PWM MD = 0, LPWR = 1



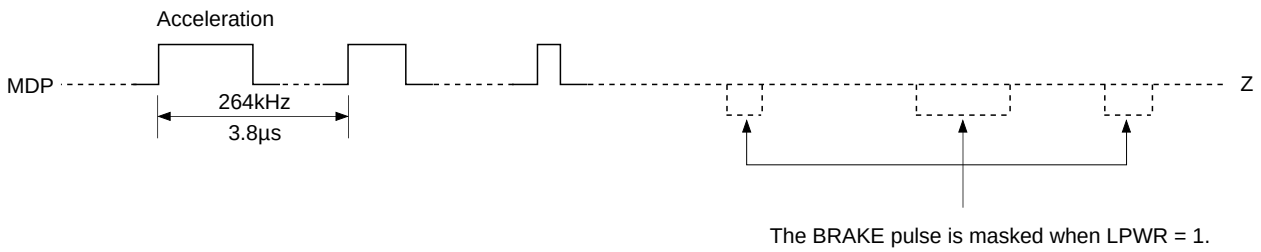
Timing Chart 1-12

CAV-W mode EPWM = DCLV PWM MD = LPWR = 0



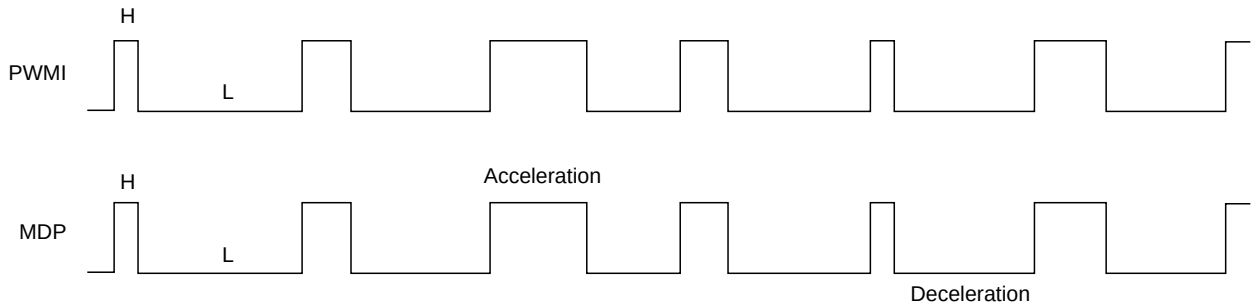
Timing Chart 1-13

CAV-W mode EPWM = DCLV PWM MD = 0, LPWR = 1



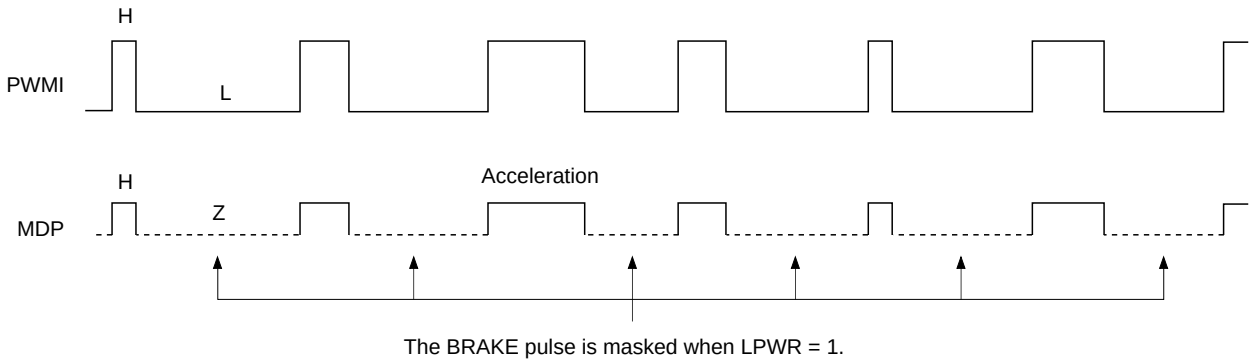
Timing Chart 1-14

CAV-W mode EPWM = 1, DCLV PWM MD = LPWR = 0



Timing Chart 1-15

CAV-W mode EPWM = 1, DCLV PWM MD = 0, LPWR = 1



Note) The CLV-W and CAV-W modes support control only by the ternary output of the MDP pin.
Therefore, when using the CLV-W and CAV-W modes, set DCLV PWM MD to 0.

1-2. Description of SENS Output

The following signals are output from SENS, depending on the microcomputer serial register value (latching not required).

Microcomputer serial register value (latching not required)	SENS output	Meaning
$0X, 1X, 2X, 3X	SEIN	SEIN, a signal input to this LSI from the SSP, is output.
$4X	XBUSY	Low while the auto sequencer is in operation, high when operation terminates.
$5X	FOK	Outputs the signal input to the FOK pin. Normally, FOK (from RF) is input. High for “focus OK”.
$6X	SEIN	SEIN, a signal input to this LSI from the SSP, is output.
$AX	GFS	High when the regenerated frame sync is obtained with the correct timing.
$EX	$\overline{\text{OV64}}$	Low when the EFM signal, after passing through the sync detection filter, is lengthened by 64 channel clock pulses or more.
$7X, 8X, 9X, BX, CX, DX, FX	“L”	SENS pin is fixed to low.

Note that the SENS output can be read out from the SQSO pin when SOCT = 0, SL1 = 1 and SL0 = 0. (See the $BX commands.)

2. Subcode Interface

This section explains the subcode interface.
There are two methods for reading out a subcode externally. The 8-bit subcodes P to W can be read out from SBSO by inputting EXCK to the CXD2529Q.
Sub Q can be read out after the CRC check of the 80 bits of data in the subcode frame. This is accomplished, after checking SCOR and CRCF, by inputting 80 clock pulses to SQCK and reading out the data from the SQSO pin.

2-1. P to W Subcode Read

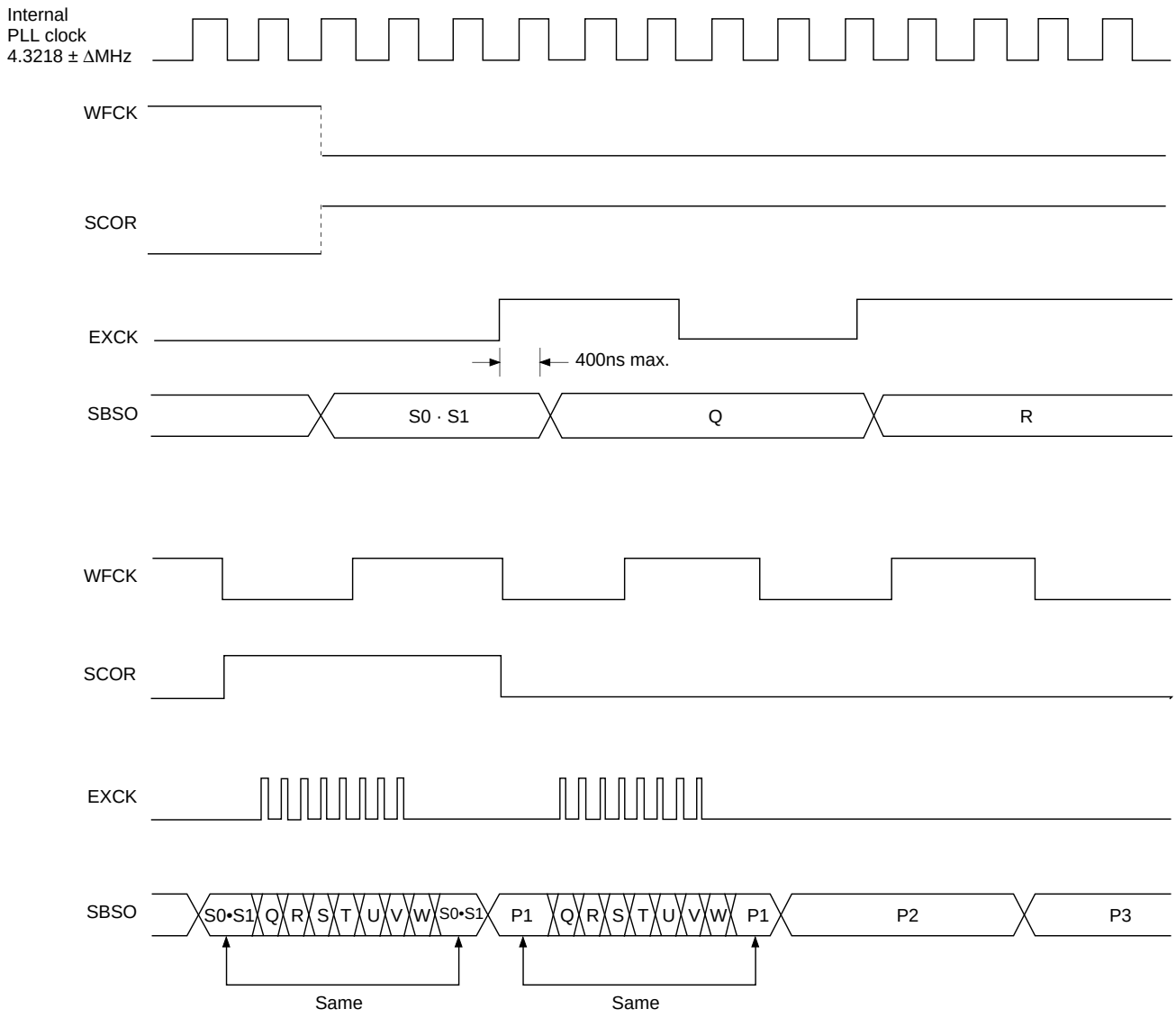
Data can be read out by inputting EXCK immediately after WFCK falls. (See the Timing Chart 2-1.)

2-2. 80-bit Sub Q Read

Fig. 2-1 shows the peripheral block of the 80-bit Sub Q register.

- First, Sub Q, regenerated at one bit per frame, is input to the 80-bit serial/parallel register and the CRC check circuit.
- 96-bit Sub Q is input, and if the CRC is OK, it is output to SQSO with CRCF = 1. In addition, the 80 bits are loaded into the parallel/serial register.
  When SQSO goes high 400µs or more (monostable multivibrator time constant) after the subcode is read out, the CPU determines that new data (which passed the CRC check) has been loaded.
- In the CXD2529Q, when 80-bit data is loaded, the order of the MSB and LSB is inverted for each byte. As a result, although the sequence of bytes is the same, the bits within the bytes are now ordered LSB first.
- Once the fact that the 80-bit data has been loaded is confirmed, SQCK is input so that the data can be read out. In the CXD2529Q, the SQCK input is detected, and when it is low the retriggerable monostable multivibrator is reset.
- The retriggerable monostable multivibrator has a time constant from 270 to 400µs. When the duration for which SQCK is high is less than this time constant, the monostable multivibrator is kept reset; during this interval, the S/P register is not loaded into the P/S register.
- While the monostable multivibrator is being reset, data cannot be loaded in the 80-bit parallel/serial register.
  In other words, while reading out with a clock cycle shorter than the monostable multivibrator time constant, the register is not rewritten by CRCOK, etc. (See the Timing Chart 2-2.)
- Although a clock is input from the SQCK pin to actually perform these operations, the high and low intervals for this clock should be between 750ns and 120µs.

Timing Chart 2-1



Sub Code P.Q.R.S.T.U.V.W Read Timing

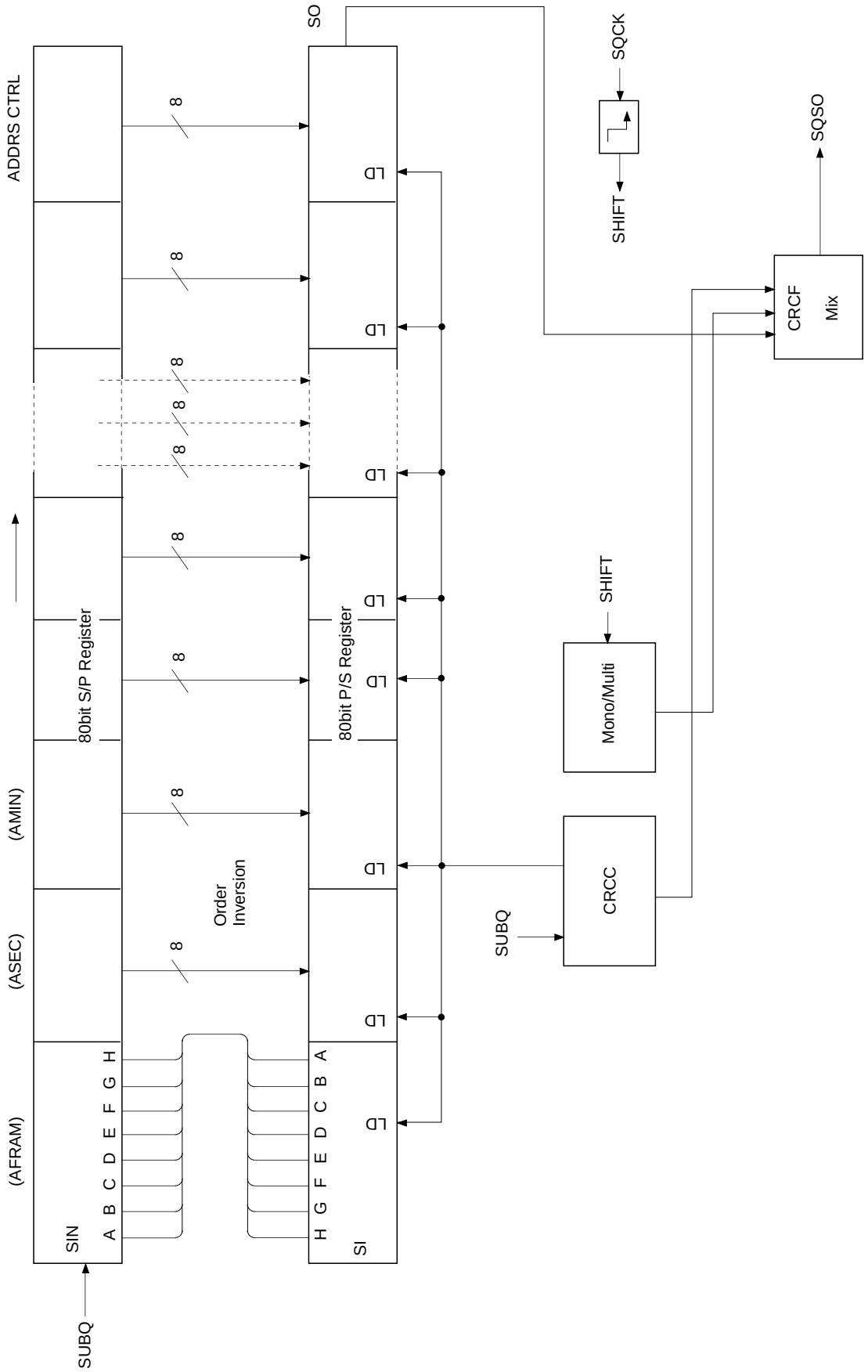
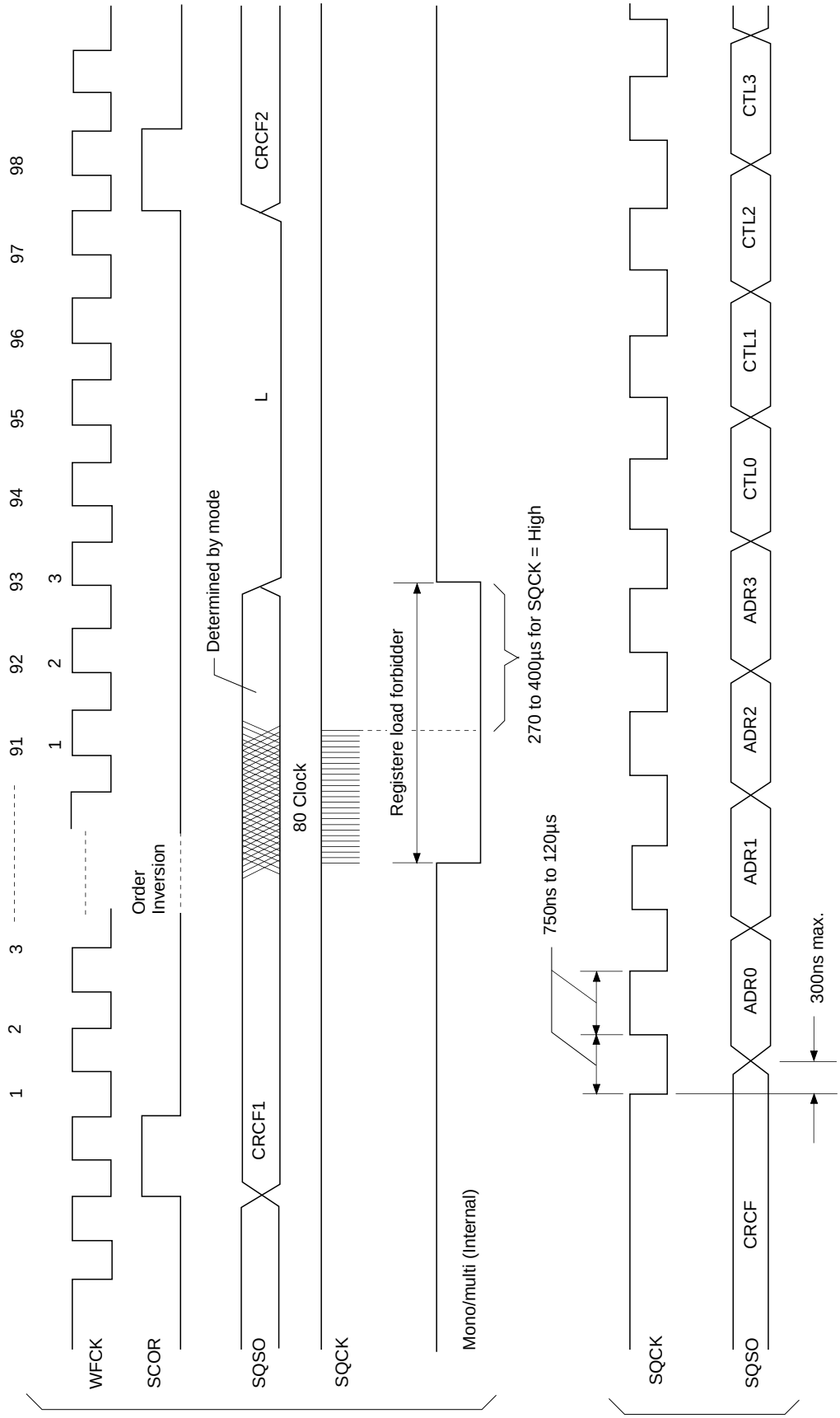
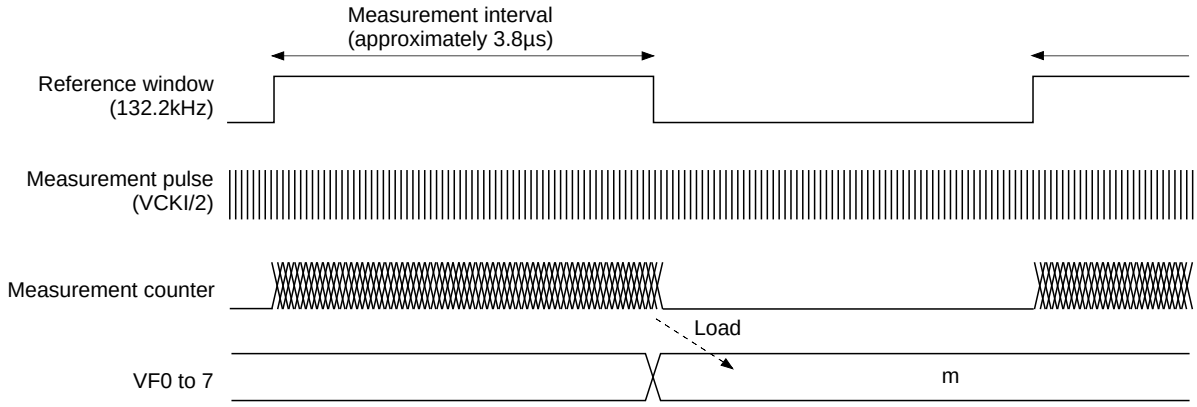


Fig. 2-1. Block Diagram

Timing Chart 2-2



Timing Chart 2-3



The relative velocity R of the disc can be expressed with the following equation.

$$R = \frac{m + 1}{32}$$ (R: Relative velocity, m: Measurement results)

VF0 to 7 is the result obtained by counting VCKI/2 pulses while the reference signal (132.2kHz) generated from the crystal (384Fs) is high. This count is 31 when the disc is rotating at normal speed and 63 when it is rotating at double speed (when DSPB is low).

3. Description of Modes

This LSI has three basic operating modes using a combination of spindle control and the PLL. The operations for each mode are described below.

3-1. CLV-N mode

This mode is compatible with the CXD2507AQ, and operation is the same as the CXD2507AQ. Accordingly, the PLL capture range is ±150kHz.

3-2. CLV-W mode

This is the wide capture range mode. This mode allows the PLL to follow the rotational velocity of the disc. This rotational following control has two types: using the built-in VCO2 or providing an external VCO. The spindle is the CLV servo like the CXD2507AQ. Operation using the built-in VCO2 is described below. (When using an external VCO, input the signal from the VPCO pin to the low-pass filter, use the output from the low-pass filter as the control voltage for the external VCO, and input the oscillation from the VCO to the VCKI pin.)

While starting to rotate a disc and/or speeding up to the lock range speed from the condition that a disc stops, CAV-W mode should be used. Specifically, first send $E665X to set CAV-W mode and kick a disc, then send $E60C to set CLV-W mode if ALOCK is high, which can be read out serially from the SQSO pin. CLV-W mode is used for playback while ALOCK is high. The microcomputer monitors the serial data output, and must return to adjust-speed operation (CAV-W mode) when ALOCK becomes low. The control flow according to the microcomputer software in CLV-W mode is shown in Fig. 3-2.

In CLV-W mode (normal), low power consumption is achieved by setting LPWR to high. Control was formerly performed by applying acceleration and deceleration pulses to the spindle motor. However, when LPWR is set to high, deceleration pulses are not output, thereby achieving low power consumption mode.

CLV-W mode supports control only by the ternary output of the MDP pin. Therefore, when using CLV-W mode, set DCLV PWM MD to low.

Note) The capture range for this mode is theoretically up to the signal processing limit.

3-3. CAV-W mode

This is the CAV mode. In this mode, the external clock is fixed but the spindle rotational velocity can be controlled as desired. The rotational velocity is determined by the VP0 to 7 setting values or the external PWM. When controlling the spindle with VP0 to 7, setting the CAV-W mode with the $E665 command and controlling VP0 to 7 with the $DX commands allows the rotational velocity to be varied from low speed to double speed. (See the $DX commands.) Also, when controlling the spindle with the external PWM, the PWMI pin is binary input which becomes KICK during high intervals and BRAKE during low intervals.

The microcomputer can know the rotational velocity using the V16M oscillation frequency. The reference frequency for the velocity measurement is the 132.3kHz signal obtained by dividing the crystal (384Fs) by 128. The velocity is obtained by counting V16M/2 pulses while the reference is high, and the result is output from the new CPU interface as 8 bits (VP0 to 7). These measurement results are 31 when the disc is rotating at normal speed or 63 when it is rotating at double speed. These values match those of the 256-n for control with VP0 to 7.

In CAV-W mode, the spindle is set to the desired rotational velocity and the operation speed for the entire system follows this rotational velocity. Therefore, the cycles for the Fs system clock, PCM data and all other output signals from this LSI change according to the rotational velocity of the disc (except for DATO, CLKO and XLTO).

Note) The capture range for this mode is theoretically up to the signal processing limit.

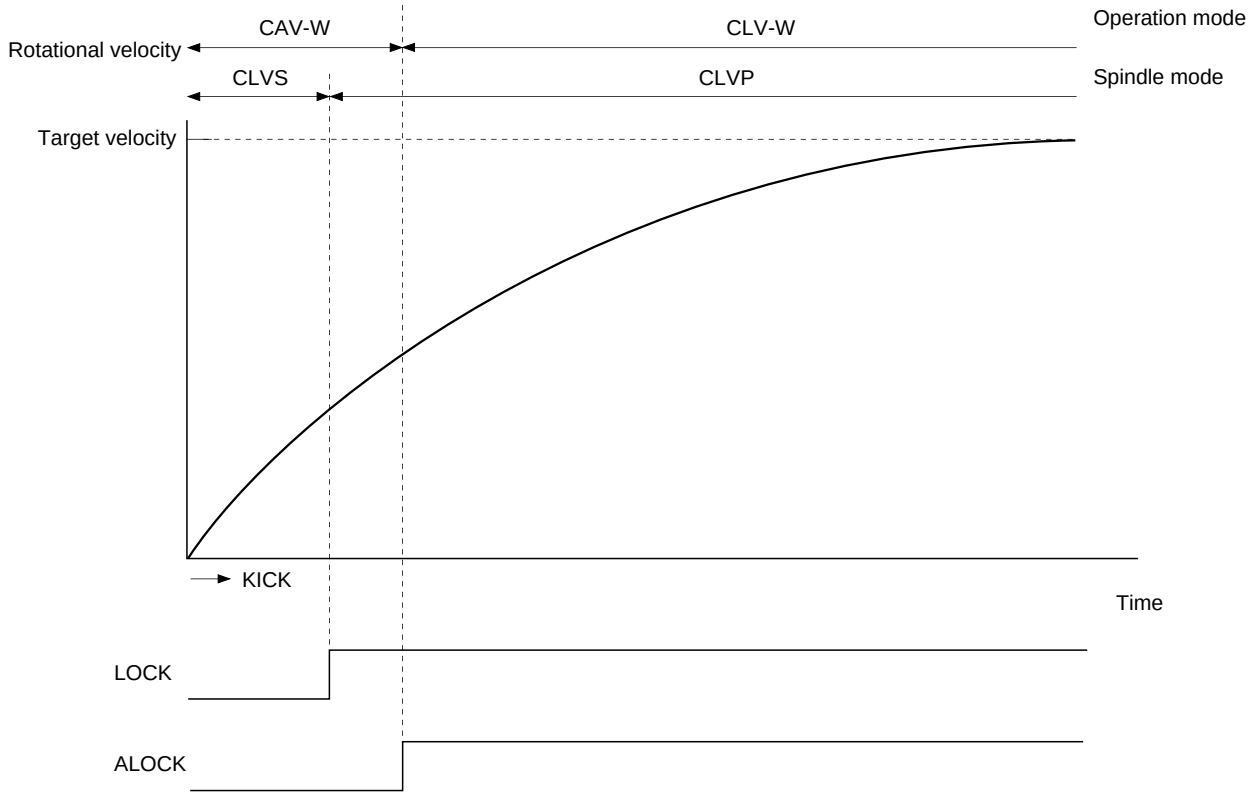


Fig. 3-1. Disc Stop to Normal Condition in CLV-W Mode

CLV-W Mode

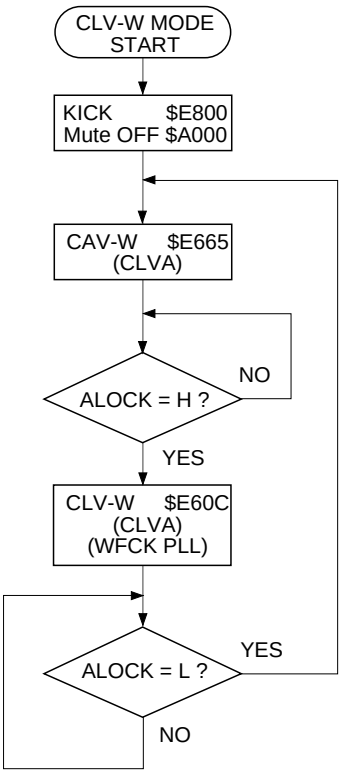


Fig. 3-2. CLV-W Mode Flow Chart

4. Description of Other Functions

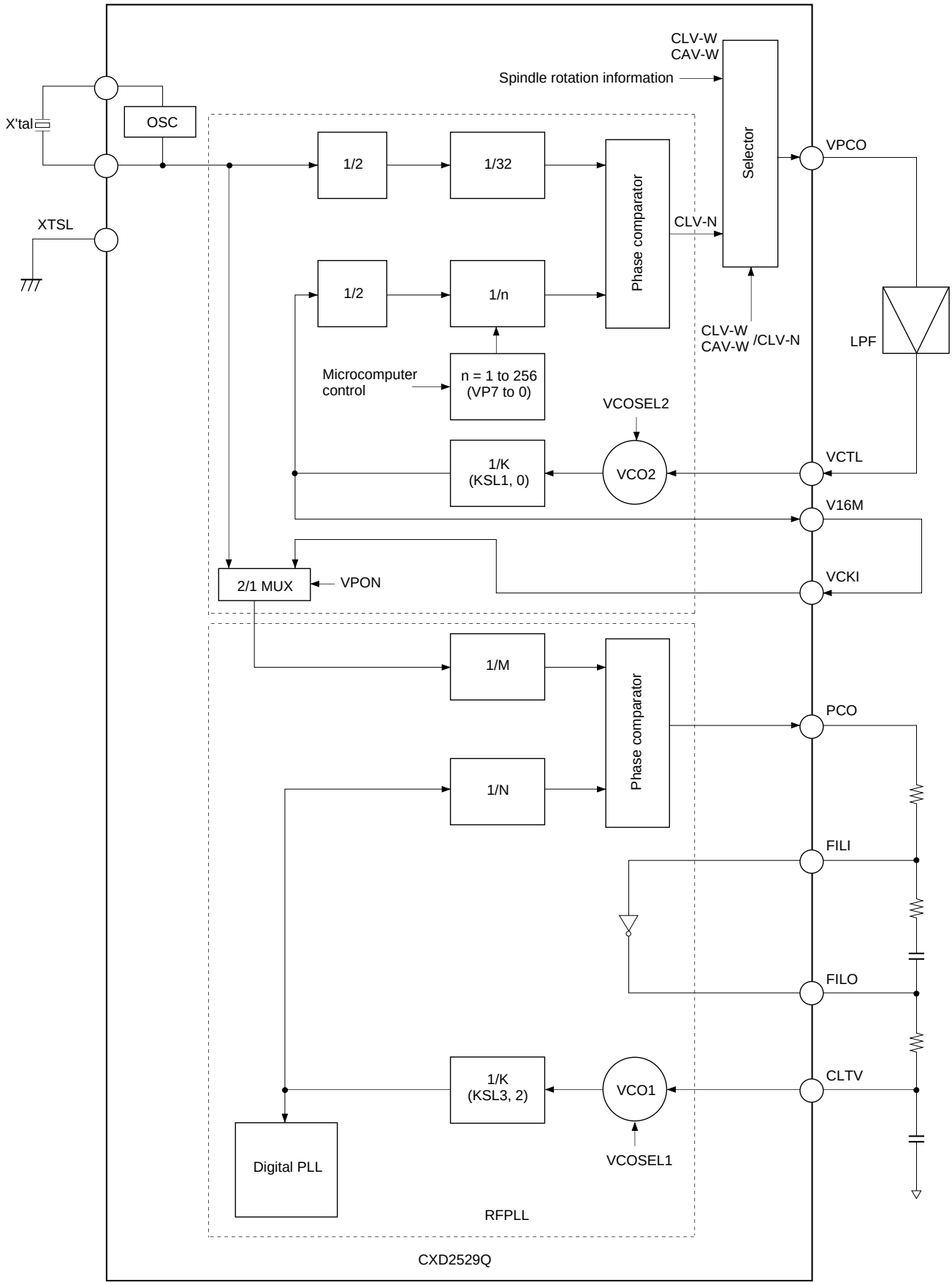
4-1. Channel Clock Regeneration by the Digital PLL Circuit

- The channel clock is necessary for demodulating the EFM signal regenerated by the optical system.
  Assuming T as the channel clock cycle, the EFM signal is modulated in an integer multiple of T from 3T to 11T. In order to read out the information in the EFM signal, this integer value must be read correctly. As a result, T, that is the channel clock, is necessary.
  In an actual player, PLL is necessary to regenerate the channel clock because the fluctuation in the spindle rotation alters the width of the EFM signal pulses.

The block diagram of this PLL is shown in Fig. 4-1.
The CXD2529Q has a built-in three-stage PLL.

- The first-stage PLL is for the wide-band PLL. When the built-in VCO2 is used, LPF is required externally. When the built-in VCO2 is not used, LPF and VCO are required externally.
  The output of this first-stage PLL is used as a reference for all clocks within the LSI.
- The second-stage PLL generates a high-frequency clock needed by the third-stage digital PLL.
- The third-stage PLL is a digital PLL that regenerates the actual channel clock.
- The new digital PLL in CLV-W mode follows the rotational velocity of the disc, in addition to the conventional secondary loop.

Block Diagram 4-1



4-2. Frame Sync Protection

- In a CD player operating at normal speed, a frame sync is recorded approximately every 136µs (7.35kHz). This signal is used as a reference to know which data is the data within a frame. Conversely, if the frame sync cannot be recognized, the data is processed as error data because it cannot be recognized what the data is. As a result, recognizing the frame sync properly is extremely important for improving playability.
- In the CXD2529Q, window protection and forward protection/backward protection have been adopted for frame sync protection. The adoption of these functions achieves very powerful frame sync protection.
  There are two window widths: one for cases where a rotational disturbance affects the player and the other for cases where there is no rotational disturbance (WSEL = 0/1). In addition, the forward protection counter is fixed to 13, and the backward protection counter is fixed to 3. In other words, when the frame sync is being played back normally and then cannot be detected due to scratches or other problems, a maximum of 13 frames are inserted. If the frame sync cannot be detected for 13 frames or more, the window is released and the frame sync is resynchronized.
  In addition, immediately after the window is released and resynchronization is executed, if a proper frame sync cannot be detected within 3 frames, the window is released immediately.

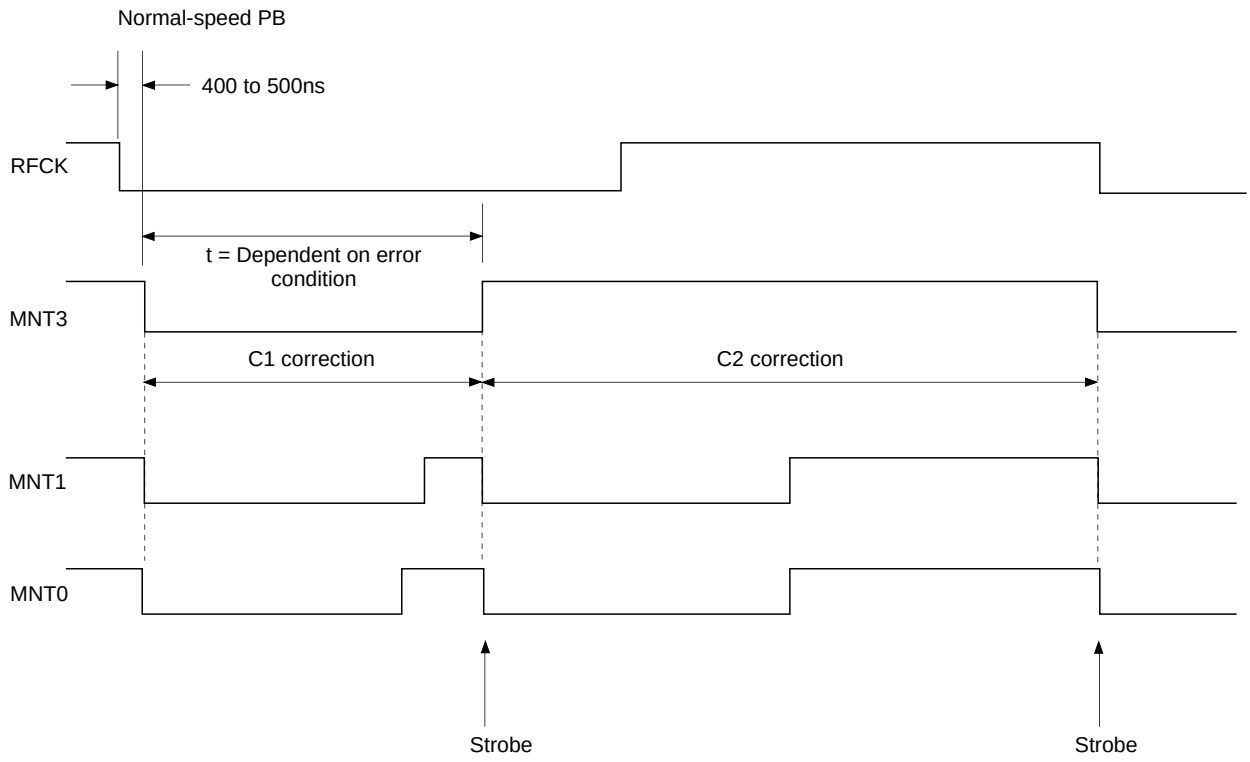
4-3. Error Correction

- In the CD format, one 8-bit data contains two error correction codes, C1 and C2. For C1 correction, the code is created with 28-byte information and 4-byte C1 parity.
  For C2 correction, the code is created with 24-byte information and 4-byte parity.
  Both C1 and C2 are Reed-Solomon codes with a minimum distance of 5.
- The CXD2529Q SEC strategy provides excellent playability through powerful frame sync protection and C1 and C2 error corrections.
- The correction status can be monitored outside the LSI.
  See Table 4-1.
- When the C2 pointer is high, the data in question was uncorrectable. Either the pre-value was held for that data, or an average value interpolation was made.

MNT3	MNT1	MNT0	Description
0	0	0	No C1 errors
0	0	1	One C1 error corrected
0	1	1	C1 correction impossible
1	0	0	No C2 errors
1	0	1	One C2 error corrected
1	1	1	C2 correction impossible

Table 4-1.

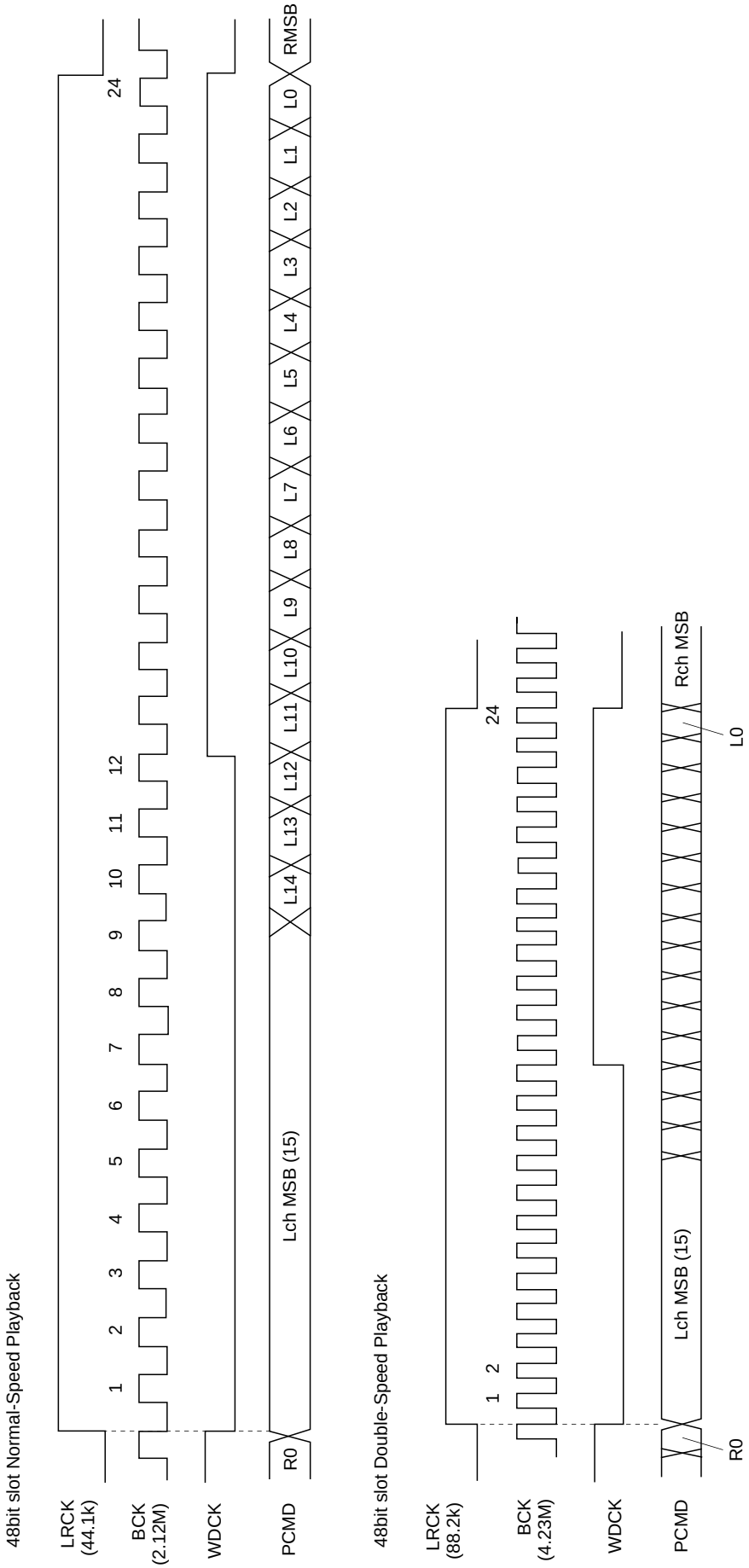
Timing Chart 4-1



4-4. DA Interface

- The CXD2529Q DA interface is as described below.
  This interface includes 48 cycles of the bit clock within one LRCK cycle, and is MSB first. When LRCK is high, the data is for the left channel.

Timing Chart 4-2



4-5. Digital Out

There are three Digital Out formats: the type 1 format for broadcasting stations, the type 2 form 1 format for home use, and the type 2 form 2 format for the manufacture of software.

The CXD2529Q supports type 2 form 1.

Sub Q data which are matched twice in succession after a CRC check are input to the first four bits (bit 0 to 3) of the channel status.

Digital Out C bit

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	From sub Q				0	0	0	0	1	0	0	0	0	0	0	0
	ID0	ID1	COPY	Emph												
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0	0
32	0															
48																
176																

Bits 0 to 3... Sub Q control bits that matched twice with CRCOK
Bit 29 ... 1 when VPON is 1

Table 4-2.

4-6. Servo Auto Sequencer

This function performs a series of controls, including auto focus and track jumps. When the auto sequence command is received from the CPU, auto focus, 1-track jump, 2N-track jumps, and N-track move are executed automatically.

SSP (servo signal processor LSI) is used in an exclusive manner during the auto sequence execution (when XBUSY = low), so that commands from the CPU are not transferred to the SSP, but can be sent to the CXD2529Q.

Connect the CPU, RF and SSP as shown in Fig. 4-2.

When CLOK goes from low to high while XBUSY is low, XBUSY does not become high for a maximum of 100µs after that point. This is designed to prevent the transfer of erroneous data to the SSP when XBUSY changes from low to high by the monostable multivibrator, which is reset by CLOK being low (when XBUSY is low).

(a) Auto Focus ($47)

Focus search-up is performed, FOK and FZC are checked, and the focus servo is turned on.

If $47 is received from the CPU, the focus servo is turned on according to Fig. 4-3. The auto focus starts with focus search-up, and the pickup should be lowered beforehand (focus search-down). In addition, blind E of register 5 is used to eliminate FZC chattering. In other words, the focus servo is turned on at the falling edge of FZC after FZC has been continuously high for a longer time than E.

Connection diagram for using auto sequencer (example)

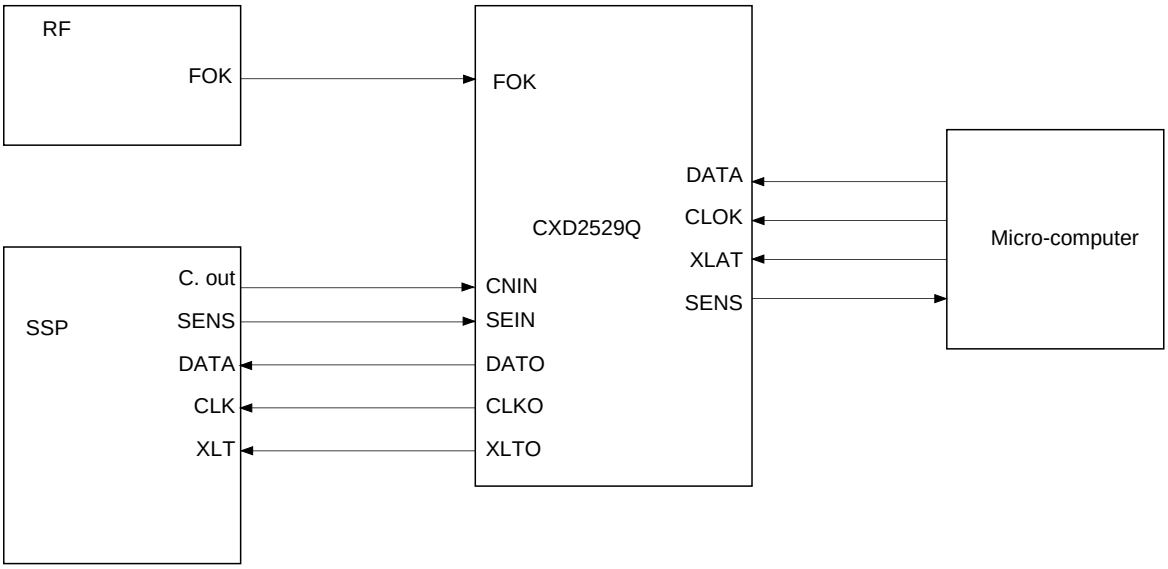


Fig. 4-2.

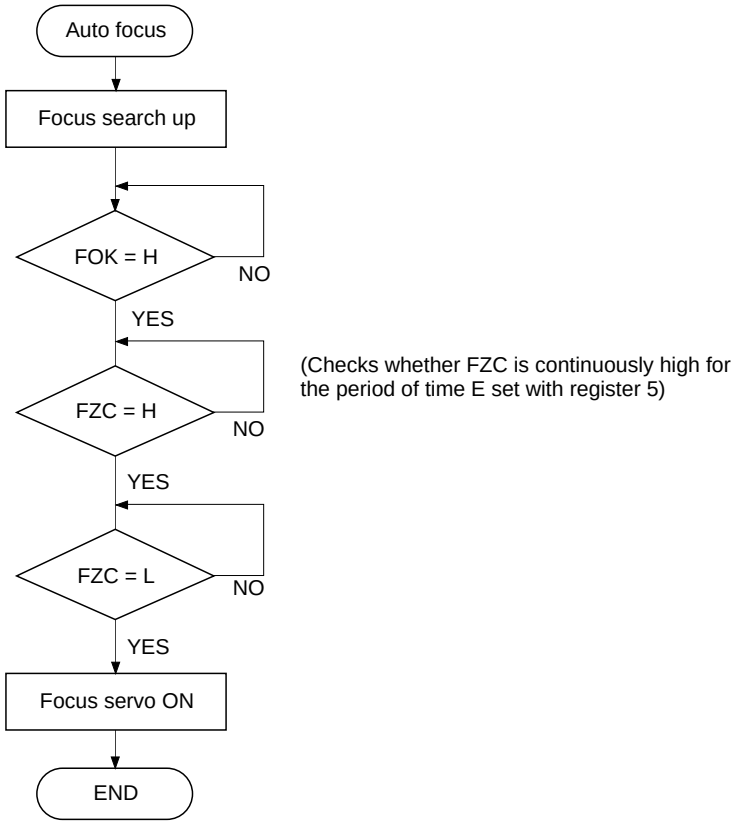


Fig. 4-3-(a). Auto Focus Flow Chart

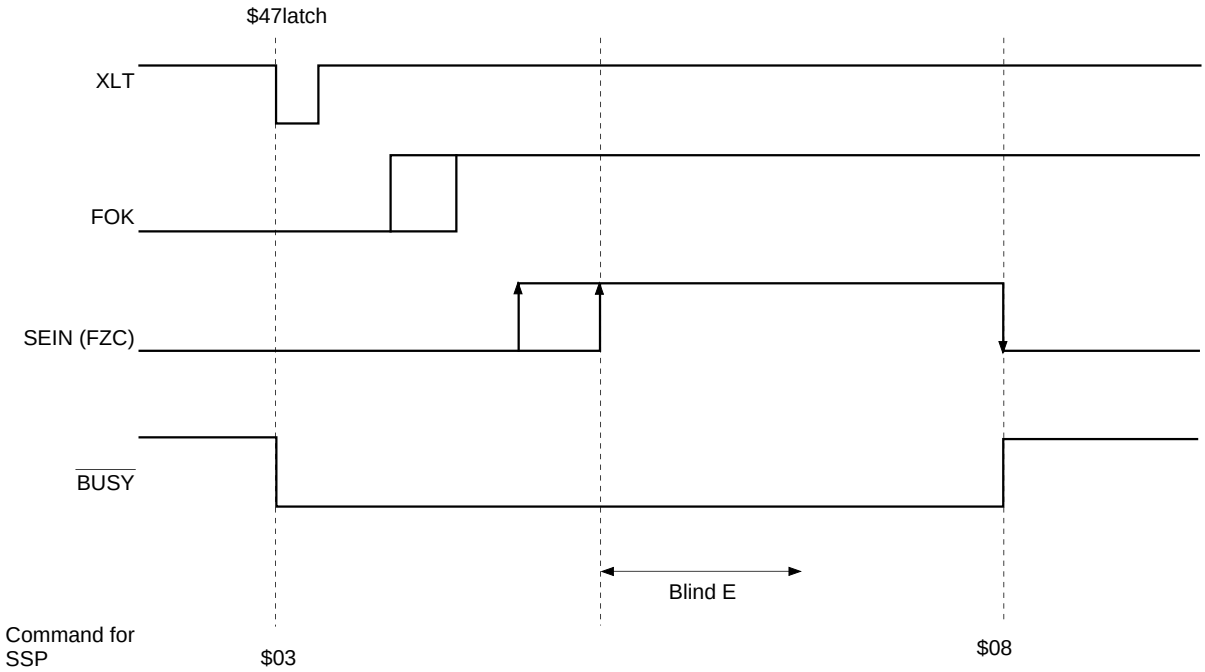


Fig. 4-3-(b). Auto Focus Timing Chart

(b) Track Jump

1, 10, and 2N-track jumps are performed respectively. Always use this when focus, tracking, and the sled servo are on. Note that tracking gain-up and braking-on should be sent beforehand because they are not performed.

- 1-track jump

  When $48 ($49 for REV) is received from the CPU, a FWD (REV) 1-track jump is performed in accordance with Fig. 4-4. Set blind A and brake B with register 5.

- 10-track jump

  When $4A ($4B for REV) is received from the CPU, a FWD (REV) 10-track jump is performed in accordance with Fig. 4-5. The principal difference between the 10-track jump and the 1-track jump is whether to kick the sled or not. In addition, after kicking the actuator, when 5 tracks have been counted through CNIN, the brake is applied to the actuator. Then, when the actuator speed is found to have slowed up enough (determined by the CNIN cycle becoming longer than the overflow C set in register 5), the tracking and sled servos are turned on.

- 2N-track jump

  When $4C ($4D for REV) is received from the CPU, a FWD (REV) 2N-track jump is performed in accordance with Fig. 4-6. The track jump count “N” is set in register 7. Although N can be set to 2^{16} tracks, note that the setting is actually limited by the actuator. CNIN is used for counting the number of jumps.

  Although the 2N track jump basically follows the same sequence as the 10-track jump, the one difference is that after the tracking servo is turned on, the sled continues to move only for “D”, set in register 6.

- N-track move

  When $4E ($4F for REV) is received from the CPU, a FWD (REV) N-track move is performed in accordance with Fig. 4-7. N can be set to a maximum of 2^{16} tracks. CNIN is used for counting the number of jumps. This N-track move uses a method in which only the sled is moved, and is suited for moves over thousands of tracks.

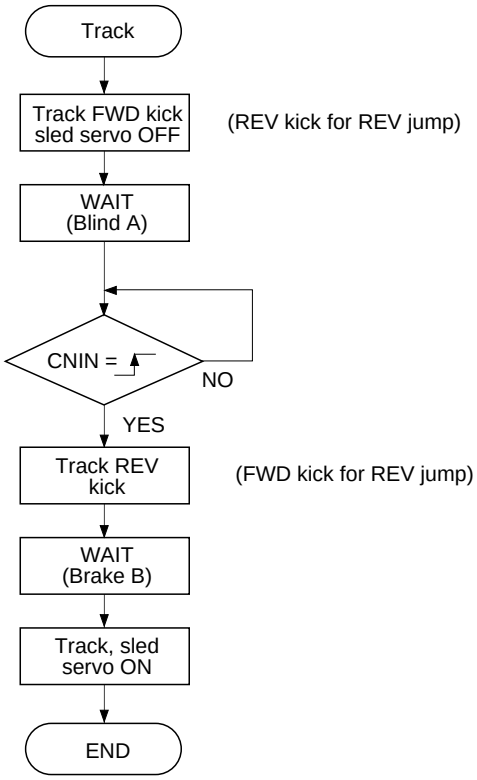


Fig. 4-4-(a). 1-Track Jump Flow Chart

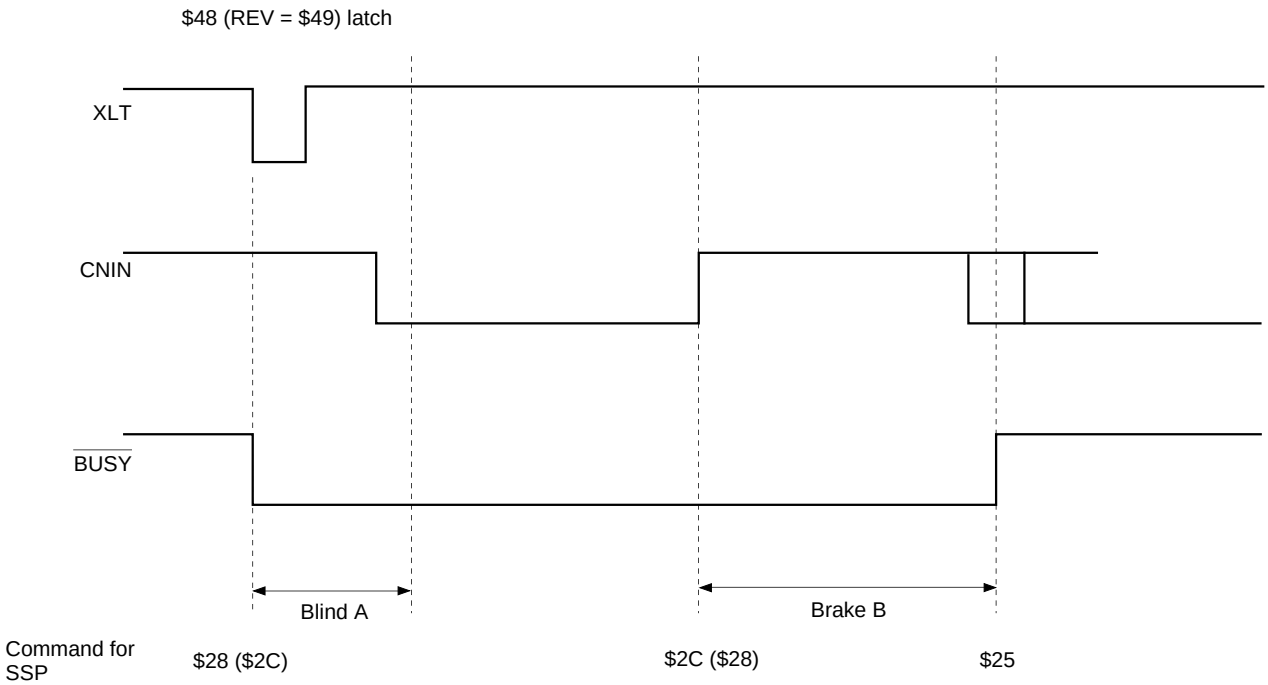


Fig. 4-4-(b). 1-Track Jump Timing Chart

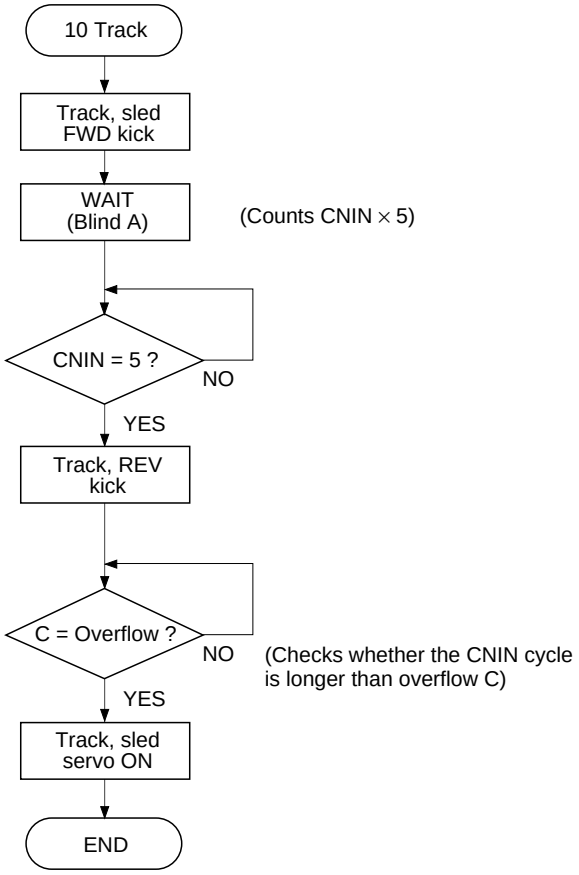


Fig. 4-5-(a). 10-Track Jump Flow Chart

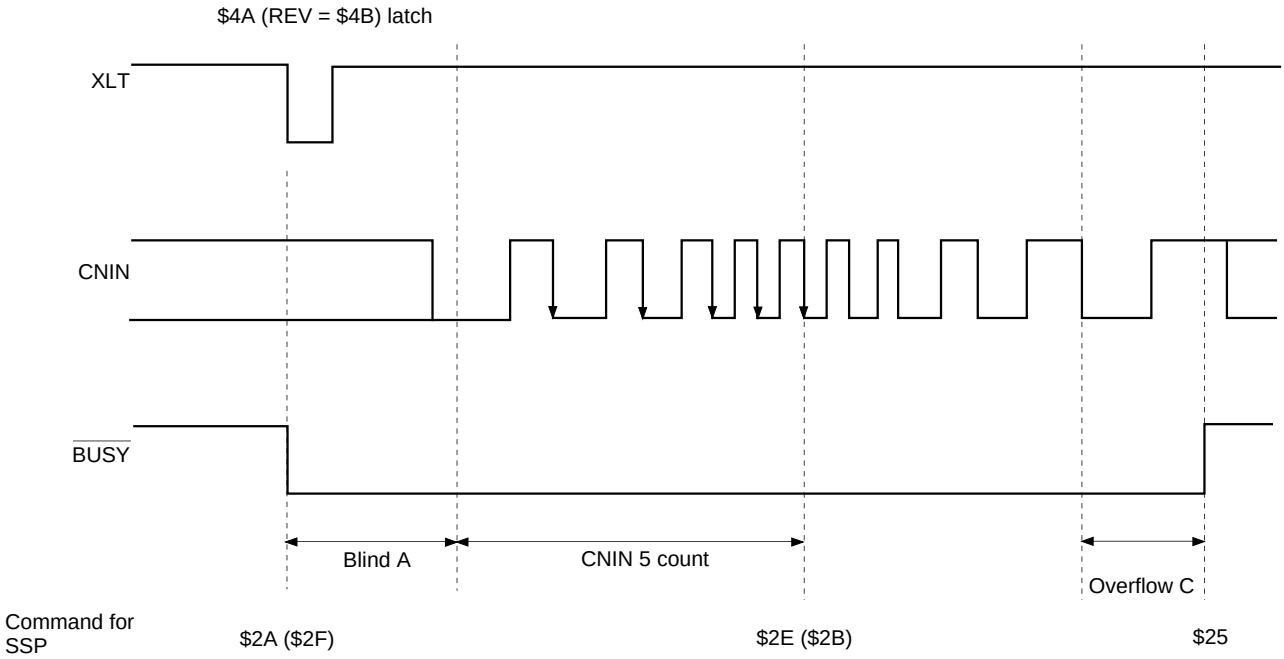


Fig. 4-5-(b). 10-Track Jump Timing Chart

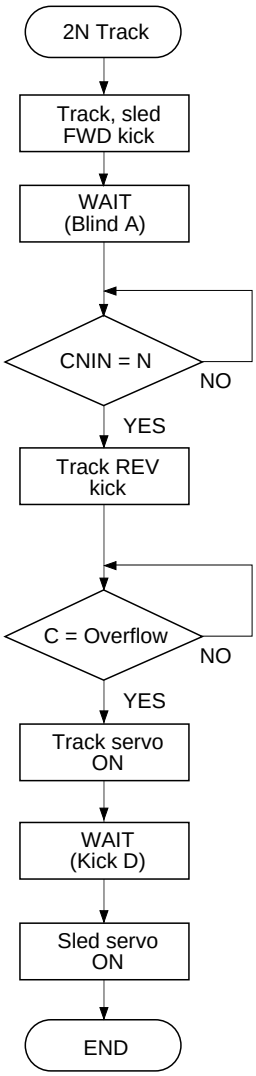


Fig. 4-6-(a). 2N-Track Jump Flow Chart

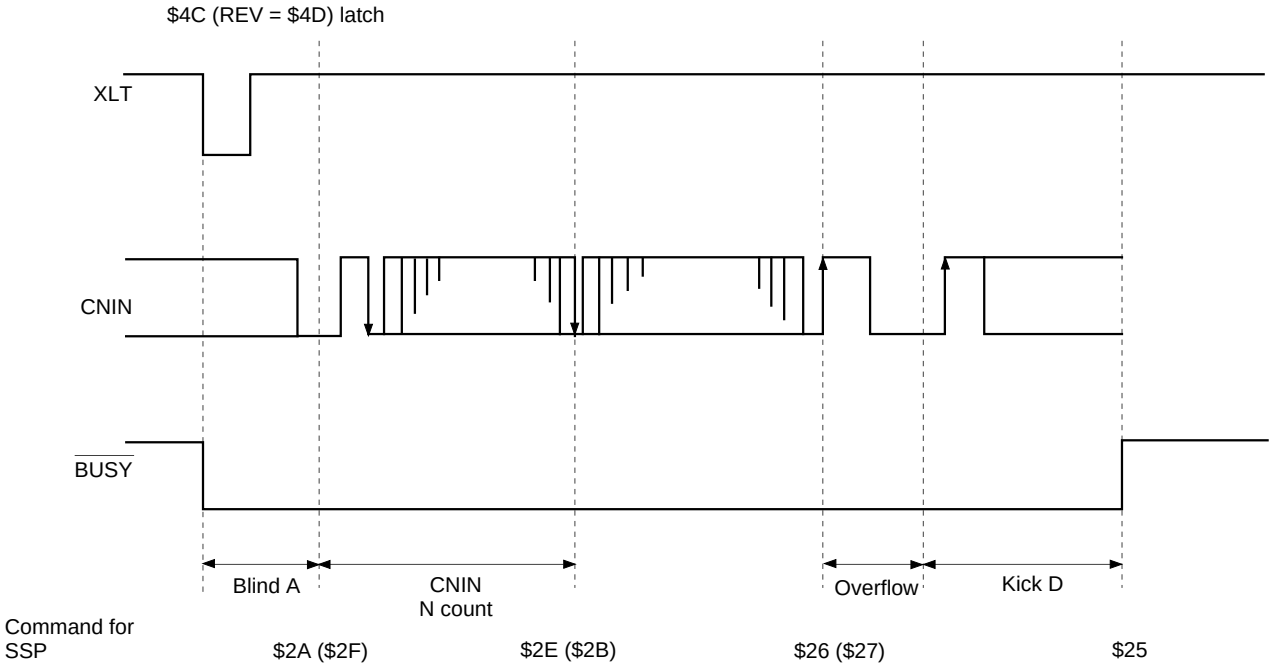


Fig. 4-6-(b). 2N-Track Jump Timing Chart

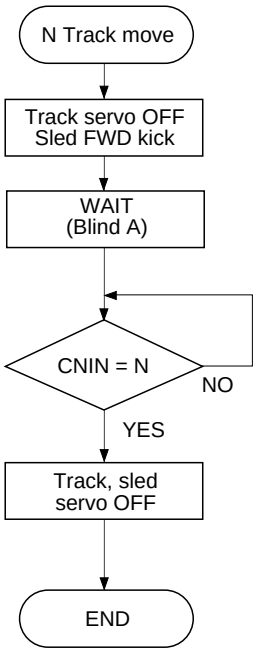


Fig. 4-7-(a). N-Track Move Flow Chart

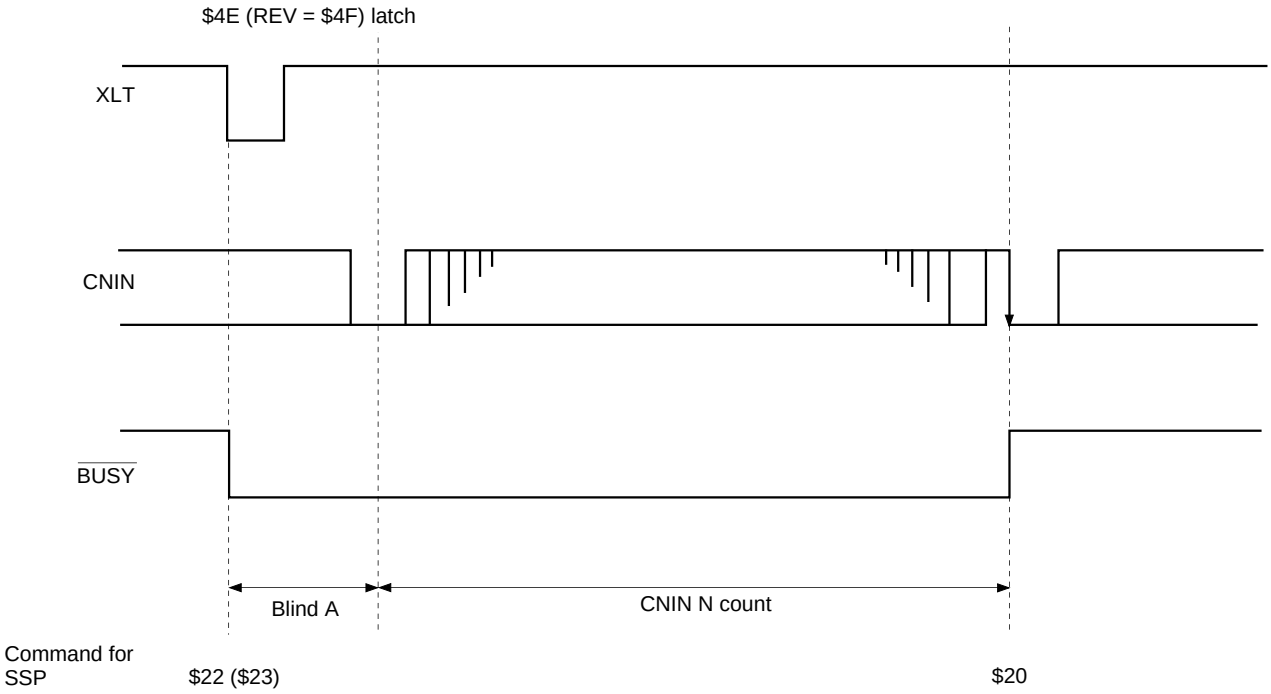
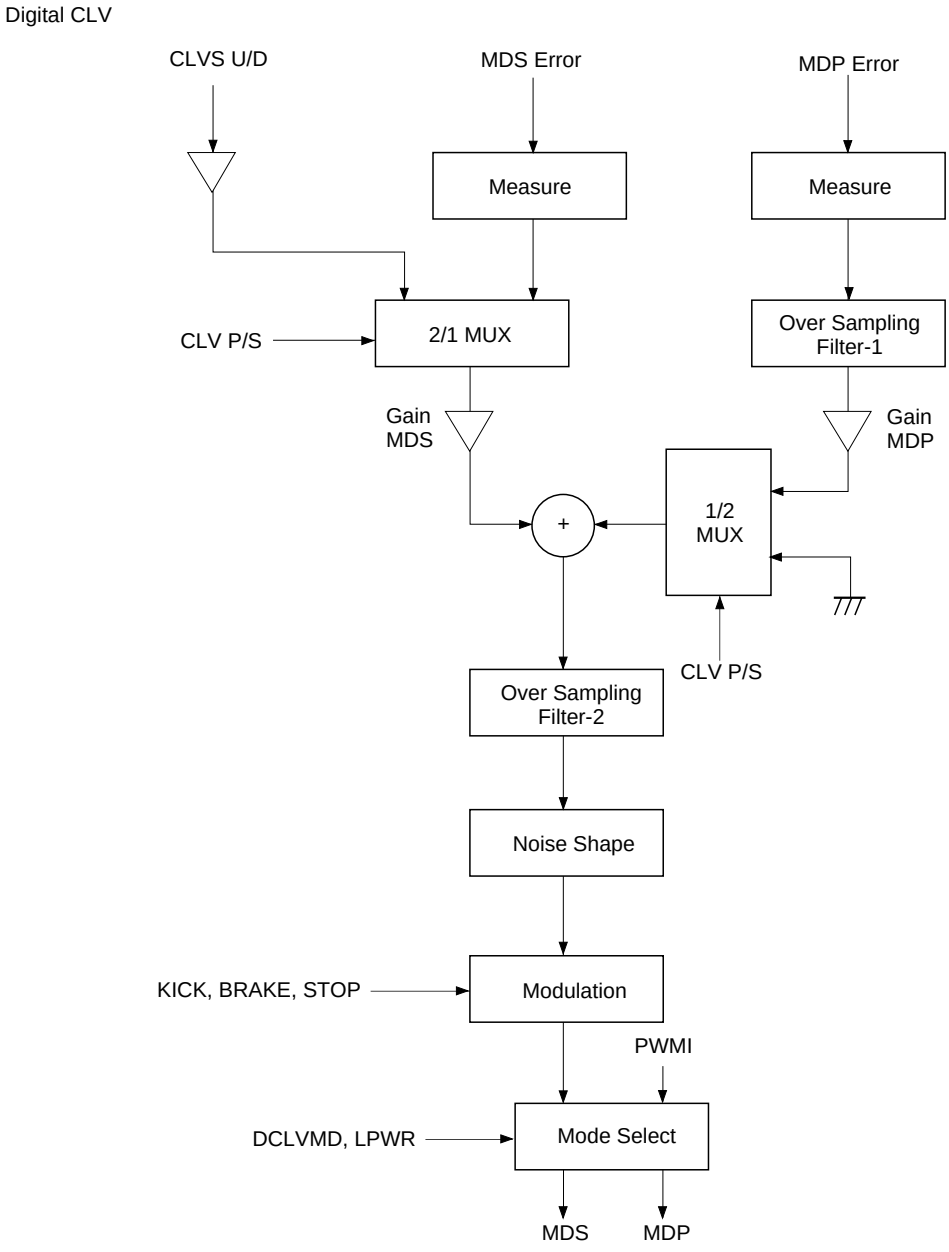


Fig. 4-7-(b). N-Track Move Timing Chart

4-7. Digital CLV

Fig. 4-8 shows the Block Diagram. Digital CLV allows PWM output in CLVS, CLVP and other modes with the MDS error and MDP error signal sampling frequency increased to 130kHz during normal-speed operation. In addition, the digital spindle servo can set the gain.



CLVS U/D: Up/down signal from the CLVS servo
MDS error: Frequency error for CLVP servo
MDP error: Phase error for CLVP servo
PWMI: Spindle drive signal from the microcomputer

Fig. 4-8. Block Diagram

4-8. Asymmetry Compensation

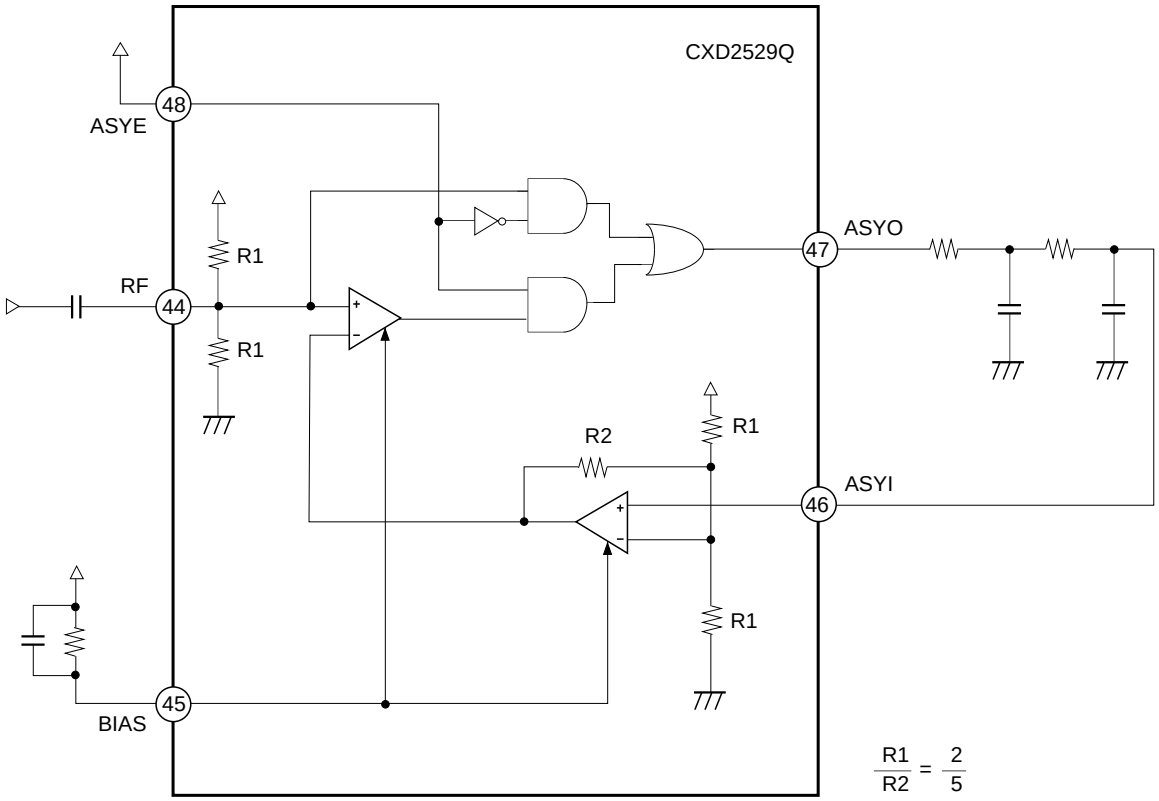


Fig. 4-9. Example of Asymmetry Compensation Application Circuit

5. 1-bit DAC Block

5-1. DAC Block Input Timing

Fig. 5-1 shows the input timing for the DAC block.

In the CXD2529Q, there is no internal transfer of audio data from the CD signal processing block to the DAC block. Therefore, data can be transferred to the DAC block through an audio DSP or similar device.

When data is input to the DAC block without passing through an audio DSP or similar device, data should be connected externally. In this case, EMPH, LRCK, BCK and PCMD can be connected directly with EMPHI, LRCKI, BCKI and PCMDI respectively.

5-2. Description of DAC Block Functions

Zero Data Detection

When the condition where the lower 4 bits of the input data are DC and the remaining upper bits are all “0” or all “1” continues for approximately 300ms, zero data is detected. Zero data detection is performed independently for the left and right channels.

Mute Flag Output

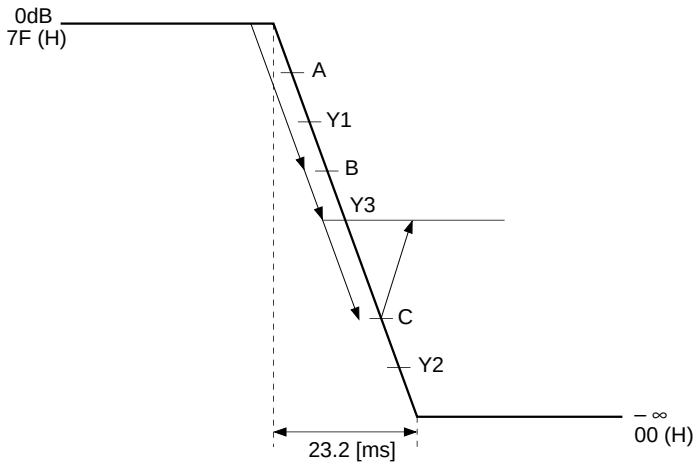
The LMUT and RMUT pins become active when any of the following conditions are met.

The polarity can be selected by the $9X command ZDPL.

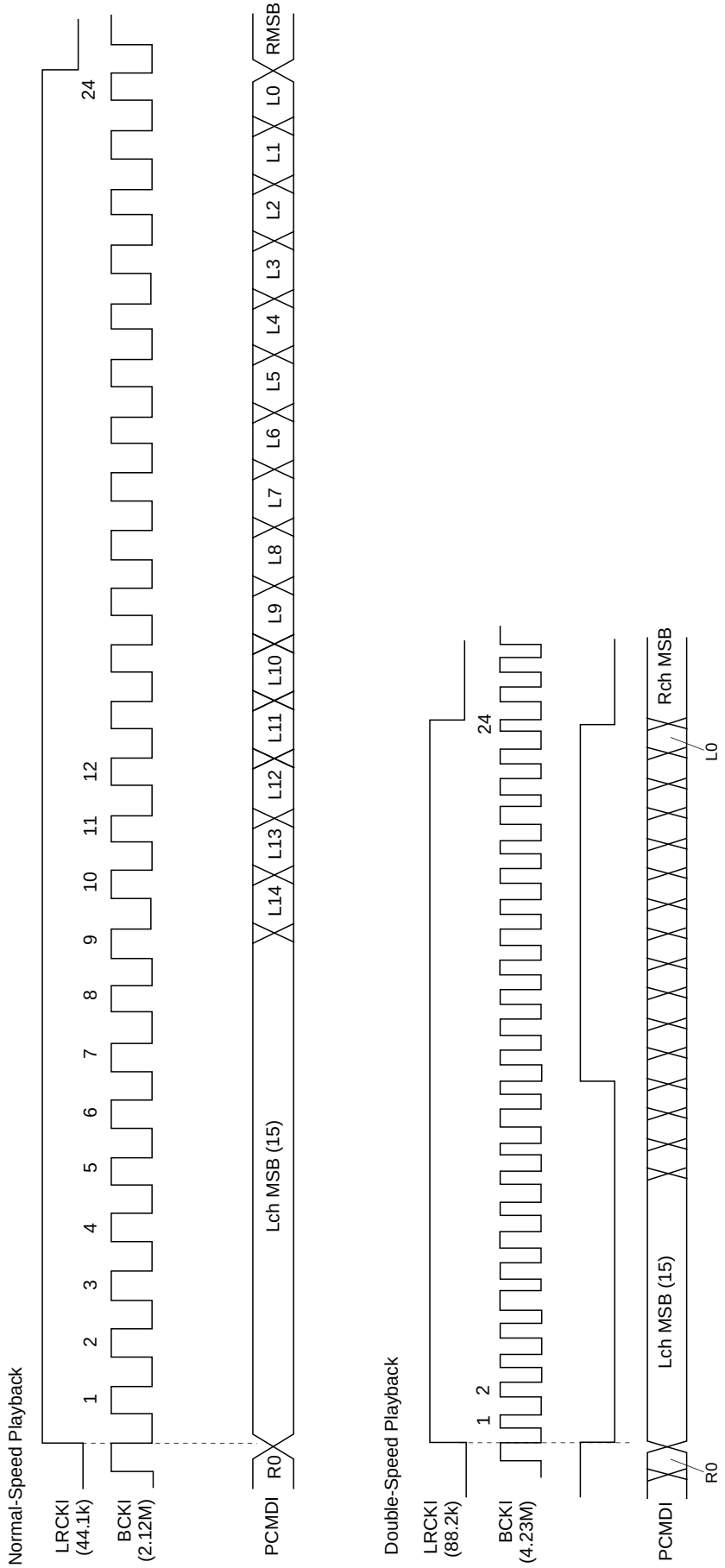
- When zero data is detected.
- When a high signal is input to the SYSM pin.
- When the $AX command SMUT is set.

Attenuation Operation

Assume attenuation data X1, X2, and X3, where X1 > X3 > X2, and audio outputs Y1, Y2, and Y3, where Y1 > Y3 > Y2. First, assume X1 is transferred and then X2 is transferred. If X2 is transferred before Y1 is reached (state “A” in the diagram), then the value continues approaching Y2. Next, if X3 is transferred before Y2 is reached (either state “B” or “C”), the value begins approaching Y3 from the value at that point (“B” or “C”).



Timing Chart 5-1



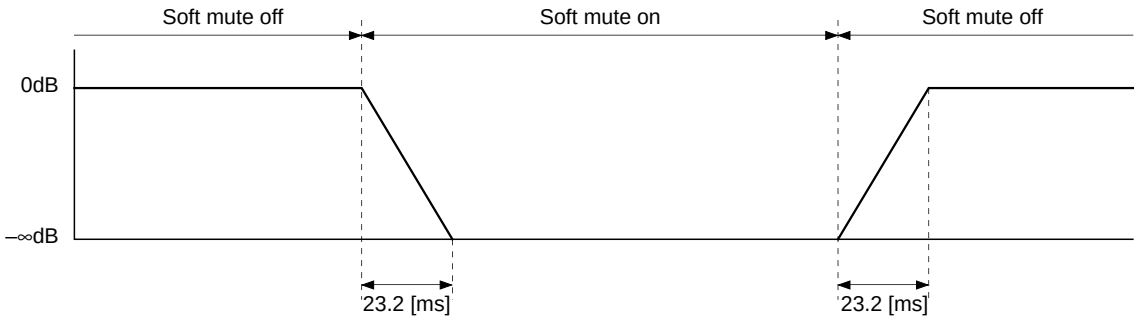
Input Timing for DAC Block

DAC Block Mute Operation

Soft mute

Soft mute is applied when any of the following conditions are met. Mute is performed, attenuating the input data.

- When attenuation data is set to 000 (h)
- When the $AX command SMUT is set to 1
- When a high signal is input to the SYSM pin



Forced mute

Forced mute is applied when the $AX command FMUT is set to 1.

The PWM output to the LPF block is fixed to low.

* Set OPSL2 to 1 for FMUT setting. (See the description of “$AX commands”.)

Zero detection mute

Forced mute is applied when the $9X command ZMUT is set to 1 and the zero data is detected for the left and right channels.

(See the description of “Zero Data Detection”.)

LRCK Synchronization

Synchronization is performed at the first LRCK input falling edge during reset. When the LRCK input frequency varies, the synchronization is lost. At that time, resynchronization should be executed.

The LRCK input frequency varies to the IC master clock switching and playback speed change when the high/low levels of the XTSL pin change, $9 command DSPB setting changes or $9X command MCSL setting changes.

Also, LRCK may be switched when there is another IC between the CD DSP block and DAC block. In this case resynchronization is required.

In order to perform resynchronization, set the $AX command LRCK to 1 and set LRWO to 0 after one LRCK cycle or more.

* Set LRWO with OPSL2 = 1. (See the description of “$AX commands”.)
* Set the $9X command SYCOF = 0 in advance when setting LRWO to 1.

SYCOF

Playback can be simply performed by setting SYCOF of address 9 to 1 when LRCK is connected to LRCKI, PCMD to PCMDI and BCK to BCK in CAV-W mode.

Normally, the memory proof and the like is used for playback in CAV-W mode.

In this mode, the LRCK output conforms not to the crystal but to the VCO. Therefore, synchronization is frequently lost.

By setting SYCOF of address 9 to 1, the synchronization loss of the LRCKI input is ignored and the playback can be simply performed.

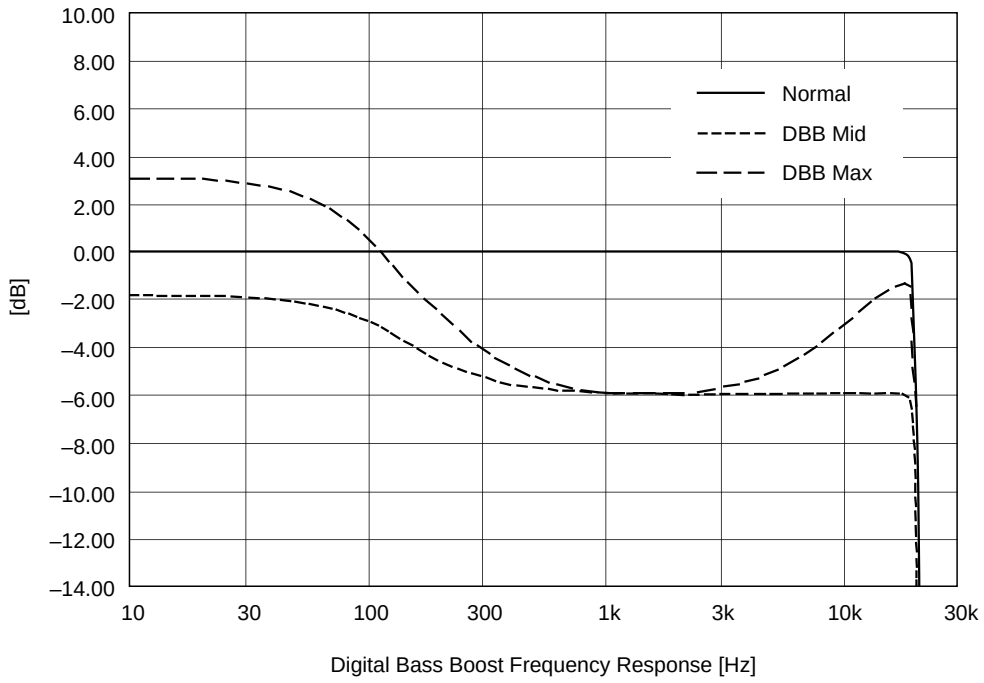
However, the playback is not perfect because the pre-value hold or data skip is occurred for the LRCKI input wow flatter.

* Set SYCOF to 0 in all cases except for the playback with LRCK directly connected to LRCKI, PCMD to PCMDI and BCK to BCK in CAV-W mode.
* Set SYCOF to 0 in advance when LRCK resynchronization is applied with LRWO = 0.

Digital Bass Boost

Bass boost without the external parts is possible by the built-in digital filter. The strength of boost has 2 levels; Mid and Max. BSBST and BBSL of address A are used for the setting.

See Graph 5-2 for the digital bass boost frequency response.



Graph 5-2.

6. LPF Block

The CXD2529Q incorporates a first-stage secondary active LPF and a reference voltage-applied operational amplifier, which require many resistors and capacitors.
The cut-off frequency fc can be freely set due to the external resistors and capacitors.
Here, the reference voltage (Vc) is (AV_{DD} – AV_{SS})/2.

Fig. 6-1 shows the LPF block application circuit.
In this circuit, the cut-off frequency is fc ≈ 40kHz.

The external capacitors' values when fc = 30kHz and 50kHz are indicated below for reference.
The resistors' values do not change.

- When fc ≈ 30kHz:
  C1 = 200pF, C2 = 910pF
- When fc ≈ 50kHz:
  C1 = 120pF, C2 = 560pF

LPF Block Application Circuit

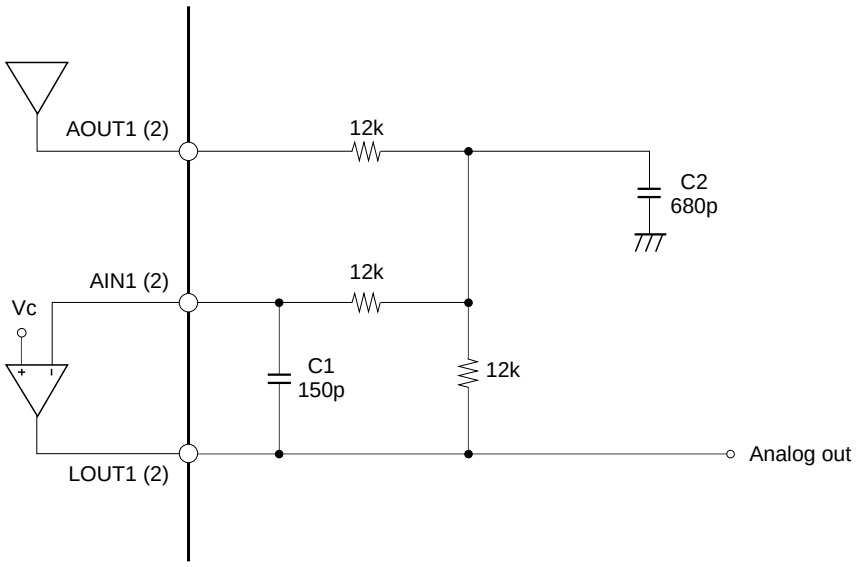


Fig. 6-1. LPF External Circuit Example

7. Setting Method of the CXD2529Q Playback Speed (in CLV-N mode)

(A) CD-DSP block

The playback modes shown below can be selected by the combination of the crystal, XTSL pin and $9X command DSPB.

CD-DSP block playback speed

Crystal	XTSL	DSPB	CD-DSP block playback speed
768Fs	1	0	×1
768Fs	1	1	×2
384Fs	0	0	×1
384Fs	0	1	×2
384Fs	1	1	×1*1

Fs = 44.1kHz

*1 Low power consumption mode. The CD-DSP processing speed is halved, allowing the power consumption to be decreased.

(B) 1-bit DAC block

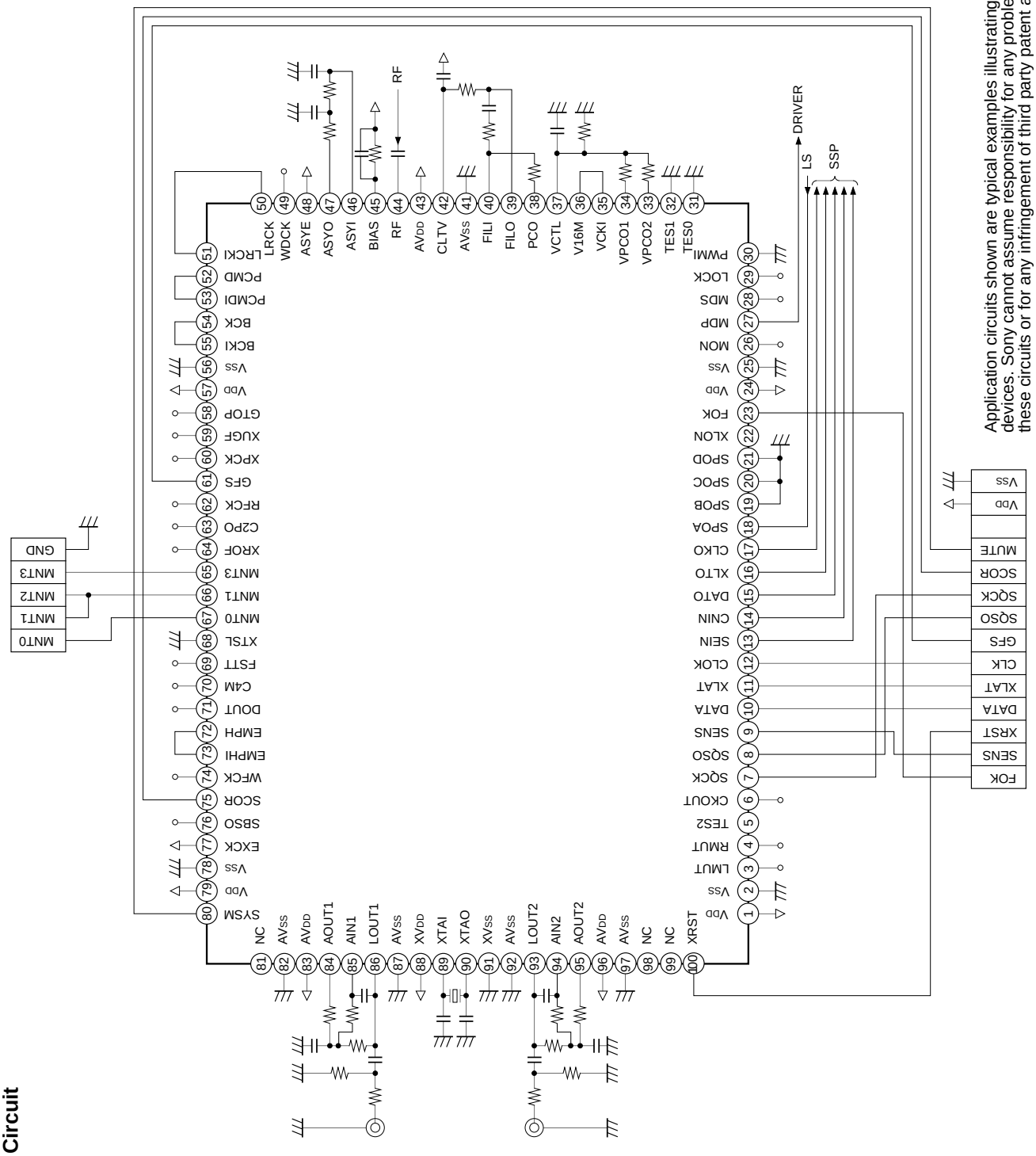
The operating speed of the DAC block is determined by the crystal and the $9X command MCSL regardless of the operating conditions of the CD-DSP block mentioned above. This allows the playback mode for the DAC block and CD-DSP block to be set independently.

1-bit DAC block playback speed

Crystal	MCSL	DAC block playback speed
768Fs	1	×1
768Fs	0	×2
384Fs	0	×1

Fs = 44.1kHz

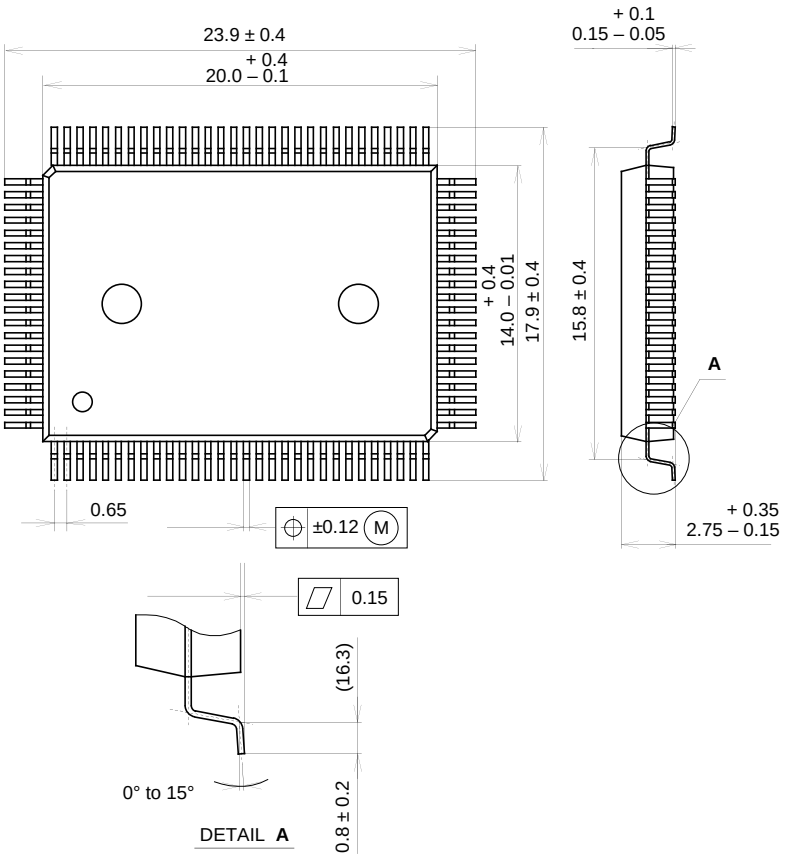
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	∗QFP100-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g