LM21305 Evaluation Board

National Semiconductor
Application Note 2042
Yang Zhang
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LM21305 Overview

The LM21305 is a full featured adjustable frequency synchronous buck regulator capable of delivering up to 5A of continuous output current. The device is optimized to work over the input voltage range of 3V to 18V and output voltage range of 0.6V to 5V, making it suitable for wide variety of applications. The LM21305 provides 1% output voltage accuracy and excellent line and fast load transient response for digital loads. The device offers flexible system configuration via programmable switching frequency through an external resistor and ability to synchronize switching frequency. The frequency of this device can be from 300 kHz to 1.5 MHz. The device also provides internal soft-start to limit in-rush current, cycle-by-cycle current limiting, and thermal shutdown.

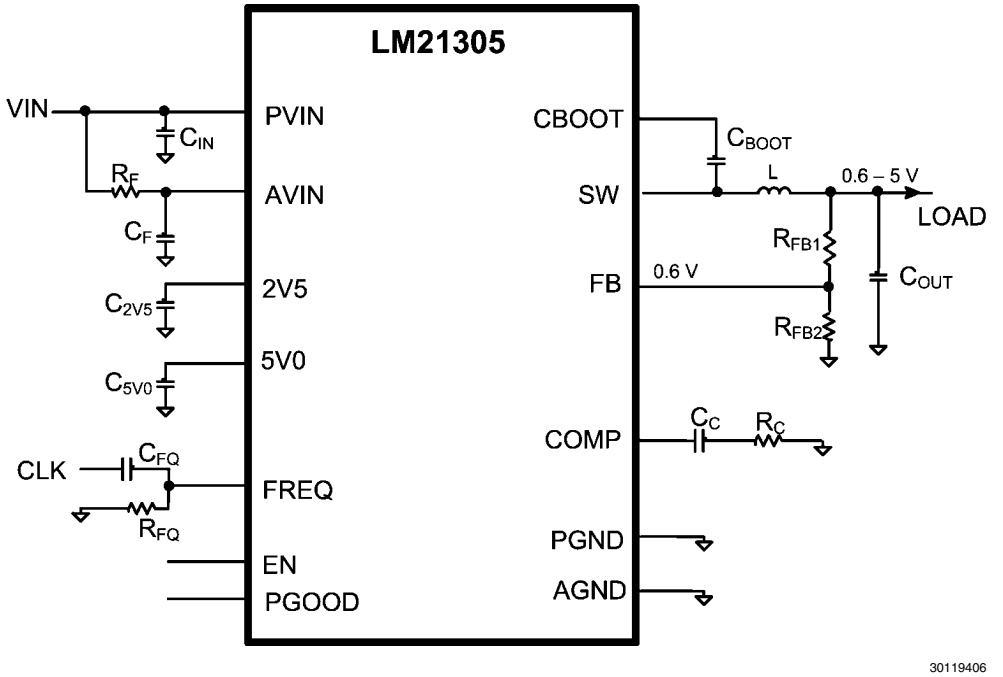
The device features internal over voltage protection (OVP) and over current protection (OCP) circuits for increased system reliability. A precision enable pin and integrated UVLO allows the turn-on of the device to be tightly controlled and sequenced. Start-up inrush currents are limited by an internal Soft-Start circuit. Fault detection and supply sequencing are possible with the integrated power good circuit.

The LM21305 is offered in a 28-pin LLP package with an exposed pad for enhanced thermal performance.

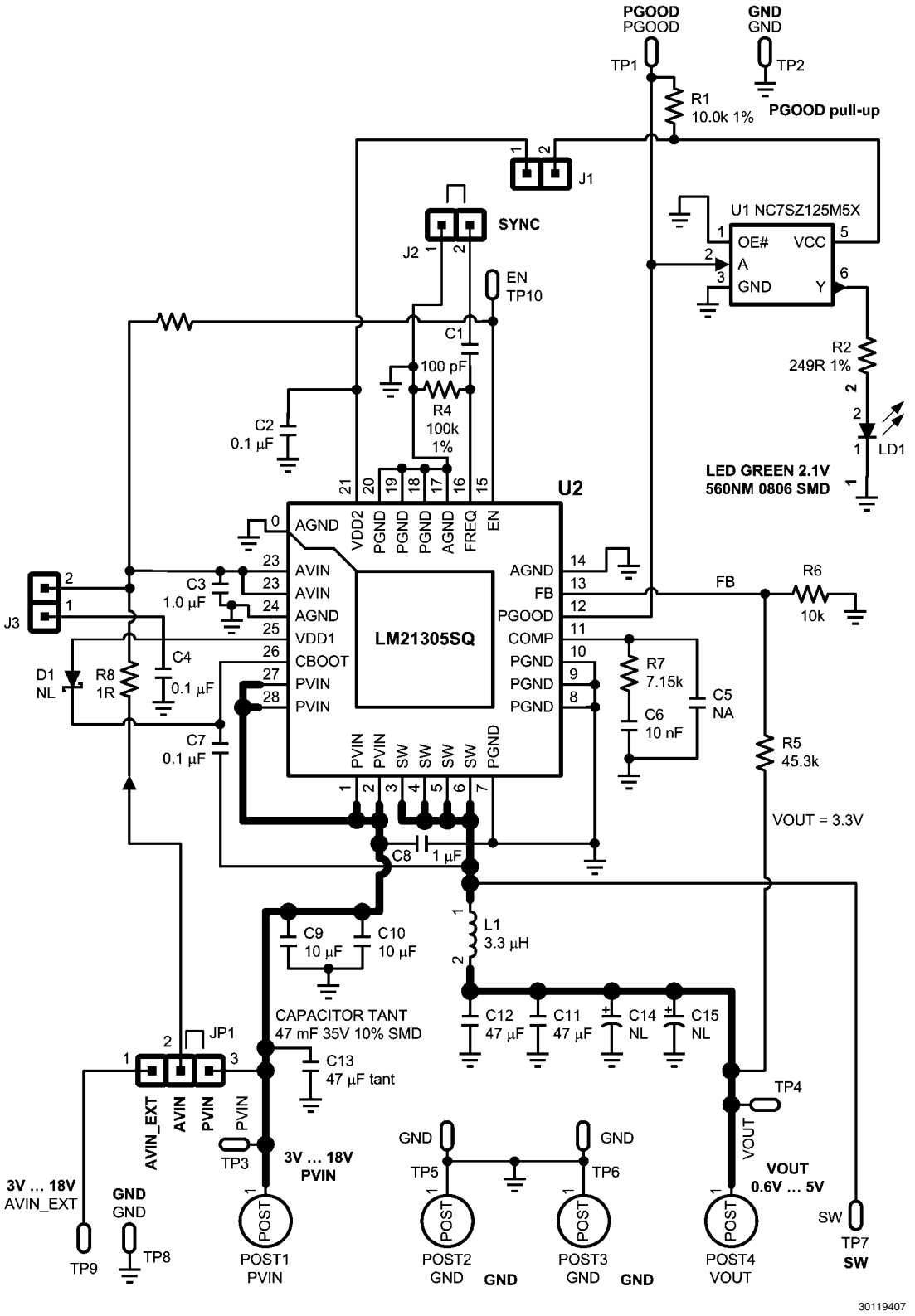
The LM21305 Evaluation board comes ready to operate at the following conditions:

Parameter	Default Voltage	Range and Options
PVIN	12V	External supply 5V to 18V
AVIN	=PVIN	=PVIN or by separate supply (3V to 18V) selected by JP1
VOUT	3.3V	0.6V to 5V by changing R5 and/or R6
Switching Frequency	500 kHz	300 kHz to 1.5 MHz by changing R4
I_{OUT}	0 to 5A	
Size	2 inches x 1.5 inches	
No. of PCB Layers	4	

Typical Application Circuit



Evaluation Board Schematic



Evaluation Board Bill of Materials

Component	Description	Part Number	Package
C1	CERAMIC 100 PF 100V	ECJ-1VC2A101J	603
C2,C4,C7	CERAMIC 0.1 µF 50V	UMK107B7104KA-T	603
C3	CERAMIC 1.0 µF 35V X5R	GMK107BJ105KA	603
C5	NL	NL	NL
C6	CERAMIC 10000 PF 25V	C1608C0G1E103J	603
C8	CERAMIC 1.0 µF 25V X7R	C3216X7R1E105K	1206
C9, C10	CERAMIC 10 µF 50V	UMK325C7106MM-T	1210
C11, C12	CERAMIC 47 µF X5R	GRM32ER61A476KE20L	1210
C13	TANT 47 µF 25V	T495X476K025ATE150	CASE D
C14, C15	NL	NL	NL
D1	NL	NL	NL
L1	3.3 µH 9.0A SMD	744314330	SMD
LD1	LED GREEN	CMDA5CG7D1Z	805
R1, R3, R6	10.0 KΩ 0603 1%	RC0603FR-710KL	603
R2	249Ω 0603 1%	RC0603FR-07249RL	603
R4	100 KΩ 0603 1%	RC0603FR-07100KL	603
R5	45.3 KΩ 0603 1%	RC0603FR-0745K3L	603
R7	7.15 kΩ 0603 1%	RC0603FR-077K15RL	603
R8	1Ω 0603 1%	RC0603FR-071RL	603
U1	IC BUFF NON-INV	NC7SZ125M5X	SOT23-5

Connection Descriptions

Terminal Silkscreen	Description
PVIN	Connect the power supply between this terminal and the GND terminal besides it. The device is rated between 3V to 18V. The absolute voltage rating is 22V.
GND	The GND terminals are meant to provide a close return path to the power and signal terminal besides them. They are all connected together on board.
SW	SW is connected to the switch node of the power stage. It can be used to monitor the switch node waveform by a scope.
VOUT	VOUT terminal is connected to the output capacitor on the board and should be connected to the load
AVIN_EX	LM21305 Evaluation Board allows using a separate supply voltage to AVIN with JP1 selection and a 2nd supply to AVIN_EX terminal. AVIN around 5V will result in the best efficiency in most of the cases.
EN	This terminal connects to the EN pin of the device. The EN is pulled up to AVIN via a 10 kΩ resistor on the board. It also can be externally controlled through this terminal. If driven externally, a voltage typically greater than 1.2V will enable the device.
PGOOD	This terminal connects to the power good output of the device. There is a 10 kΩ pull-up resistor from this pin to the 2V5 pin.

Jumper Settings

Terminal Silkscreen	Description
JP1	Sets the AVIN of LM21305. Pin 2,3 (upper) connected gives AVIN = PVIN. Pin 1,2 connected gives AVIN = AVIN_EX Default pin 2 and 3 connected
J1	Enables the on board LED LD1. When J1 is ON, LD1 will be ON if PGOOD is high. When J1 is OFF, power used to drive LD1 is saved. Default ON
J2	Synchronizing clock input. When J2 is ON, CFQ is connected to ground and switching frequency is controlled by the on board resistor RFQ. When J2 is OFF, switch node waveform will be synchronized to the clock source connected to J2. Default ON
J3	Only should be connected when AVIN = 5V. When AVIN is below 5V, especially around 3.3V, connecting J3 can result in better efficiency. Default OFF Caution: if AVIN > 5.5V, connecting J3 could damage the device.

Other Design Examples

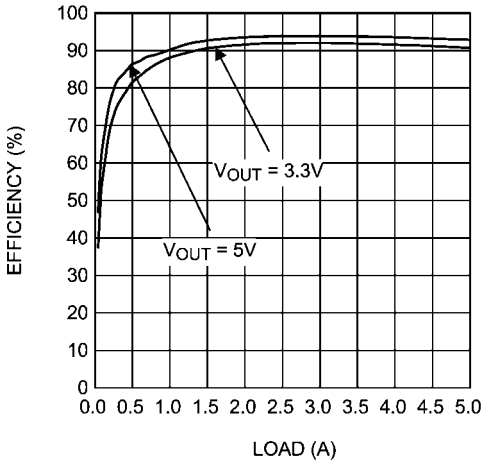
LM21305 is designed to fit a wide variety of applications. A few examples are given for ease of use. Only the components need to be modified are listed below.

Design examples for PVIN = 12V, fs = 500 kHz, $I_{OUT-MAX}$ = 5A, V_{OUT} = 1.2V, 1.8V, 2.5V, 3.3V and 5V:

V_{OUT}	1.2V	1.8V	2.5V	3.3V	5V
C8	10000 pF 25V	10000 pF 25V	4700 pF 25V	4700 pF 25V	4700 pF 25V
L1	1.2 µH	2.2 µH	2.2 µH	3.3 µH 9.0A	3.3 µH
R5	10.0 kΩ 1%	20 kΩ 1%	31.6 kΩ 1%	45.3 kΩ 1%	73.2 kΩ 1%
R7	2.40 kΩ 1%	3.60 kΩ 1%	5.10 kΩ 1%	6.65 kΩ 1%	10.0 kΩ 1%

Typical Performance Characteristics

Efficiency with PVIN = AVIN = 12V
V_{OUT} = 3.3V and 5V, fs = 500 kHz



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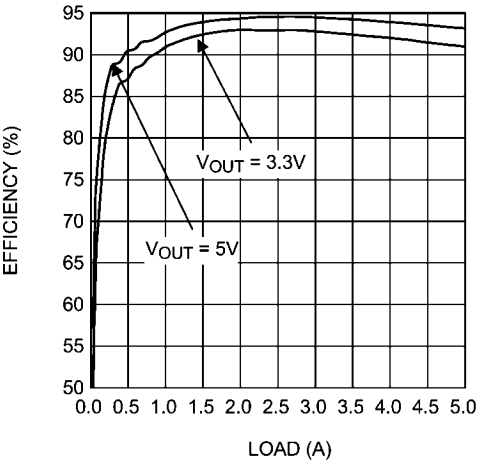
Efficiency with PVIN = 12V, AVIN = 5V
V_{OUT} = 3.3V and 5V, fs = 500 kHz



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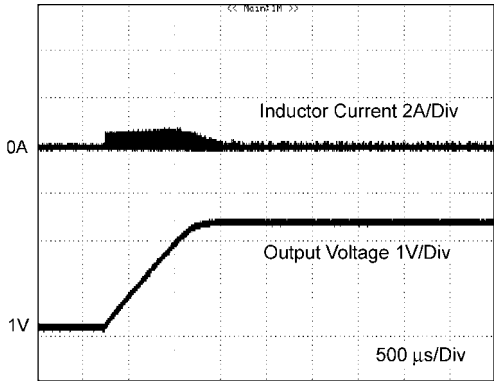
Soft Start with 1V Pre-Bias Voltage, No Load



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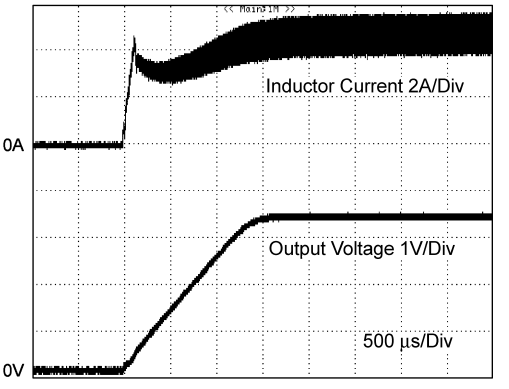
Soft Start with 5A Load



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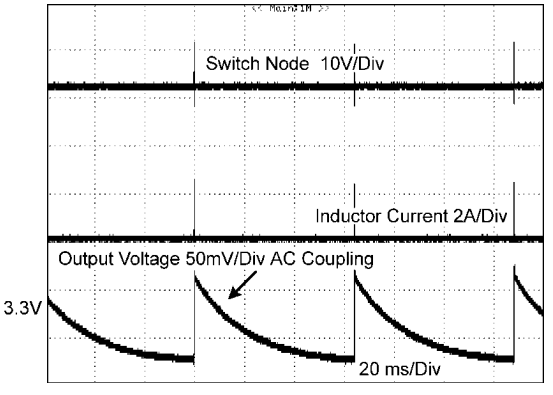
Switching Waveform with 0A Load (DCM Mode)



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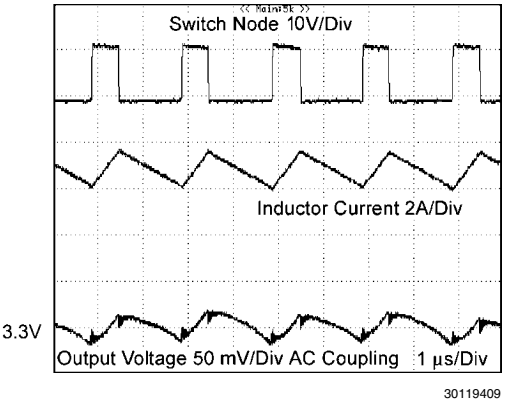
Switching Waveform with 5A Load



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Component Selection

This section provides a simplified design procedure necessary to select the external components to build a fully functional efficient step-down power supply. As with any DC-DC converter, numerous tradeoffs are possible to optimize the design for efficiency, size, and performance. Unless otherwise indicated all formulas assume units of amps (A) for current, farads (F) for capacitance, henries (H) for inductance, volts (V) for voltages and Hertz (Hz) for frequencies. For more details, please refer to the LM21305 datasheet.

INPUT CAPACITORS

PVIN is the supply voltage for the switcher power stage. It is the supply that delivers the output power. The input capacitors on PVIN supplies the large AC switching current drawn by the switching action of the internal MOSFETs. The input current of a buck converter is discontinuous, so the ripple current supplied by the input capacitor is large. The input capacitor must be rated to handle this current. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS\_CIN} = I_{OUT}\frac{\sqrt{V_{OUT}\,(V_{PVIN} - V_{OUT})}}{V_{PVIN}}\ (A)$$

The power dissipated in the input capacitor is given by:

$P_{D\_CIN} = I^{2}_{RMS\_CIN}R_{ESR\_CIN}$

where RESR_CIN is the ESR of the input capacitor. This formula has a maximum at PVIN = $2V_{OUT}$, where $I_{RMS} \cong I_{OUT/2}$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes. A 0.1 µF or a 1µF ceramic bypass capacitor is also recommended to be placed right between the PVIN and PGND pins. Please refer to the layout recommendation section.

AVIN FILTER

to AVIN. These can be seen on the schematic as components RF and CF. There is a practical limit to the size of the resistor RF as the AVIN pin will draw a short 60mA burst of current during startup, and if RF is too large the resulting voltage drop can trigger the UVLO comparator. For the demo board a 1Ω resistor is used for RF ensuring that UVLO will not be triggered after the part is enabled. A recommended 1µF CF capacitor coupled with the 1Ω resistor provides roughly 16 dB of attenuation at the 1MHz switching frequency.

SWITCHING FREQUENCY SELECTION

LM21305 supports a wide range of switching frequencies: 300 kHz to 1.5 MHz. The choice of switching frequency is usually a compromise between efficiency and size of the circuit. Lower switching frequency usually means lower switching losses (including gate charge losses, transition IV loss etc.) and would result in a better efficiency most of the time. But higher switching frequency allows using smaller LC filters (more compact design). Smaller L also helps transient response and reduces the conduction loss by smaller DCR. The best switching frequency for efficiency needs to be determined case by case. It is related to the input voltage, the output voltage, the most frequent load level, external component choices, and circuit size requirement. The choice of switching frequency is also limited if an operation condition is possible to trigger Ton-min and Toff-min. The maximum frequency can be used for given input and output voltage can be found by:

$$f_{s\text{-}max} = \frac{V_{OUT}}{V_{PVIN\text{-}max}} \times \frac{1}{T_{ON\text{-}MIN}}$$

The following equation should be used to calculate the resistor R4 value in order to obtain a desired frequency of operation:

$F[kHz] = 31000 * R^{-0.9}[k\Omega]$

INDUCTOR

A general recommendation for the inductor in the LM21305 application is keeping a peak-to-peak ripple current between 20% and 40% of the maximum DC load current (5 A), 30% is desired. It also should have a high enough current rating and DCR as small as possible.

The peak-to-peak current ripple can be calculated by:

$$\Delta i_{Lp\text{-}p} = \frac{(1 - D) \times V_{OUT}}{f_S \times L}$$

The current ripple is larger with smaller inductance and/or lower switching frequency. In general, with a fixed Vout, the higher the PVIN, the higher the inductor current ripple. If PVIN is kept constant, the higher the Vout, the higher the inductor current ripple, as long as , otherwise, ripple will decrease with Vout increase. It is recommended to choose L such that:

$$\frac{(1 - D) \times V_{OUT}}{f_S \times 0.4 \times I_{L(MAX)}} \le L \le \frac{(1 - D) \times V_{OUT}}{f_S \times 0.2 \times I_{L(MAX)}}$$

The inductor should be rated to handle the maximum load current plus the ripple current.

$I_{L(MAX)} = I_{LOAD(MAX)} + \Delta i_{L(MAX)}/2$

An inductor with saturation current higher than the over current protection limit is a safe choice. It is desired to have small inductance in switching power supplies, because it usually means faster transient response, smaller DCR, and smaller size for more compact design. But too small inductance will generate too large inductor current ripple and it could falsely trigger over current protection at the maximum load. It also generates more conduction loss, since the RMS current is higher comparing to smaller ripple with the same DC current. Larger inductor current ripple generates larger output voltage ripple with the same output capacitors as well. With peak current mode control, it is not recommended to have too small inductor current ripple either, so that the peak current comparator has enough signal-to-noise ratio.

OUTPUT CAPACITOR

The device is designed to be used with a wide variety of LC filters. While it is generally desired to use as little output capacitance as possible to keep costs and size down. The output capacitors C_{OUT} should be chosen with care since it directly affects the steady state output voltage ripple, loop stability and the voltage over/undershoot during a load transient. The output voltage ripple is composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance (ESR) of the output capacitors:

$\Delta V_{OUT\text{-}ESR} = \Delta i_{LP\text{-}P} * ESR$

The other is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT-C} = \frac{\Delta i_{Lp-p}}{8 f_S C_{OUT}}$$

Since the two components in the ripple are not in phase, the actual peak-to-peak ripple is smaller than the sum of the two peaks:

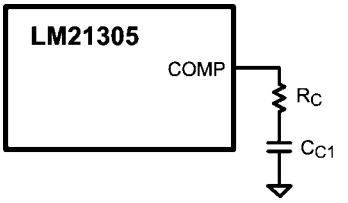
$$\Delta V_{OUT} < \Delta i_{Lp-p} \times \left(\frac{1}{8 f_S C_{OUT}} + ESR \right)$$

Output capacitance is usually limited by transient performance if the system requires tight voltage regulation with presence of large current steps and fast slew rate. To maintain a small over- or undershoot during transient, small ESR and large capacitance are desired. But these also come with higher cost and size. The control loop should also be fast to reduce the voltage droop.

One or more ceramic capacitors are recommended because they have very low ESR and remain capacitive up to high frequencies. The dielectric should be X5R, X7R, or comparable material to maintain proper tolerances. Other types of capacitors also can be used if large capacitance is needed, such as tantalum, poscap and OSCON. Such capacitors have lower $1/(2\pi ESR * C)$ frequency than ceramic capacitors. The lower RC frequency could affect the control loop if it is close to the crossover frequency. If high switching frequency and high crossover frequency are desired, all ceramic design is more appropriate.

COMPENSATION CIRCUIT

achieve high performance in terms of the transient response, audio susceptibility and output impedance. The LM21305 will typically require only a single resistor Rc and capacitor Cc1 for compensation, but depending on the power stage it could require a second capacitor for a high frequency pole.



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Compensation Network for LM21305

To select the compensation components, a desired cross over frequency fc should be selected first. It is recommended fc is equal to or lower than fs/8. A simplified procedure is given below for Rc and Cc1, assuming the capacitor ESR zero is at least 3 times higher than fc. The compensation resistor can be found by:

$$R_c \approx \frac{1}{Gain_0} \times \frac{f_c}{f_p} = \frac{V_{OUT}}{V_{FB}} \times 197 \times fc \times C_{OUT}$$

Cc1 does not affect the crossover frequency fc, but it sets the compensator zero fzcomp and affects the phase margin of the loop. For a fast design, Cc1 = 10 nF gives adequate performance in most LM21305 applications. Larger Cc1 gives larger phase margin, while lower Cc1 gives higher gain at lower frequency thus faster transient respond. It is recommended to set the compensation zero no higher than fc/3 to ensure enough phase margin, meaning:

$$C_{c1} \geq \frac{3}{2\pi R_c f_c}$$

For more details, please refer to the LM21305 datasheet.

PCB Layout

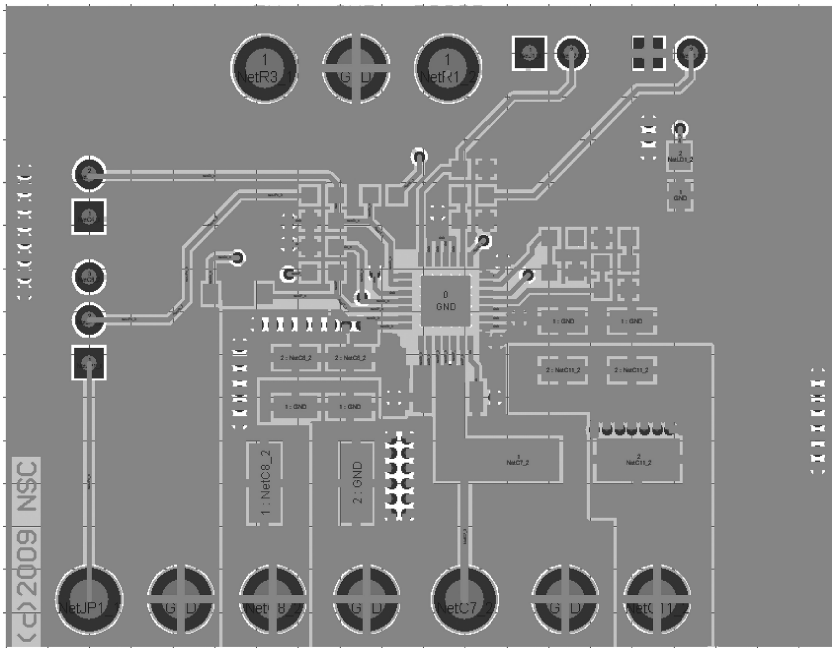

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FIGURE 1. Top Layer

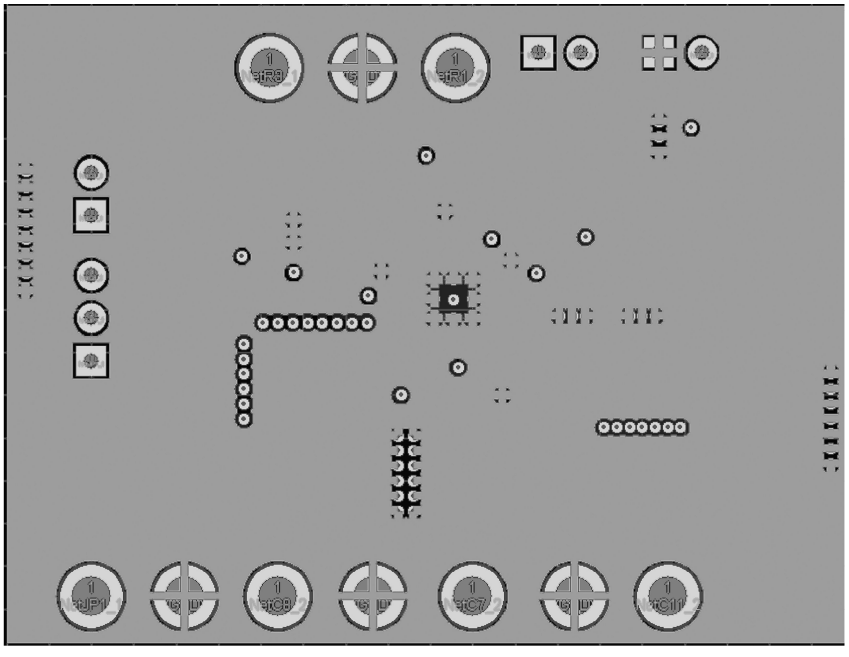

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FIGURE 2. Middle Layer 1

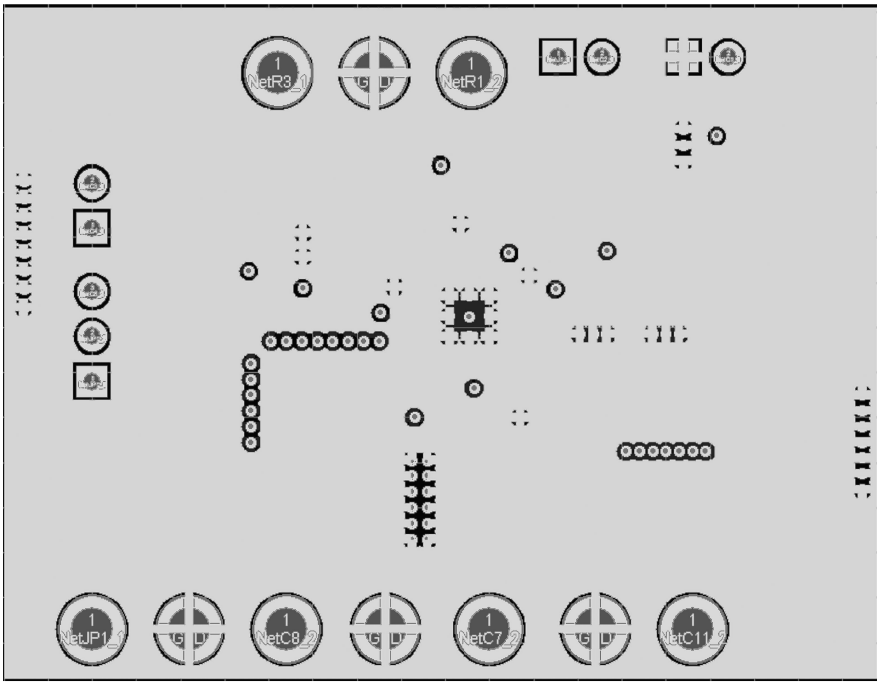

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FIGURE 3. Middle Layer 2

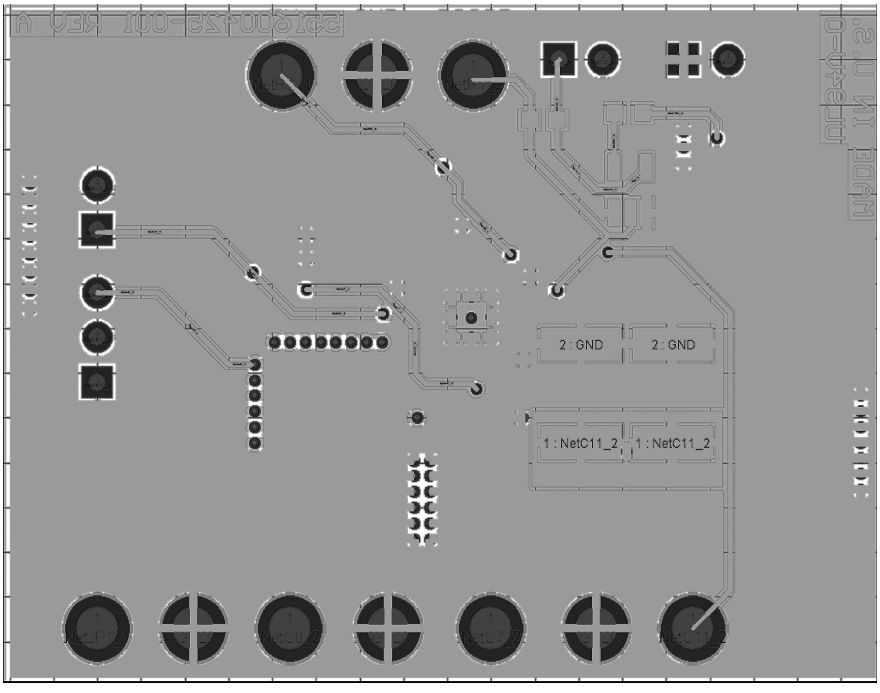

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FIGURE 4. Bottom Layer

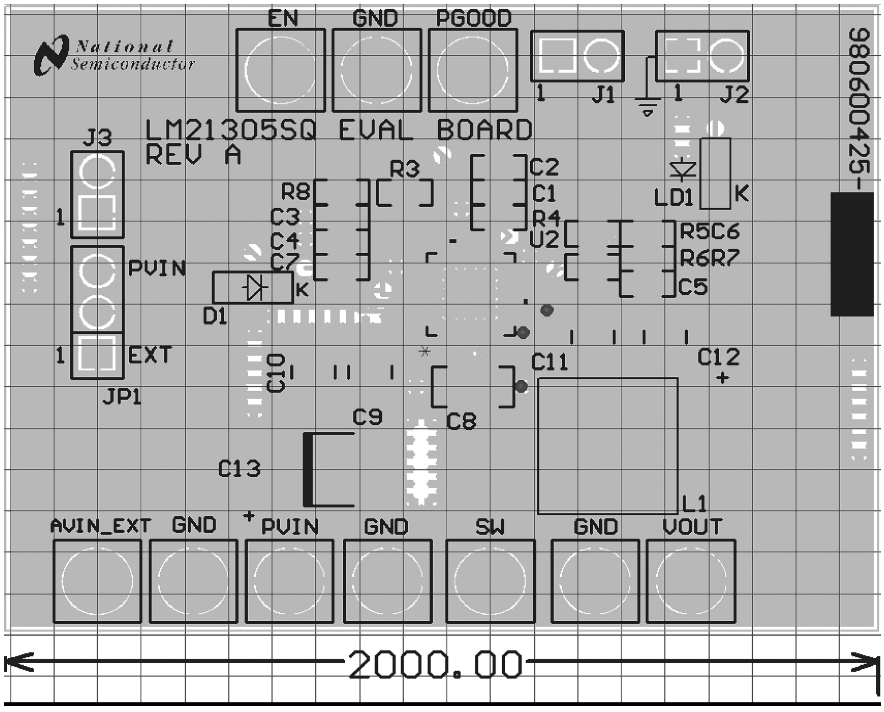

FIGURE 5. Top Overlay

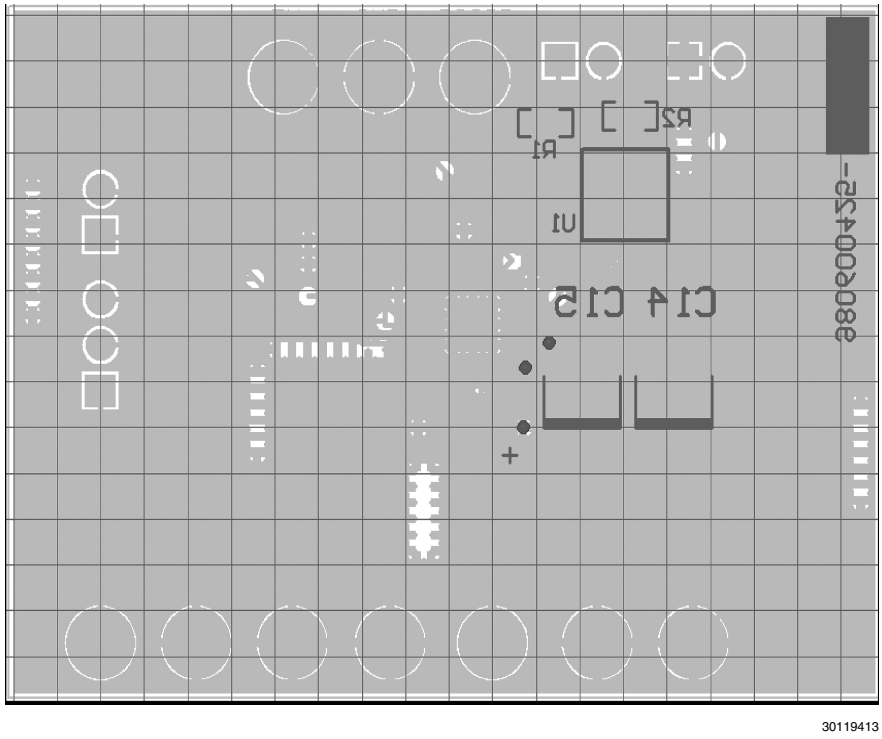

FIGURE 6. Bottom Overlay

Notes

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