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FDD5680

FDD5680

N-Channel, PowerTrench™ MOSFET

General Description

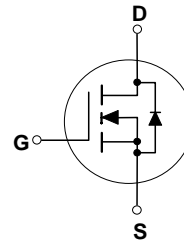
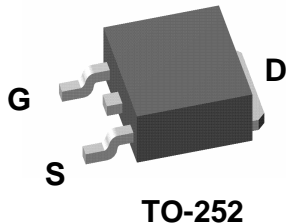
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

Applications

- DC/DC converter
- Motor drives

Features

- 38 A, 60 V. $R_{DS(on)} = 0.021 \Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(on)} = 0.025 \Omega @ V_{GS} = 6 \text{ V}$.
- Low gate charge (33nC typical).
- Fast switching speed.
- High performance trench technology for extremely low $R_{DS(on)}$.



Absolute Maximum Ratings T_A=25°C unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|-----------------------------------|--|-------------|-------|
| V _{DSS} | Drain-Source Voltage | 60 | V |
| V _{GSS} | Gate-Source Voltage | ±20 | V |
| I _D | Maximum Drain Current - Continuous <small>(Note 1)</small> <small>(Note 1a)</small> | 38 | A |
| | Maximum Drain Current - Pulsed | 8.5 | |
| P _D | Maximum Power Dissipation @ T _C = 25°C <small>(Note 1)</small> | 60 | W |
| | T _A = 25°C <small>(Note 1a)</small> | 2.8 | |
| | T _A = 25°C <small>(Note 1b)</small> | 1.3 | |
| T _J , T _{stg} | Operating and Storage Junction Temperature Range | -55 to +150 | °C |

Thermal Characteristics

| | | | |
|------------------|---|-----|------|
| R _{θJC} | Thermal Resistance, Junction-to- Case <small>(Note 1)</small> | 2.1 | °C/W |
| R _{θJA} | Thermal Resistance, Junction-to- Ambient <small>(Note 1b)</small> | 96 | °C/W |

Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|----------------|---------|-----------|------------|----------|
| FDD5680 | FDD5680 | 13" | 16mm | 2500 |

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
|--------|-----------|-----------------|-----|-----|-----|-------|

Off Characteristics

| | | | | | | |
|--------------------------------------|--|---|----|----|------|----------------------------|
| W_{DSS} | Single Pulse Drain-Source Avalanche Energy | $V_{DD} = 30\text{ V}, I_D = 38\text{ A}$ | | | 140 | mJ |
| I_{AR} | Maximum Drain-Source Avalanche Current | | | | 38 | A |
| BV_{DSS} | Drain-Source Breakdown Voltage | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ | 60 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\ \mu\text{A}$, Referenced to 25°C | | 60 | | $\text{mV}/^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$ | | | 1 | μA |
| I_{GSSF} | Gate-Body Leakage Current, Forward | $V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$ | | | 100 | nA |
| I_{GSSR} | Gate-Body Leakage Current, Reverse | $V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$ | | | -100 | nA |

On Characteristics (Note 2)

| | | | | | | |
|--|--|--|----|-------------------------|-------------------------|----------------------------|
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ | 2 | 2.4 | 4 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D = 250\ \mu\text{A}$, Referenced to 25°C | | -6.4 | | $\text{mV}/^\circ\text{C}$ |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS} = 10\text{ V}, I_D = 8.5\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 8.5\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 6\text{ V}, I_D = 7.5\text{ A}$ | | 0.017 0.028 0.019 | 0.021 0.042 0.025 | Ω |
| $I_{D(on)}$ | On-State Drain Current | $V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$ | 50 | | | A |
| g_{FS} | Forward Transconductance | $V_{DS} = 5\text{ V}, I_D = 8.5\text{ A}$ | | 30 | | S |

Dynamic Characteristics

| | | | | | | |
|-----------|------------------------------|--|--|------|--|----|
| C_{iss} | Input Capacitance | $V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$ | | 1835 | | pF |
| C_{oss} | Output Capacitance | | | 210 | | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 90 | | pF |

Switching Characteristics (Note 2)

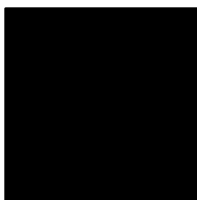
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|--------------|---------------------|--|--|-----|----|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 30\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$ | | 15 | 27 | ns |
| t_r | Turn-On Rise Time | | | 9 | 18 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 35 | 56 | ns |
| t_f | Turn-Off Fall Time | | | 16 | 26 | ns |
| Q_g | Total Gate Charge | $V_{DS} = 30\text{ V}, I_D = 8.5\text{ A},$ $V_{GS} = 10\text{ V},$ | | 33 | 46 | nC |
| Q_{gs} | Gate-Source Charge | | | 6.5 | | nC |
| Q_{gd} | Gate-Drain Charge | | | 7.5 | | nC |

Drain-Source Diode Characteristics and Maximum Ratings

| | | | | | | |
|----------|---|--|--|------|-----|---|
| I_S | Maximum Continuous Drain-Source Diode Forward Current | | | 2.3 | | A |
| V_{SD} | Drain-Source Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = 2.3\text{ A}$ (Note 2) | | 0.75 | 1.2 | V |

NOTES:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the drain tab. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



- a) $R_{\theta JA} = 45^\circ\text{C}/\text{W}$ when mounted on a 1in^2 pad of 2oz copper.

- b) $R_{\theta JA} = 96^\circ\text{C}/\text{W}$ when mounted on a 0.076in^2 pad of 2oz copper.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

Typical Characteristics

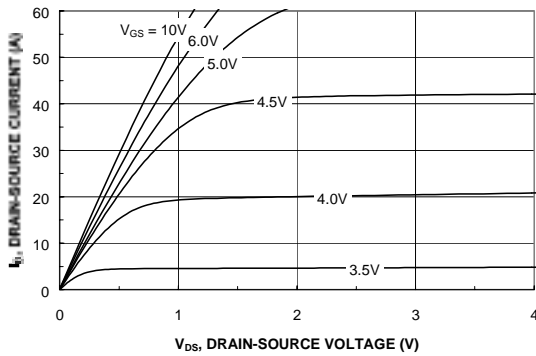


Figure 1. On-Region Characteristics.

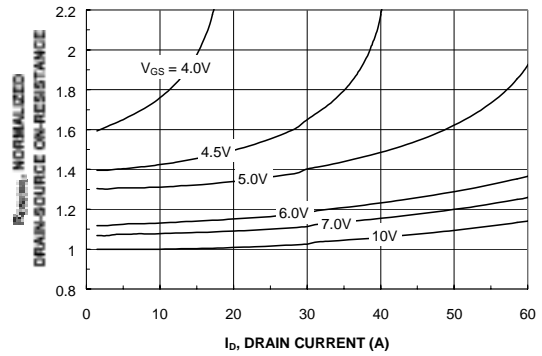


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

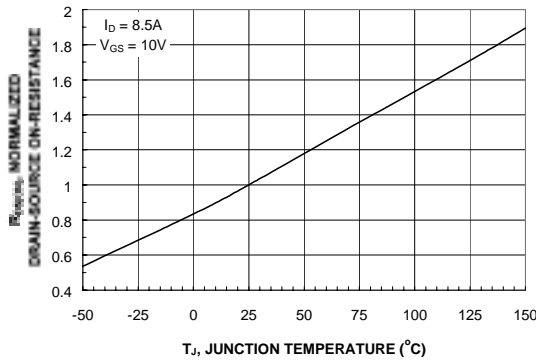


Figure 3. On-Resistance Variation with Temperature.

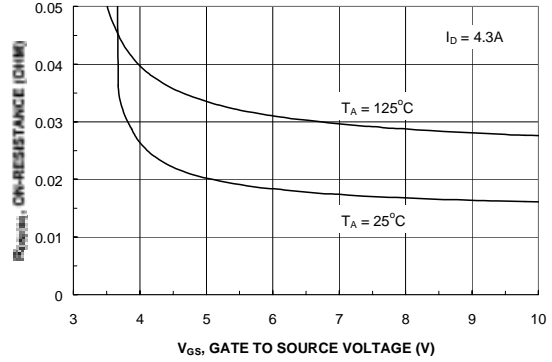


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

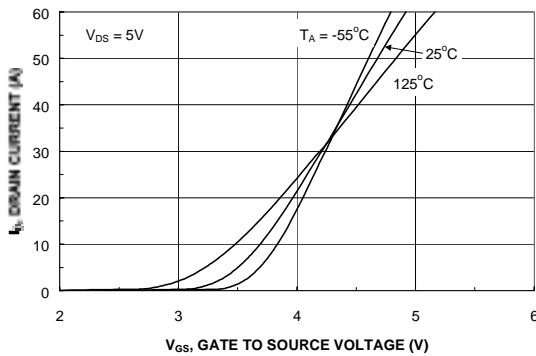


Figure 5. Transfer Characteristics.

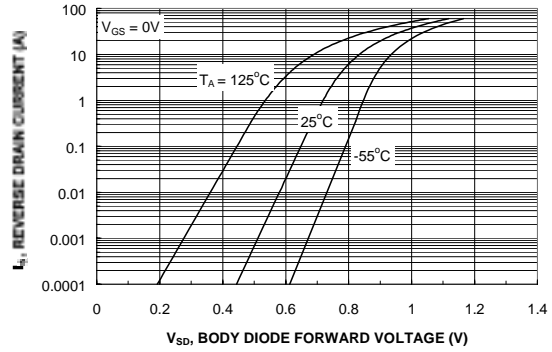


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

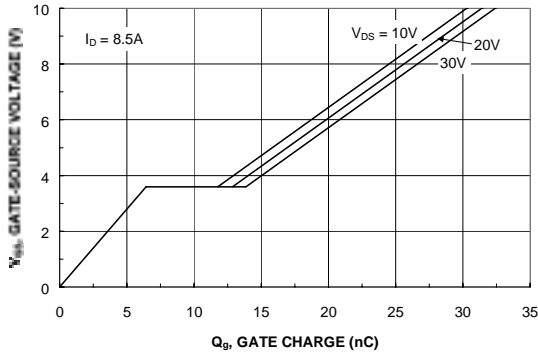


Figure 7. Gate-Charge Characteristics.

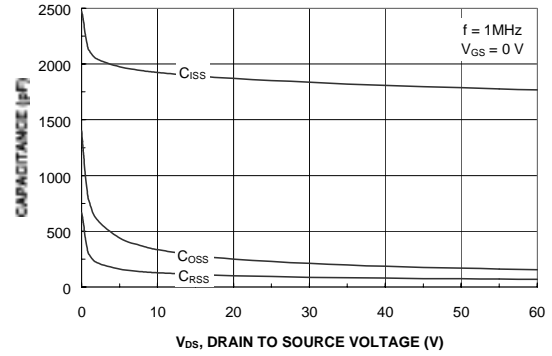


Figure 8. Capacitance Characteristics.

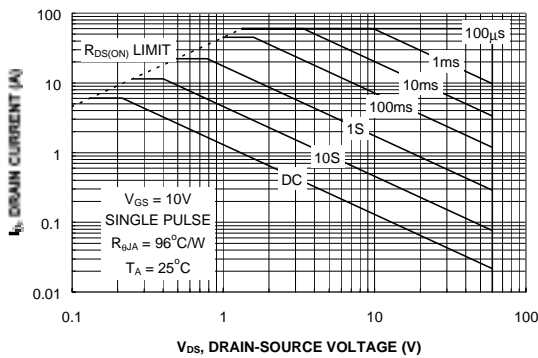


Figure 9. Maximum Safe Operating Area.

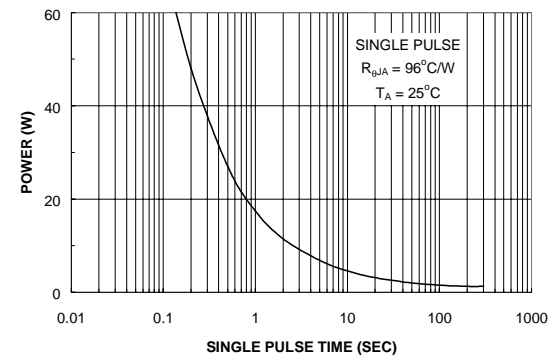


Figure 10. Single Pulse Maximum Power Dissipation.

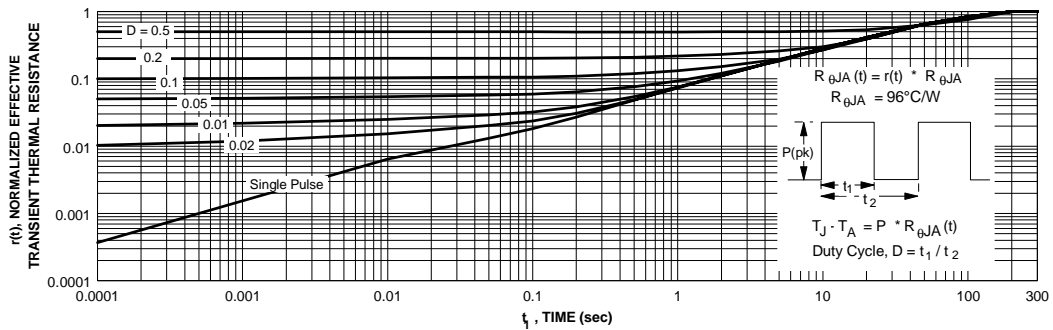
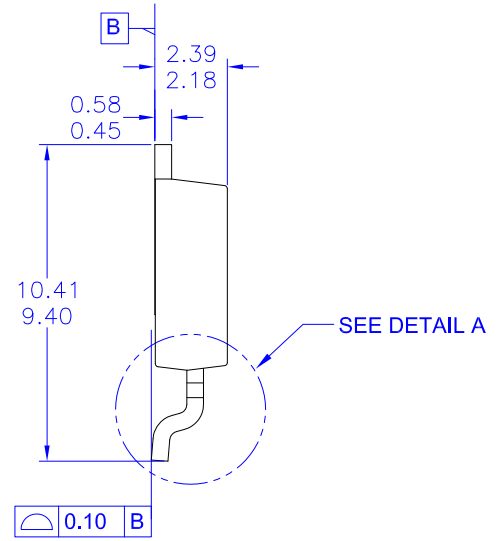
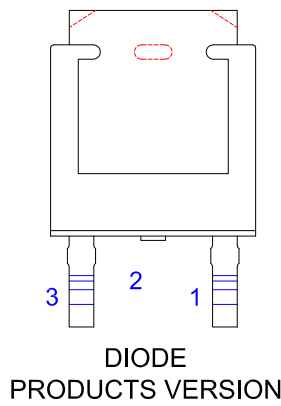
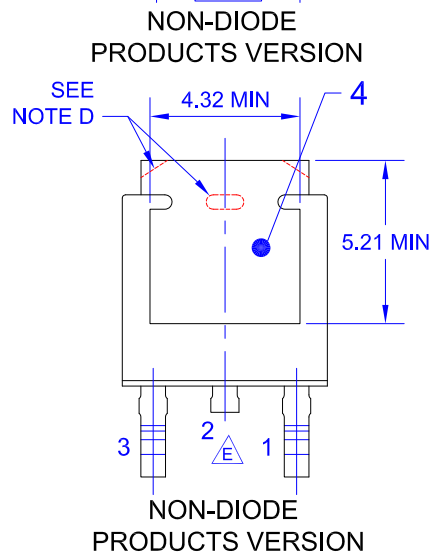
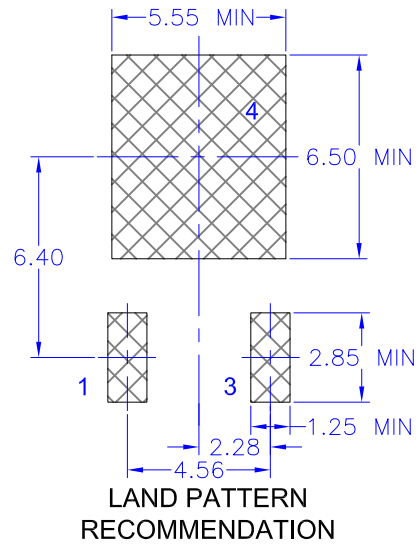
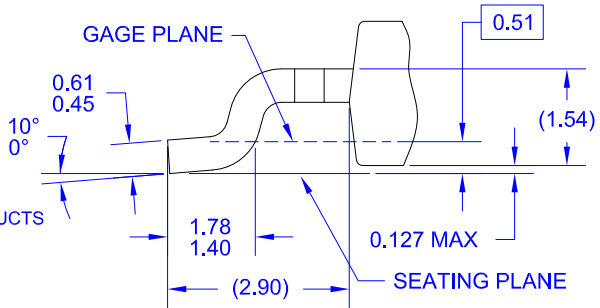


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.



- NOTES: UNLESS OTHERWISE SPECIFIED
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 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
 - D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
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 - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
 - H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



DETAIL A
(ROTATED -90°)
SCALE: 12X



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