SN74LVC1G139 2-to-4 Line Decoder

1 Features

- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Supports Down Translation to V_{CC}
- Maximum t_{pd} of 4.9 ns at 3.3 V and 15 pF
- Low Power Consumption, 10-µA Maximum I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- AV Receivers
- Solid State Drives (SSDs): Client and Enterprise
- TVs: LCD, Digital, and High-Definition (HD)
- Tablets: Enterprise
- Video Analytics: Server

3 Description

This SN74LVC1G139 2-to-4 line decoder is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G139 2-line to 4-line decoder is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When used with high-speed memories using a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

NanoStar and NanoFree package technology is a major breakthrough in device packaging concepts, using the die as the package.

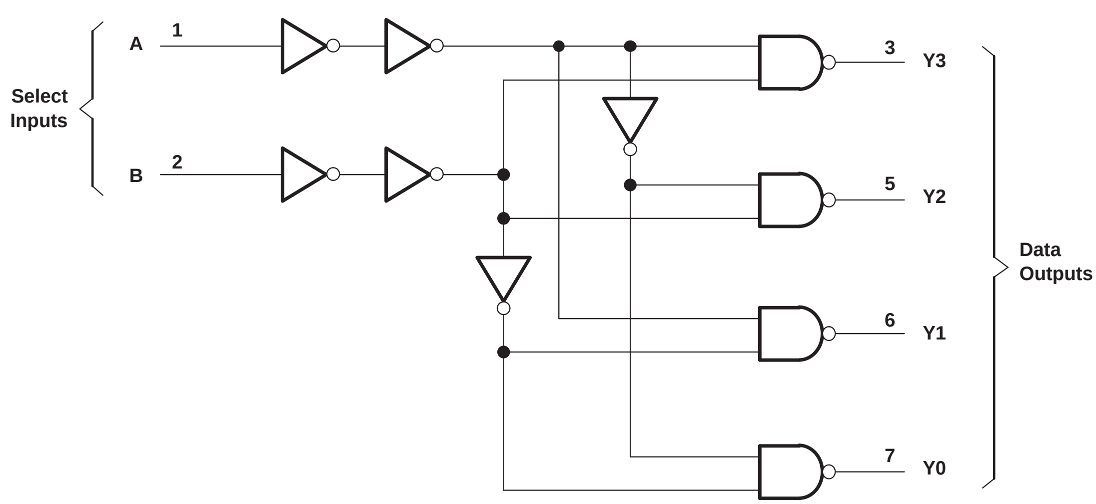
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1G139DCT	SM8 (8)	2.95 mm × 2.80 mm
SN74LVC1G139DCU	VSSOP (8)	2.30 mm × 2.00 mm
SN74LVC1G139YZP	DSBGA (8)	1.91 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (February 2014) to Revision E — **Page**

- Updated the YZP package drawing ... 3

Changes from Revision C (December 2005) to Revision D — **Page**

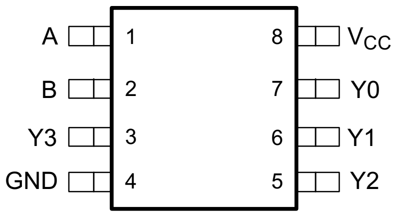
- Added *Applications* section, *Device Information* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics* section, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision B (December 2005) to Revision C — **Page**

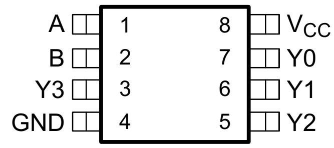
- Updated document to new TI data sheet format. ... 1
- Updated *Features*. ... 1
- Removed *Ordering Information* table. ... 1

5 Pin Configuration and Functions

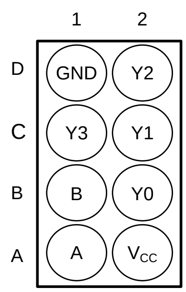
DCT Package
8-Pin SM8
Top View



DCU Package
8-Pin VSSOP
Top View



YZP Package
8-Pin DSBGA
Bottom View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	DCT, DCU	YZP		
A	1	A1	I	Adress input, bit 0
B	2	B1	I	Adress input, bit 1
Y_3	3	C1	O	Output 3, low when B is high and A is high
GND	4	D1	—	Ground
Y_2	5	D2	O	Output 2, low when B is high and A is low
Y_1	6	C2	O	Output 1, low when B is low and A is high
Y_0	7	B2	O	Output 0, low when B is low and A is low
V_{CC}	8	A2	—	Power pin

6 Specification

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage, V_{CC}		–0.5	6.5	V
Input Voltage, V_I		–0.5	6.5	V
Voltage applied to any output in the high-impedance or power-off state, V_O (2)		–0.5	6.5	V
Voltage applied to any output in the high or low state, V_O (2)(3)		–0.5	V_{CC} + 0.5	V
Input clamp current, I_{IK}	$V_I < 0$		–50	mA
Output clamp current, I_{OK}	$V_O < 0$		–50	mA
Continuous output current, I_O			±50	mA
Continuous current through V_{CC} or GND, I_{CC}			±100	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		15	
		V_{CC} = 5 V ± 0.5 V		10	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report.

6.4 Thermal Information

THERMAL METRIC[1]		SN74LVC1G139			UNIT
		DCT (SM8)	DCU (VSSOP)	YZP (DSBGA)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	194	195	106	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	124	74	1.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	106	74	11	°C/W
ψ_{JT}	Junction-to-top characterization parameter	48	6.7	3.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	105	73	11	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –100 µA, V_{CC} = 1.65 V to 5.5 V	V_{CC} – 0.1			V
		I_{OH} = –4 mA, V_{CC}= 1.65 V	1.2			
		I_{OH} = –8 mA, V_{CC} = 2.3 V	1.9			
		I_{OH} = –16 mA, V_{CC} = 3 V	2.4			
		I_{OH} = –24 mA, V_{CC} = 3 V	2.3			
		I_{OH} = –32 mA, V_{CC} = 4.5 V	3.8			
V_{OL}	Low-level output voltage	I_{OL} = 100 µA, V_{CC} = 1.65 V to 5.5 V			0.1	V
		I_{OL} = 4 mA, V_{CC} = 1.65 V			0.45	
		I_{OL} = 8 mA, V_{CC} = 2.3 V			0.3	
		I_{OL} = 16 mA, V_{CC} = 3 V			0.4	
		I_{OL} = 24 mA, V_{CC} = 3 V			0.55	
		I_{OL} = 32 mA, V_{CC} = 4.5 V			0.55	
I_I	Inflection-point current	A or B inputs: V_I = 5.5 V or GND, V_{CC} = 0 to 5.5 V			±1	µA
I_{off}	Off-state current	V_I or V_O = 5.5 V, V_{CC} = 0			±5	µA
I_{CC}	Supply current	V_I = 5.5 V or GND, I_O = 0, V_{CC} = 1.65 V to 5.5 V			10	µA
ΔI_{CC}	Supply current change	One input at V_{CC} – 0.6 V, other inputs at V_{CC} or GND, V_{CC} = 3 V to 5.5 V			500	µA
C_i	Input capacitance	V_I = V_{CC} or GND, V_{CC} = 3.3 V		4		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
t_{pd}	Propagation delay time	A or B-to-Y	See Table 2	V_{CC} = 1.8 V ± 0.15 V	2.7	15.3	ns
				V_{CC} = 2.5 V ± 0.2 V	1.5	7.5	
				V_{CC} = 3.3 V ± 0.3 V	0.9	4.9	
				V_{CC} = 5 V ± 0.5 V	0.8	3.6	
			See Table 3	V_{CC} = 1.8 V ± 0.15 V	3	16.7	
				V_{CC} = 2.5 V ± 0.2 V	1.6	8.2	
				V_{CC} = 3.3 V ± 0.3 V	1.2	5.9	
				V_{CC} = 5 V ± 0.5 V	1.1	4.2	

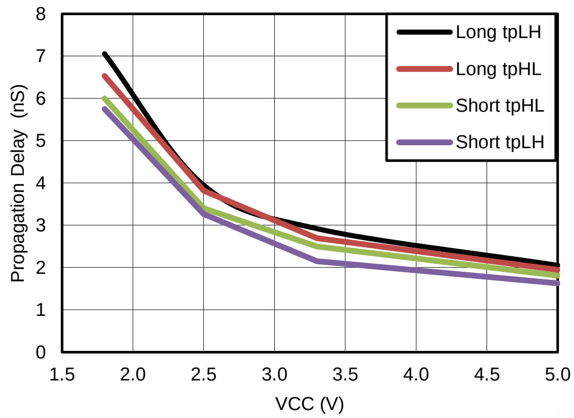
6.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pd}(1)	Power dissipation capacitance	f = 10 MHz	V_{CC} = 1.8 V		31		pF
			V_{CC} = 2.5 V		34		
			V_{CC} = 3.3 V		36		
			V_{CC} = 5 V		39		

(1) Two outputs switching.

7 Typical Characteristics



(1) Short is 2 inverter path. Long is 3 inverter path.

Figure 1. Propagation Delay vs VCC

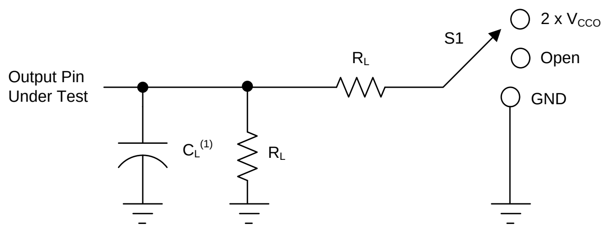
8 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators that have the following characteristics:

- PRR ≤ 10 MHz
- Z_O = 50 Ω

NOTE

All parameters and waveforms are not applicable to all devices.



(1) C_L includes probe and jig capacitance.

Figure 2. Load Circuit

Table 1. Loading Conditions for Parameter

TEST	S1
t_{PLH}(1), t_{PHL}(1)	Open
t_{PLZ}(2), t_{PZL}(3)	V_{LOAD}
t_{PHZ}(2), t_{PZH}(3)	GND

(1) t_{PLH} and t_{PHL} are the same as t_{pd}.
(2) t_{PLZ} and t_{PHZ} are the same as t_{dis}.
(3) t_{PZL} and t_{PZH} are the same as t_{en}.

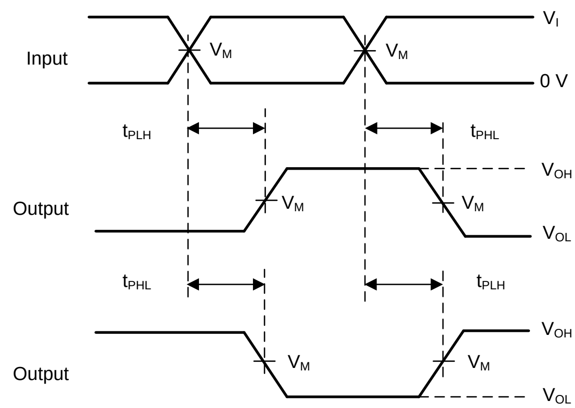
Table 2. Loading Conditions for V_{CC} – Case 1

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤ 2 ns	V_{CC} / 2	2 × V_{CC}	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤ 2 ns	V_{CC} / 2	2 × V_{CC}	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ± 0.5 V	V_{CC}	≤ 2.5 ns	V_{CC} / 2	2 × V_{CC}	15 pF	1 MΩ	0.3 V

Table 3. Loading Conditions for V_{CC} – Case 2

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤ 2 ns	V_{CC} / 2	2 × V_{CC}	30 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤ 2 ns	V_{CC} / 2	2 × V_{CC}	30 pF	500 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	30 pF	500 MΩ	0.3 V
5 V ± 0.5 V	V_{CC}	≤ 2.5 ns	V_{CC} / 2	2 × V_{CC}	30 pF	500 MΩ	0.3 V

Figure 3. Voltage Waveforms: Pulse Duration



(1) The outputs are measured one at a time, with one transition per measurement.

Figure 4. Voltage Waveforms: Propagation Delay Times Inverting And Noninverting Outputs

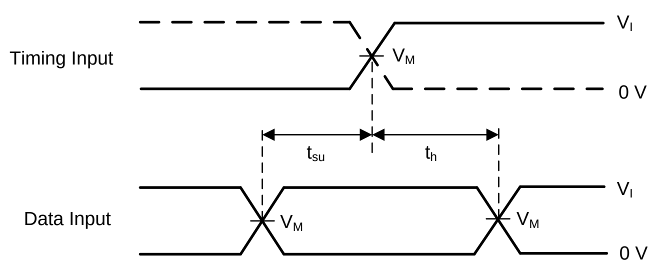
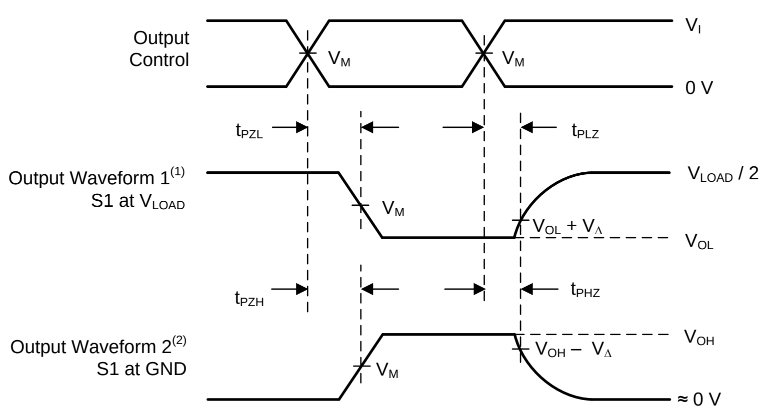


Figure 5. Voltage Waveforms: Setup and Hold Times



(1) Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.

(2) Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

(3) The outputs are measured one at a time, with one transition per measurement.

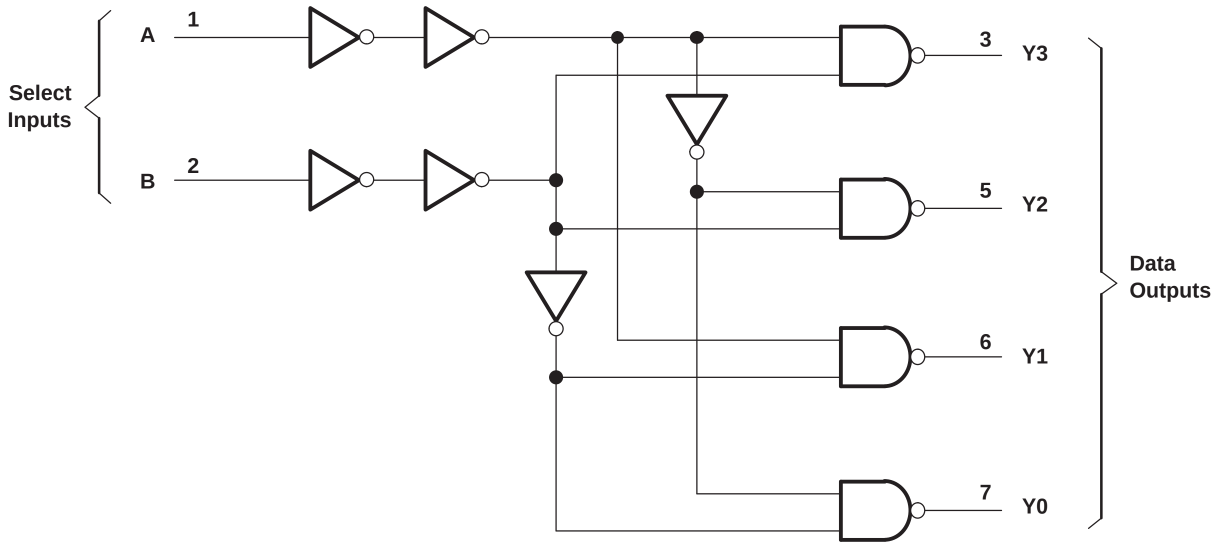
Figure 6. Voltage Waveforms: Enable and Disable Times, Low- and High-Level Enabling

9 Detailed Description

9.1 Overview

The LVC1G139 device decodes the 2-bit input to one of the four outputs. The B input is the most significant bit and the Y outputs are active low. The propagation delays are very short and well matched (see Figure 1). Supply voltage from 1.65-V to 5.5-V is supported.

9.2 Functional Block Diagram



9.3 Feature Description

NanoStar and NanoFree package technology is a major breakthrough in device packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

9.4 Device Functional Modes

Table 4 lists the functional modes of the SN74LVC1G139 device.

Table 4. Function Table

INPUTS		OUTPUTS			
B	A	Y_0	Y_1	Y_2	Y_3
L	L	L	H	H	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	L

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74LVC1G139 device is a 2-of-4 decoder and demultiplexer. This device decodes the 2-bit address on inputs A (bit 0) and B (bit 1) then provides a logic low on the matching address output. It can produce 24 mA of drive current at 3.3 V, making it ideal for driving multiple outputs.

10.2 Typical Application

This is an address line decoder using a 16-bit bus example; address bus lines 14 and 15 are decoded and drive four active low chip selects. Each output covers 16K address space mapped by the address bus lines 0 through 13.

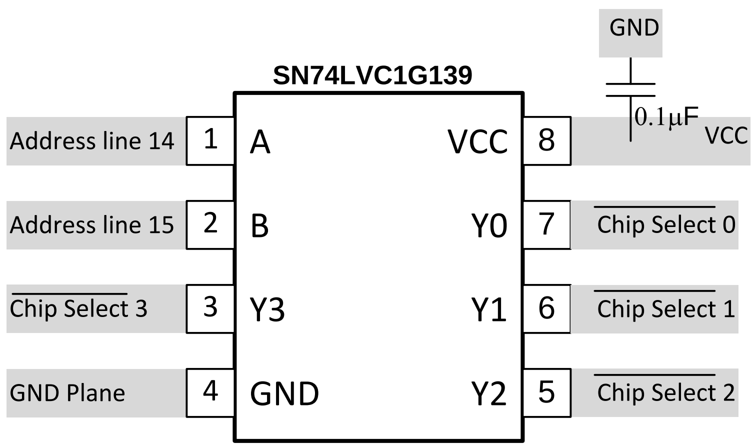


Figure 7. Typical Application Diagram

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   – Rise time and fall time specifications ($\Delta t/\Delta V$) are shown in the *Recommended Operating Conditions* table.
   – Specified high (V_{IH}) and low voltage (V_{IL}) levels are shown in the *Recommended Operating Conditions* table.
   – Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommend Output Conditions:
   – Load currents should not exceed 50 mA per output and 100 mA total for the part.
   – Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

Typical Application (continued)

10.2.3 Application Curve

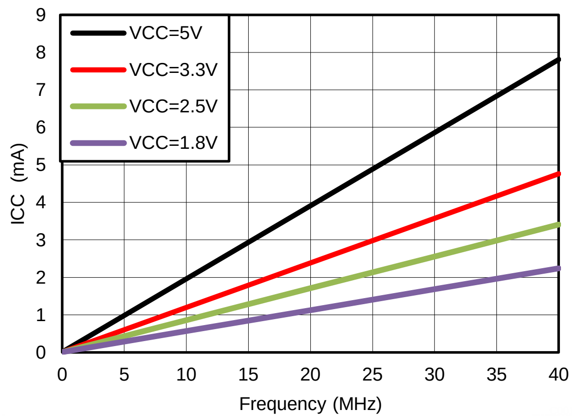


Figure 8. I_{CC} vs Frequency
Load is 15 pF

11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended. If there are multiple V_{CC} terminals, then 0.01-µF or 0.022-µF capacitors are recommended for each power terminal. Parallel multiple bypass capacitors are allowed to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 9 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient.

12.2 Layout Example

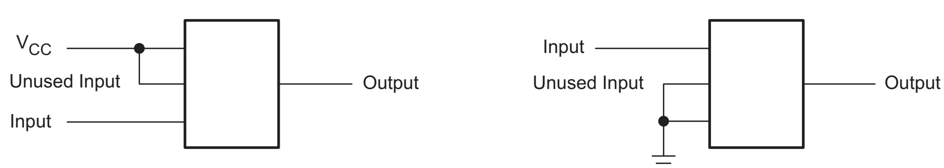


Figure 9. Layout Diagram

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

NanoStar, NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVC1G139DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C39 (R, Z)	Samples
74LVC1G139DCTTE4	ACTIVE	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C39 (R, Z)	Samples
74LVC1G139DCUTG4	ACTIVE	VSSOP	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C39R	Samples
SN74LVC1G139DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C39 (R, Z)	Samples
SN74LVC1G139DCTT	ACTIVE	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C39 (R, Z)	Samples
SN74LVC1G139DCUR	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	(C39Q, C39R)	Samples
SN74LVC1G139DCUT	ACTIVE	VSSOP	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	(C39Q, C39R)	Samples
SN74LVC1G139YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DFN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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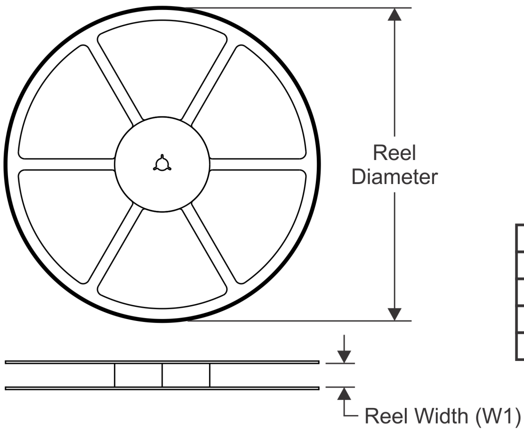
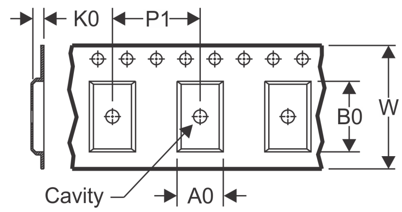
TAPE AND REEL INFORMATION

REEL DIMENSIONS

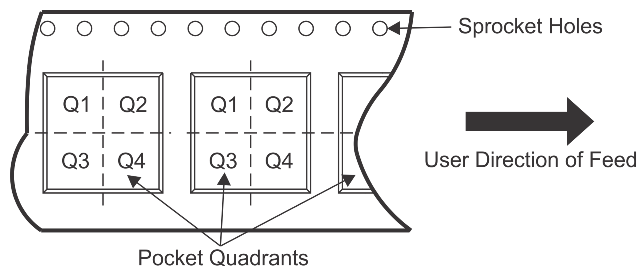


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

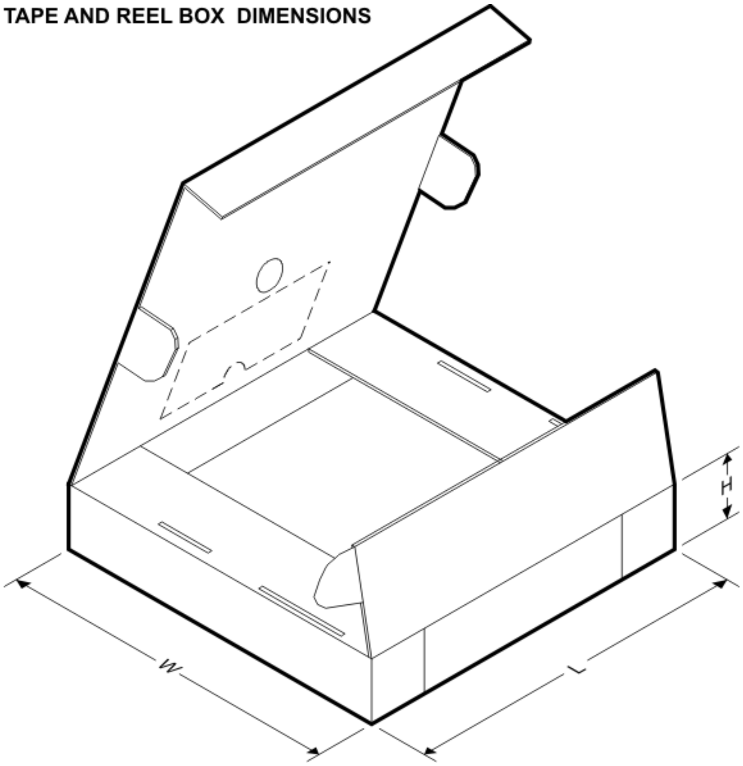
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1G139DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G139DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC1G139DCTT	SM8	DCT	8	250	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC1G139DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G139DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G139DCUT	VSSOP	DCU	8	250	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G139YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

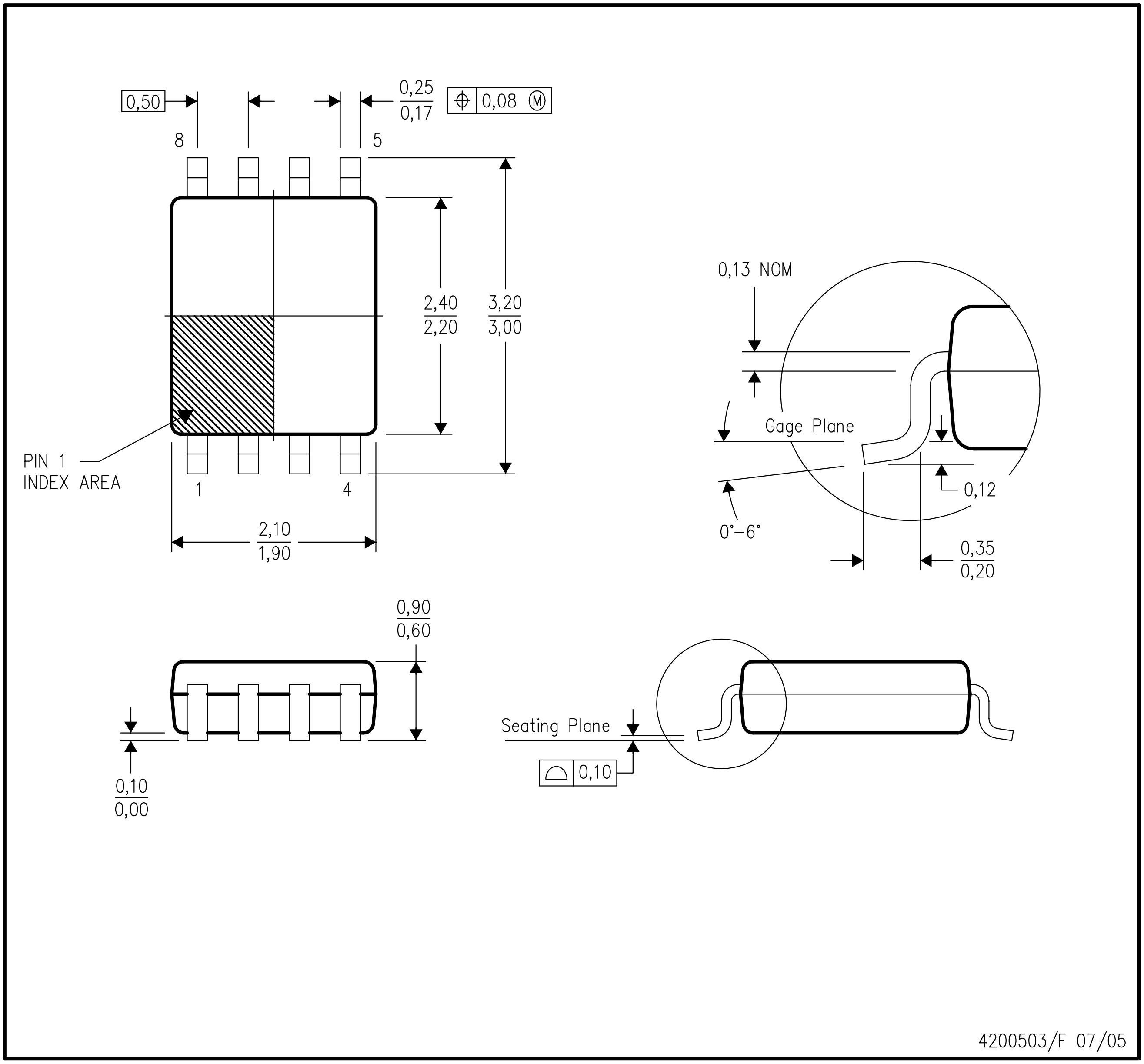
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

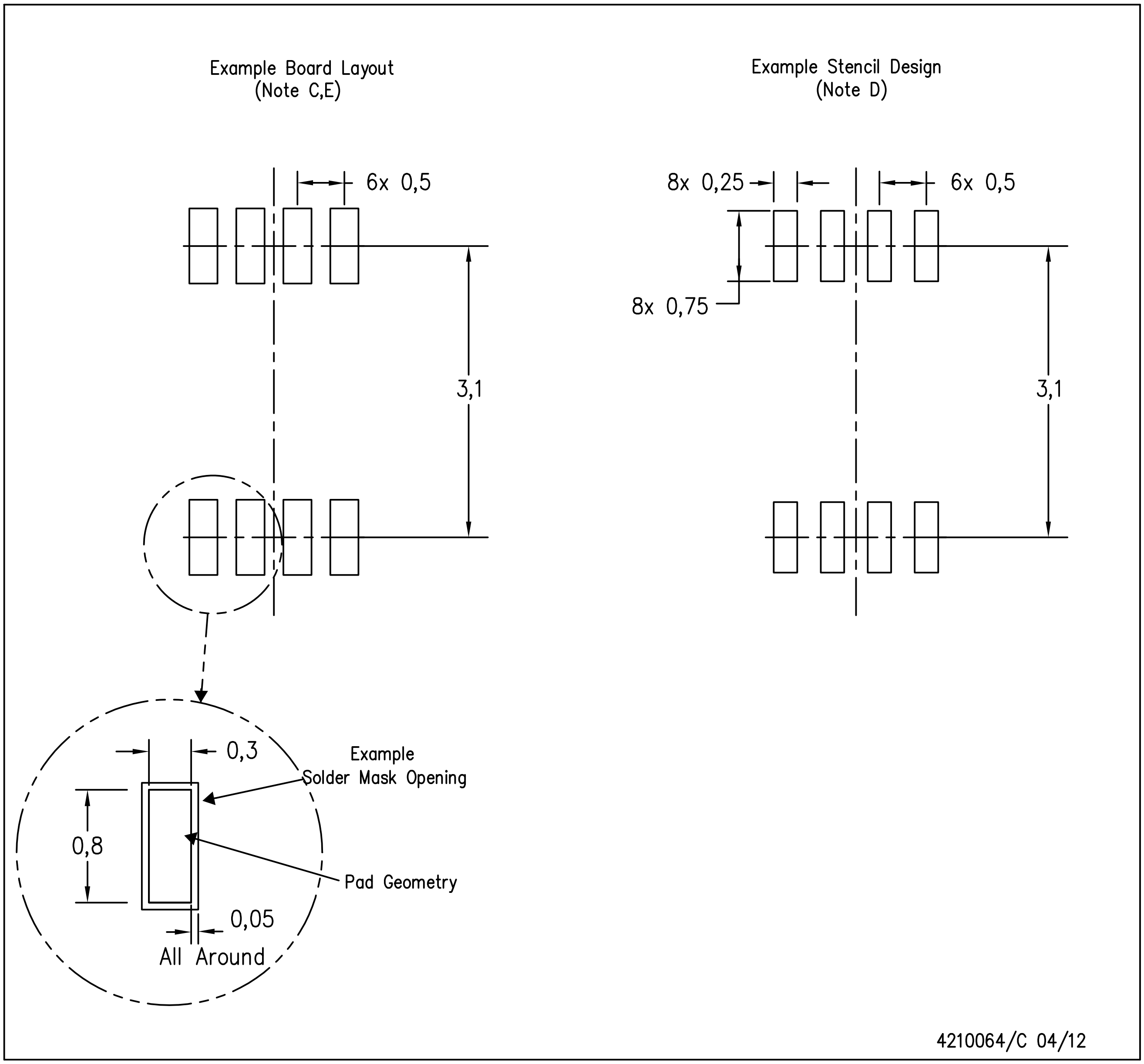
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC1G139DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC1G139DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC1G139DCTT	SM8	DCT	8	250	182.0	182.0	20.0
SN74LVC1G139DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC1G139DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC1G139DCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC1G139YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

DCU (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



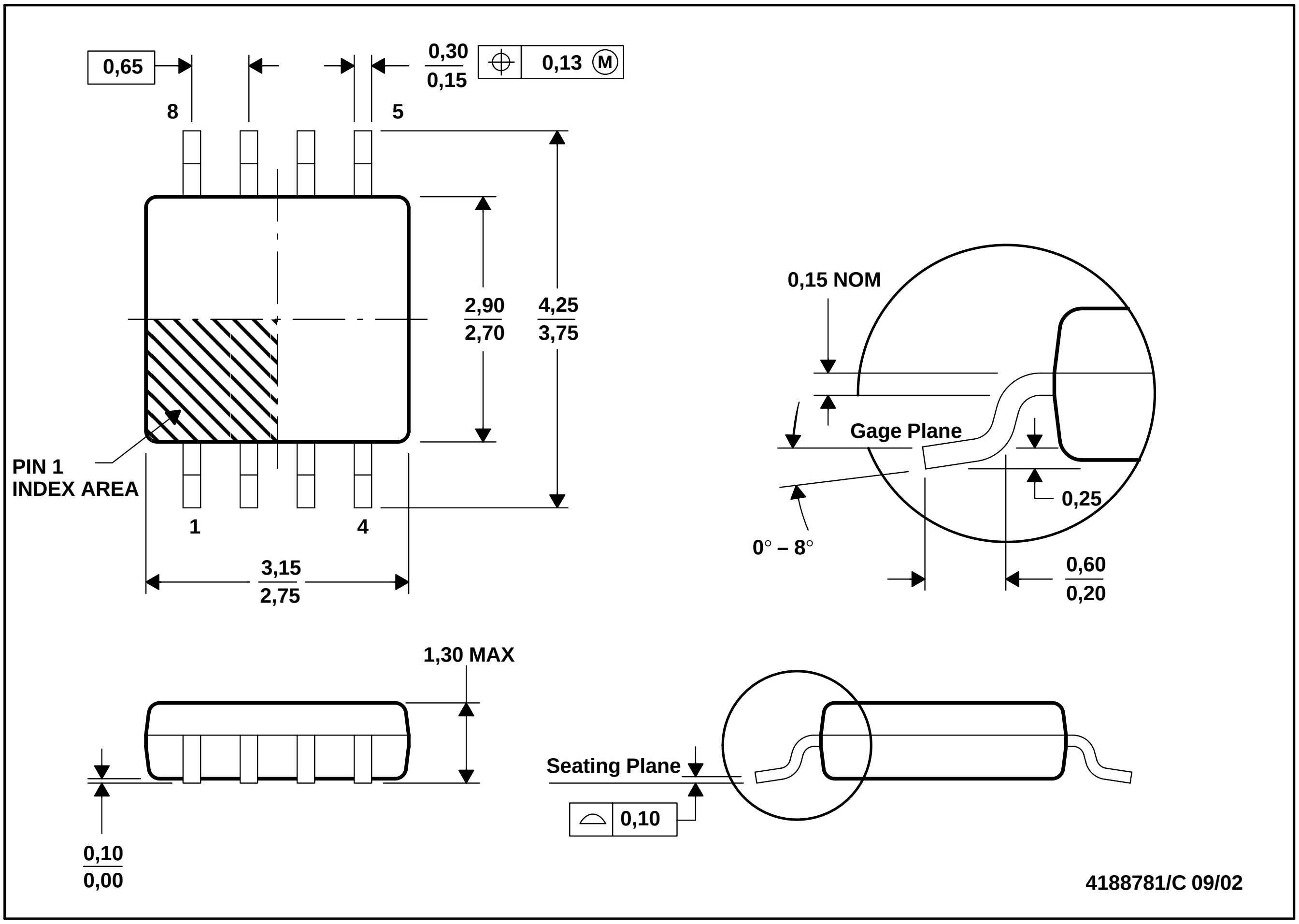
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



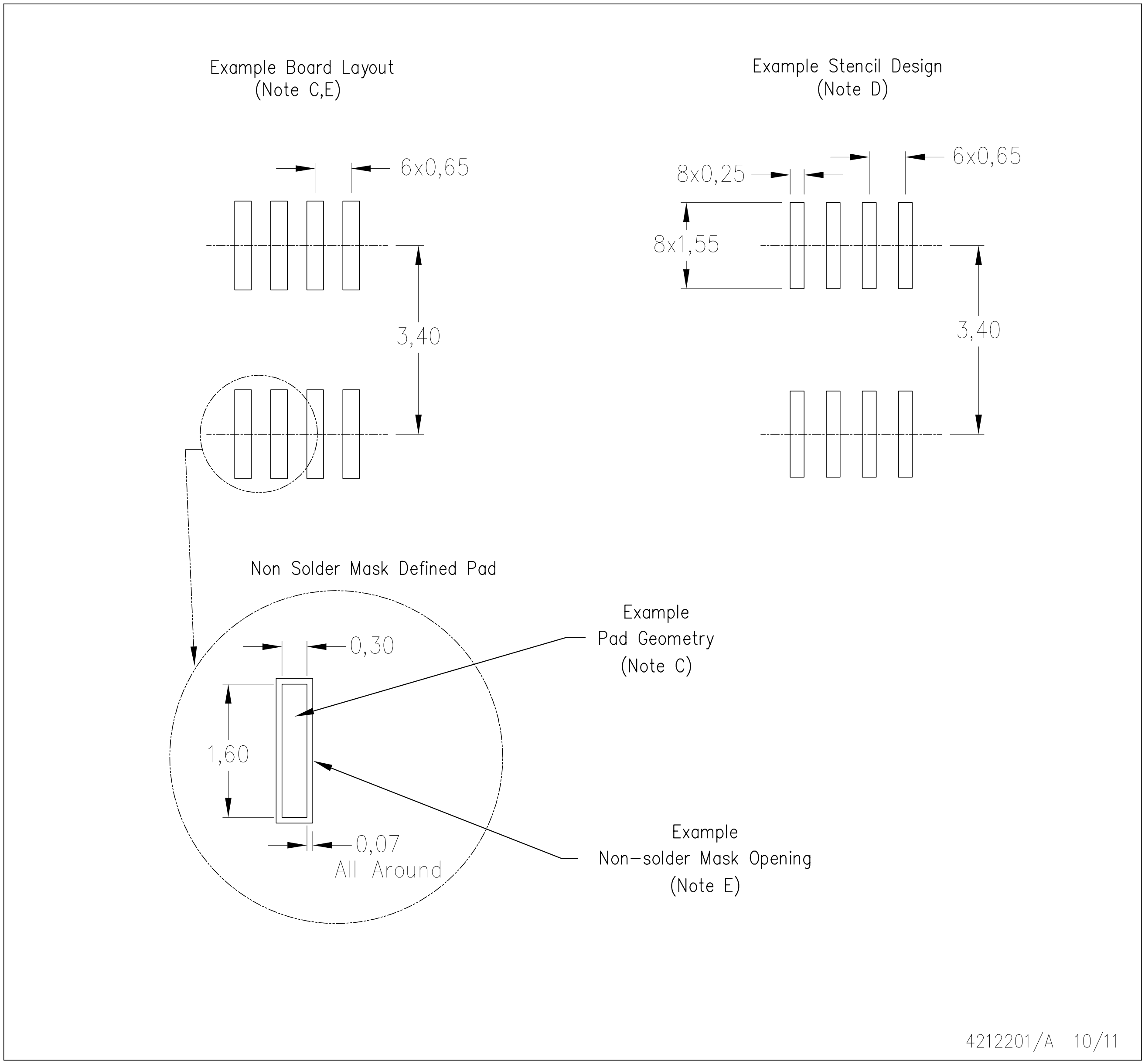
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DCT (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**

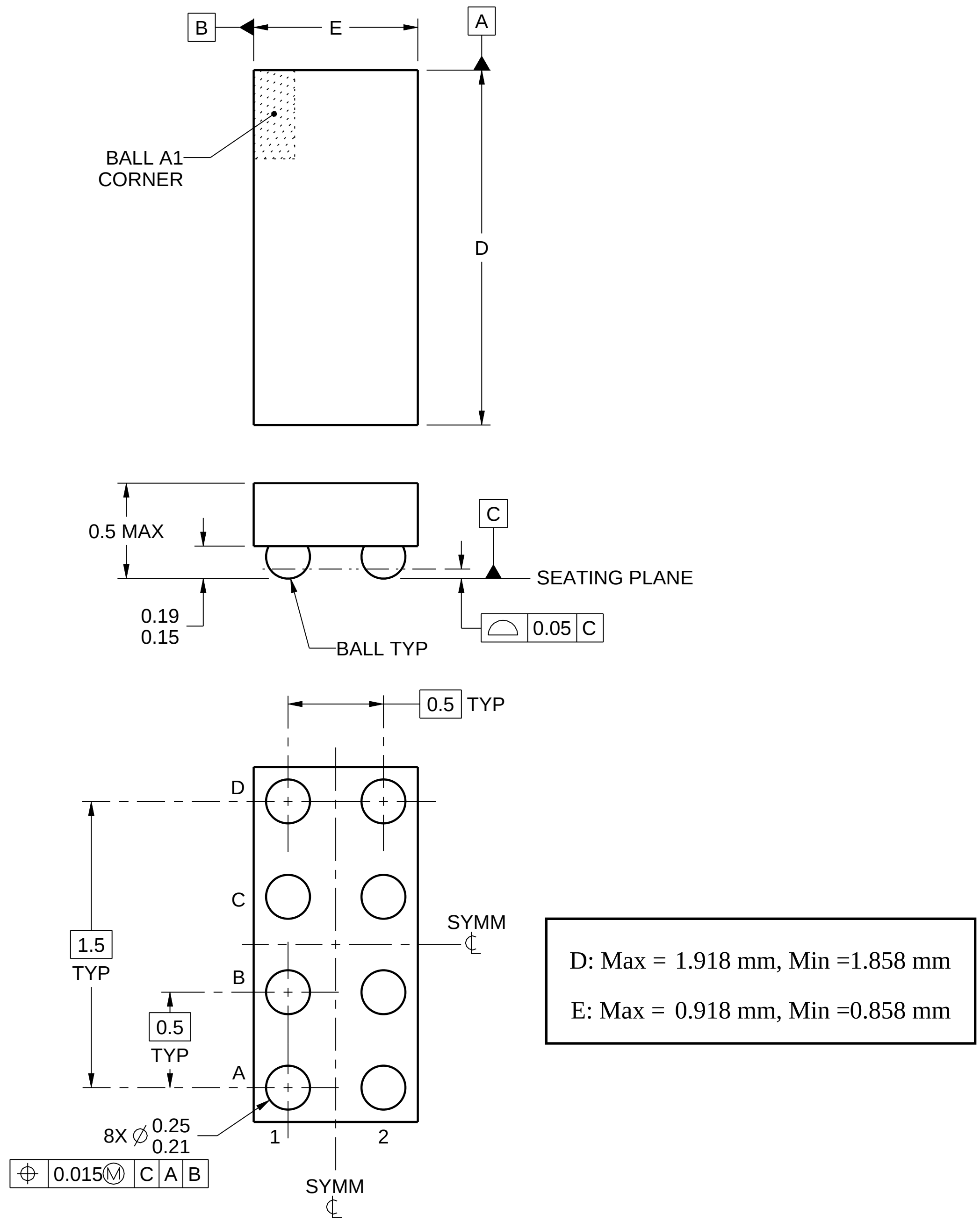


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. Falls within JEDEC MO-187 variation DA.

DCT (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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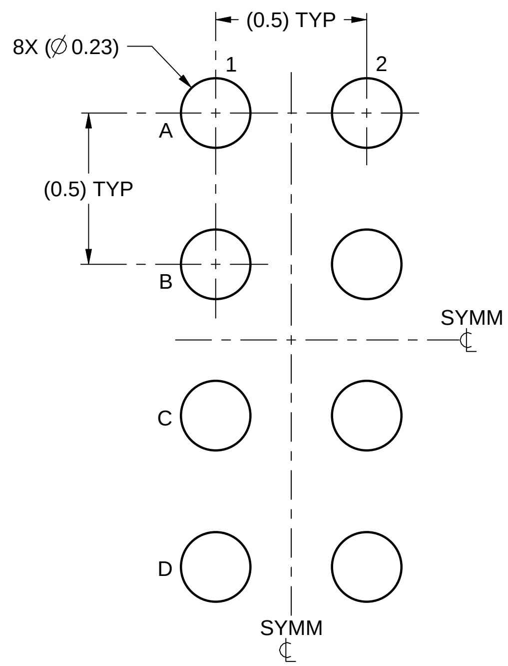
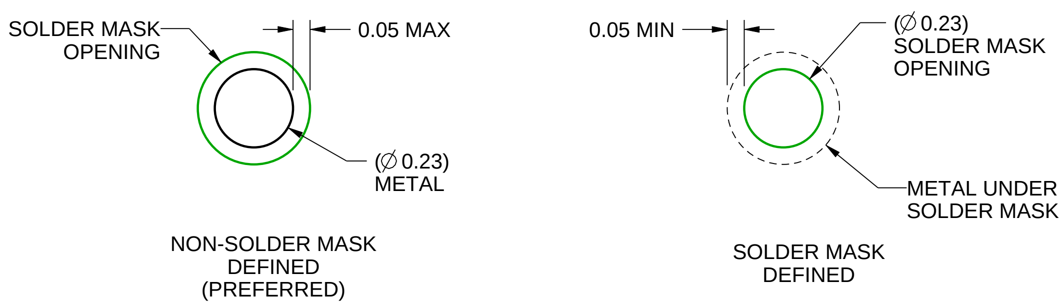
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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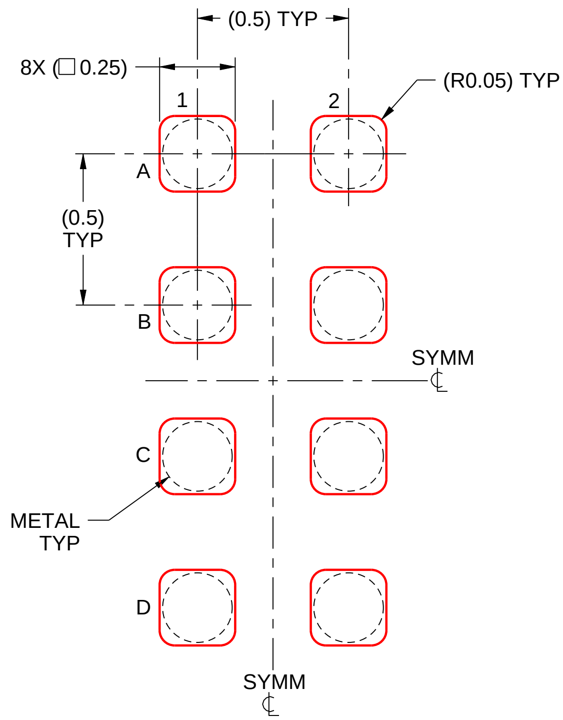
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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