



SANYO Semiconductors

DATA SHEET

LA6560 — Monolithic Linear IC For CD Five-Channel Driver (BTL : Four-Channel, H Bridge : One-Channel)

Overview

The LA6560 is a 5-channel driver (BTL : 4-channel, H bridge : 1-channel) for CD players.

Functions

- Power amplifier 5-channel built-in. (Bridge-connection (BTL) : 4-channel, H bridge : 1-channel)
- I_O max 1A
- Level shift circuit built-in (except H bridge).
- Mute circuit (output ON/OFF) built-in.
(Operable with BTL AMP and not operable for the H bridge of 5VREG)
- 5V regulator built-in (external PNP transistor).
- With VREF changeover function (H : external, L : internal (2.5V) selected)
- Overheat protection circuit (thermal shutdown) built-in.

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		14	V
Allowable power dissipation	P_d max	Independent IC	2.0	W
		Mounted on specified board. *	0.8	W
Maximum output current	I_O max	Each output for H bridge, channel 1 to 4.	1	A
Maximum input voltage	V_{INB}		13	V
MUTE pin voltage	V_{MUTE}		13	V
Operating temperature	T_{opr}		-30 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

* Specified board size : 76.1×114.3×1.6mm³, glass epoxy.

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		5.6 to 13	V

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LA6560

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 8\text{V}$, $V_{REF} = 2.5\text{V}$, unless especially specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
ALL Blocks						
No-load current drain ON	I_{CC-ON}	BTL-AMP output ON, LOADING block OFF *1		30	50	mA
No-load current drain OFF	I_{CC-OFF}	All outputs OFF *1		10	15	mA
Thermal shutdown temperature	TSD	Design guarantee value	150	175	200	$^\circ\text{C}$
VREF AMP						
VREF-AMP offset voltage	VREF-OFFSET		-10		10	mV
VREF Input voltage range	VREF-IN		1		$V_{CC}-1.5$	V
VREF-OUT output current	I-VREF-OUT	CH1 input reference voltage	2	5	6.6	mA
BTL AMP Block (CH1 to CH4)						
Output offset voltage	V_{OFF}	Voltage difference between outputs for BTL AMP, each channel. *2	-50		50	mV
Input voltage range	V_{IN}	Input voltage range for input for OP-AMP.	0		$V_{CC}-1.5$	mA
Output voltage	V_O	Each voltage between V_{O+} and V_{O-} when $R_L = 8\Omega$. *3	5.7	6.2		V
Closed-circuit voltage gain	VG	Input and output gain. Input OP-AMP:BUFFER	3.6	4	4.4	Times
Slew rate	SR	AMP Independent Multiply 2 between outputs.		0.5		V/ μs
MUTE ON voltage	VMUTE-ON	Output ON voltage, each MUTE *4	2			V
MUTE OFF voltage	VMUTE-OFF	Output OFF voltage, each MUTE *4			0.5	V
Input AMP Block (CH1 to 4)						
Input voltage range	V_{IN-OP}		0		$V_{CC}-1.5$	V
Output current (SINK)	SINK-OP		2			mA
Output current (SOURCE)	SOURCE-OP	*5	300	500		μA
Output offset voltage	V_{OFF-OP}		-10		10	mV
CH1 input changeover voltage 1	VSW-OP1	CH1 input AMP(B), external VREF select *6	2			V
CH1 input changeover voltage 2	VSW-OP2	CH1 input AMP(A), internal VREF select *6			0.5	V
Loading Block (CH5, H bridge)						
Output voltage	V_{O-LOAD}	At forward and reverse rotation, $R_L = 8\Omega$, $V_{CONT}=V_{CC}$ *3	5.7	6.5		V
Break output saturation voltage	$V_{CE-BREAK}$	Output voltage at braking *7			0.3	V
Input low level	V_{IN-L}				1	V
Input high level	V_{IN-H}		2			V
Power Supply Block (PNP transistor : 2SB632K-use)						
5V supply voltage	V_{OUT}	$I_O = 200\text{mA}$	4.8	5.0	5.2	V
REG-IN SINK current	REG-IN-SINK	Base current of external PNP *8	5	10		mA
Line regulation	ΔV_{OLN}	$6\text{V} \leq V_{CC} \leq 12\text{V}$, $I_O = 200\text{mA}$		10	100	mV
Load regulation	ΔV_{OLD}	$5\text{mA} \leq I_O \leq 200\text{mA}$		10	100	mV

Note *1 : Current dissipation that is a sum of V_{CC1} and V_{CC2} at no load.

*2 : Input AMP is a BUFFER AMP.

*3 : Voltage difference between both ends of load (8Ω). Output saturated.

*4 : Output ON with MUTE : [H] and OFF with MUTE : [L] (HI impedance).

*5 : The source of input OP-AMP is a constant current. As the $11\text{k}\Omega$ resistance to the next stage is a load, pay due attention when setting the input OP-AMP gain.

*6 : With V_{IN1-SW} : [L], the input AMP selects AMP-A while VREF selects internal VREF ($\approx 2.5\text{V}$).

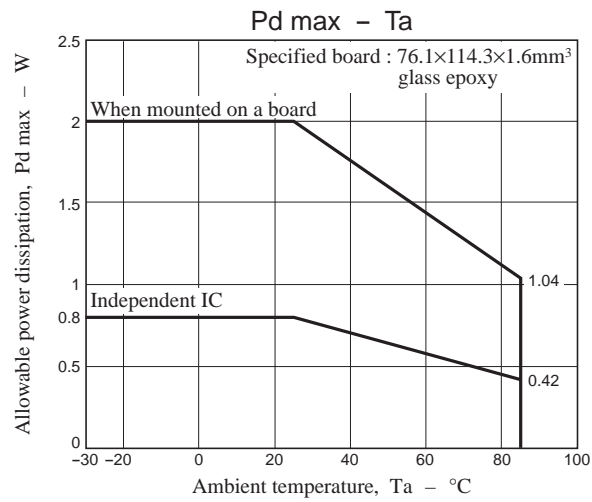
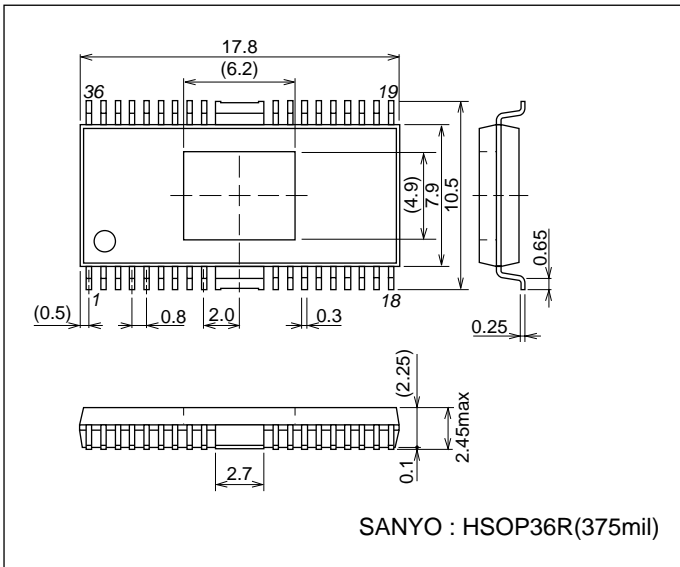
With V_{IN1-SW} : [H], the input AMP selects AMP-B while VREF selects external VREF ($\approx V_{REF-IN}$).

*7 : Short (GND) brake used. SINK side output ON.

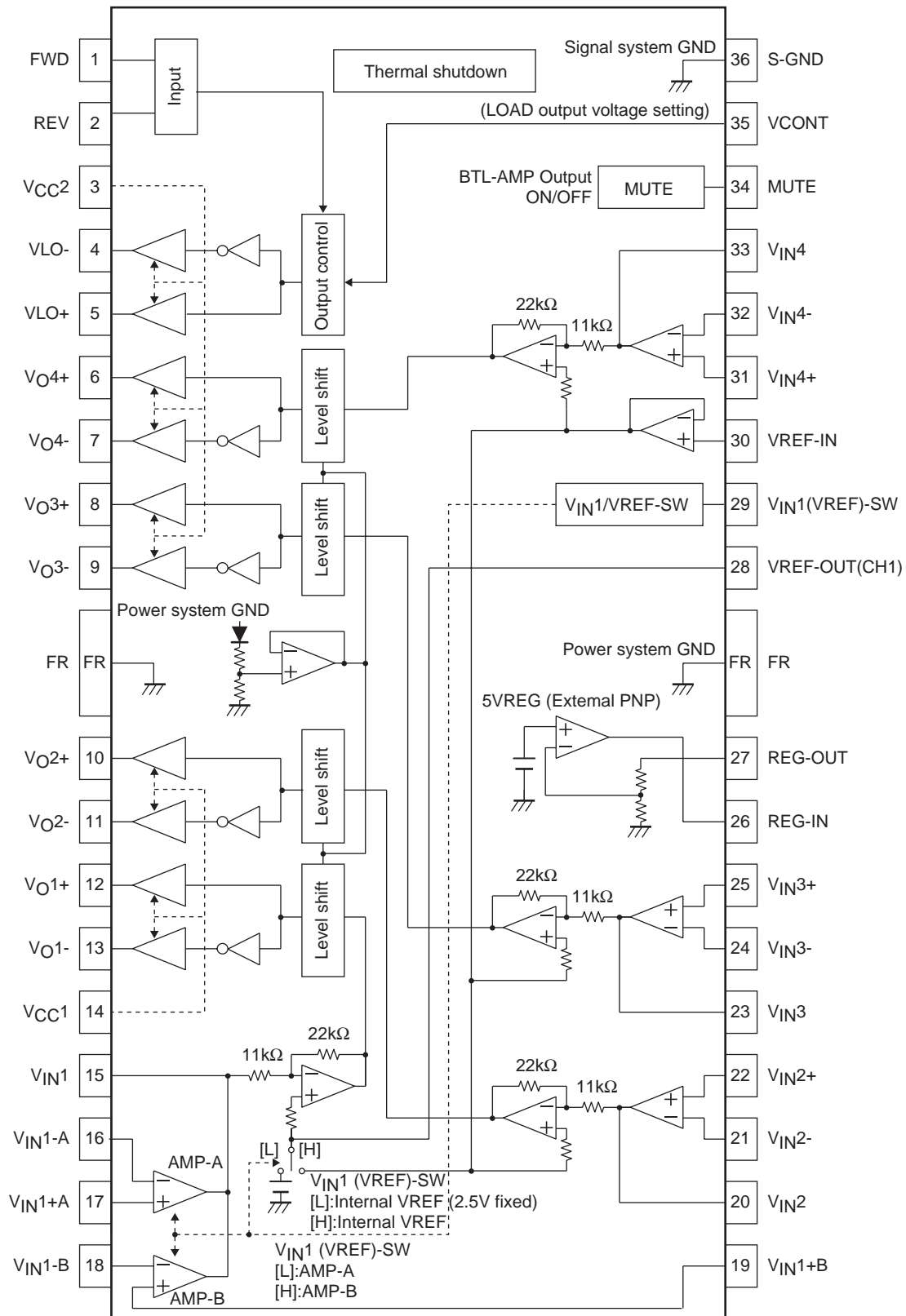
*8 : 5VREG incorporates a drooping protection circuit and operated when the base current is 10mA (TYP).

Package Dimensions

unit : mm (typ)
3251



Block Diagram



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Pin Functions

Pin No.	Symbol	Pin descriptions
1	FWD	Output change pin (FWD) for 5CH (VLO), logic input for loading block.
2	REV	Output change pin (REV) for 5CH (VLO), logic input for loading block.
3	V _{CC2}	Power supply for CH3, 4, and 5.
4	VLO-	Loading output (-)
5	VLO+	Loading output (+)
6	V _{O4+}	Output pin (+) for channel 4
7	V _{O4-}	Output pin (-) for channel 4
8	V _{O3+}	Output pin (+) for channel 3
9	V _{O3-}	Output pin (-) for channel 3
10	V _{O2+}	Output pin (+) for channel 2
11	V _{O2-}	Output pin (-) for channel 2
12	V _{O1+}	Output pin (+) for channel 1
13	V _{O1-}	Output pin (-) for channel 1
14	V _{CC1}	Power supply for CH1, 2 (BTL).
15	V _{IN1}	Input pin for channel 1
16	V _{IN1-A}	OP-AMP input AMP-A input pin (-)
17	V _{IN1+A}	OP-AMP input AMP-A input pin (+)
18	V _{IN1-B}	Input AMP-B input pin (-) for channel 1
19	V _{IN1+B}	Input AMP-B input pin (+) for channel 1
20	V _{IN2}	Input pin for channel 2, input AMP output
21	V _{IN2-}	Input pin (-) for channel 2
22	V _{IN2+}	Input pin (+) for channel 2
23	V _{IN3}	Input pin for channel 3, input AMP output
24	V _{IN3-}	Input pin (-) for channel 3
25	V _{IN3+}	Input pin (+) for channel 3
26	REG-IN	PNP transistor base connected
27	REG-OUT	5V power output to which the PNP transistor collector connected.
28	VREF-OUT	CH1 reference voltage output. Outputs internal VREF (2.5V : TYP) or external VREF.
29	V _{IN1} (VREF) -SW	Pin for changeover between input AMP-A/internal VREF (TYP2.5V) and input AMP-B/ external VREF.
30	VREF-IN	Reference voltage applied pin
31	V _{IN4+}	Input pin (+) for channel 4
32	V _{IN4-}	Input pin (-) for channel 4
33	V _{IN4}	Input pin for channel 4, input AMP output
34	MUTE	All BTL AMP output ON/OFF
35	VCONT	LOADING output voltage setting
36	S-GND	Signal system GND

Note : Center frame (FR) becomes GND for the power system (P-GND). Set this to the minimum potential together with S-GND.

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Pin Description

Pin No.	Symbol	Pin function	Description	Equivalent circuit
17 19 16 18 15 22 21 20 25 24 23 32 31 33	V_{IN1+A} V_{IN1+B} V_{IN1-A} V_{IN1-B} V_{IN1} V_{IN2+} V_{IN2-} V_{IN2} V_{IN3+} V_{IN3-} V_{IN3} V_{IN4-} V_{IN4+} V_{IN4}	Input (CH1 to 4)	Input pin (CH1 to 4)	
1 2	FWD REV	Input (H bridge)	Logic input pin. By combining H and L of this pin, any one of four modes (forward/reversed/brake/idling) can be selected.	
12 13 10 11 8 9 6 7	V_{O1+} V_{O1-} V_{O2+} V_{O2-} V_{O3+} V_{O3-} V_{O4+} V_{O4-}	Output (BTL-AMP)	Output for channel 1 to 4.	
4 5 35	VLO- VLO+ VCONT	Output (H bridge)	H bridge (LOADING) output and LOADING output setting pin	
34	MUTE	MUTE	BTL AMP output, which turns ON/OFF the output, MUTE : H Output OFF MUTE : L Output OFF	

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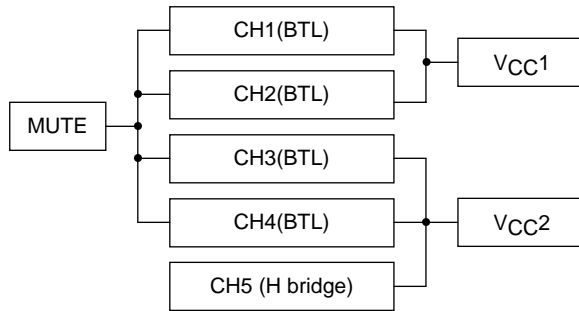
Truth Table (loading (H bridge) section)

FWD	REV	VLO+	VLO-	Loading output
L	L	OFF	OFF	OFF *1
	H	H	L	Forward
H	L	L	H	Reversed
	H	L	L	(Short) brake *2

*1 The output has a high impedance.

*2 At brake, the SINK side transistor is ON (short brake).
VLO+ and VLO- are approximately on the GND level.

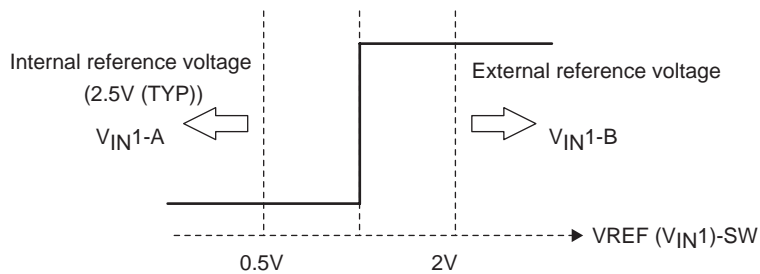
Relation of MUTE and Power (VCC*)



V_{IN1} (VREF)-SW (CH1 input AMP selection and internal/external VREF selection function)

(Relation between input AMP (CH1 only) and VREF)

V _{IN1} _SW	Input AMP (CH1) state	VREF state
H	V _{IN1} -A (AMP-A)	Internal VREF (2.5V : TYP)
L	V _{IN1} -B (AMP-B)	External VREF

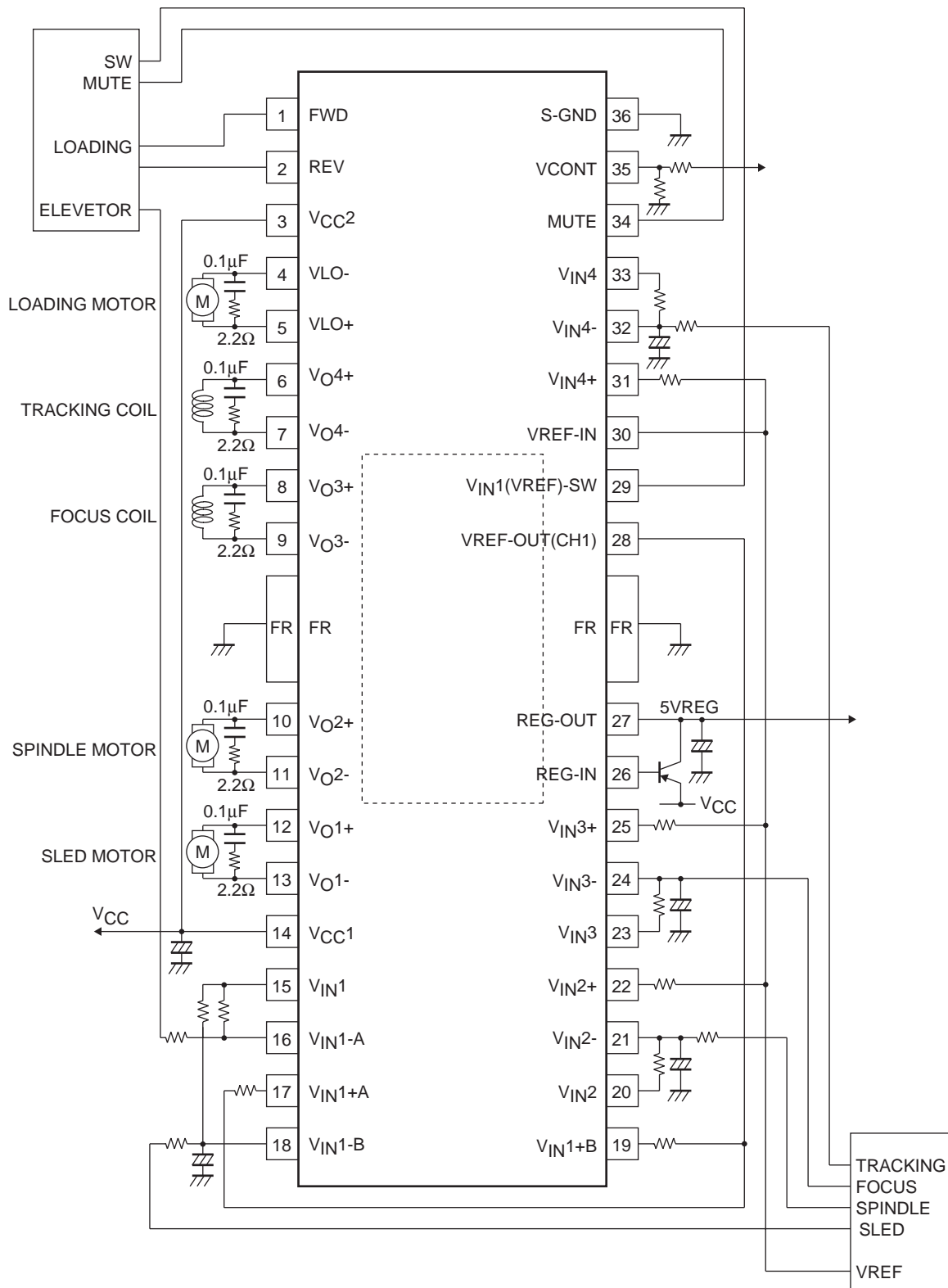


On MUTE

MUTE	BTLAMP output	VREF-OUT
L	OFF	
H	ON	

VREF-OUT operates in an interlock with MUTE.

Sample Application Circuit



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